VCI 2016 – The 14th Vienna Conference on Instrumentation

15-19 February 2016, Vienna University of Technology

The ALPIDE Pixel Sensor Chip for the Upgrade of the ALICE Inner Tracking System

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On behalf of the ALICE Collaboration

Outline

1. ALICE Inner Tracking System Upgrade and Chip Requirements

2. The ALPIDE Pixel Chip

   Description and Key Features

3. Experimental results with pALPIDE-2 and pALPIDE-3 prototypes

ALICE Inner Tracking System Upgrade Objectives

1. Improve impact parameter resolution by a factor ~3

   Get closer to IP (radius of first layer): 39 mm -> 23 mm

   Reduce pixel size: currently 50 μm x 425 μm -> O(30 μm x 30 μm)

   Reduce x/X_0/layer from ~1.14% -> ~0.3% (inner layers)

2. Better tracking efficiency and p_T resolution at low p_T

   Finer granularity: from 6 to 7 layers and all layers with pixels

3. Fast readout

   Readout Pb-Pb interactions at 100 kHz

   Readout pp interactions at >200 kHz (current ITS limited at 1 kHz)

4. Design for fast removal and insertion

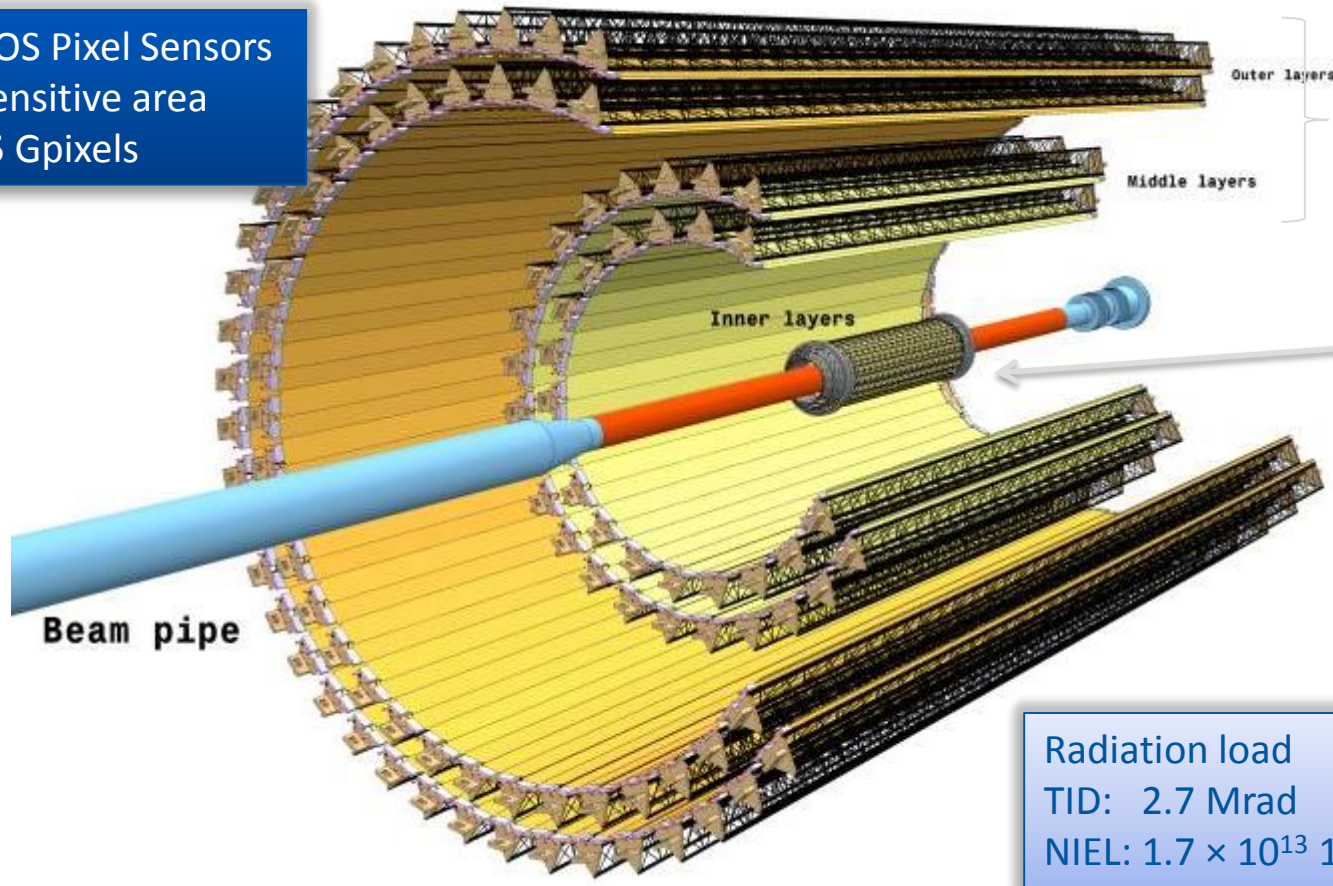
   Maintenance during yearly shutdown

Technical Design Report for the Upgrade of the ALICE Inner Tracking System
J. Phys. G 41 (2014) 087002
CERN-LHCC-2013-024 ; ALICE-TDR-017

Installation of the new detector during LHC Long Shutdown 2 (2019-2020)

New ALICE ITS Layout

~24000 CMOS Pixel Sensors
10 m² sensitive area
12.5 Gpixels



Outer Barrel

Inner Barrel

Radiation load
TID: 2.7 Mrad
NIEL: 1.7×10^{13} 1 MeV n_{eq}/cm^2

Barrel geometry

3 Inner Barrel layers (**IB**) **0.3% X_0**
4 Outer Barrel layers (**OB**) **1% X_0**

Coverage

23 mm < r < 400 mm, $|\eta| < 1.22$

Layers z-lengths: 27 - 150 cm

ITS Chip General Requirements

Parameter	Inner Barrel	Outer Barrel
Chip size (mm x mm)	15 x 30	
Chip thickness (μm)	50	100
Spatial resolution (μm)	5	10 (5)
Detection efficiency	> 99%	
Fake hit rate	$< 10^{-5}$ evt^{-1} pixel^{-1} (ALPIDE $<< 10^{-5}$)	
Integration time (μs)	< 30 (< 10)	
Power density (mW/cm^2)	< 300 (~35)	< 100 (~20)
TID radiation hardness (krad) (**)	2700	100
NIEL radiation hardness (1 MeV n_{eq}/cm^2) (**)	1.7×10^{13}	1.7×10^{12}
Readout rate, Pb-Pb interactions (kHz)	100	
Hit Density, Pb-Pb interactions (cm^{-2})	18.6	2.8

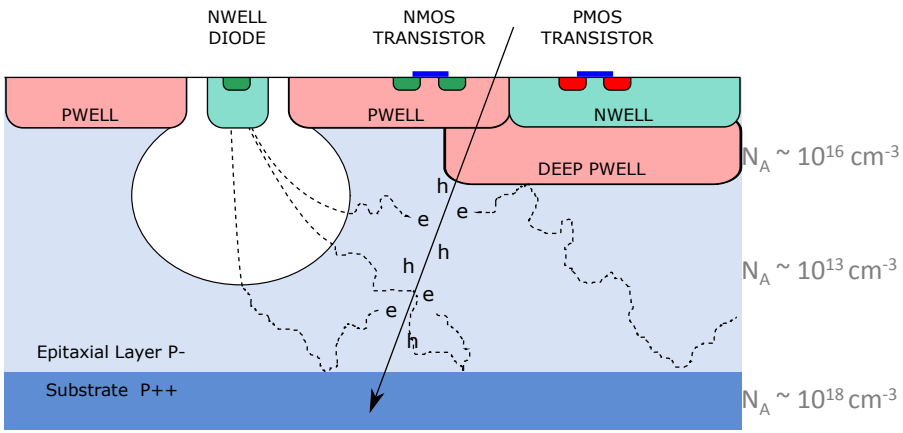
(*) In color: ALPIDE performance figure where above requirements

(**) 10x radiation load integrated over approved program (~ 6 years of operation)

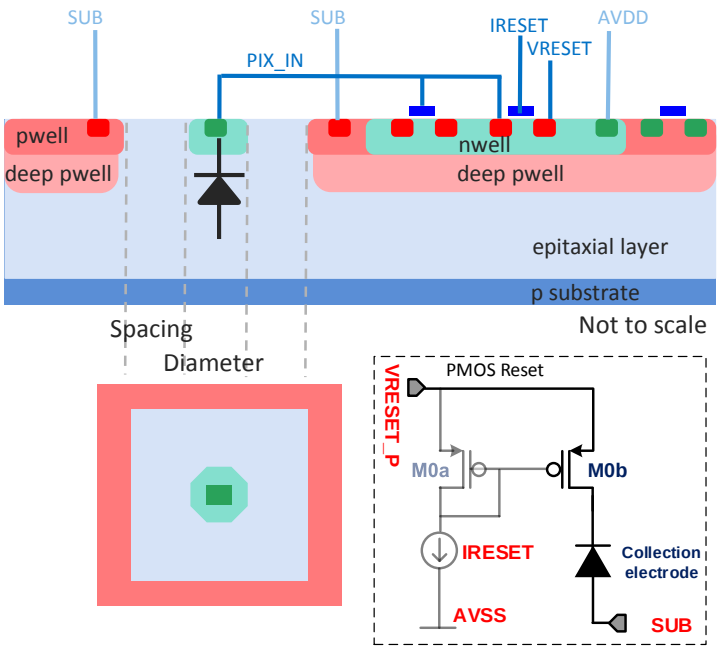
ALPIDE Technology

Pixel Sensor CMOS 180 nm Imaging Process (TowerJazz)

3 nm thin gate oxide, 6 metal layers

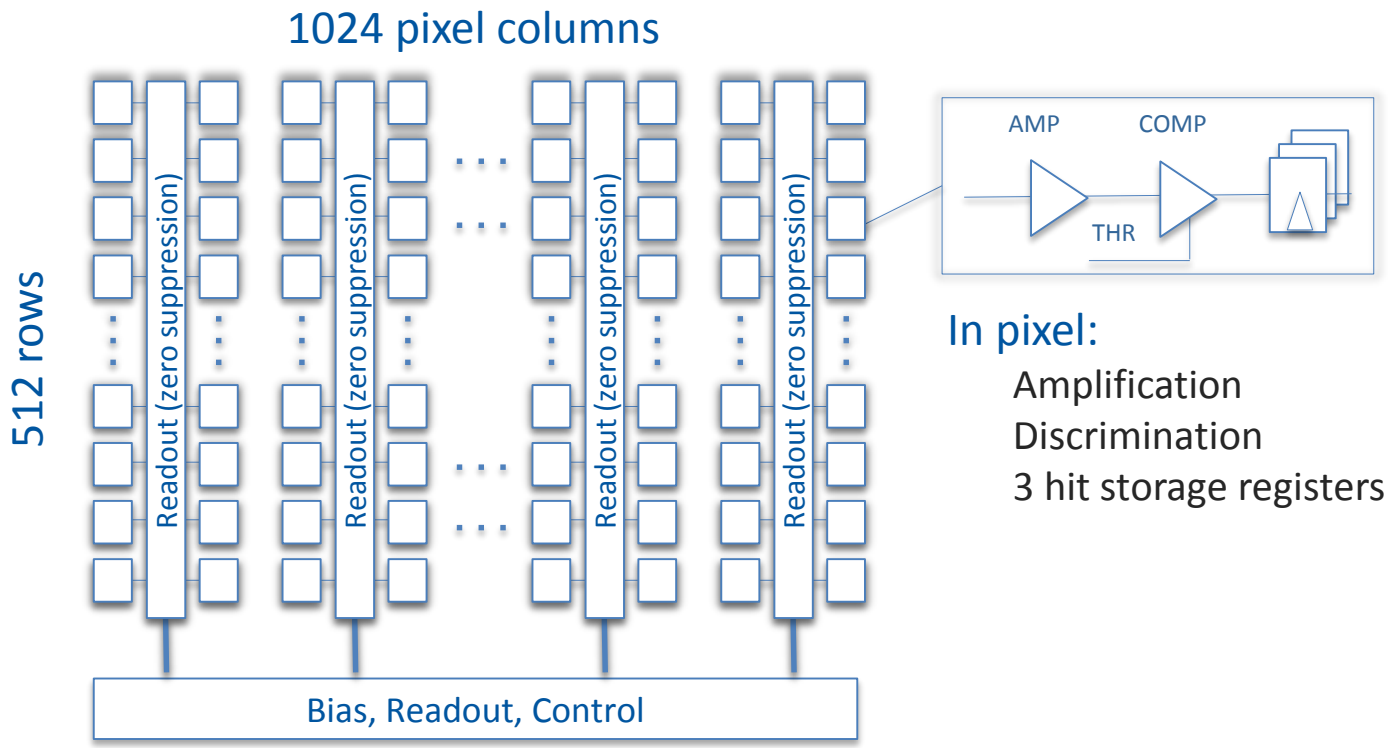


Not to scale



- High-resistivity (> 1kΩ cm) p-type epitaxial layer (18 μm to 30 μm) on p-type substrate
- Deep PWELL shielding NWELL allowing PMOS transistors (full CMOS within active area)
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance => large S/N
- Reverse bias can be applied to the substrate to increase the depletion volume around the NWELL collection diode

ALPIDE Architecture



In pixel:

- Amplification
- Discrimination
- 3 hit storage registers (MEB)

29 μm x 27 μm pixel pitch

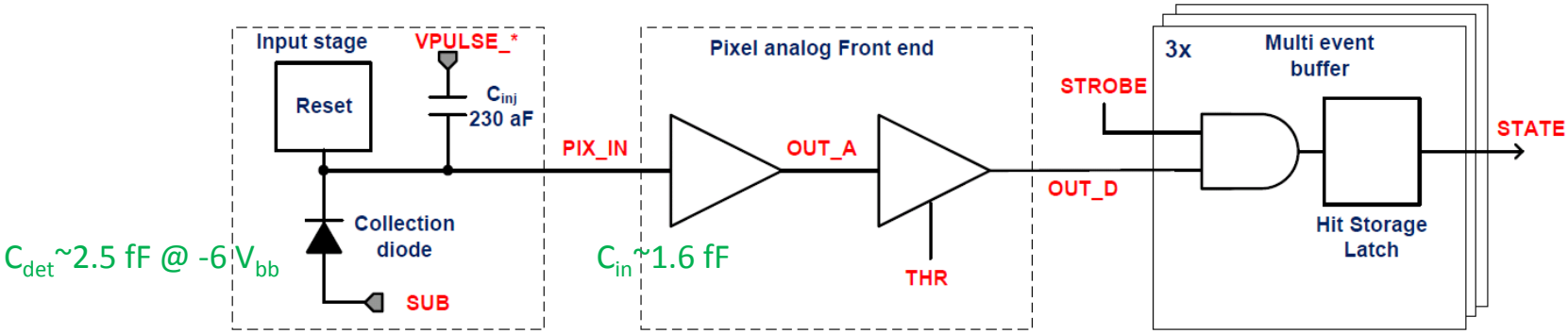
Continuously active front-end

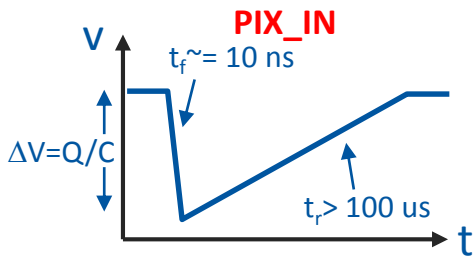
Global shutter

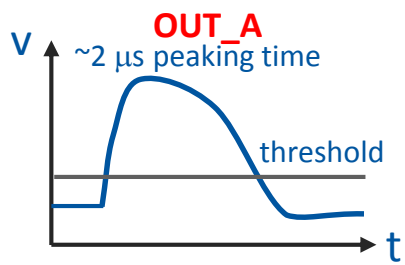
Zero-suppressed matrix readout

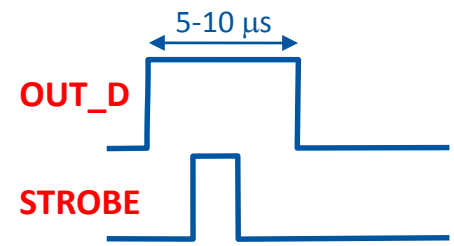
Triggered or continuous readout modes

Pixel









Analog front-end and discriminator continuously active

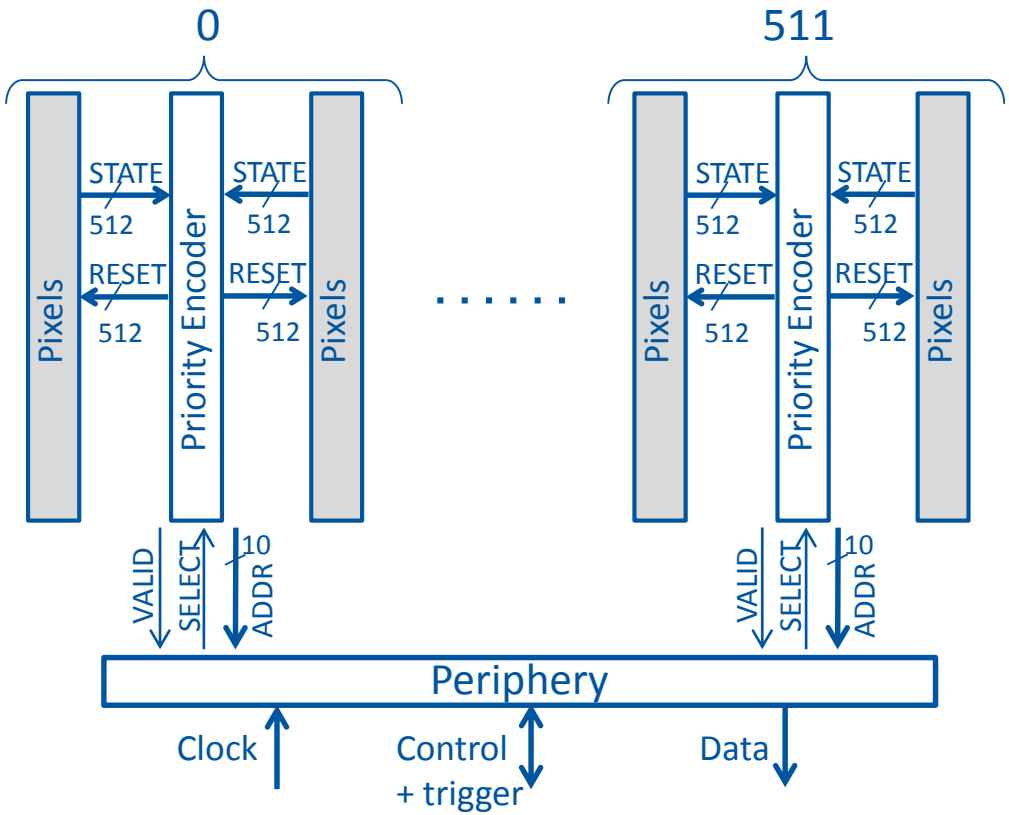
- Non-linear and operating in weak inversion. Ultra-low power: 40 nW/pixel
- The front-end acts as analogue delay line
- Test pulse charge injection circuitry
- Global threshold for discrimination -> binary pulse OUT_D

Front End Characteristics	
Gain (small signal) [mV/e]	4
ENC [e]	3.9
Threshold [e]	92 ± 2

Digital pixel circuitry with three hit storage registers (multi event buffer)

- Global shutter (STROBE) latches the discriminated hits in next available register
- In-Pixel *masking* logic

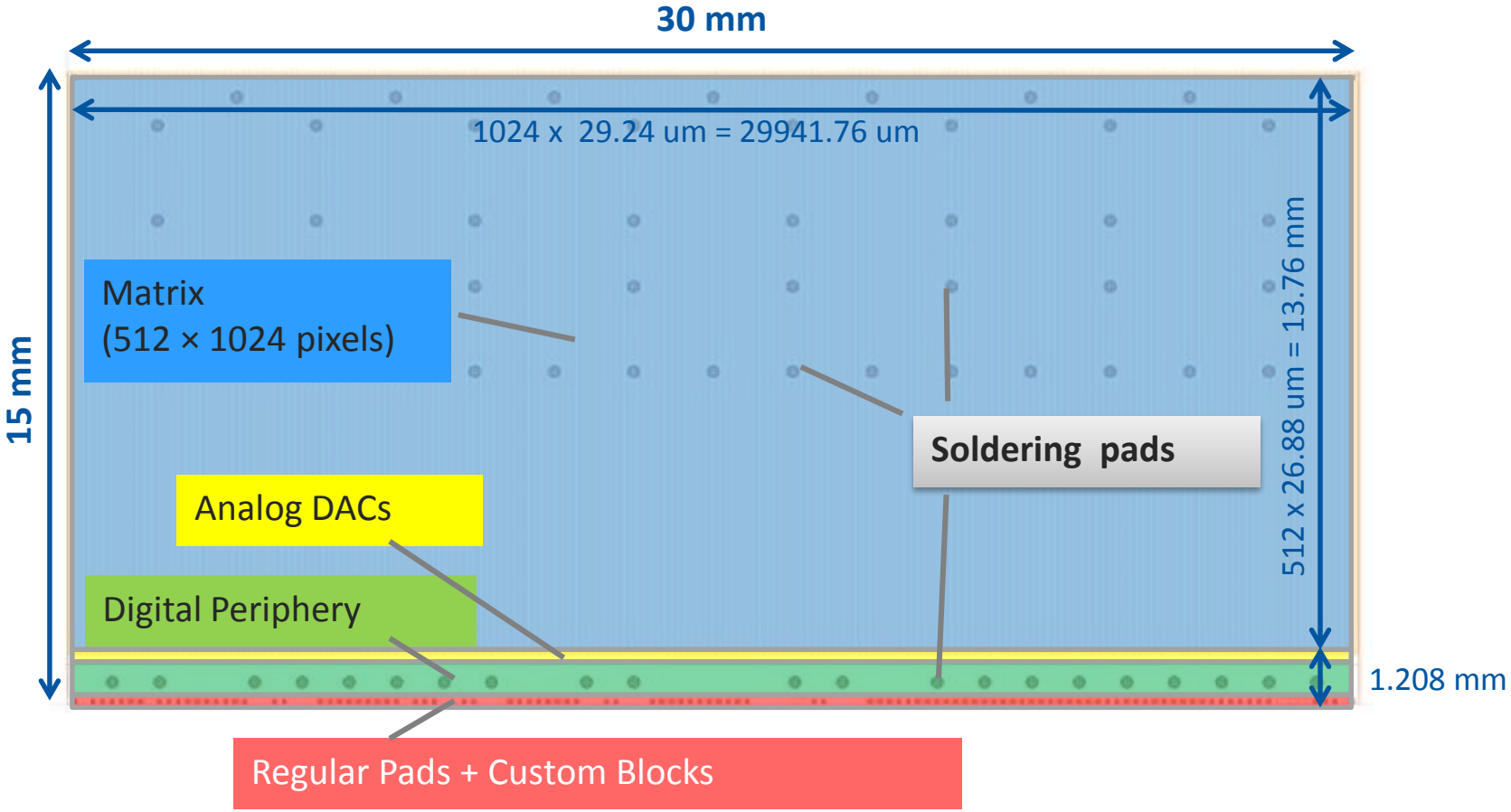
Matrix Readout



The Priority Encoder sequentially provides the addresses of all hit pixels in a double column

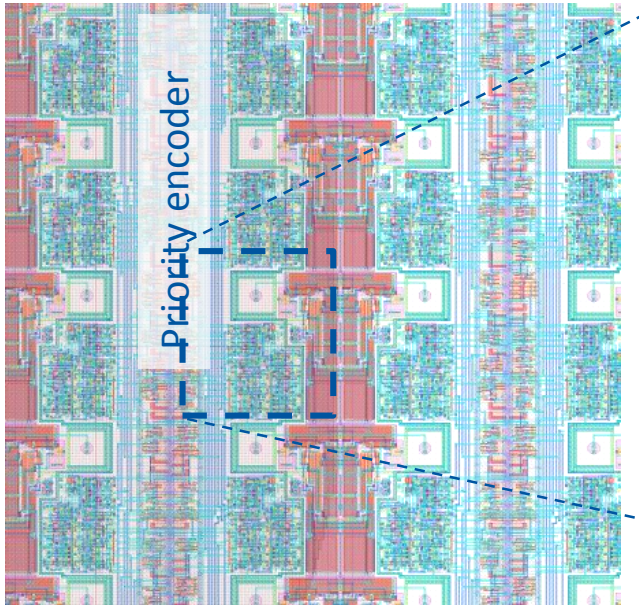
- Combinatorial digital circuit steered by peripheral sequential circuits during readout of a frame
- No free running clock over matrix. No activity if there are no hits
- Energy per hit: E_h ~= 100 pJ -> ~3 mW for nominal occupancy and readout rate
- Buffering and distribution of global signals (STROBE, MEMSEL, PIXEL RESET)

ALPIDE Chip Floorplan

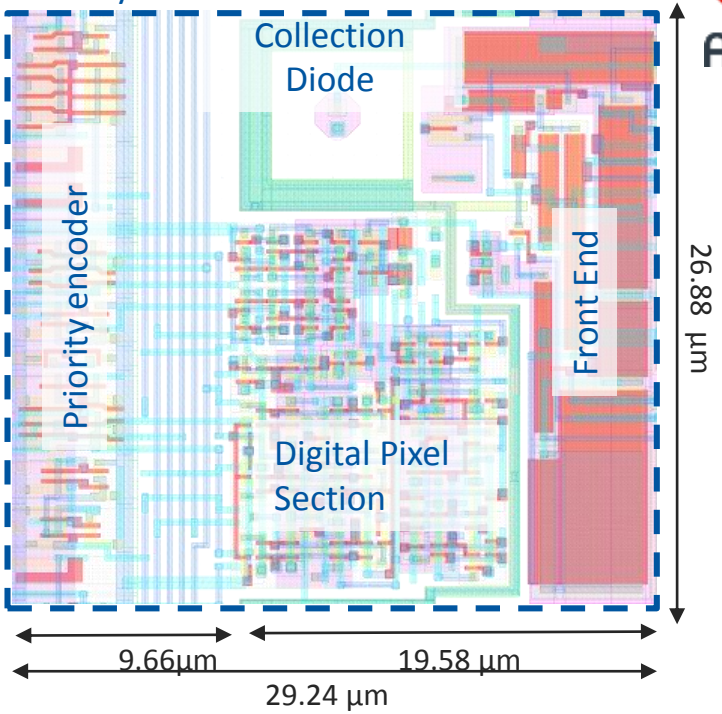


Layout Features

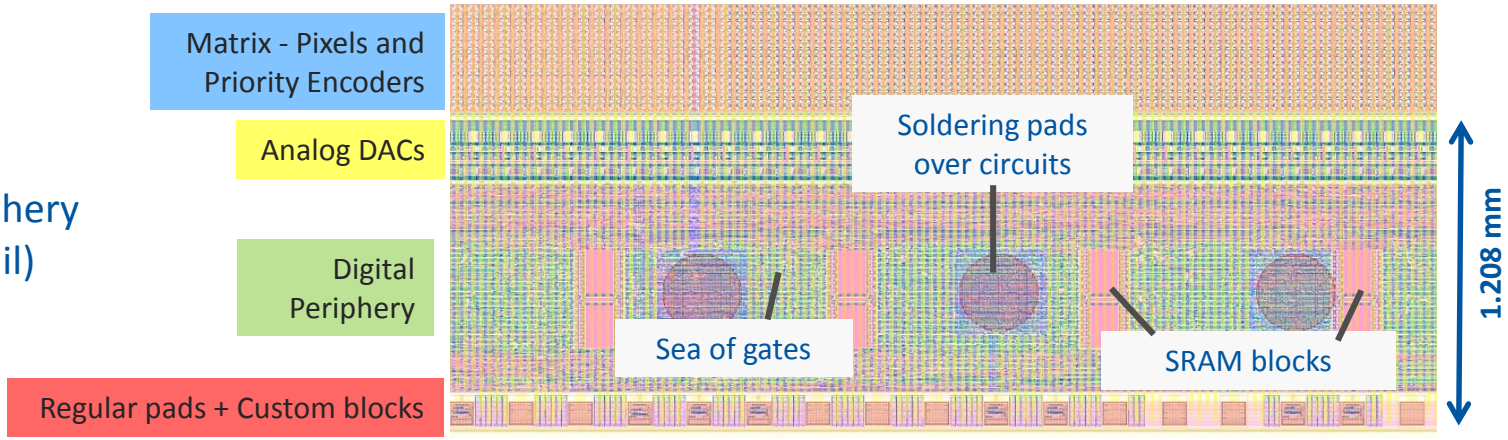
Matrix (detail)



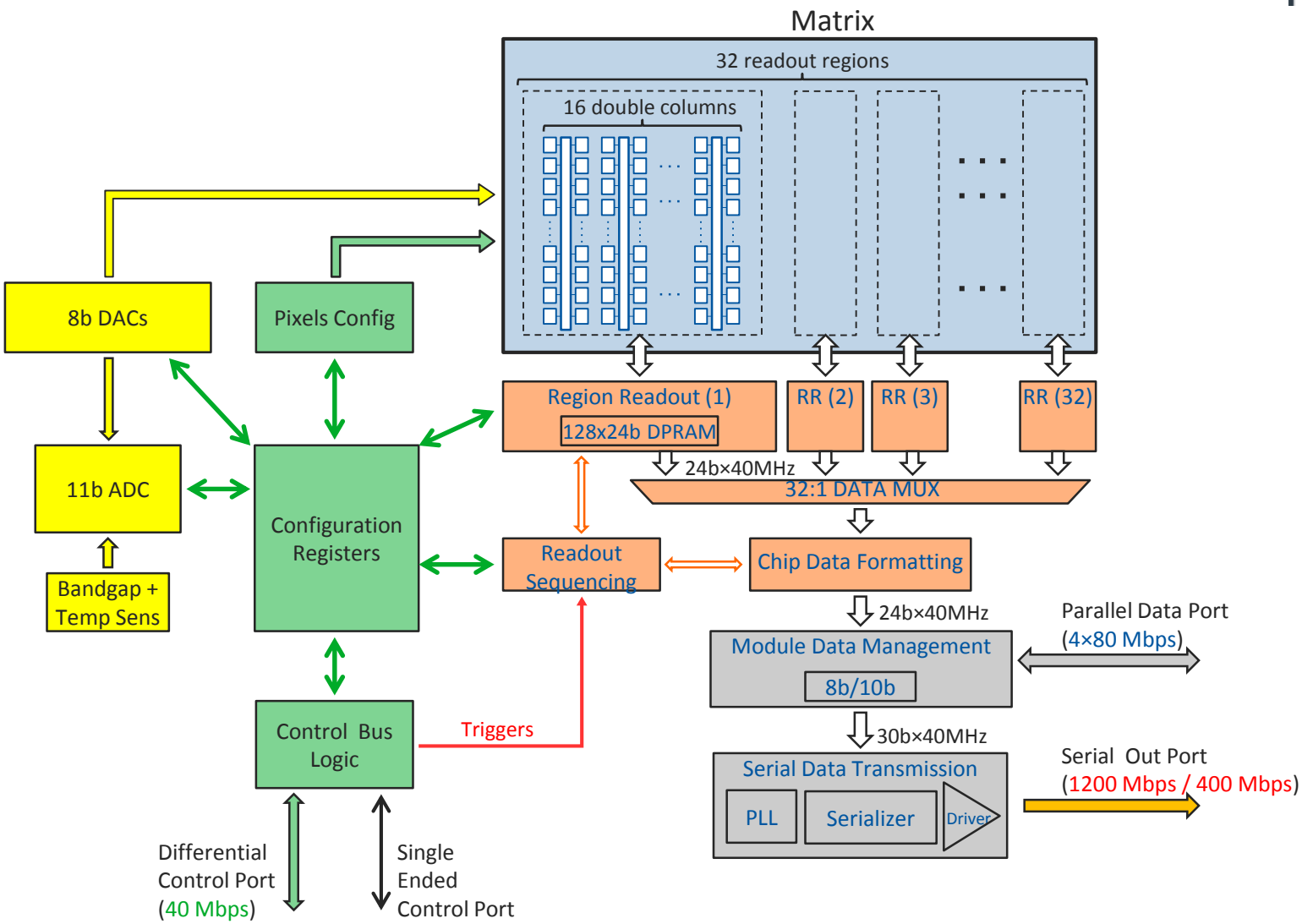
Pixel layout



Periphery (detail)

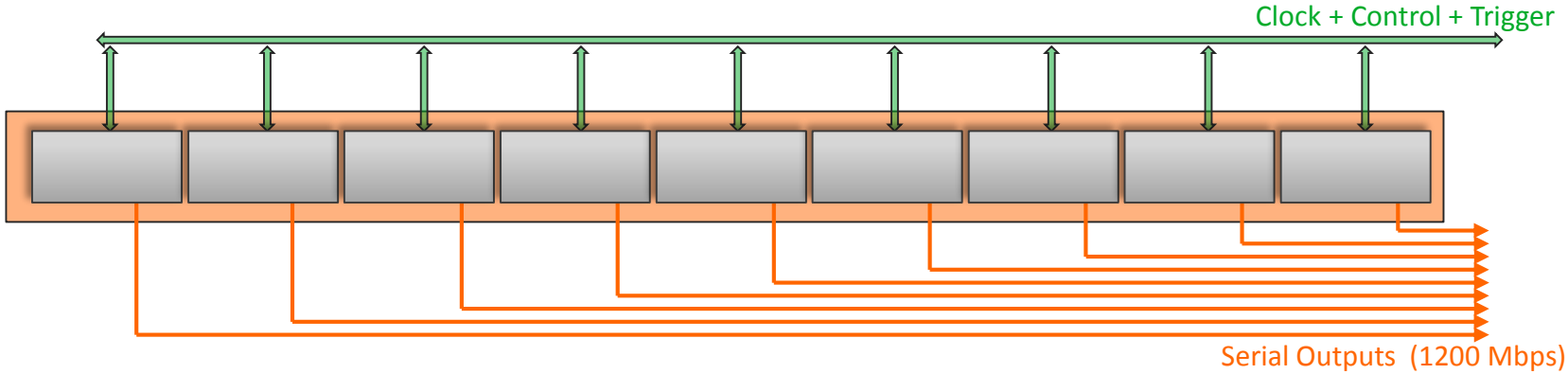


ALPIDE Readout and Control Features



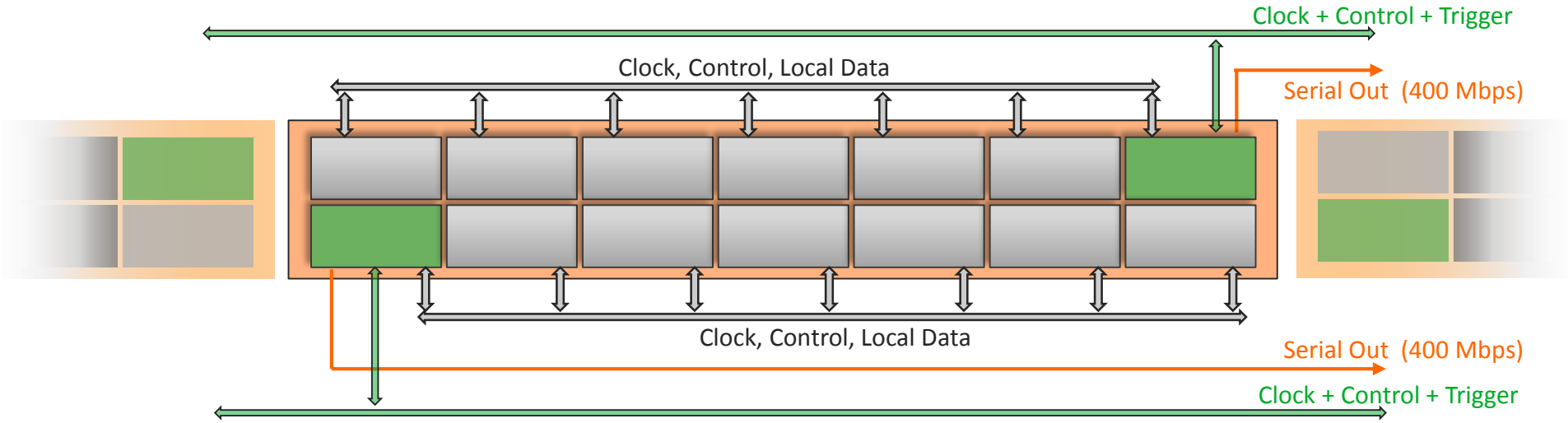
Detector Modules with ALPIDE Chips

ITS Inner Barrel Module – 9 chips, common clock and control, independent data lines

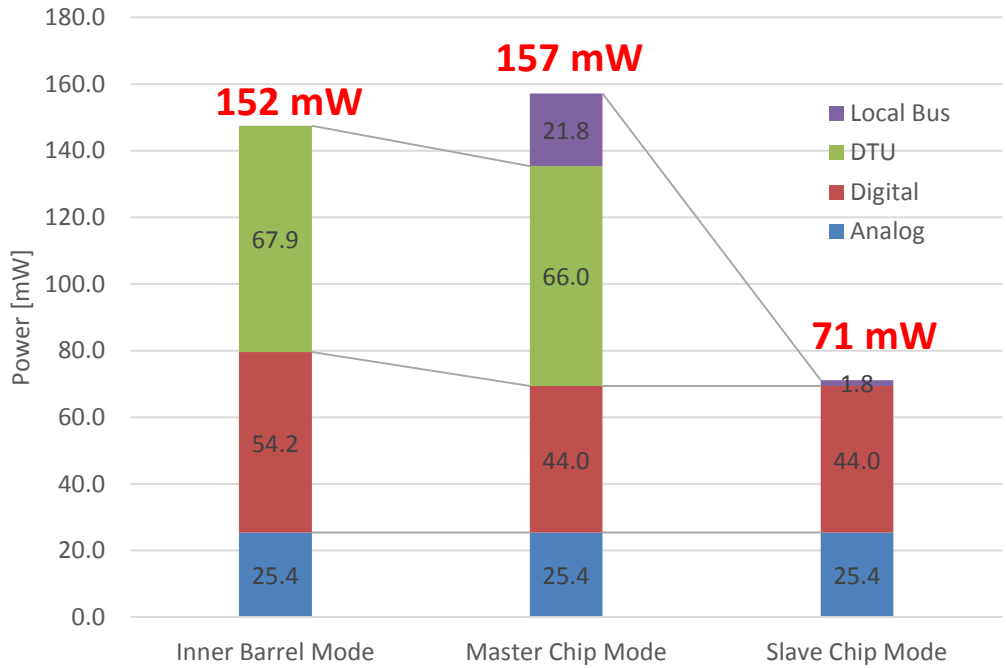


ITS Outer Barrel Module – 2 groups of chips, Master + 6 Slaves

Only the Master interfaces to the external world and bridges control and data transfer



ALPIDE Power Estimates



Inner Barrel: 34 mW/cm^2

Outer Barrel: 18.5 mW/cm^2

Digital power estimates with highest design occupancy and readout rate

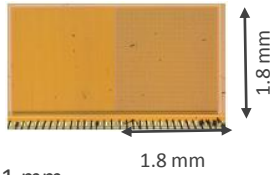
Low Power Techniques

- Front-end transistors operating in weak inversion
- Clock gating in digital periphery
  - Clock enabled on detection of SEU errors for synchronous correction

ALPIDE Development

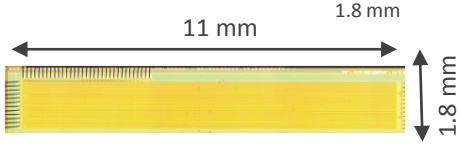
2012 — **Explorer**

20μm x 20μm and 30μm x 30μm pixels (analogue readout)
pixel geometry, starting material, sensitivity to radiation



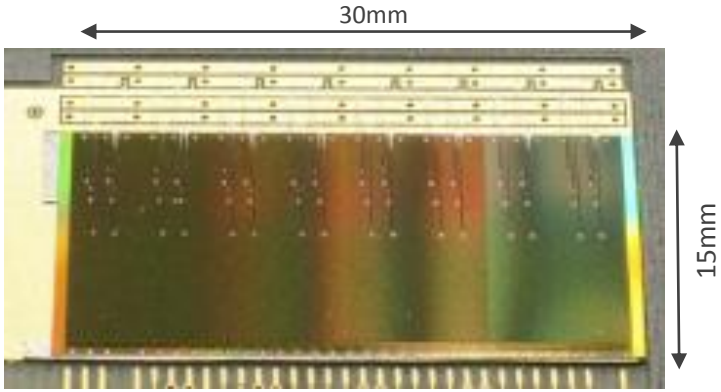
2013 — **pALPIDEss-0**

Matrix with 64 columns x 512 rows
22 μm x 22 μm pixels
In-pixel discrimination and buffering
Zero suppression within pixel matrix



2014 — **pALPIDE-1**

Full-scale prototype
Pixel pitch: 28 μm x 28 μm
4 sectors with pixel variants
1 register/pixel, no final interface



Apr-2015 — **pALPIDE-2**

4 sectors with pixel variants
Optimization of circuits
Allowing integration in ITS modules
No high-speed serial output (1.2 Gbit/s replaced by 40 Mb/s)

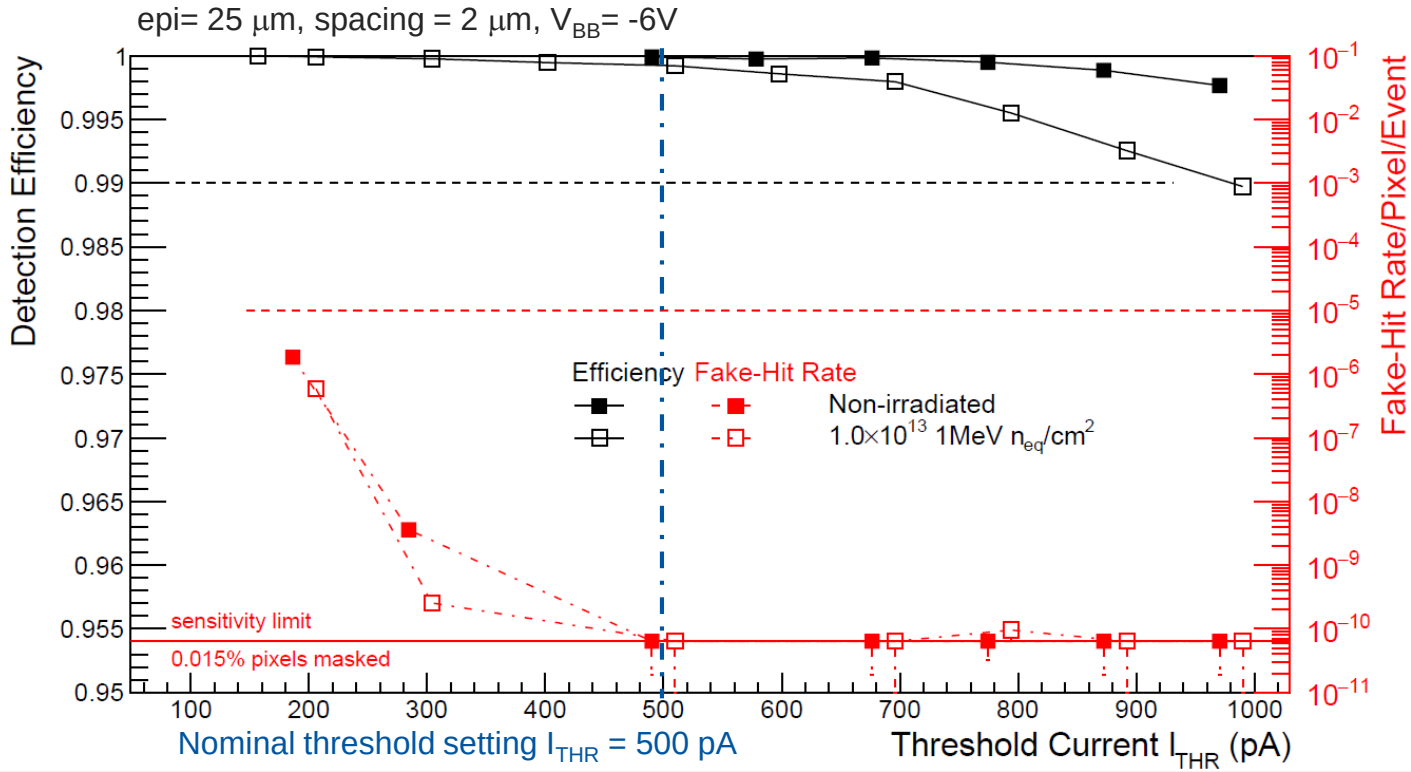
Oct-2015 — **pALPIDE-3**

8 sectors with pixels variant
All Final Functionalities and Features

ALPIDE

pALPIDE-2 Test Beam Results

Detection Efficiency and Fake Hit Rate before and after irradiation



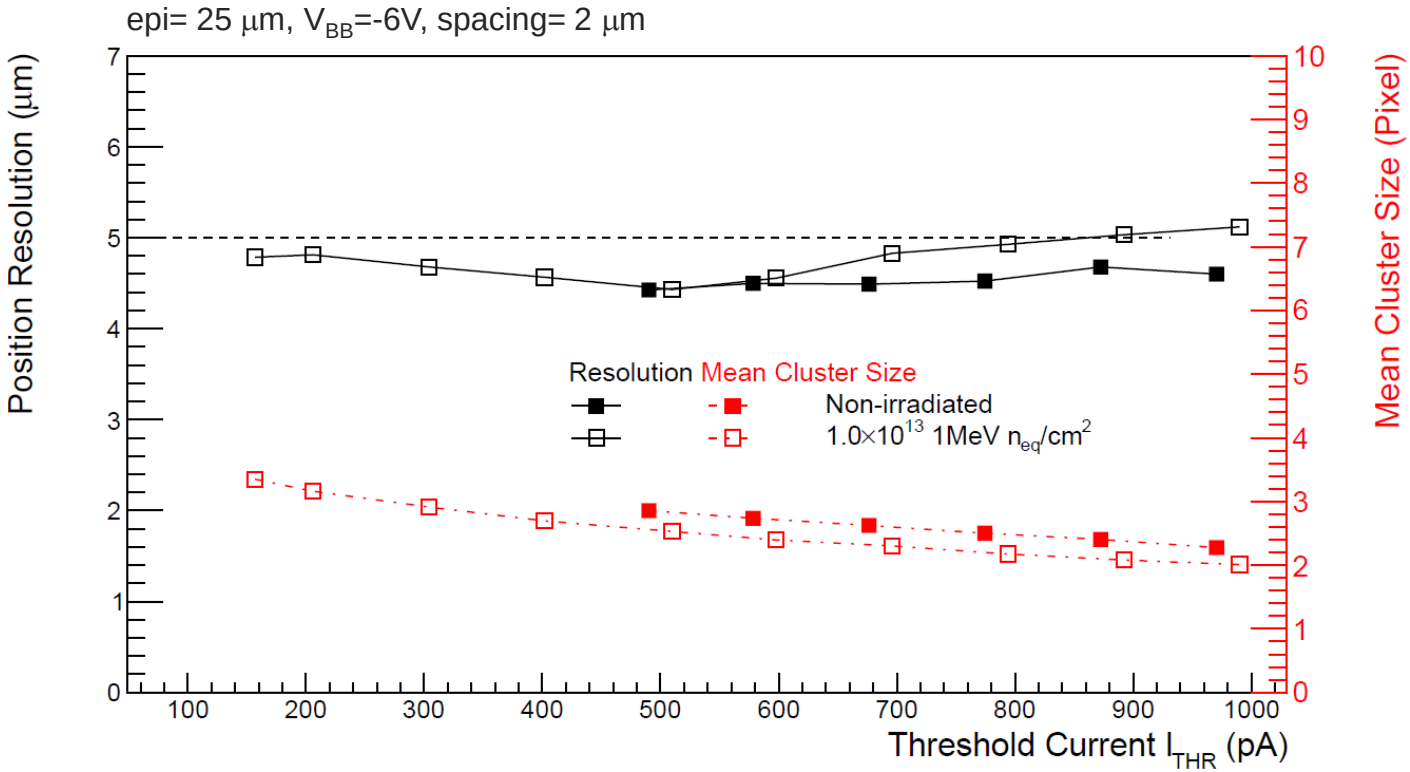
ε_{det} > 99% @ λ_{fake} << 10^{-5} / event/pixel -> large margin over design requirements

Measurements on chips with 25 μm high-resistivity epitaxial layer, thinned to 50 μm, -6 V reverse bias

1 non irradiated and 1 irradiated with $1.0 \cdot 10^{13}$ 1 MeV n_{eq}/cm^2

pALPIDE-2 Test Beam Results

Position Resolution and Cluster Size before and after irradiation



$\sigma_{det} \approx 5\ \mu m$ is achieved before and after irradiation

Measurements on chips with 25 μm high-resistivity epitaxial layer, thinned to 50 μm

1 non irradiated and 1 irradiated with 1.0×10^{13} 1 MeV n_{eq}/cm^2

pALPIDE-3 Preliminary Results

Laboratory Testing

25/29 chips fully functional after mounting on chip carriers

Configuration, Readout, Charge Injection, Multi Event Buffers
-> **OK!**

Systematic characterization continuing

Serial Data Transmission Unit functional

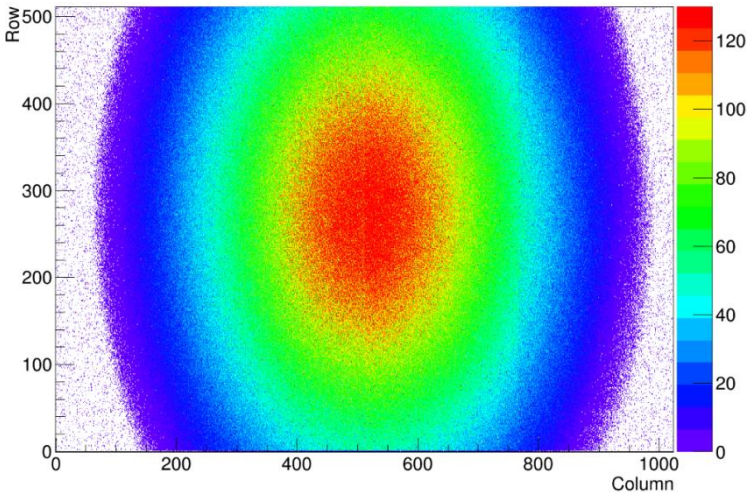
Sustained readout at 1.2 Gbps

Excess of jitter due to coupling of digital supply noise => separation of supply domains in ALPIDE

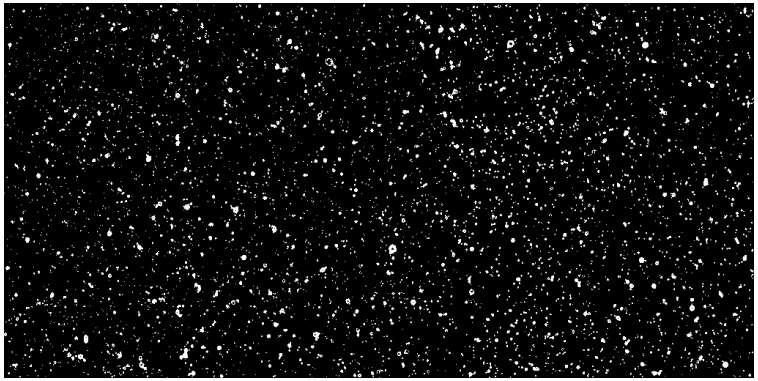
Irradiation tests ongoing

Test Beam campaigns and data analysis ongoing

^{55}Fe Radioactive source



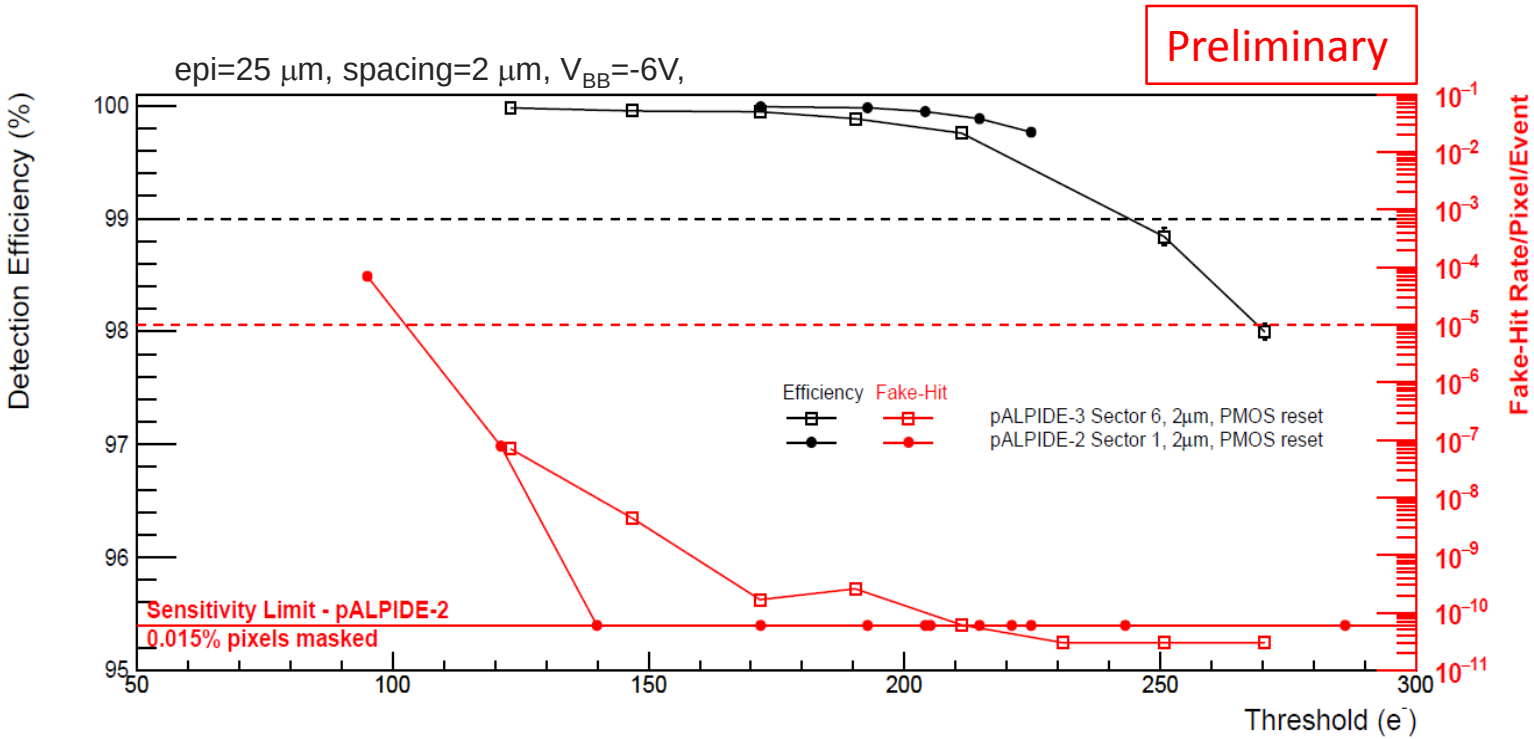
High occupancy event



SEU tests data, 200 MeV p at PSI

pALPIDE-3 Test Beam Results

Detection Efficiency and Fake Hit Rate, pALPIDE-3



ε_{det} > 99% @ λ_{fake} << 10^{-5} / event/pixel -> behavior of pALPIDE-2 reproduced with pALPIDE-3

Comparison of corresponding sectors of pixels with similar characteristics on pALPIDE-2 and pALPIDE-3 chips

25 μm high-resistivity epitaxial layer, -6 V reverse bias

Summary

ALPIDE Chip

Monolithic CMOS Pixel Sensor developed for the upgrade of the Inner Tracking System of the ALICE experiment at CERN LHC

Used also for the new Muon Forward Tracker (MFT) detector

Key features

15 mm × 30 mm, 512 × 1024 pixels, 29 μm x 27 μm pitch

High resistivity epitaxial layer, deep pwell, reverse bias

Ultra-low power analog front-end, in-pixel discrimination and multi-event buffer

Global Shutter (<10 us). Triggered or Continuous readout modes

Versatile interfaces and features for the integration of multi-chip modules

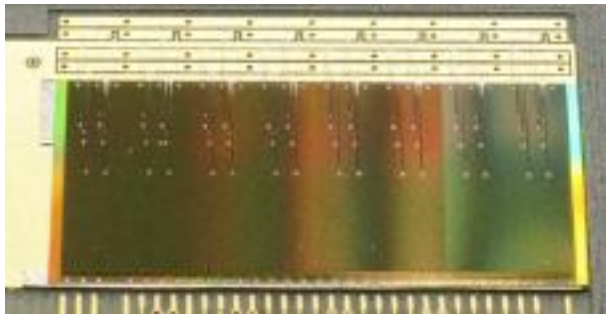
Power density < 35 mW/cm^2 (<20 mW/cm^2 with readout from parallel port)

Performance of full-scale prototypes in test beams

Detection Efficiency > 99%

Fake hit rate << 10^{-5} /event/pixel

Position resolution < 5 μm



SPARE SLIDES

pALPIDE-2 Test Beam

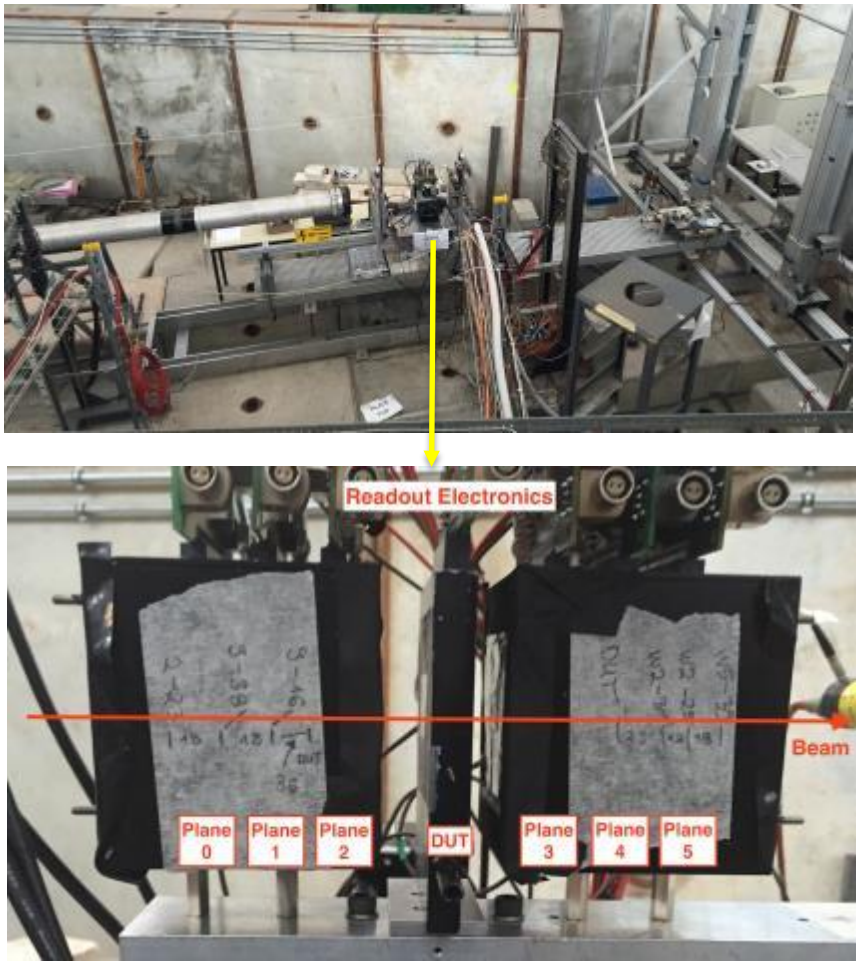
Several campaigns at different beam facilities

Set-up of Test Beam at CERN PS

- 6 GeV/c π^- beam
- 6 reference planes based on pALPIDE-1
- Single pALPIDE-2 as Device Under Test (DUT) in the center
- Track resolution of about 2.8 μm (<< 28 μm)

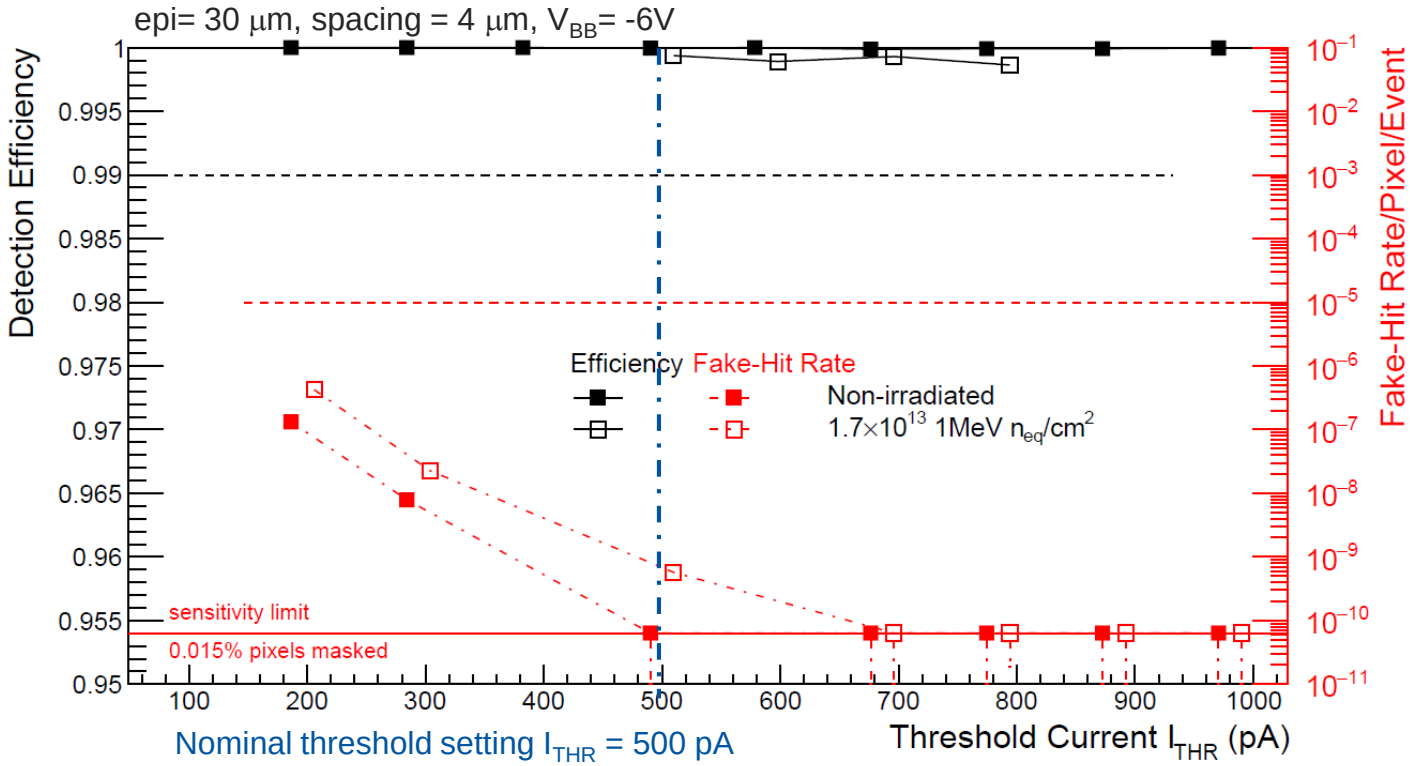
Analysis

- Extrapolate track from reference planes through DUT
- Search for clusters close to extrapolated impinging point -> *Detection Efficiency*
- Obtain *Cluster Size* and weighted hit position
- Compare extrapolated and actual position -> *Position Resolution*



pALPIDE-2 Test Beam Results

Detection Efficiency and Fake Hit Rate before and after irradiation



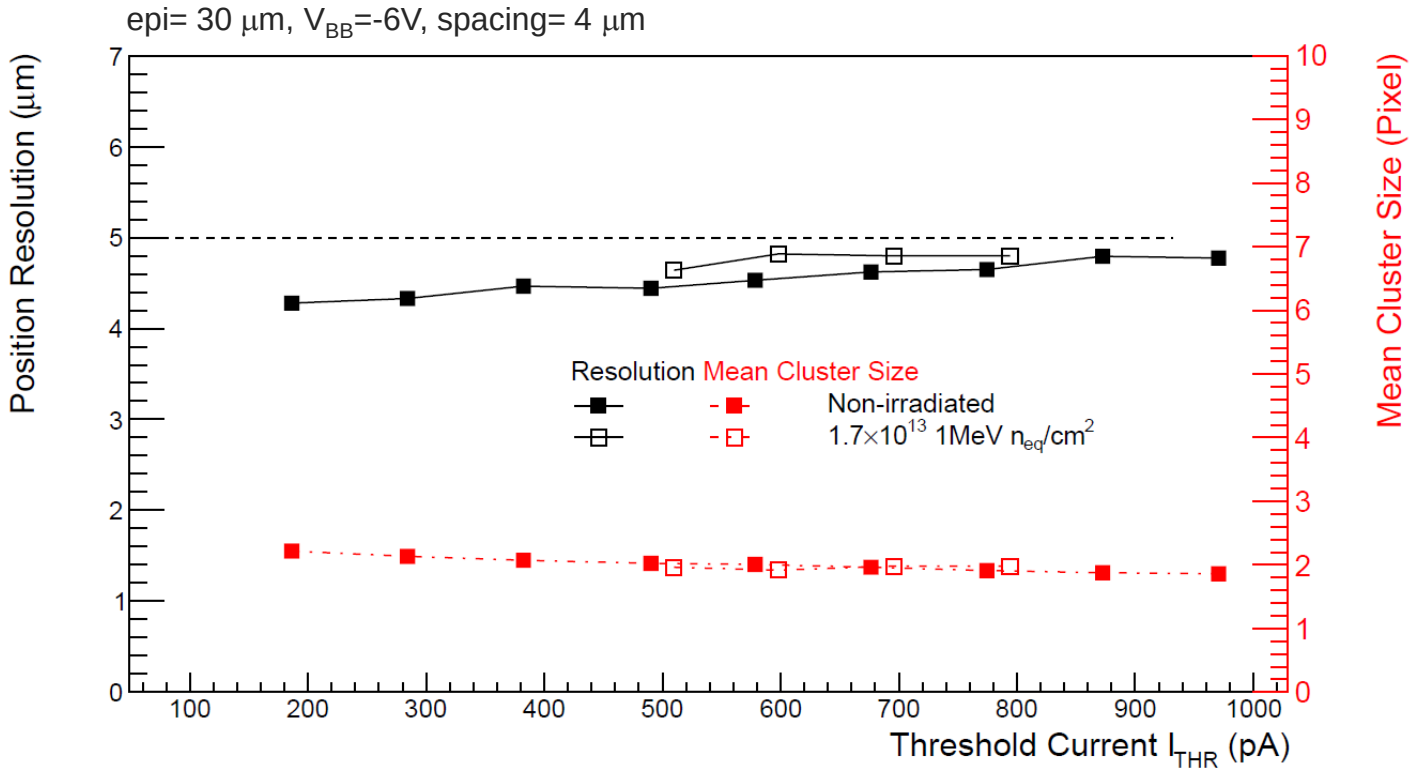
ε_{det} > 99% @ λ_{fake} << 10^{-5} / event/pixel -> large margin over design requirements

Measurements on chips with 30 μm high-resistivity epitaxial layer, thinned to 50 μm, -6 V reverse bias

1 non irradiated and 1 irradiated with $1.7 \cdot 10^{13}$ 1 MeV n_{eq}/cm^2

pALPIDE-2 Test Beam Results

Position Resolution and Cluster Size before and after irradiation



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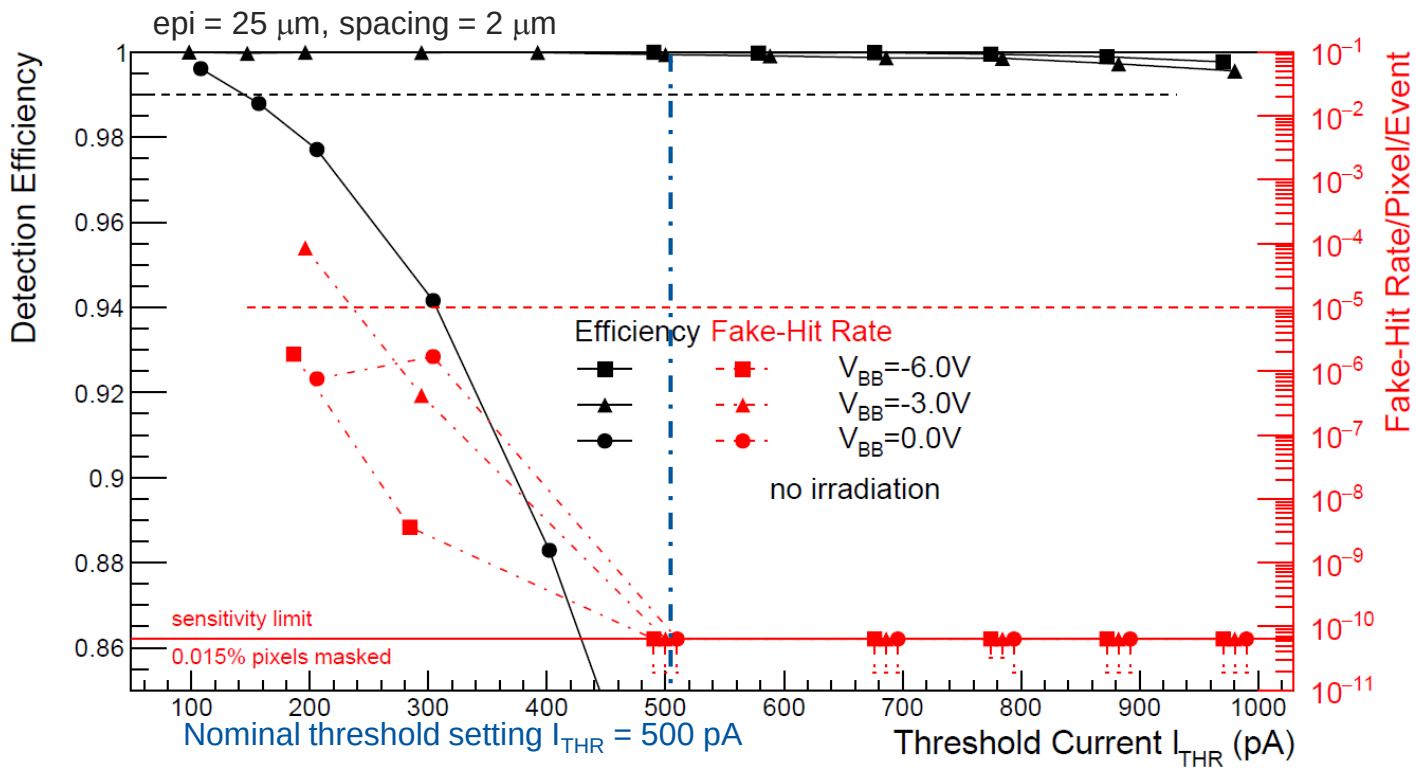
pALPIDE-2 Test Beam Results

Detection Efficiency and Fake Hit Rate vs. Reverse Bias

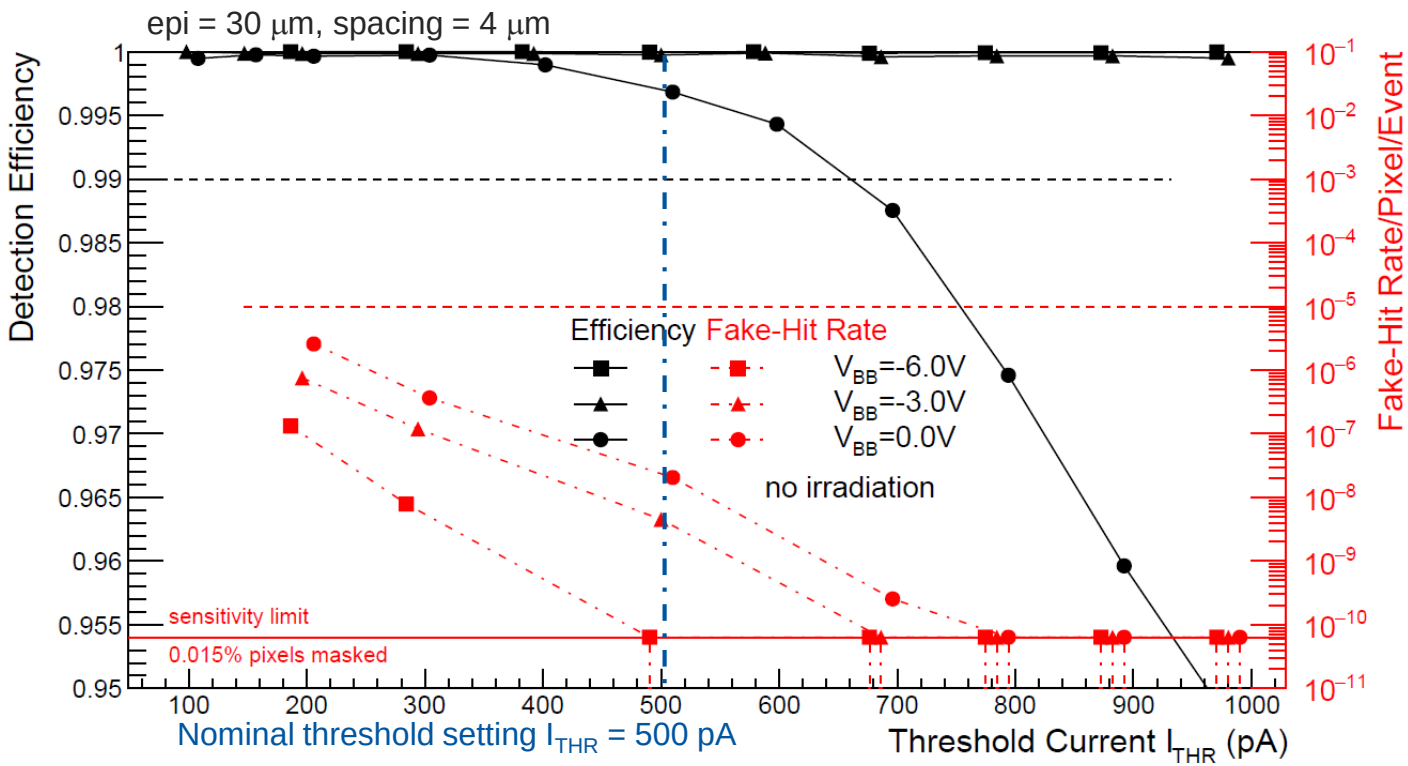


Detection efficiency significantly enhanced with **reverse bias**

Measurements on chip with 25 μm high-resistivity epitaxial layer, thinned to 50 μm

pALPIDE-2 Test Beam Results

Detection Efficiency and Fake Hit Rate vs. Reverse Bias

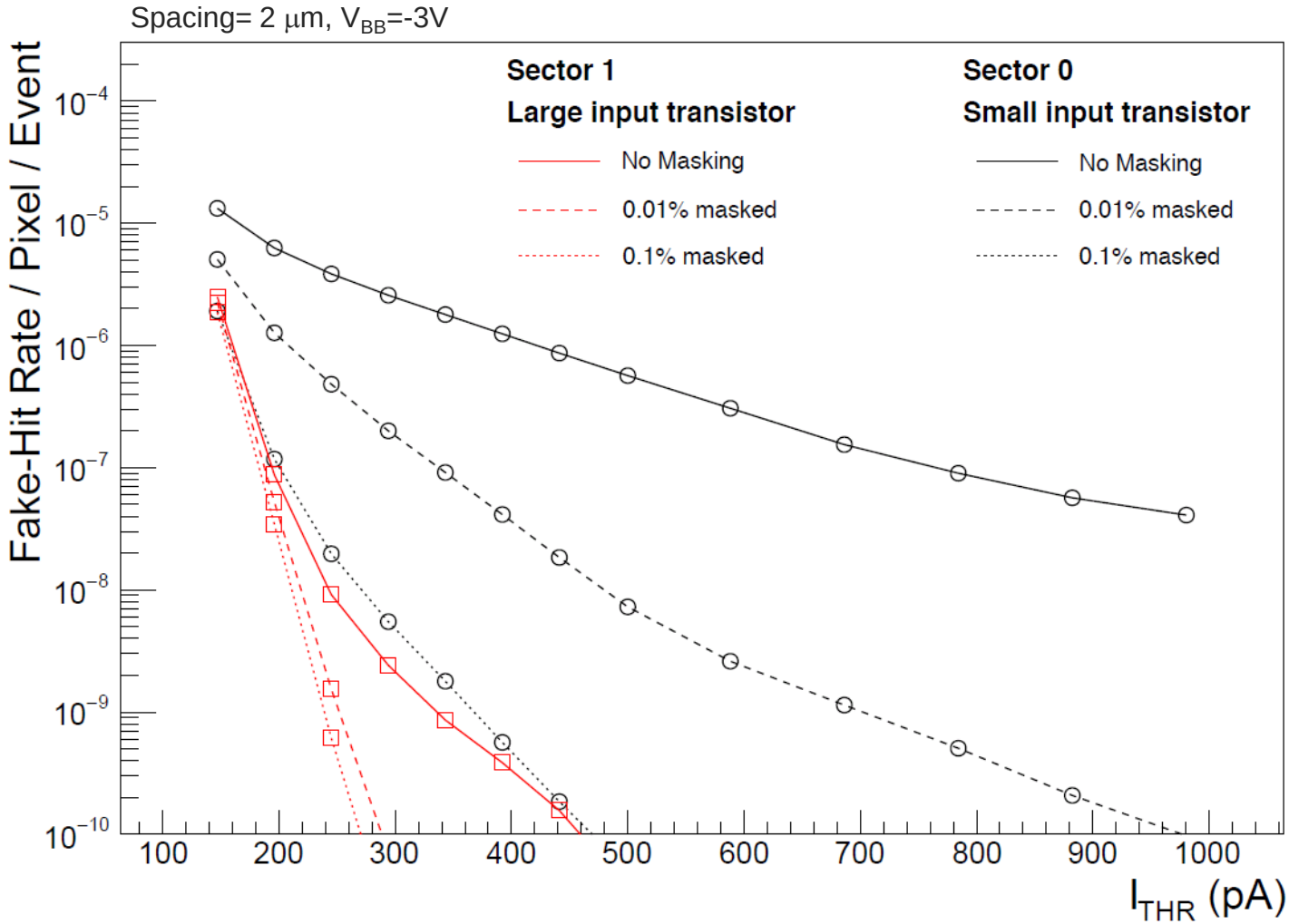


Operational margin significantly increased with **reverse bias**

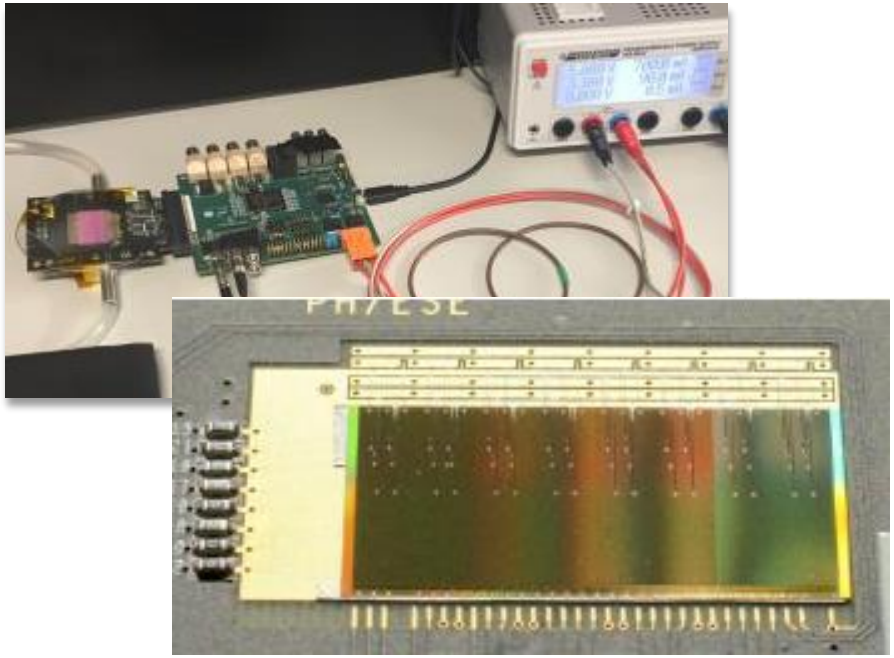
Measurements on chip with 30 μm high-resistivity epitaxial layer, thinned to 50 μm

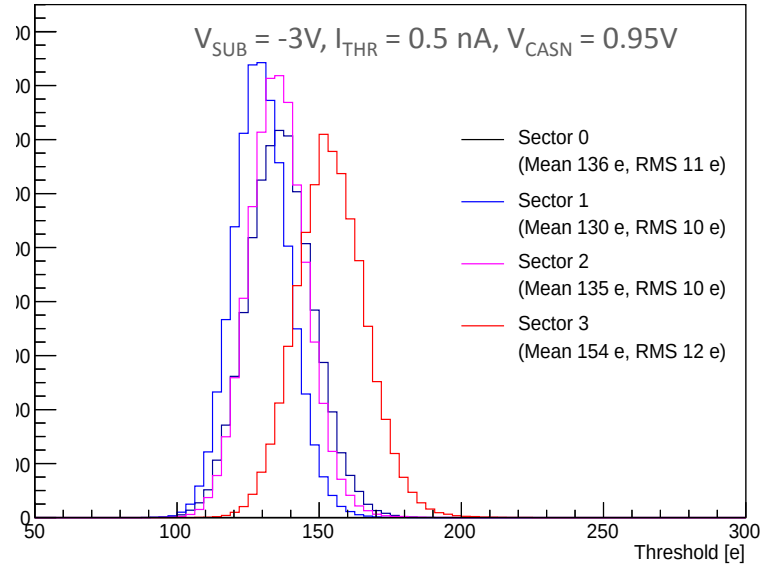
pALPIDE-2 laboratory measurements

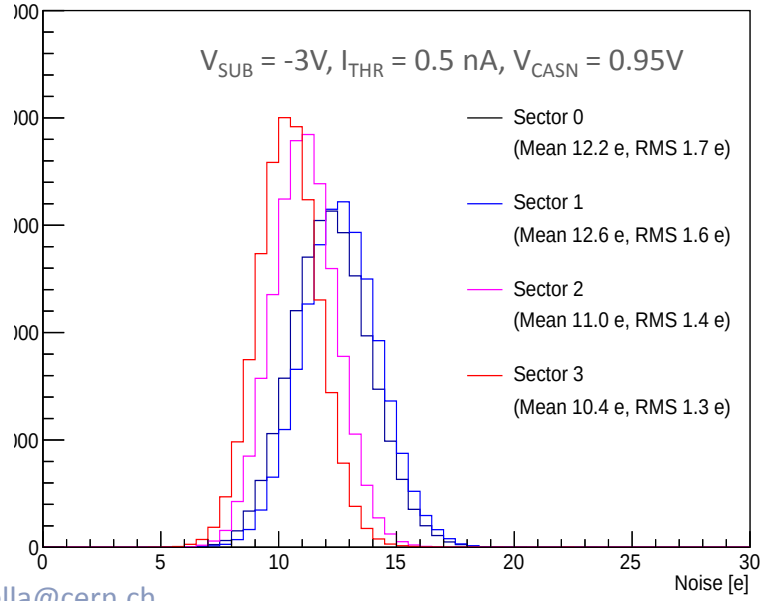
Fake hit rate vs input transistor area



pALPIDE-2 Laboratory Measurements





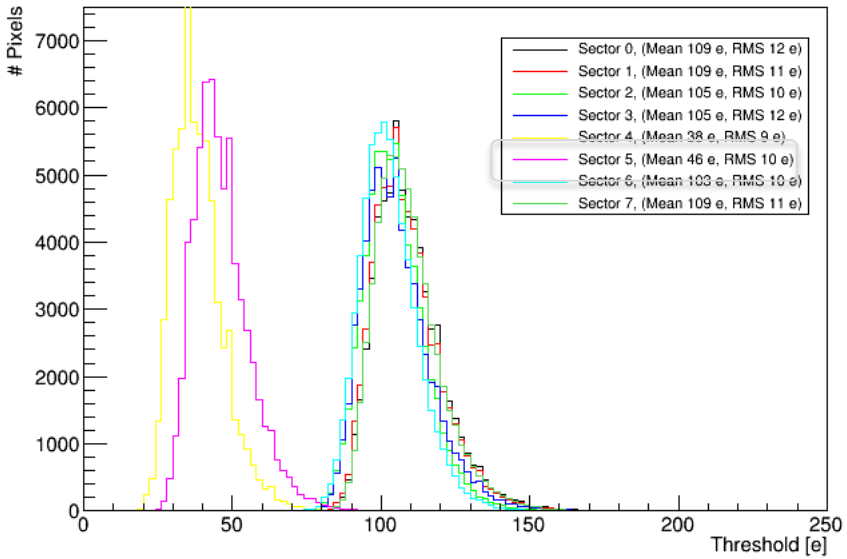


- All sectors present similar threshold and noise distributions
- Noise value comparable with threshold RMS
- Mean threshold 10x higher than noise
- Threshold 7x smaller than most-probable energy los signal of a MIP in 18μm of silicon

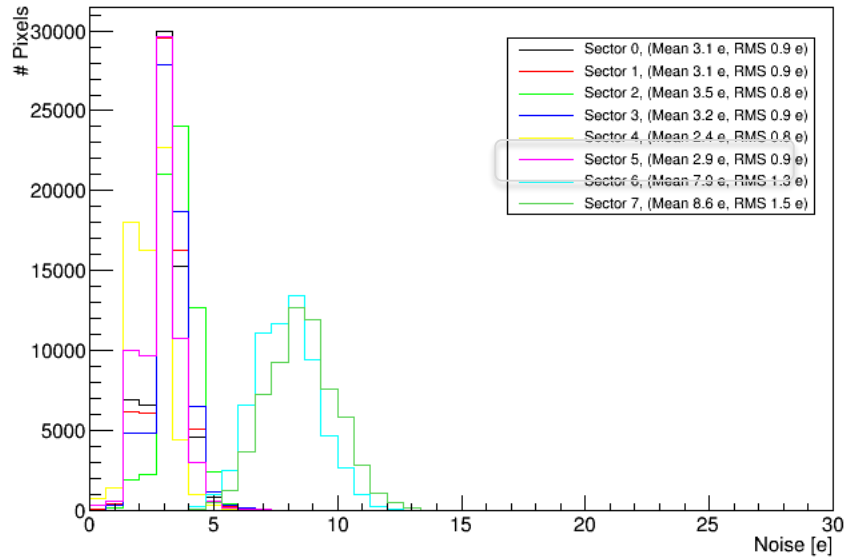
pALPIDE-3 Preliminary Results

Laboratory measurements

Threshold distribution



Noise distribution



8 sectors (pixel variants)

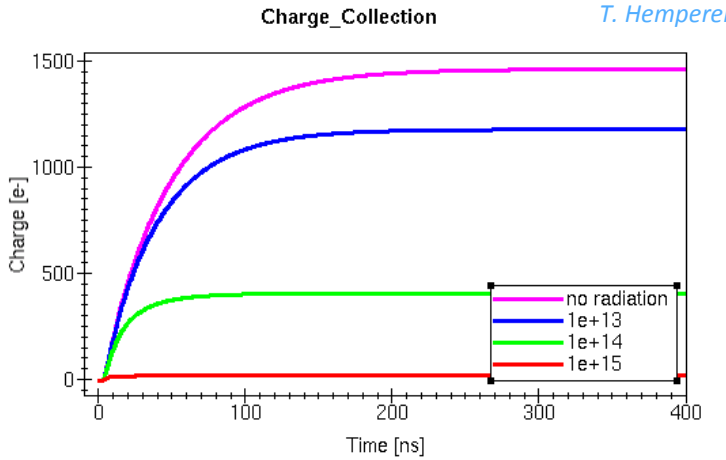
Sector 4 and 5 with higher gain -> lower thresholds

Sector 6 and 7 PMOS reset, remaining ones with diode reset

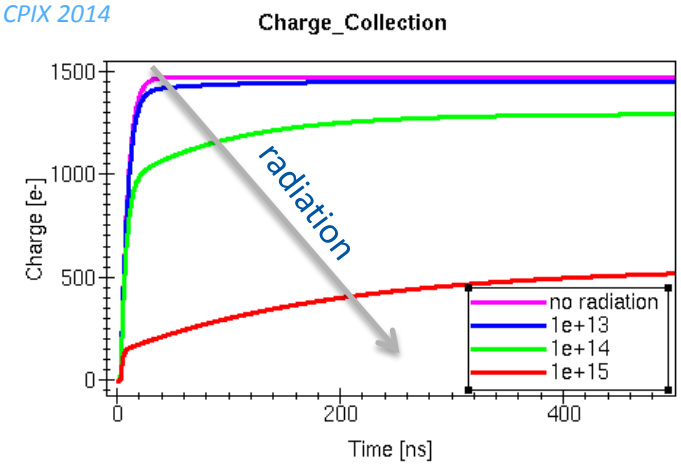
ITS Pixel Chip – epitaxial layer

Charge collection time and recombination depend on doping concentration (Si resistivity) and radiation induced dislocations

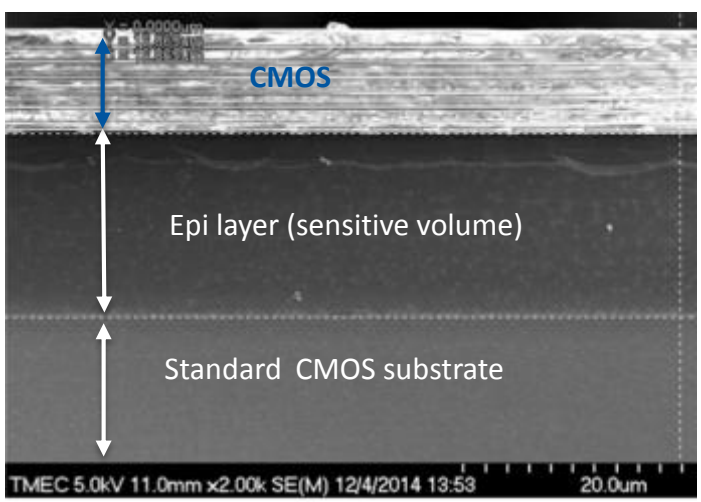
T. Hemperek (Uni Bonn) – CPIX 2014



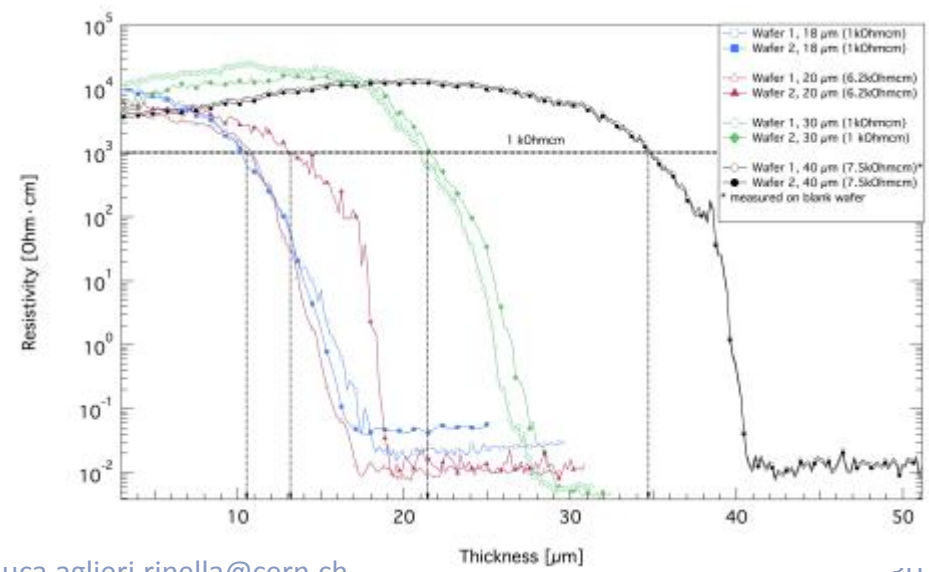
Substrate: 10 Ohm cm, NWELL: @1V PW: @ 0V



Substrate: 2k Ohm cm, NWELL: @1V PW: @ 0V

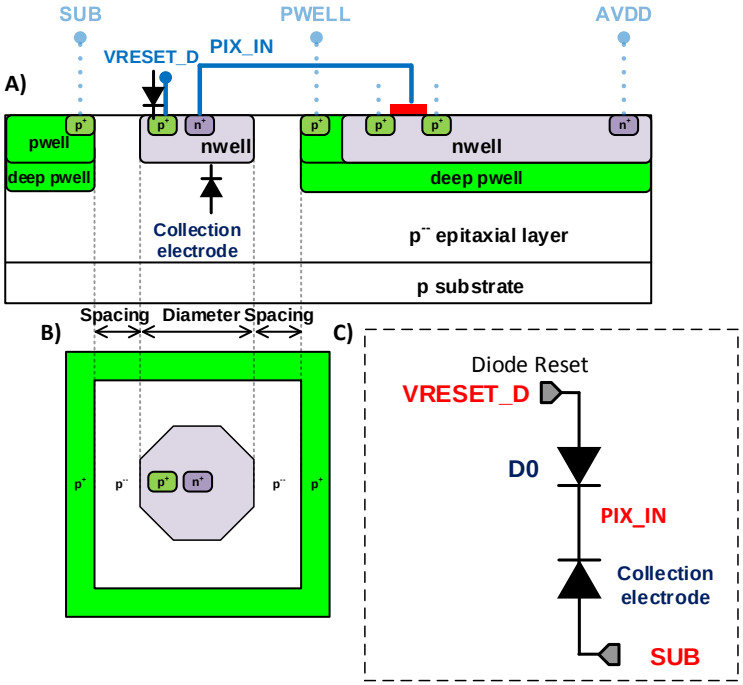


ALICE ITS, SEM picture of prototype chip

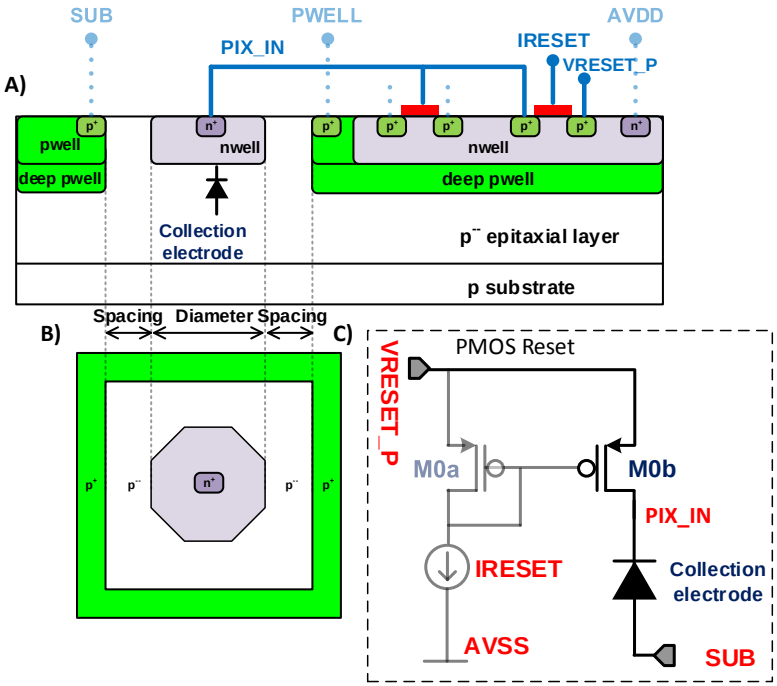


Charge collection electrode and reset

< Diode reset >

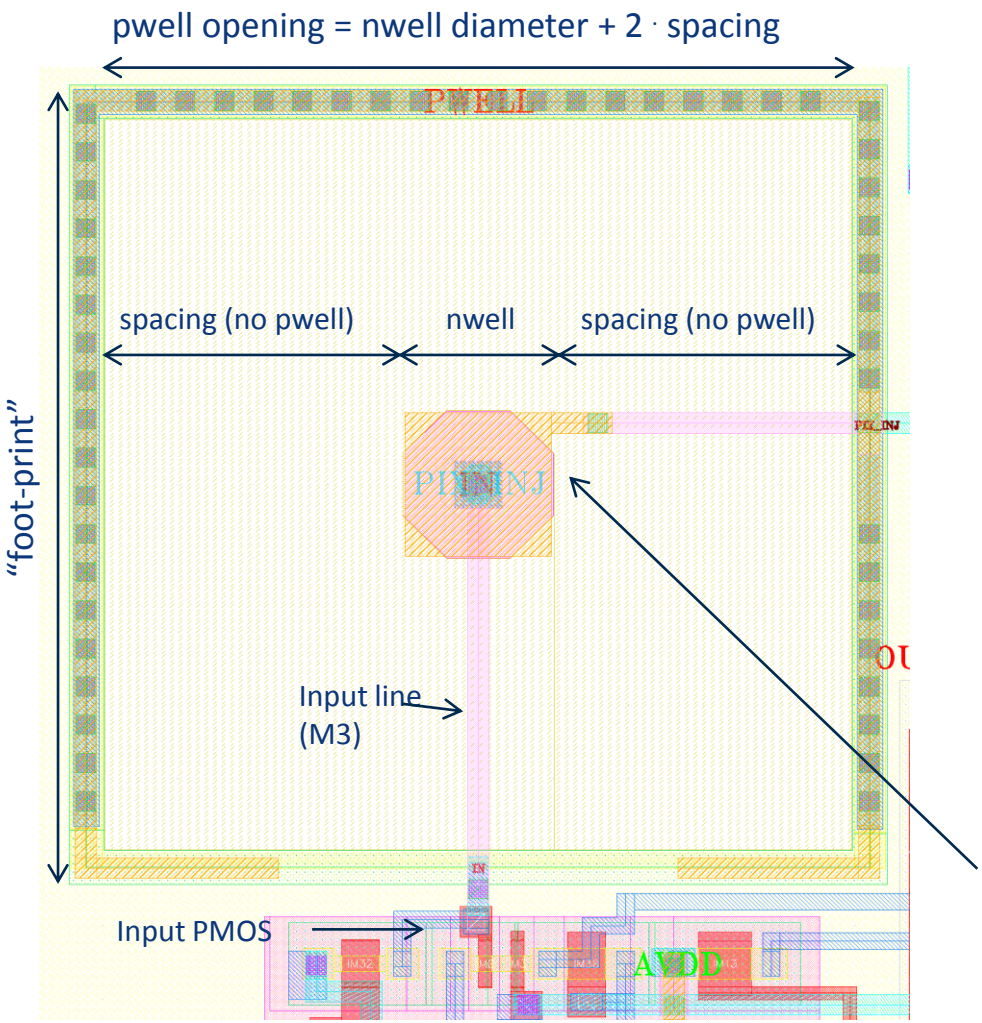


< PMOS reset >



- Sensor : collection electrode
  - Octagon shape with Diameter parameter
  - Spacing between NWELL and PWELL
- Reset mechanism
  - Diode reset : Reset current depends on the sensor leakage and signal amplitude
  - PMOS reset :
    - Reset current limited by IRESET (> leakage) → control on the reset circuit conductance
    - Additional capacitance on node PIX_IN

Collection Electrode



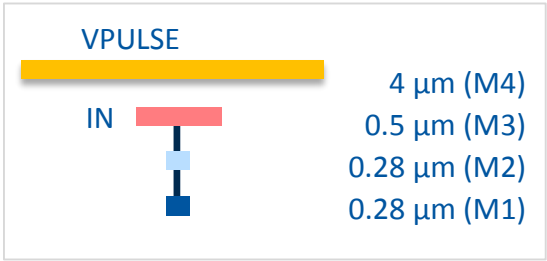
Spacings used on full scale prototypes:

pALPIDE-1 : 1, 2 and 4 µm

pALPIDE-2 : 2 and 4 µm

pALPIDE-3 : 2 and 3 µm

Pulsing capacitor (0.16 fF) cross section

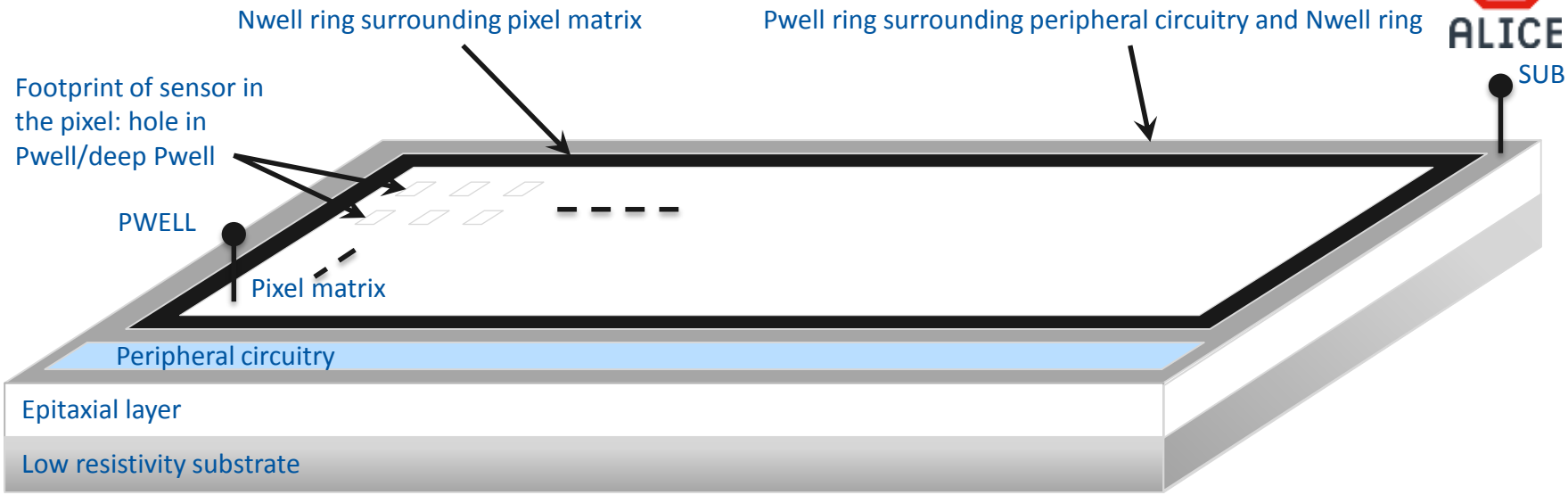


Evolution of full-scale prototypes

	Collection electrode to Pwell spacing	Multi(3)-event buffer in-pixel	General clock gating for power optimization	Chip-to-chip communication	1.2Gb/s serial output
pALPIDE-1	1, 2, 4 µm				
pALPIDE-2	2 and 4 µm			X	
pALPIDE-3	2 and 3 µm	X		X	X
ALPIDE	3..4 µm	X	X	X	X

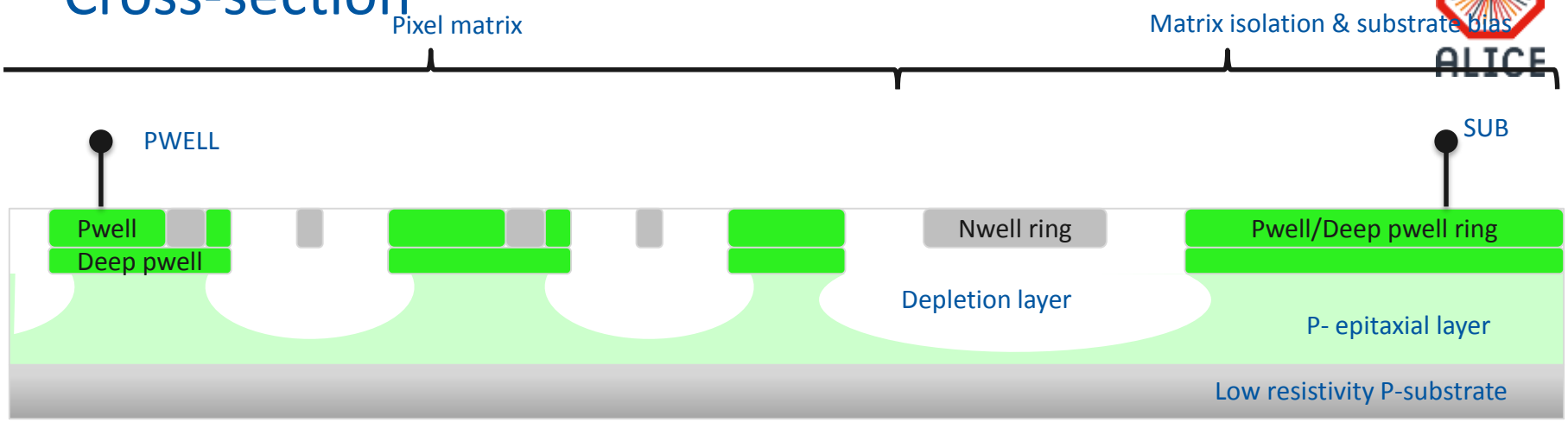
- Excellent sensor performance validated on pALPIDE-1&2
- pALPIDE-3 includes almost all features of final chip (missing: ADC)
- Towards ALPIDE:
  - Final pixel selection after characterization of pALPIDE-3
  - Power optimization on digital (clock-gating) and custom blocks like Data Transmission Unit
  - System features finalization: operation modes, testability, monitoring…

Matrix isolation and reverse substrate bias

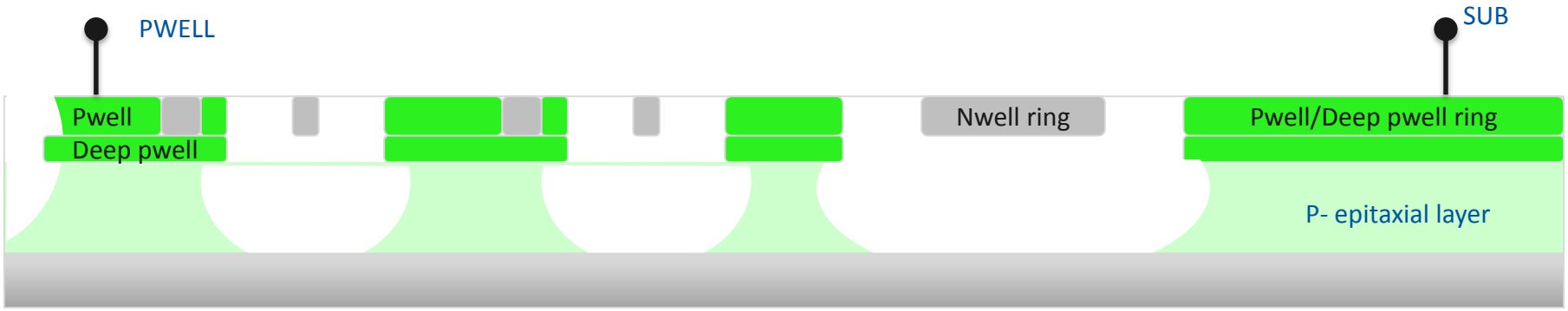


- The low resistivity substrate (SUB) is biased through Pwell ring surrounding peripheral circuitry and Nwell ring.
- The Nwell ring provides isolation of the pixel matrix from the rest of the chip.
- The Pwell (& deep pwell) within the matrix are biased using the pwell contact
- Substrate and Pwell within the pixel matrix are connected through the epitaxial layer if the epitaxial layer is not fully depleted.
- Peripheral circuit is implemented in triple well structure with Nwell and Deep Nwell, so is isolated from the substrate by the Nwell/DeepNwell to substrate diode.

Cross-section

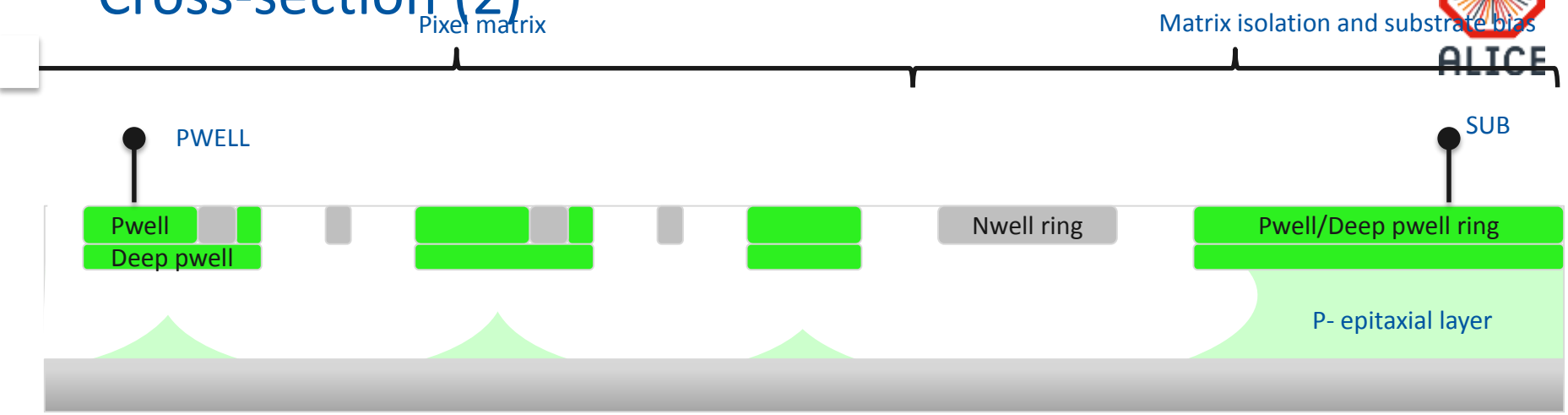


Very small reverse substrate bias



Larger reverse substrate bias

Cross-section (2)



If depletion fully extends underneath the pwell/deep pwell in the pixel matrix, pwell/deep pwell and P-substrate are isolated, otherwise they are connected by the undepleted part of the epitaxial layer. Such full extension will only be possible if the Pwell/Deep pwell occupies not too large a fraction of the pixel area.

Resistance between pwell/deep pwell ring and low resistivity substrate, for the largest epi resistivity and thickness:

$$R = r\frac{t}{A} \approx 8k\Omega\, cm\frac{0.0025cm}{0.03x3cm^2} \approx 220\Omega$$

Resistance between pwell in matrix and low resistivity substrate, for the largest epi resistivity and thickness, assuming only partial depletion:

$$R = r\frac{t}{A} \approx 8k\Omega\, cm\frac{0.0025cm}{0.7x1.4x3cm^2} \approx 6\Omega$$

ITS Modules Integration Requirements

Electrical connection to Flexible Printed Circuit

Solder-ball technique →
Large Pads Over Circuits

Same chip plays 3 roles

Inner Barrel Chip
Outer Barrel *Master*
Outer Barrel *Slave*

Minimum wiring on modules and to off detector electronics

Clock Link

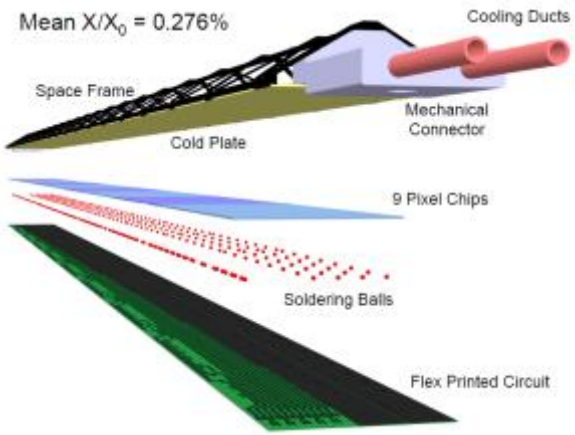
Control and Trigger Link

Data Link

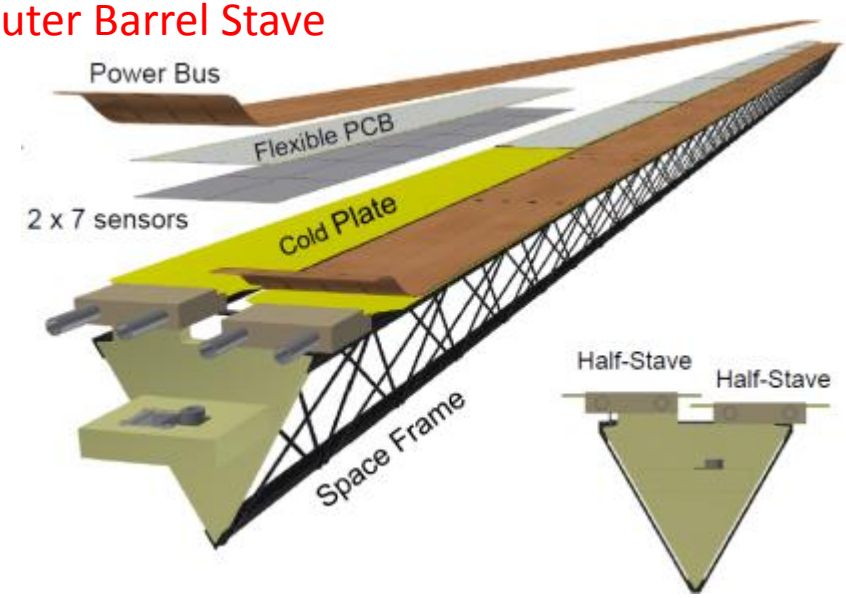
1.2 Gbs Inner Barrel

400 Mbps Outer Barrel Master

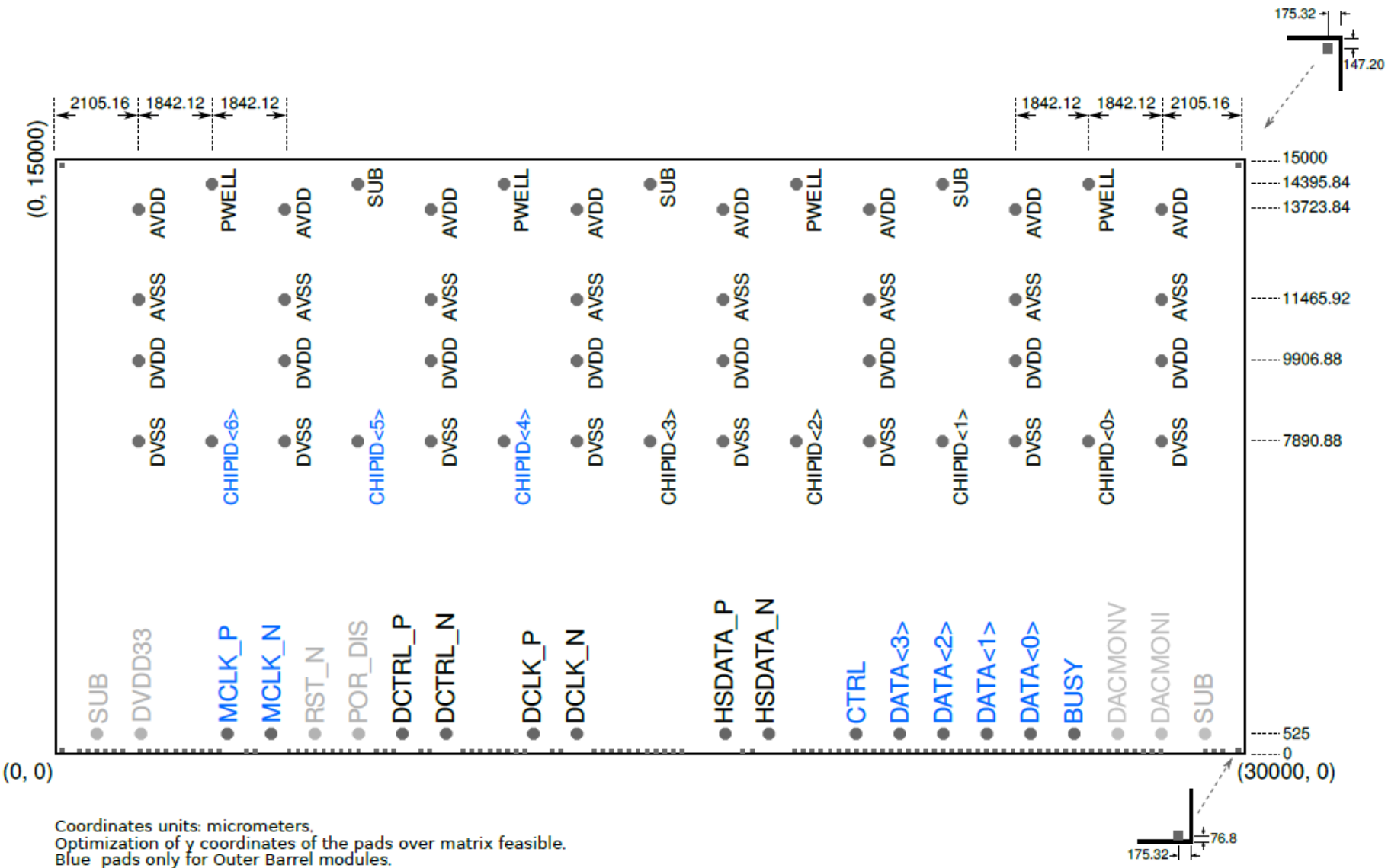
Inner Barrel Stave



Outer Barrel Stave

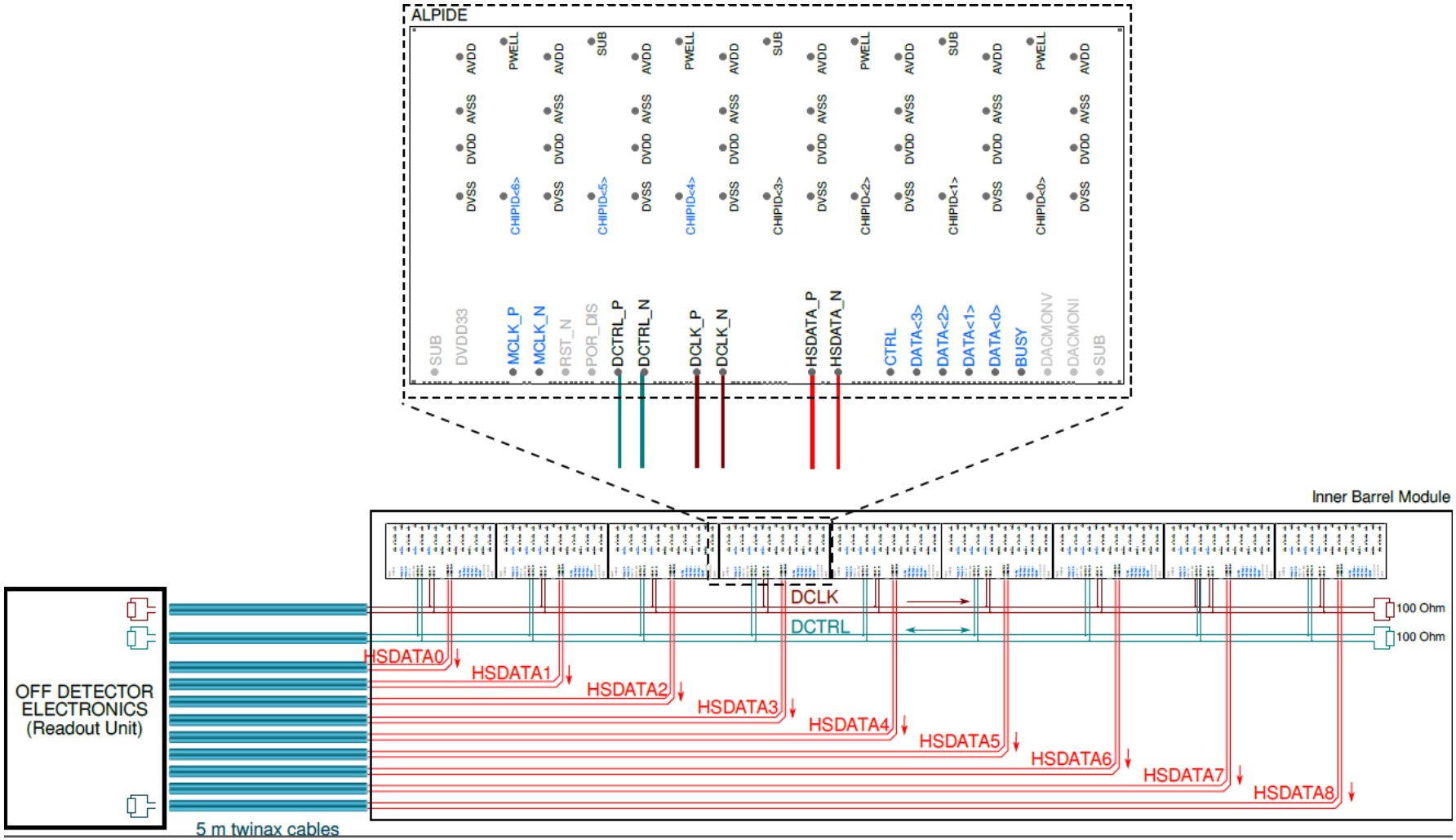


ALPIDE Pinout

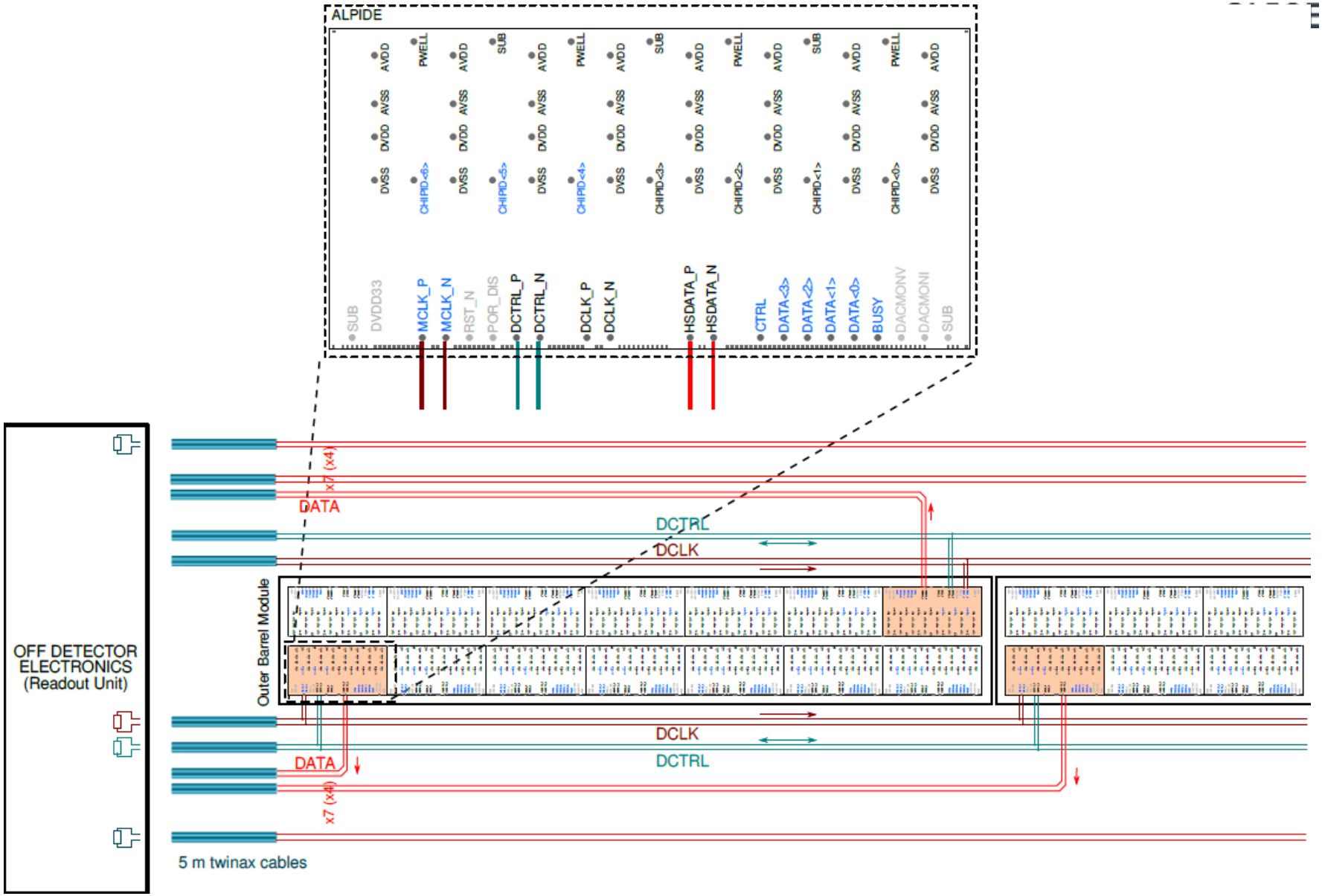


Coordinates units: micrometers.
Optimization of y coordinates of the pads over matrix feasible.
Blue pads only for Outer Barrel modules.
Light gray pads can be left unconnected and could disappear from the chip.

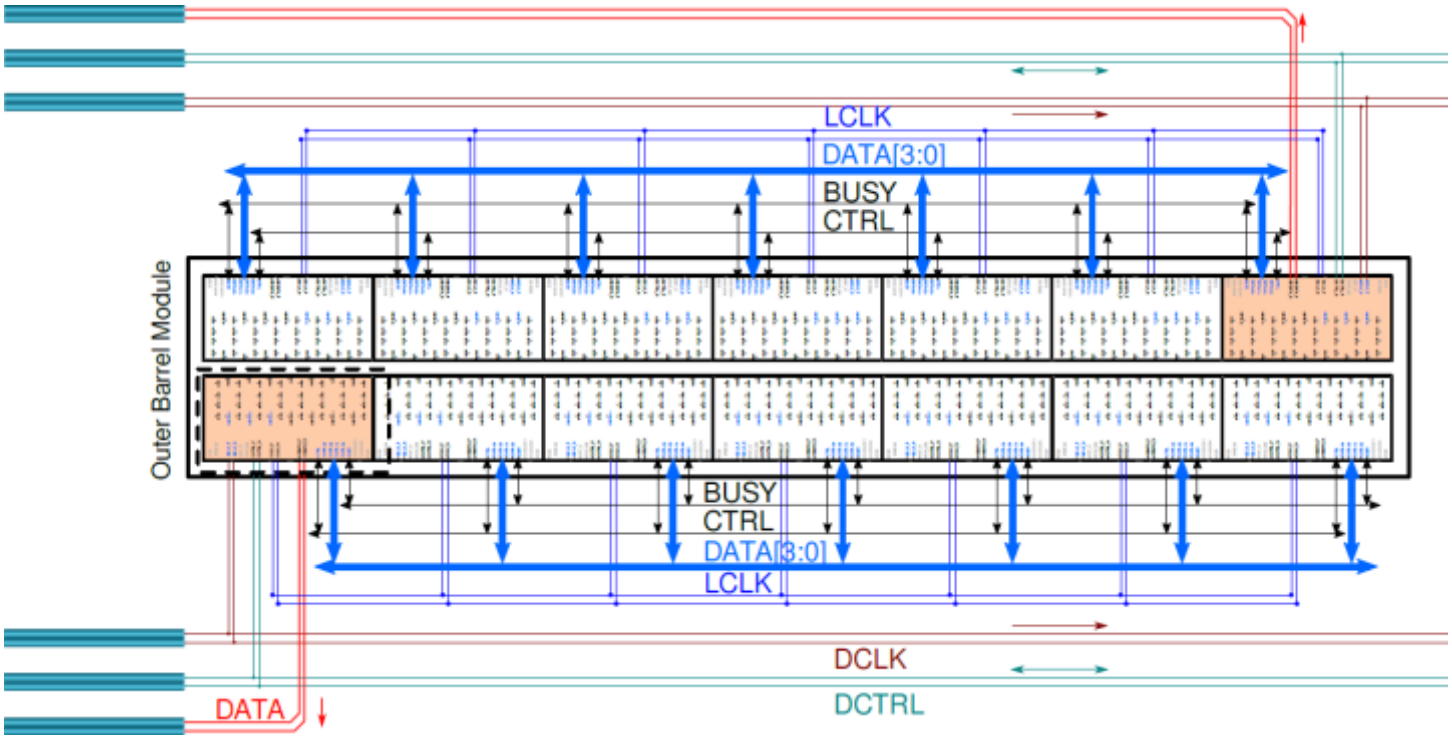
Inner Barrel Module



Outer Barrel Modules (2)

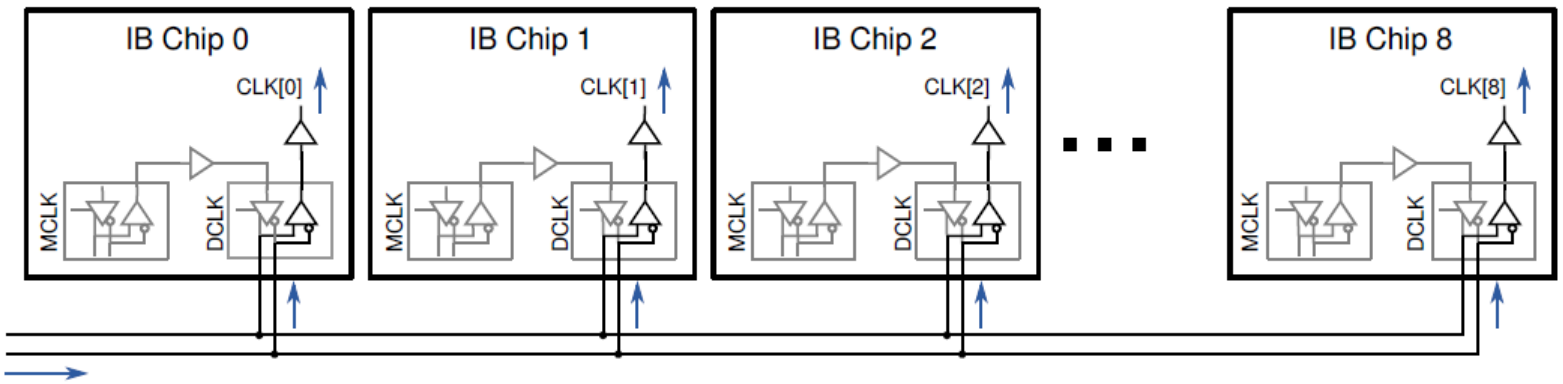


Outer Barrel Module (3), Local Buses

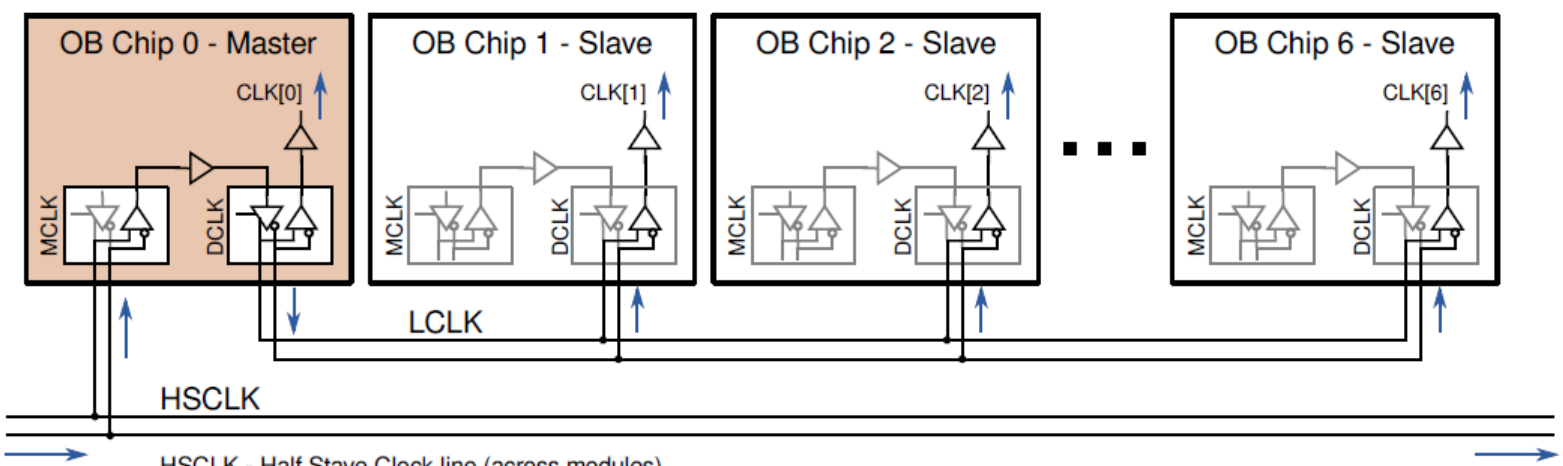


Clock distribution schemes

Inner Barrel Module



Outer Barrel Module



HSCLK - Half Stave Clock line (across modules)
LCLK - Local Clock line (half module)
CLK[6:0] - Chip core clock
On chip termination resistors of LCKL line enabled in Chip 0 and 6, disabled in Chips 1 to 5

Mitigation of Single Event Effects

Periphery Logic

Triple Modular Redundancy for state machines, control logic FIFO pointers

- Self-correction and SEU events counters
- TMR of asynchronous RESET trees
- *1 SEFI / 73 Myrs*

Registers based FIFOs with Hamming coding

- Full TMR for FIFO pointers
- *1 SEFI / 70 kyrs*

DPRAMs partially protected

- Data format bits protected with TMR or Hamming → Negligible SEFI rate
- SEU events can change the coordinate of a hit, prob. < 10^{-11} bit^{-1} << Fake hits

PLL and Serializer with TMR redundancy also against Single Event Transients

Pixel logic

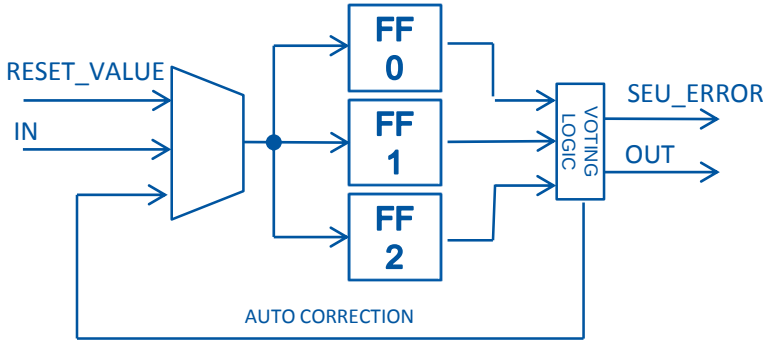
No area for redundancy

- Refresh the pixel *mask bit* in background (every several hours)

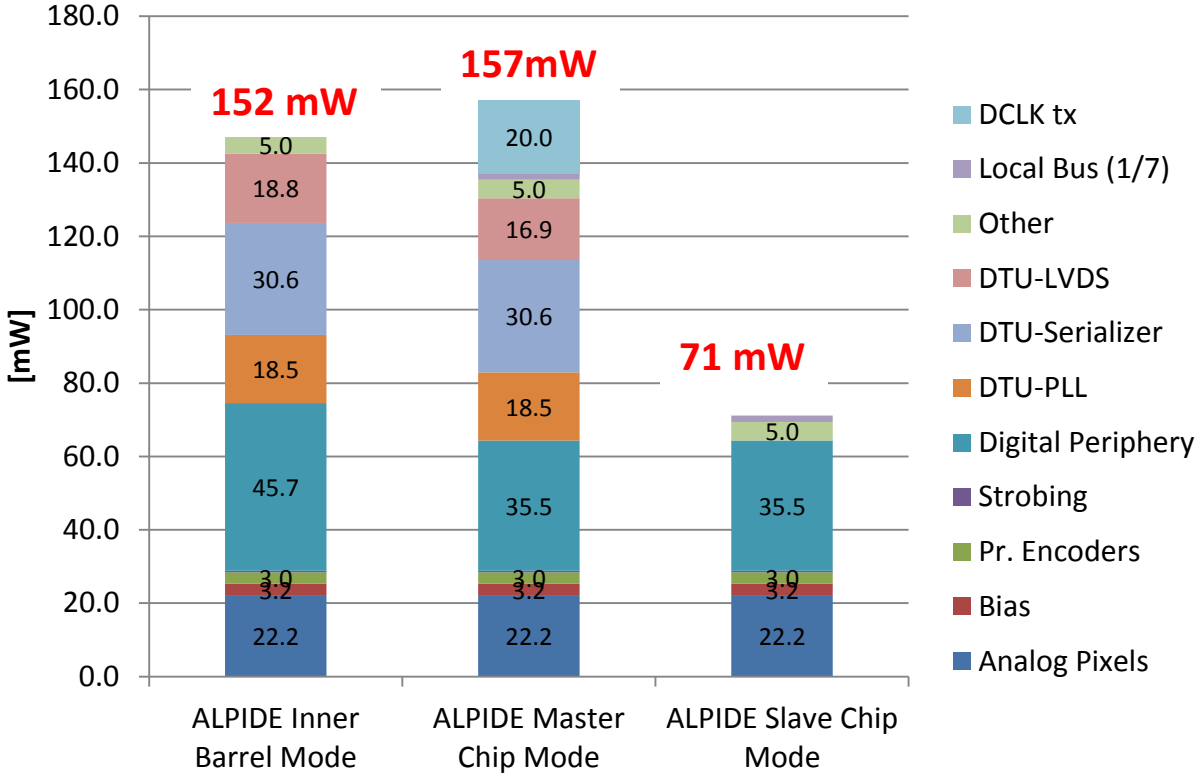
	Charged Hadron Flux (>20 MeV) [kHz/cm²]
Layer 0	**770**
Layer 3	**14**

	SEU Cross Section σ [cm²/bit]
Standard flops	**< 5×10^{-14}**
In-pixel flops	**< 2.5×10^{-13}**
DPRAM cell	**< 12×10^{-14}**

Basic TMR register cell



ALPIDE Power Breakdown



Inner Barrel: 34 mW/cm^2

Outer Barrel: 18.5 mW/cm^2

Chip and Modules Testability Features (1)

In-pixel pulsing

Test Charge Injection circuitry (*analog pulsing*)

In-Pixel state latches can be written from control (*digital pulsing*)

Arbitrary hit pattern can be forced into the pixels memories

Analog DACs monitoring ports

On-chip DACs can be monitored through DACMONV, DACMONI analog pads

Chip and Modules Testability Features (2)

Digital Periphery

- Write/Read to all locations of **SRAM blocks** from control interface
- Digital **State and Inputs snapshot**
  - All internal states (SMs, Counters, FIFO pointers) and chip inputs can be latched in shadow registers. Sampling triggered by dedicated broadcast command.
  - Shadow registers readable from control port during normal readout activity
- Direct drive of chip outputs via Control Interface
  - Chip-to-chip communication testing
  - OB Module connectivity testing
- **Counters of Single Event Upset events** in Flip-Flops
  - Single bit flip events in registers are self-corrected and counted

DTU test features

- Internal pattern generator driving DTU parallel input (constant, counter, PRBS)
- Monitor and counter of PLL transitions to lock state