The RD53 effort towards the development of a 65 nm CMOS pixel readout chip for extreme data rates and radiation levels

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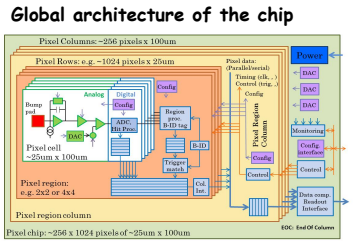
Abstract

The next generation of silicon pixel detectors for the phase-II upgrade of ATLAS and CMS at the High Luminosity LHC sets unprecedented requirements to the microelectronic readout systems. Front-end integrated circuits must provide advanced analog and digital functions in pixel readout cells with a pitch of a few tens of a μm. Operating at low power dissipation, they must handle huge data rates and stand extreme radiation levels. The community of designers is studying the 65nm CMOS technology as a tool to achieve the ambitious goals of these future pixel systems, and has organized itself in the RD53 project to tackle the challenges associated with mixed-signal design in this process.

New challenges of the RD53 collaboration

Global architecture of the chip



- 95% digital, Charge digitization
- ~256k pixel channels per chip
- Pixel regions with buffering
- Data compression in End Of Column
- Chip must work with large pixels for outer layers

ATLAS and CMS Phase 2 Pixel Detector Requirements:

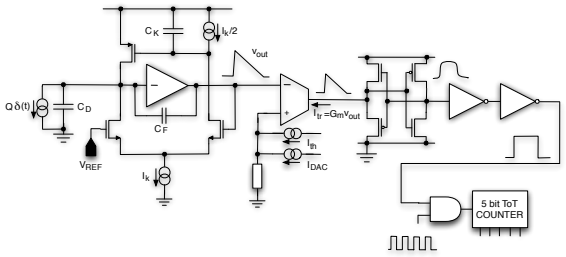
- Small pixels: 50x50 μm² (or 25x100 μm²)
- Large chips: > 2cm x 2cm (~1 billion transistors)
- Hit rates: ~3 GHz/cm²
- Radiation: 1 Grad, 10^{16} n/cm² (unprecedented)
- Trigger: 1 MHz, 10 μs (~100x buffering and readout)
- Total power budget: ≤ 1 W/cm²
- Minimum threshold: 1000 electrons

RD53 Goals

- Detailed understanding of radiation effects in 65nm
- Development of a simulation and verification framework with realistic hit generation
- Design and test of small-medium size pixel readout chips
- Design of a shared rad-hard IPs library
- Design, characterization and test beam of common engineering run with full sized pixel array chip > 1cm²

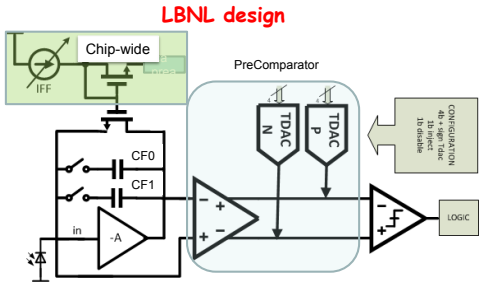
Analog Front-end design

INFN-Pavia design



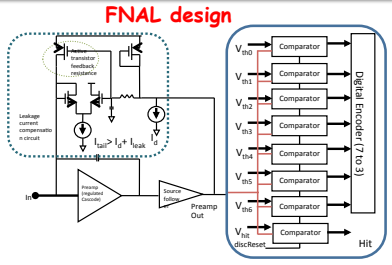
- Single amplification stage for minimum power dissipation
- Krummenacher feedback to comply with the expected large increase in the detector leakage current
- High speed, low power current comparator
- Relatively slow ToT clock – 40 MHz (using both CLK edges)
- 5 bit counter – 400 ns maximum time over threshold
- 30000 electron maximum input charge, ~450 mV preamplifier output dynamic range
- Selectable gain and recovery current

LBNL design



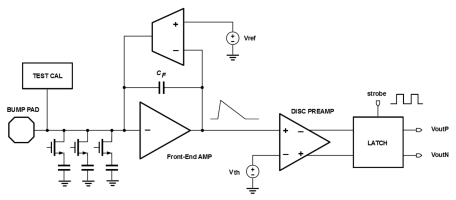
- Based on the new geometry C_D of 100fF maximum is assumed
- Leakage current compensation a la FEI4 (not shown), 10nA nominal
- 5b (4b + sign) tuning DAC
- Few different variants are considered
- Globally settable feedback cap (2bit)
- Target total analog current is <5 μA/pixel

FNAL design



- **Synchronous** front-end
- Preamplifier (Regulated cascode) with an active feedback transistor and a leakage current compensation circuit
- Comparator: compact, single-ended architecture, AC coupled to the preamplifier, does not require trimming DACs, 12.5ns reset phase; 12.5ns active comparison, 2nd stage has additional gain with positive regeneration
- Zero dead time (can latch hits in adjacent bunch crossings)
- Require distribution of BXclk across a large chip

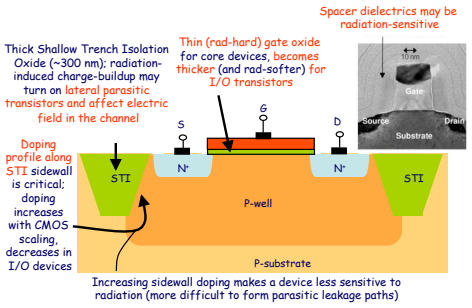
INFN-Torino design

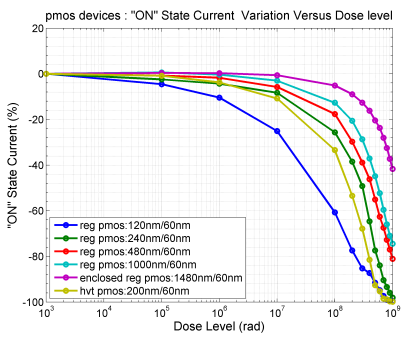


- Single stage front end with CSA + synch discriminator
- Low power: <6 μW/pixel cell [<0.24 W/cm²]
- Low noise: <100e rms for C_D~100 fF
- Fast peak-time: below 25ns
- ToT: 30ke- signal max into max 250nsec
- High resolution of digital information: 5 to 8 bits configurable
- No-threshold trimming with DAC
- Autozero comparator

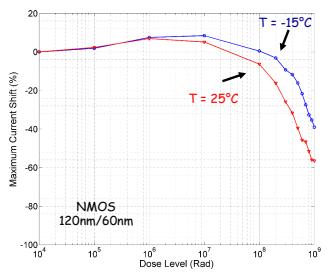
Radiation tolerance

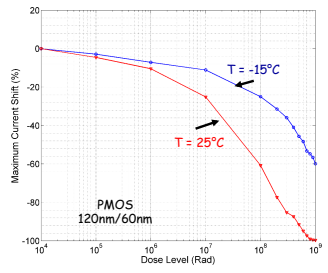
- At the HL-LHC design luminosity, for an operational lifetime of 10 years, the innermost pixel layer will be exposed to a total ionizing dose of 1 Grad, and to an equivalent fluence of 1-MeV neutrons of 2 x 10^{16} n/cm²
- If the degradation is unacceptable, **a replacement strategy** must be applied for inner pixel layers.
- Nanoscale CMOS (with very thin gate oxide) has a large intrinsic degree of tolerance to ionizing radiation: what happens at 1 Grad?
- Radiation induced electric charge is associated with thick lateral isolation oxides





- Among other effects, PMOSFETs (especially minimum size ones) show a large transconductance degradation, which becomes very steep over 100 Mrad (partial recover after annealing)
- This is probably not so critical for the design of analog blocks, where minimum size transistors can be avoided if necessary; the study of radiation effects on noise is ongoing
- Damage mechanisms have yet to be fully understood; they appear to be **less severe at** the foreseen operating temperature of the pixel detector at HL-LHC (**about -15 °C**)



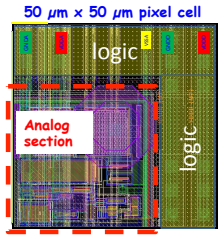


Top Level and Chip Integration

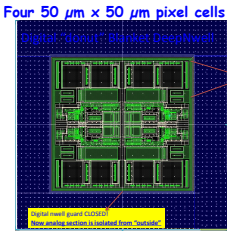
Pixel analog front-end inside a large mixed-signal (mostly digital) integrated system -> the **"analog island"** concept

- In modern pixel readout chips, the analog front-end cell is embedded in an extremely complex microelectronic system, where analog and digital circuits coexist in the same small readout cell
- A correct layout is crucial to avoid digital interferences in the low-noise analog front-end; immunity to disturbances on analog supply lines ("PSRR") is also essential

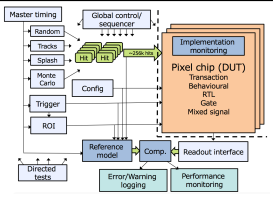
50 μm x 50 μm pixel cell



Four 50 μm x 50 μm pixel cells

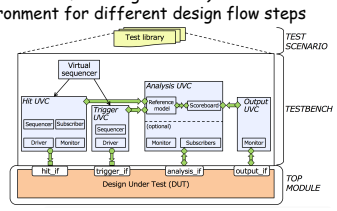


Simulation



VEPIX53: Verification Environment for RD53 PIXel chips
Implemented in SystemVerilog + UVM library (advanced verification features)
- hit generation and injection
- monitoring of pixel chip input and output
- conformity checks and statistics collection

Requirements
- flexible generation of input stimulus (constrained-random + directed tests (extreme cases); imported from sensor/MC simulations; combination of the two)
- simulation at different levels of description
- automated verification: (statistics on performance, generation and classification of warnings/errors)
- same environment for different design flow steps



I/O

Requirements
1. Single (differential) input line —> Encoding Clock and Data
2. Continuous triggering Capability
3. DC balancing (8b/10b encoding)
4. Run length less or equal to 6 (like in 8b/10b encoding)
5. Clock Phase alignment (needed because Clk frequency > 40MHz)
6. LPGBT compatibility
7. Low Trigger latency
8. Immunity to (at least) one bit flip on the line per data word
9. Full chip operation (during Run and Configuration phases)

Two possible solutions
- Input speed baseline will be 160 Mbps
- DC balancing is achieved without using 8b/10b encoding
- Using 8 bit wide data symbols —> 2 machine clock cycles per symbol
- Provide DC balancing choosing data symbols only amongst the 70 available ones

IP Blocks

- Band Gap
- Monitoring ADC
- Temperature Sensor
- Radiation Sensor
- Config. Memories
- DAC
- SRAM Pix/EOC
- SLVDS driver/receiver
- PLL
- SER/DES
- CDR
- Shunt LDO
- Rail-to-Rail Analog Buff
- Power-ON Reset
- VCO
- EFUSE

RD53 Institutes

- INFN Bari and Politecnico di Bari
- Bonn
- CERN
- CPPM
- Fermi National Accelerator Laboratory
- Lawrence Berkeley National Laboratory
- Laboratoire de Physique Nucléaire et de Hautes Energies, Paris
- Laboratoire de Physique Subatomique et de Cosmologie (LPSC)
- Laboratoire d'Annecy-le-Vieux de Physique des Particules (LAPP)
- NIKHEF
- University of New Mexico
- INFN Milano and University of Milano
- INFN Padova and University of Padova
- INFN Pavia, University of Pavia and University of Bergamo
- INFN Pisa and University of Pisa
- INFN Perugia and University of Perugia
- Institute of Physics and Czech Technical University
- Paul Scherrer Institute
- Rutherford Appleton Laboratory
- University of California Santa Cruz
- INFN Torino and University of Torino
- University of Sevilla and Instituto de Fisica de Cantabria

Frontier Detector for Frontier Physics - 13th Pisa Meeting on Advanced Detectors, May 24 – 30, 2015, La Biodola, Isola d'Elba (Italy)