

White Rabbit status and roadmap

Javier Serrano

CERN BE-CO
Hardware and Timing section

Geneva, 23 June 2015

1 Some background

2 Status

3 Roadmap

Outline

1 Some background

2 Status

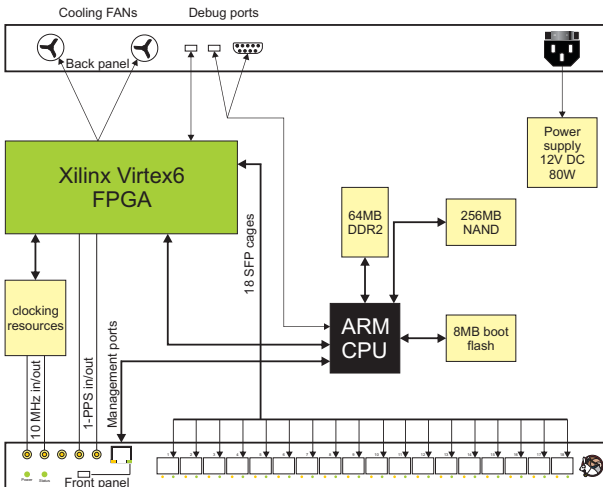
3 Roadmap

White Rabbit Switch

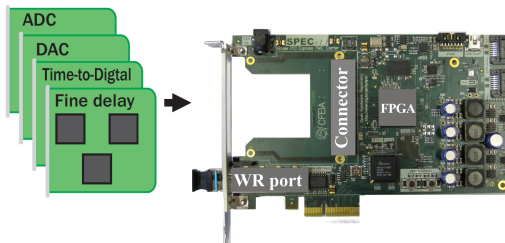


- Central element of WR network
- Original design optimized for timing, designed from scratch
- 18 1000BASE-BX10 ports
- Open design (H/W and S/W)
- Commercially available

White Rabbit Switch inside



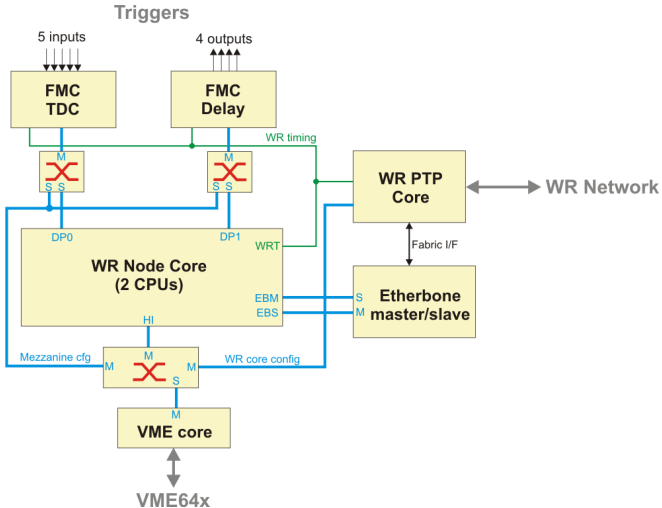
WR Node example : SPEC board



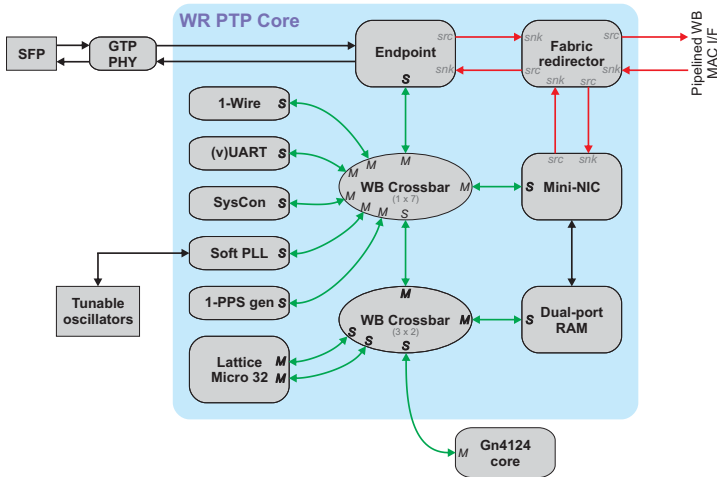
FMC-based Hardware Kit

- All carrier cards are equipped with a White Rabbit port.
- Mezzanines can use the accurate clock signal and “TAI” (synchronous sampling clock, trigger time tag, ...).

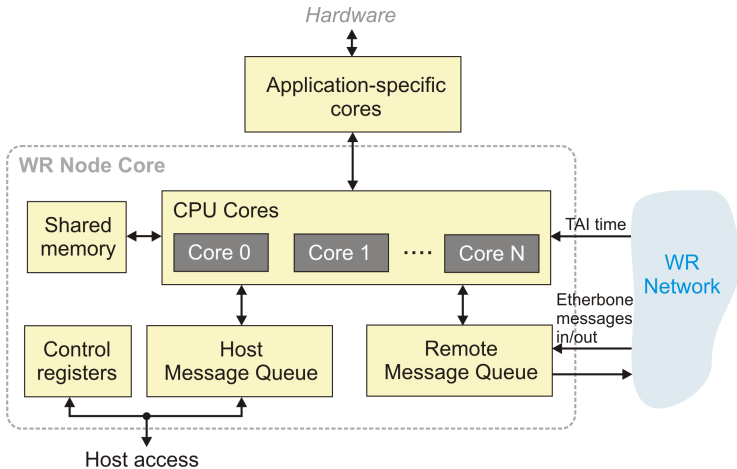
Example White Rabbit node



White Rabbit PTP Core



White Rabbit Node Core



Outline

1 Some background

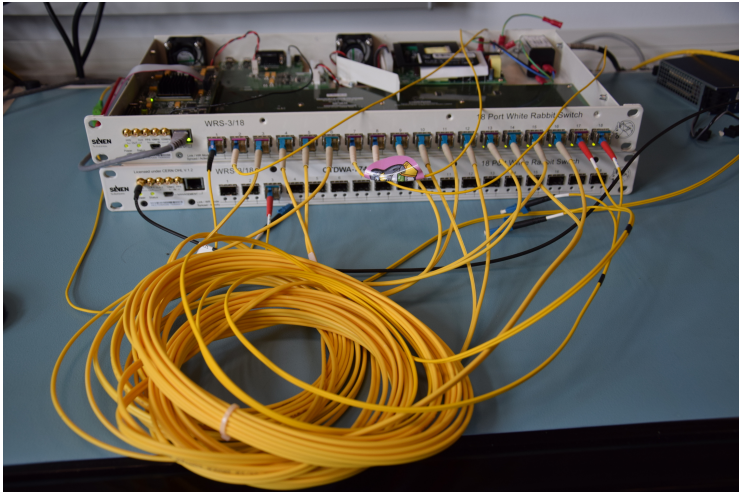
2 Status

3 Roadmap

Switch status

- Version 4.1.2 of gateway/software released in December 2014.
- Supports 3.4 hardware.
- Supports VLANs and statistics.
- Still some bugs visible at high loads.

Snake test for the switch



Node status

- Several applications operational, using SPEC and SVEC, e.g. LHC instability studies.
- The WR Node Core makes application development faster and easier.
- Ironing out a few bugs in PPSi.

Outline

1 Some background

2 Status

3 Roadmap

Switch roadmap

Short term

- Fix all bugs uncovered by snake test.
- Complete SNMP support.
- Add monit support to detect and restart stopped processes.
- Update documentation.
- Release in July 2015.

Medium term

- End of Summer: support for MTTF/MTBF estimation. Logging up time, temperatures. . .
- Q4 2015: update buildroot to latest version.
- 2016: clock and data switch-over, clock hold-over.

Node roadmap

Short term

- Fix PPSi bugs.
- Improve WR Node Core and offer it as a documented service.
- RF distribution over WR.

Medium term

- Integrate WR into CERN's General Machine Timing system.
- Integrate new RISC-V processor core into WRNC.