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Dániel Darvas (EN-ICE-PLC)

Formal verification of industrial control systems… at CERN

1st Developers@CERN Forum
29/09/2015

Contains joint work of B. Fernández, E. Blanco, S. Bliudze, J.O. Blech,
J-C. Tournier, T. Bartha, A. Vörös, I. Majzik, R. Speroni, M. Lettrich

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http://go.cern.ch/**7L9h**

Source: http://www.iphonetextgenerator.com/

Context – CERN

- PLCs for controlling **vacuum**, **cryogenics, CV**, etc. systems

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- Failures might have *negative impact*
- **Increasing complexity** without **decreasing quality**?

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  robust industrial computers

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- **1000+ PLCs** at CERN

Goal

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- **Integrate** formal verification to the development process

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Real System (hardware, software) → Formal Model → Formal Requirement

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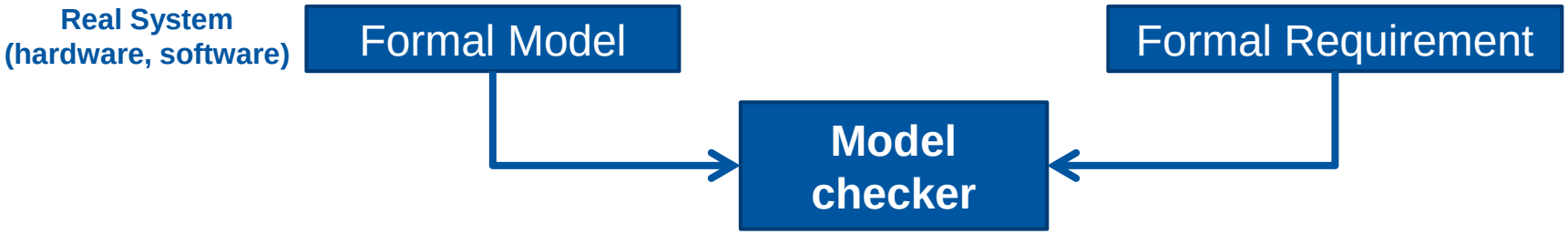

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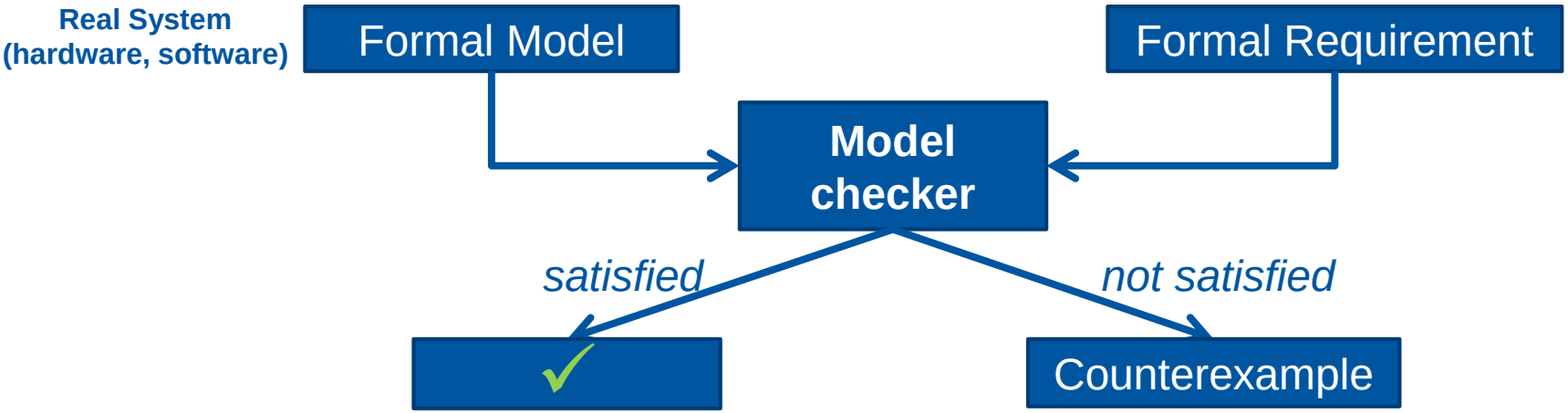

Testing vs. model checking

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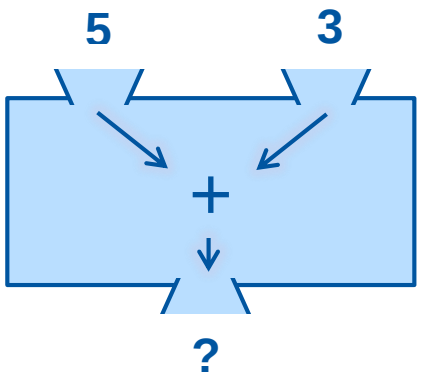
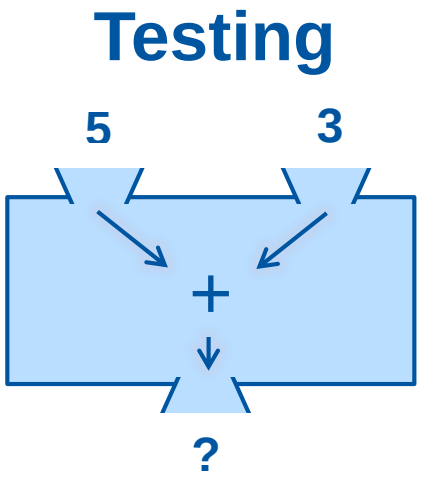



```
add(5,3)=8 ?
```

Testing vs. model checking



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Testing vs. model checking

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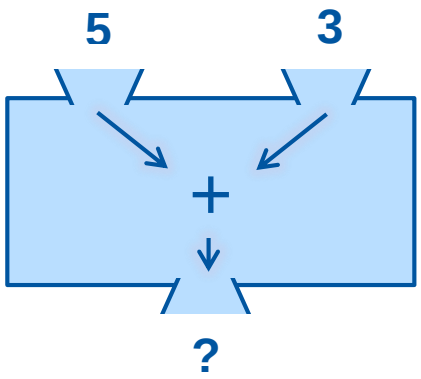

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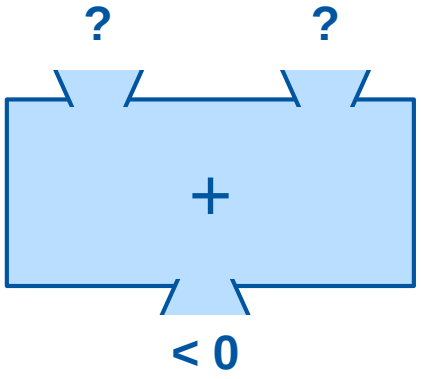

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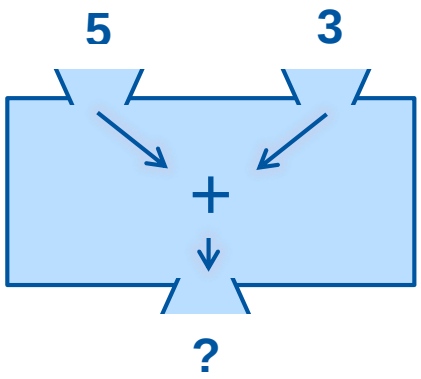

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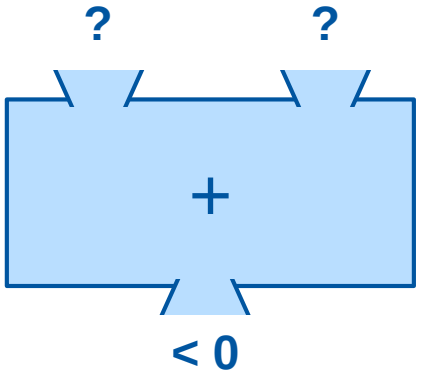

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- E.g. the possibility of an **output combination** is checked.
- Can be used in other ways too.

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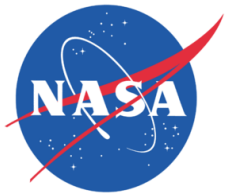

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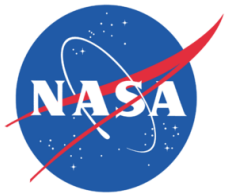
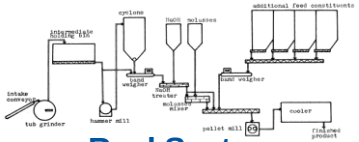


- Formal verification for **PLCs**
  - mostly in academic environment
  - not widely spread yet in industry – **too difficult**!

Challenges and answers



Real System
(hardware, software)

Specifications

Formal Model

Formal Requirement

Model checker

satisfied

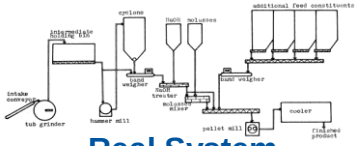
not satisfied

✓

Counter-example

Challenges and answers

How to get models?



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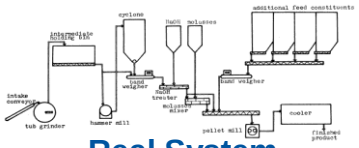

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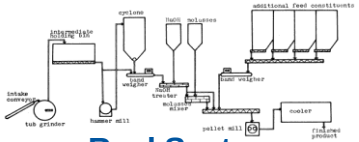

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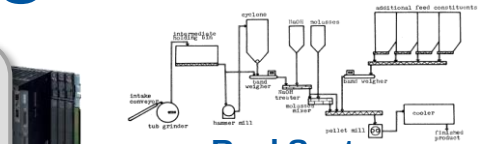

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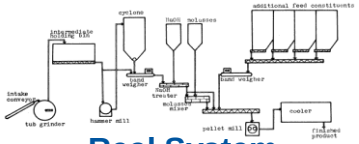

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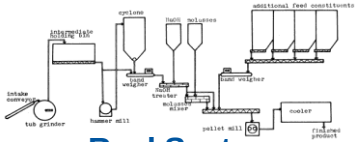

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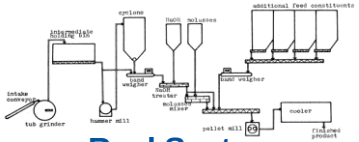

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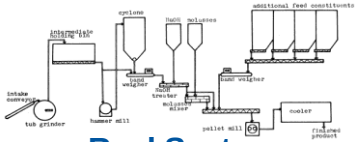

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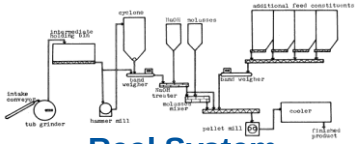

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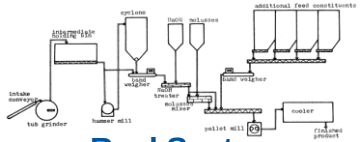

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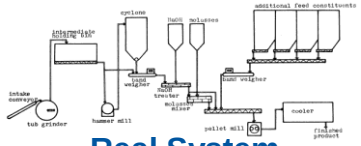

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And it should be integrated to the development process.

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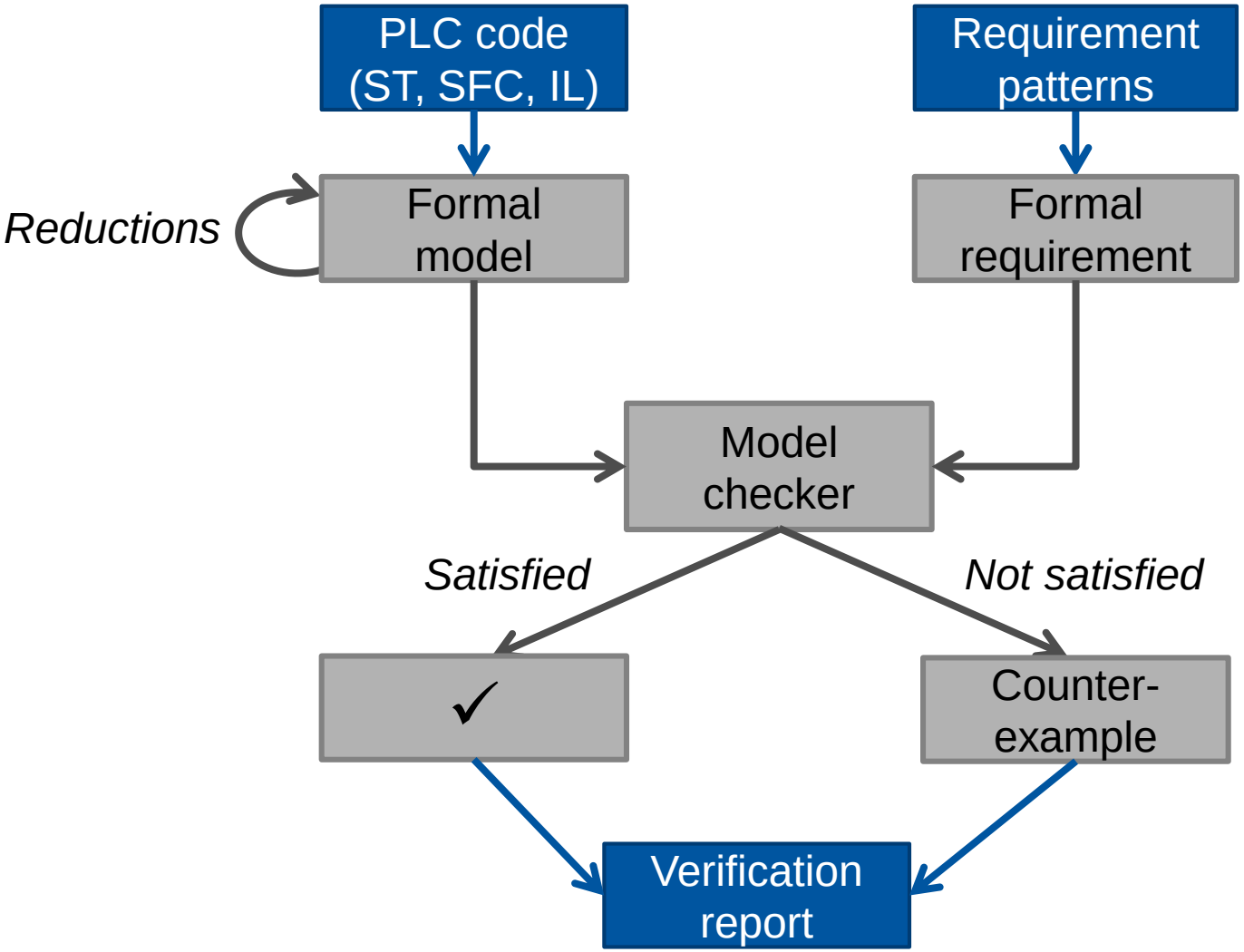
Model checking (extended workflow for PLCs)



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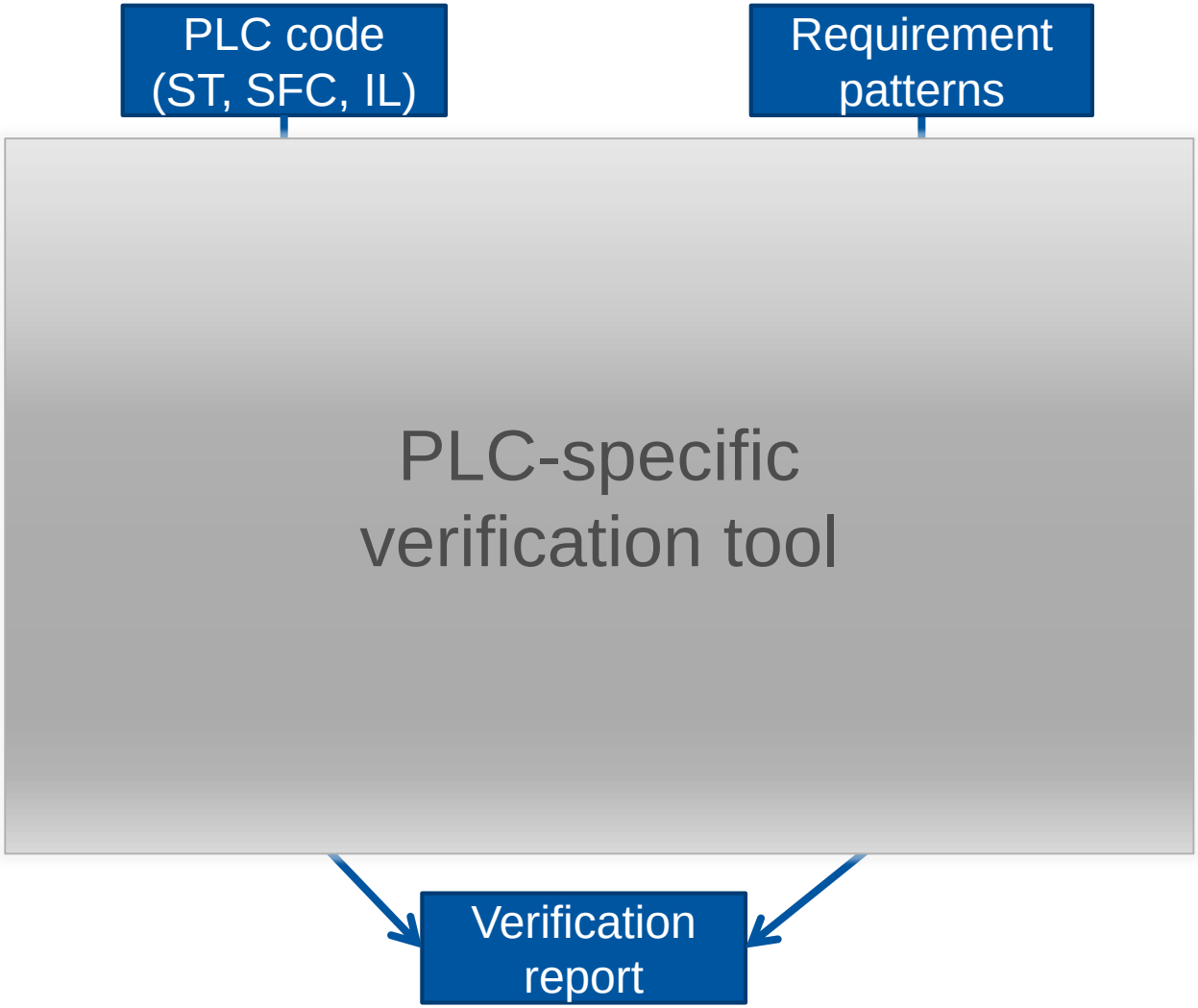
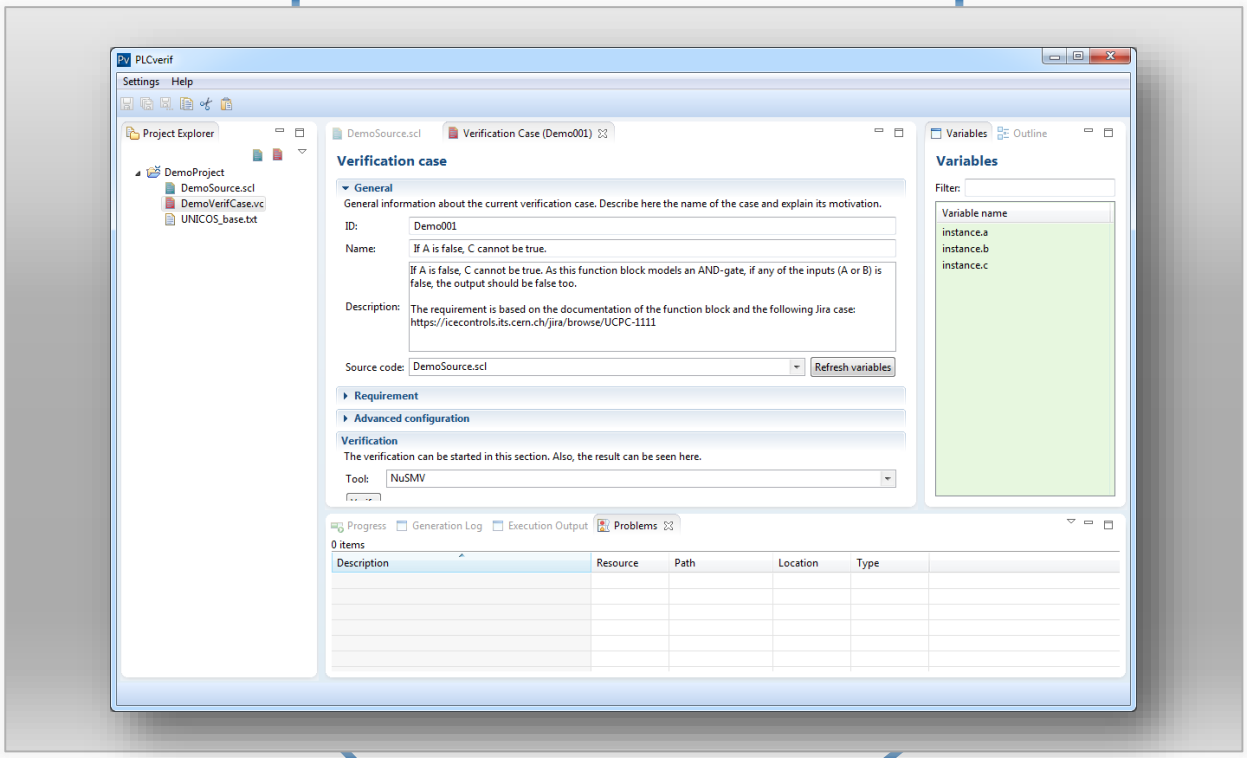


Model checking (extended workflow for PLCs)

PLC code (ST, SFC, IL)

Requirement patterns



Verification report

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Model checking in practice (at CERN)

The PLCverif tool

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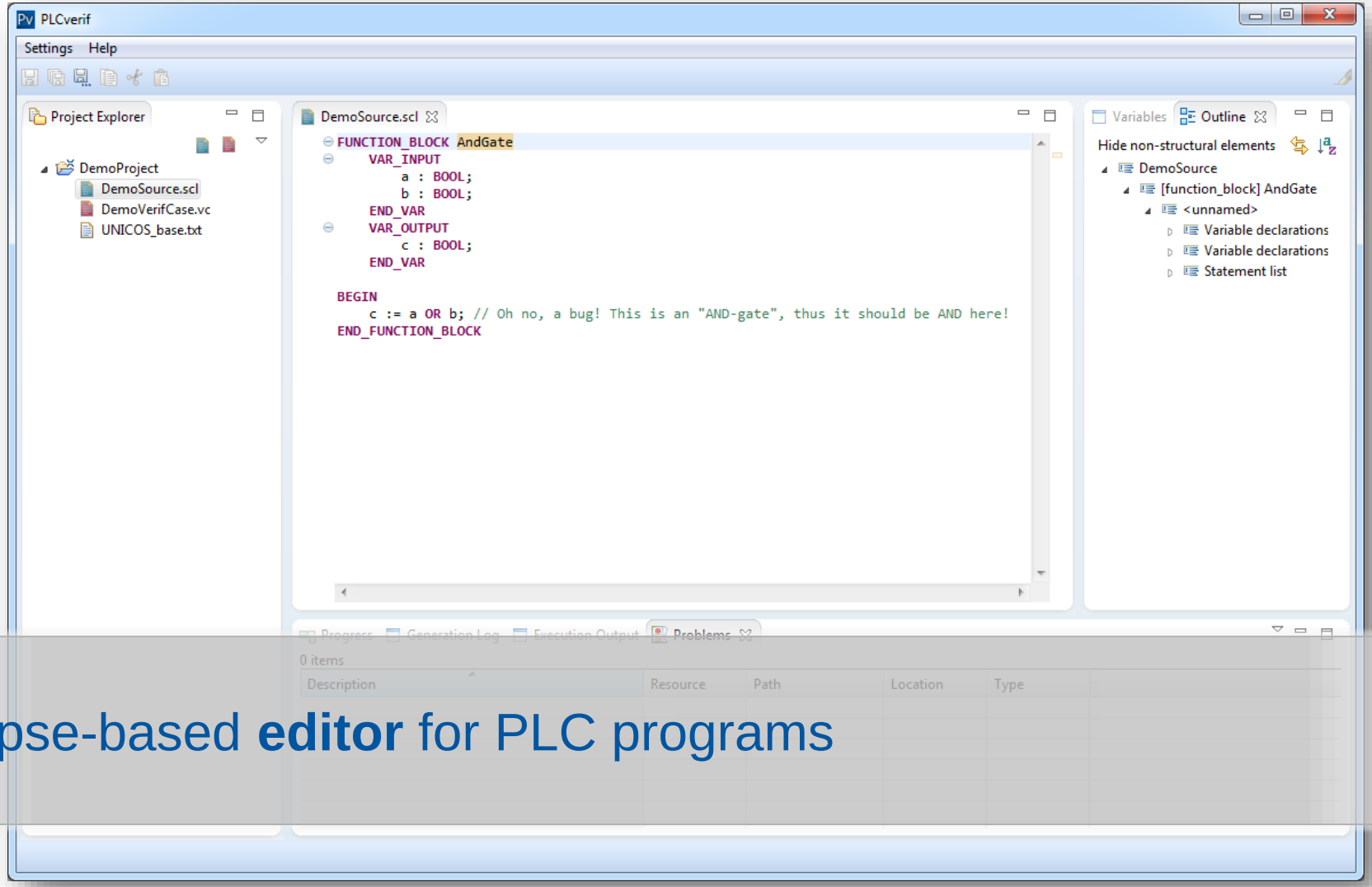

Eclipse-based **editor** for PLC programs

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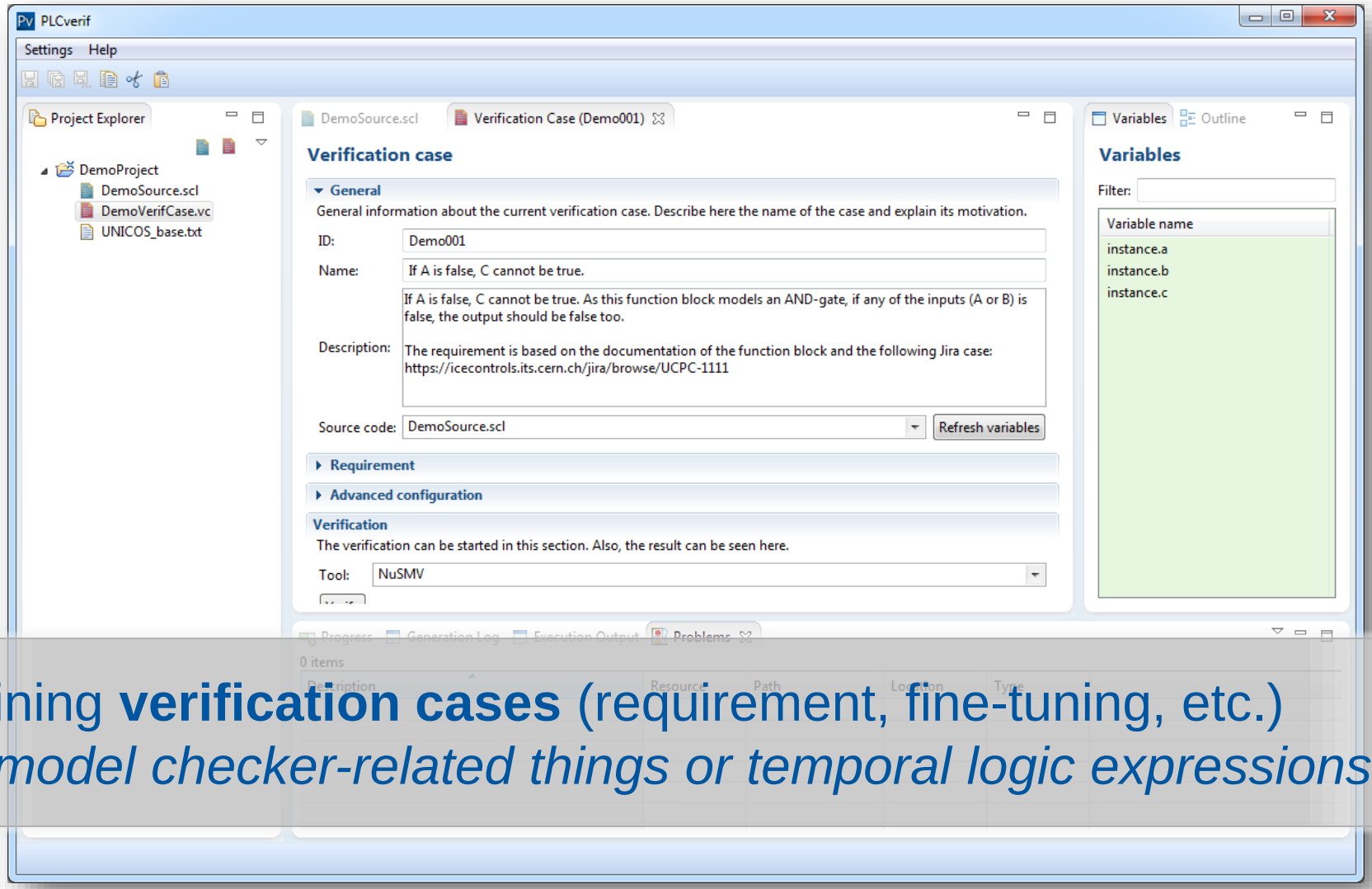

Defining **verification cases** (requirement, fine-tuning, etc.)

No model checker-related things or temporal logic expressions

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The PLCverif tool

PLCverif — Verification report

Generated at Mon Jul 07 15:19:22 CEST 2014 | PLCverif v2.0.1 | (C) CERN EN-ICE-PLC | Show/hide expert details

ID:	**Demo001**
Name:	If A is false, C cannot be true.
Description:	If A is false, C cannot be true. As this function block models an AND-gate, if any of the inputs (A or B) is false, the output should be false too. The requirement is based on the documentation of the function block and the following Jira case: https://icecontrols.its.cern.ch/jira/browse/UCPC-1111
Source file:	DemoSource.scl
Requirement:	3. A = false & C = true is impossible at the end of the PLC cycle.
Result:	**Not satisfied**

Tool: nusmv
Total runtime (until getting the verification results): 212 ms
Total runtime (incl. visualization): 361 ms

Counterexample

	Variable	End of **Cycle 1**
Input	**a**	FALSE
Input	**b**	TRUE
Output	**c**	TRUE

Click-button verification,
verification **report** with the analysed **counterexample**

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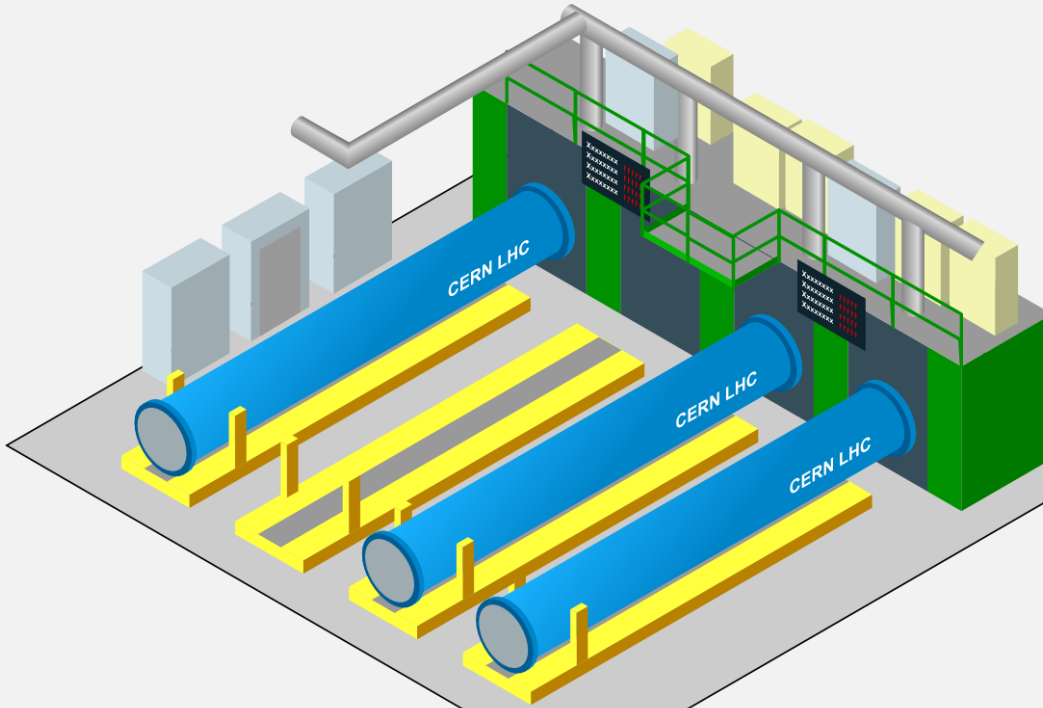
Example – SM18 safety system



SM18

Goal: ensuring **safety** by allowing/forbidding tests

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Core:

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SM18

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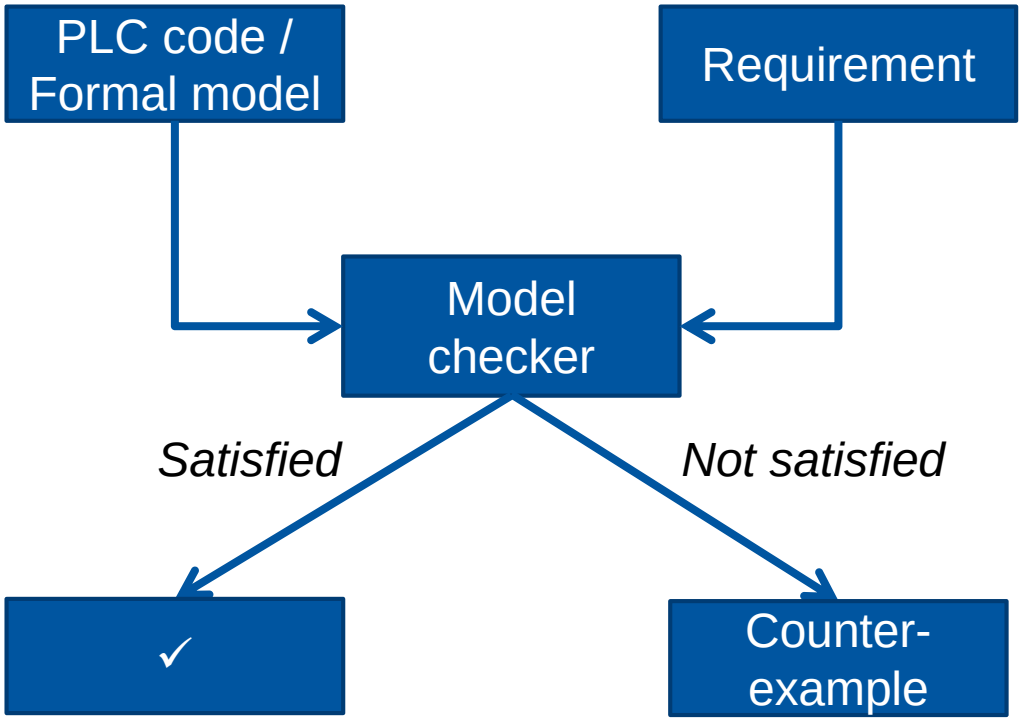
Model checking workflow for SM18



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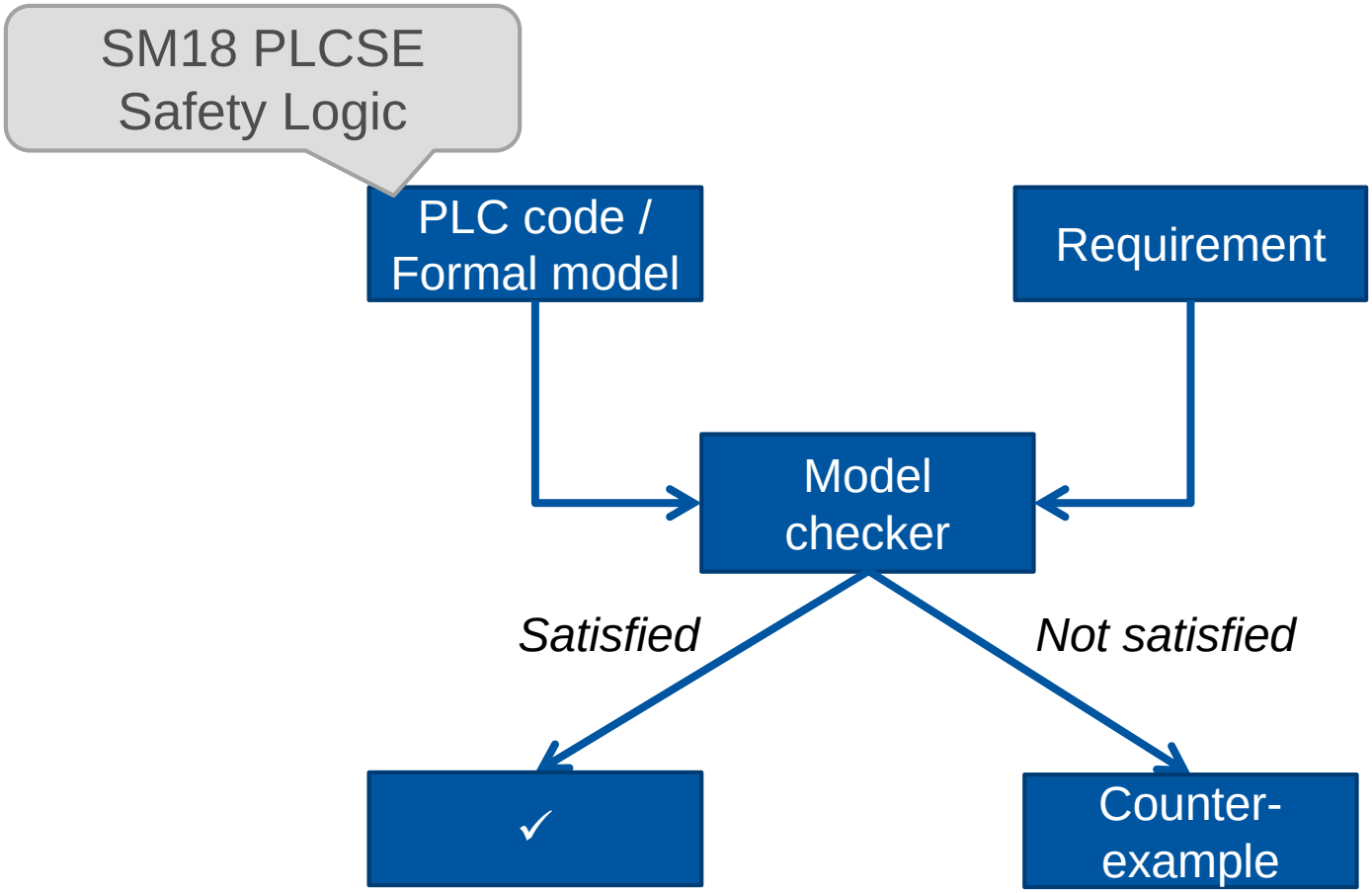

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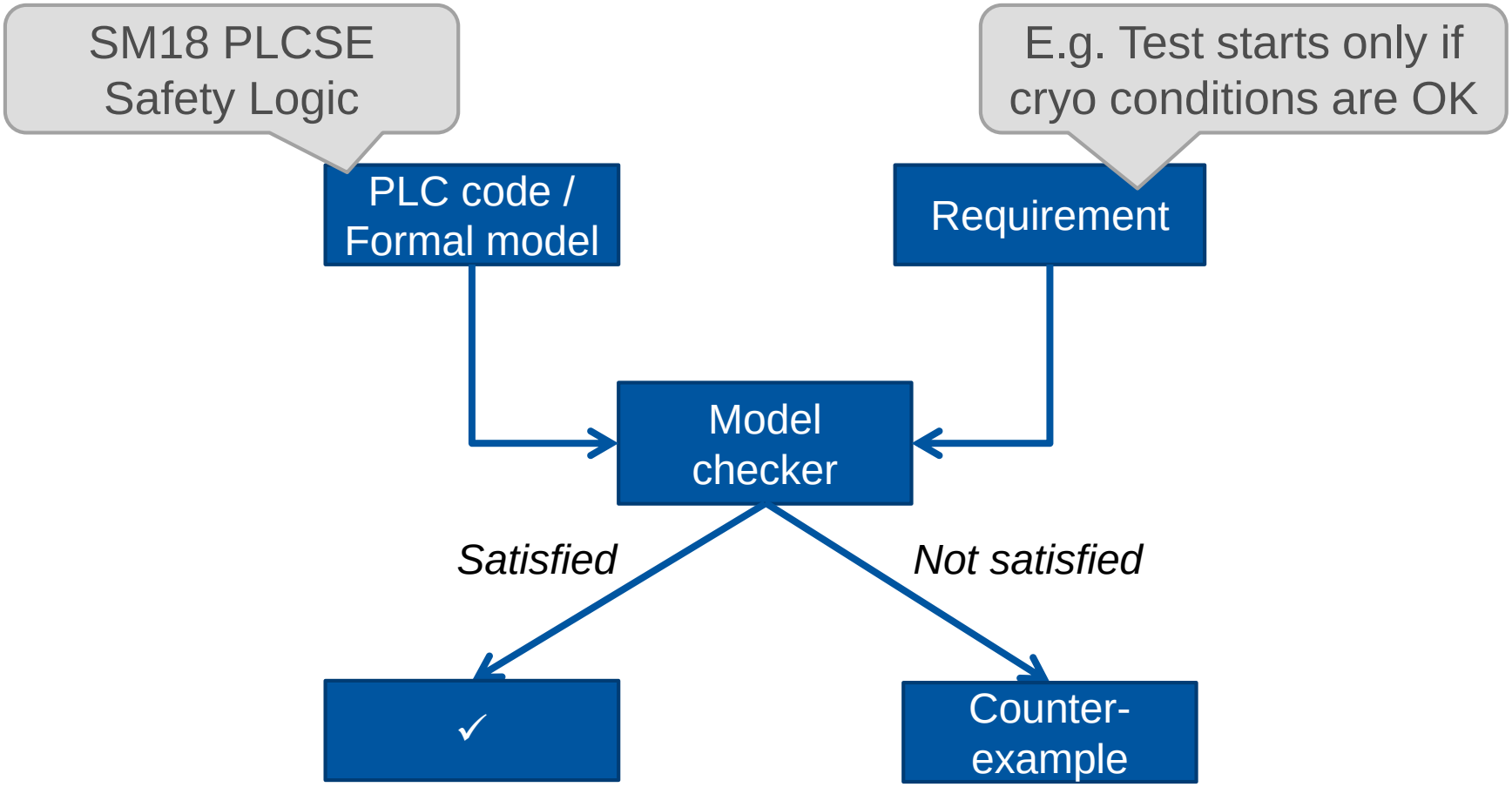

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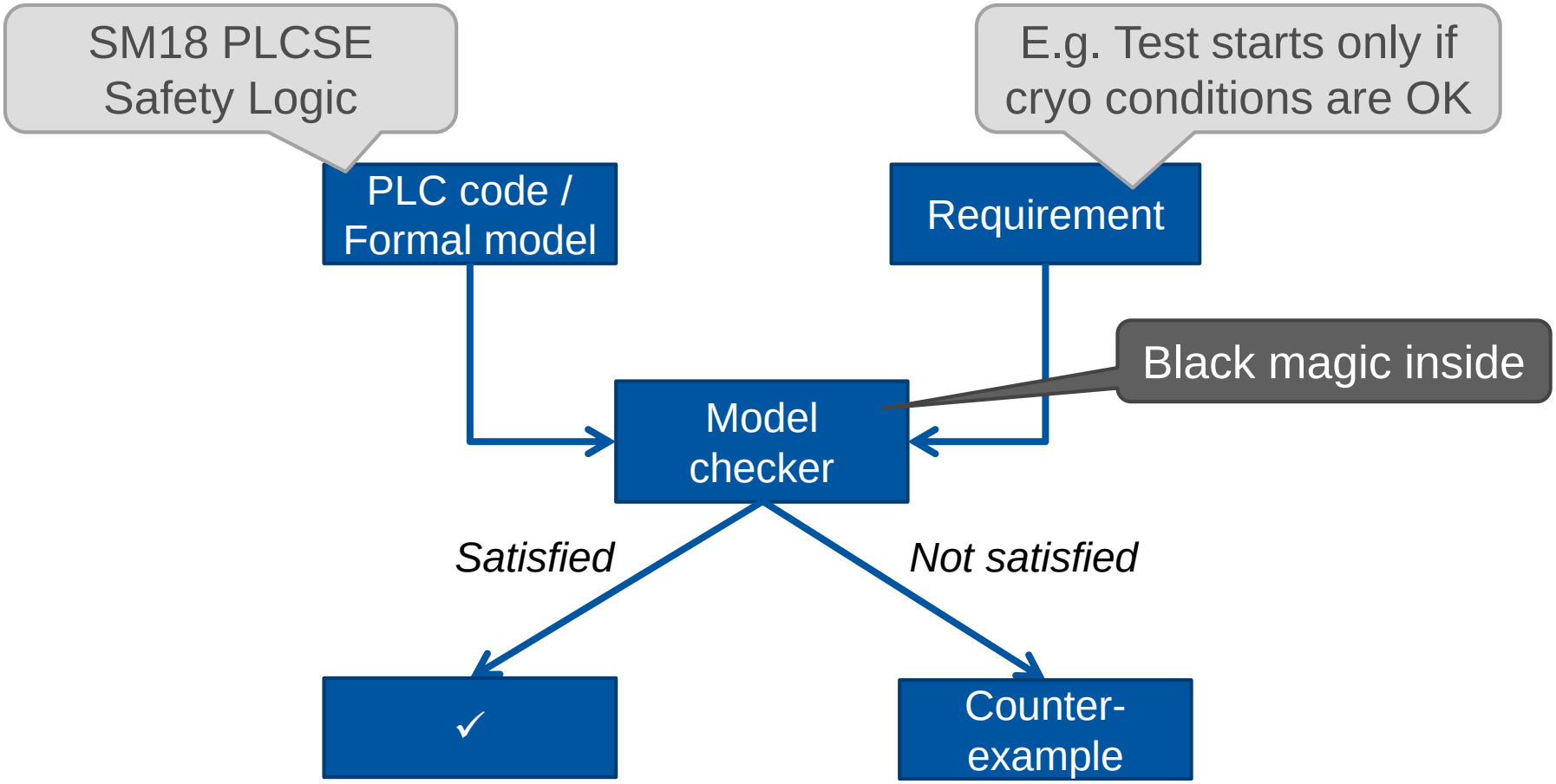

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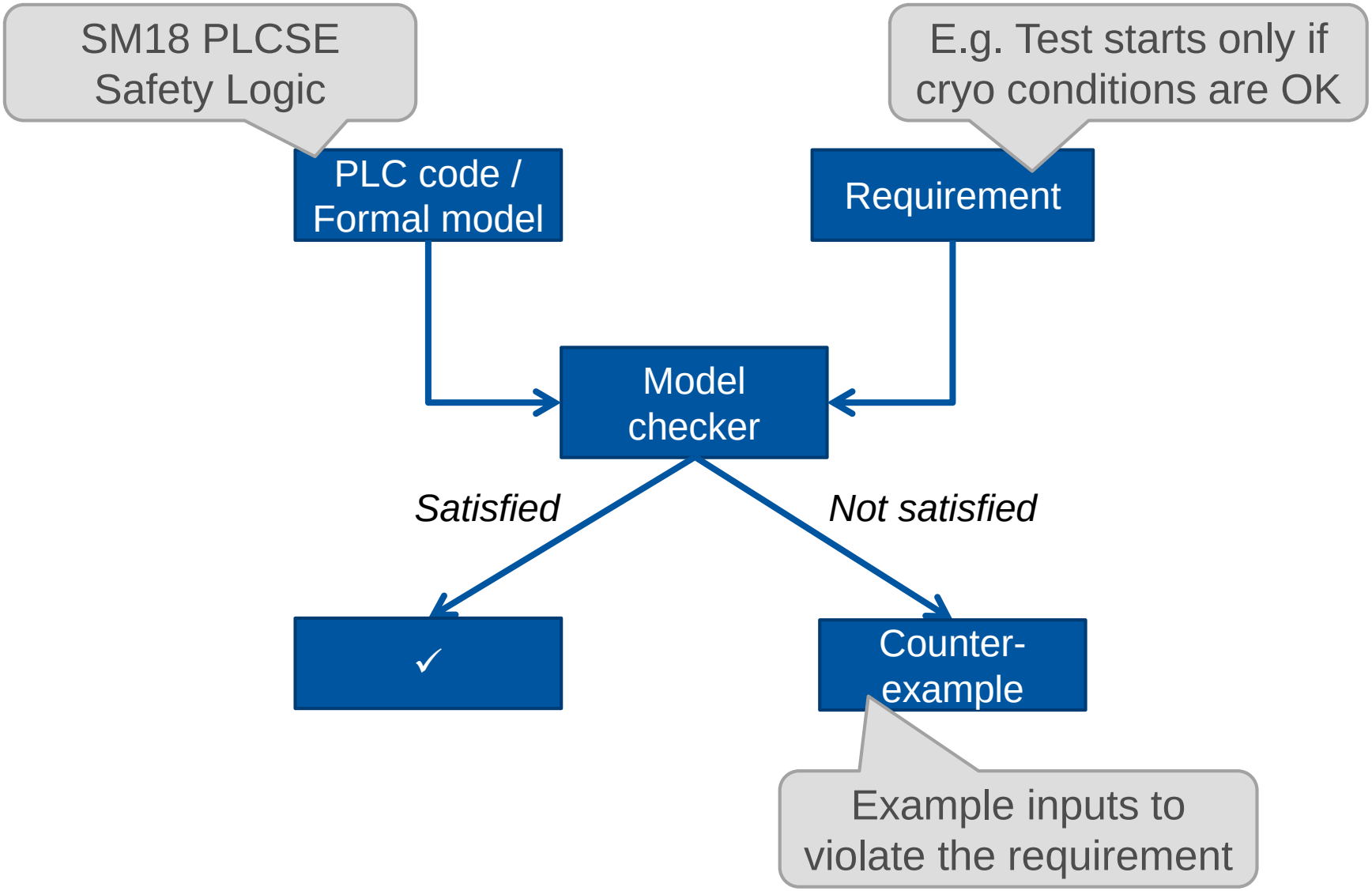
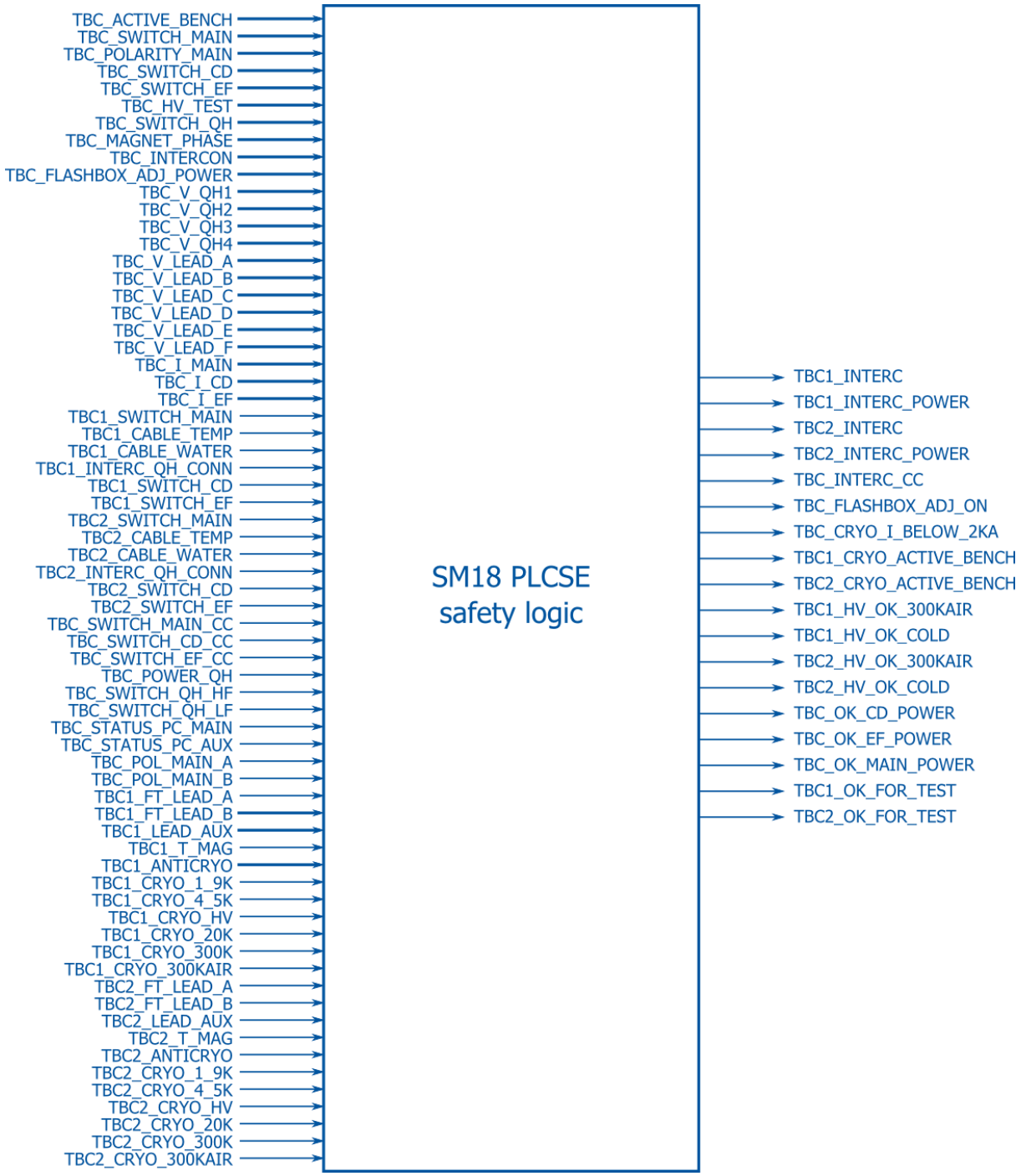



selected test
switch statuses
current voltages
cryo conditions
SM18 PLCSE
safety logic
test allowed


TBC_ACTIVE_BENCH
TBC_SWITCH_MAIN
TBC_POLARITY_MAIN
TBC_SWITCH_CD
TBC_SWITCH_EF
TBC_HV_TEST
TBC_SWITCH_QH
TBC_MAGNET_PHASE
TBC_INTERCON
TBC_FLASHBOX_ADJ_POWER
TBC_V_QH1
TBC_V_QH2
TBC_V_QH3
TBC_V_QH4
TBC_V_LEAD_A
TBC_V_LEAD_B
TBC_V_LEAD_C
TBC_V_LEAD_D
TBC_V_LEAD_E
TBC_V_LEAD_F
TBC_I_MAIN
TBC_I_CD
TBC_I_EF
TBC1_SWITCH_MAIN
TBC1_CABLE_TEMP
TBC1_CABLE_WATER
TBC1_INTERC_QH_CONN
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TBC_STATUS_PC_AUX
TBC_POL_MAIN_A
TBC_POL_MAIN_B
TBC1_FT_LEAD_A
TBC1_FT_LEAD_B
TBC1_LEAD_AUX
TBC1_T_MAG
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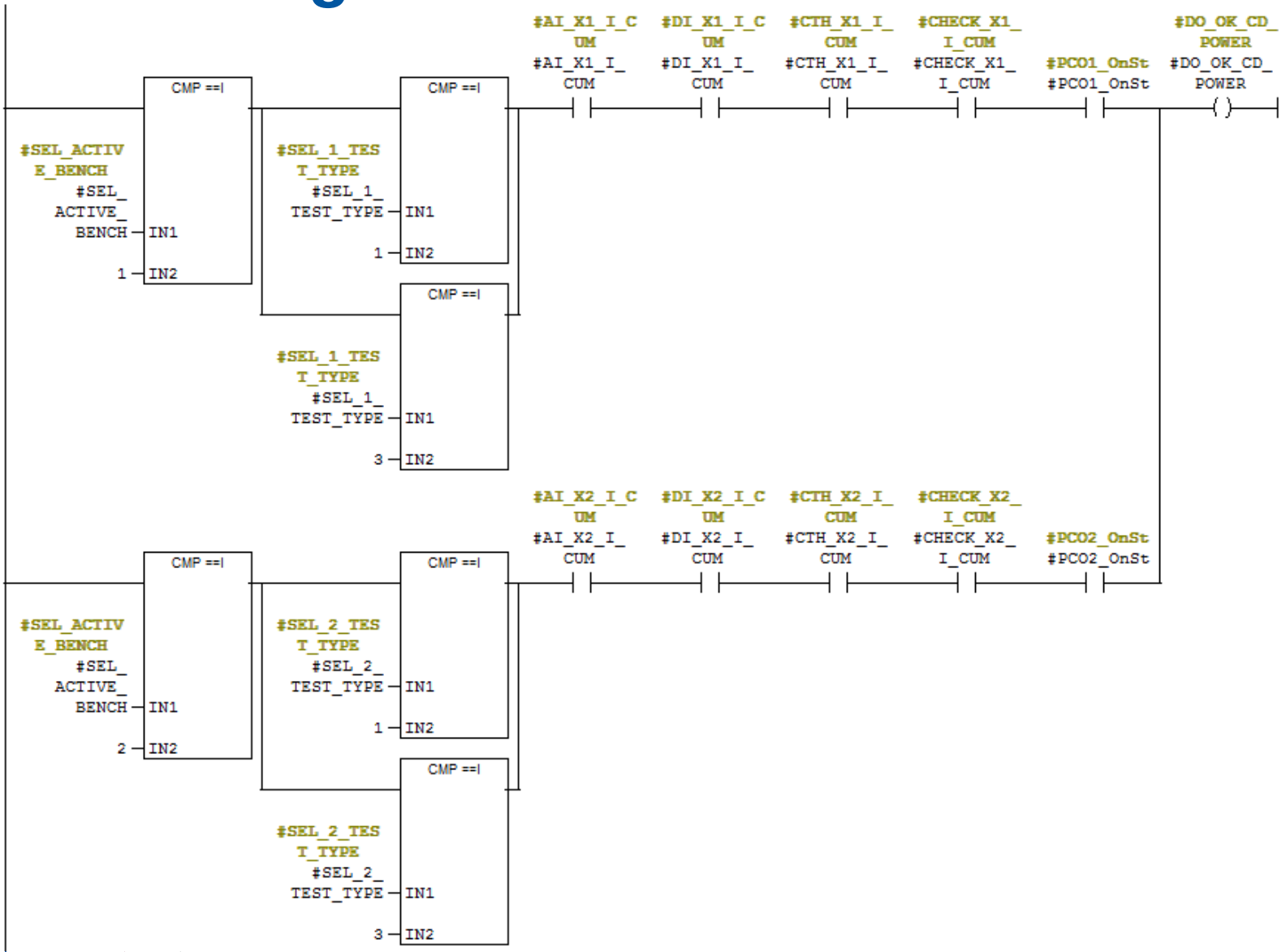
TBC2_FT_LEAD_A
TBC2_FT_LEAD_B
TBC2_LEAD_AUX
TBC2_T_MAG
TBC2_ANTICRYO
TBC2_CRYO_1_9K
TBC2_CRYO_4_5K
TBC2_CRYO_HV
TBC2_CRYO_20K
TBC2_CRYO_300K
TBC2_CRYO_300KAIR
SM18 PLCSE
safety logic
TBC1_INTERC
TBC1_INTERC_POWER
TBC2_INTERC
TBC2_INTERC_POWER
TBC_INTERC_CC
TBC_FLASHBOX_ADJ_ON
TBC_CRYO_I_BELOW_2KA
TBC1_CRYO_ACTIVE_BENCH
TBC2_CRYO_ACTIVE_BENCH
TBC1_HV_OK_300KAIR
TBC1_HV_OK_COLD
TBC2_HV_OK_300KAIR
TBC2_HV_OK_COLD
TBC_OK_CD_POWER
TBC_OK_EF_POWER
TBC_OK_MAIN_POWER
TBC1_OK_FOR_TEST
TBC2_OK_FOR_TEST

Ladder Diagram



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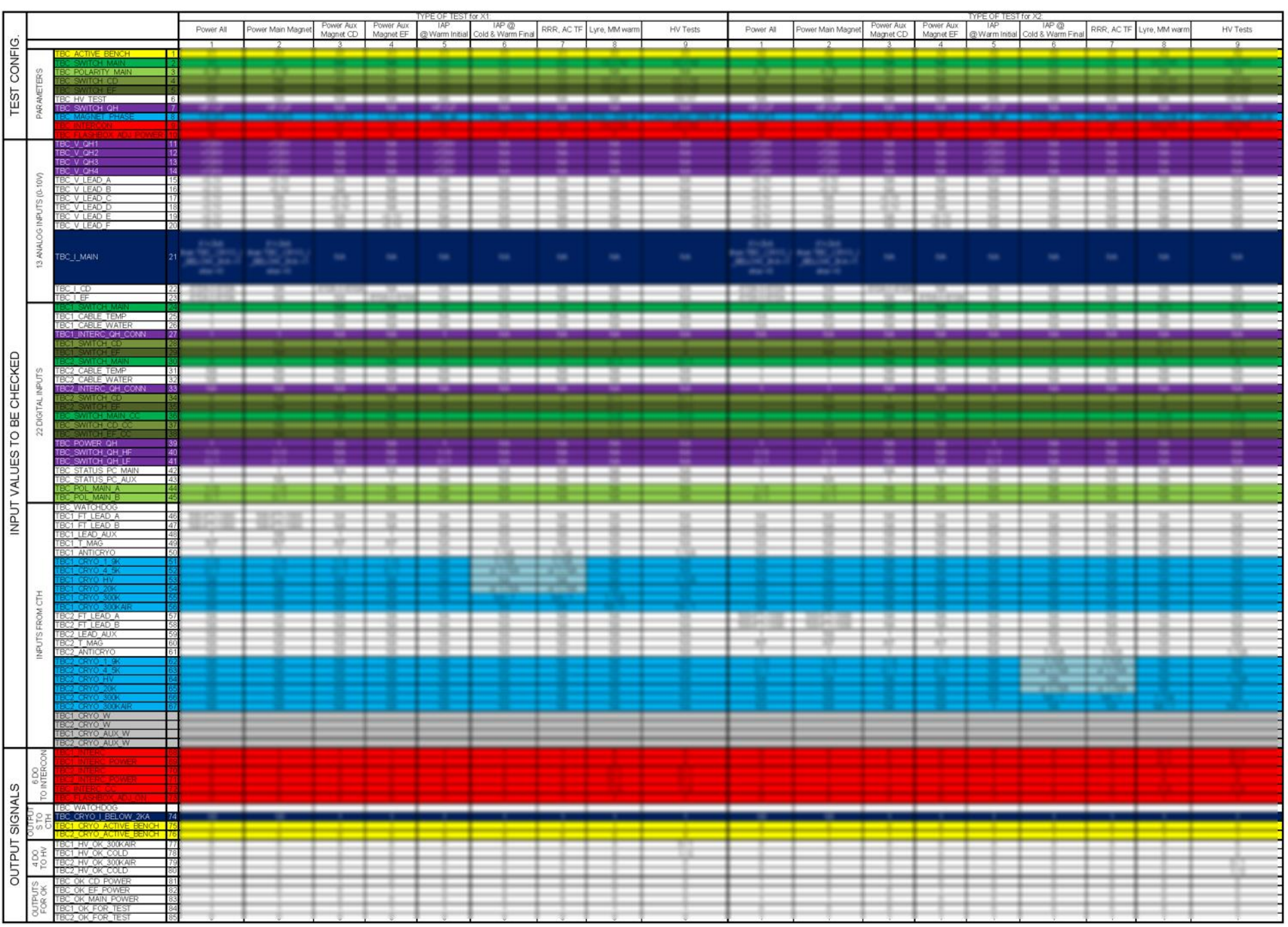
Excerpt from the work of R. Speroni



From M. Charrondiere

Problems found *(before putting in production!)*

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Requirement misunderstanding

- Recognised while specifying requirements

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Safety problems

- “The [magnet] test **should NOT start**, but it does.”

Problems found *(before putting in production!)*

Requirement misunderstanding

- Recognised while specifying requirements

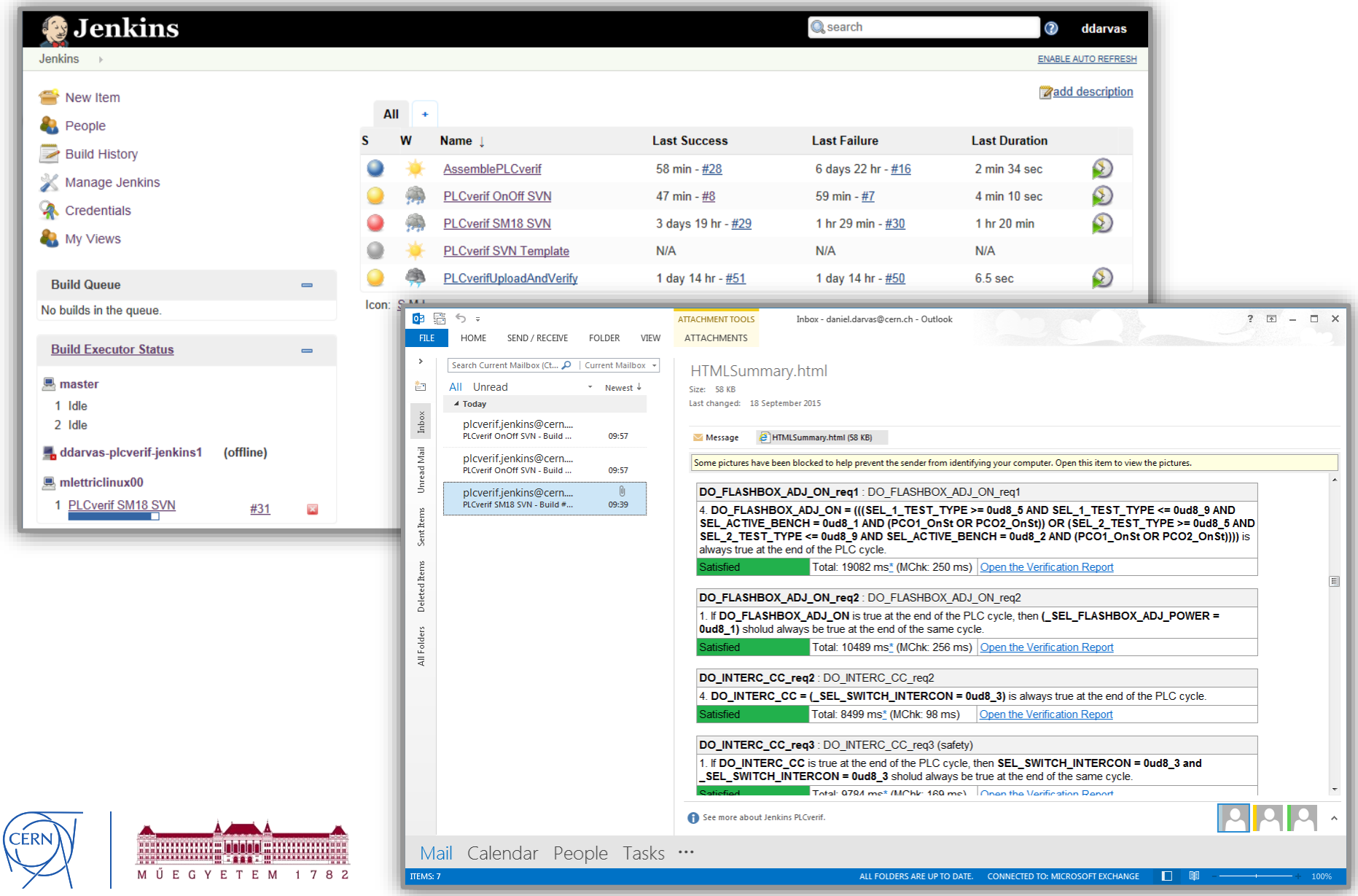
Functionality problems

- “The [magnet] test should start, but it doesn’t.”

Safety problems

- “The [magnet] test **should NOT start**, but it does.”
- Some really hidden:
  65536 input combinations for 1 magnet test scenario
  start should be allowed in 2 of them

Verification workflow in practice



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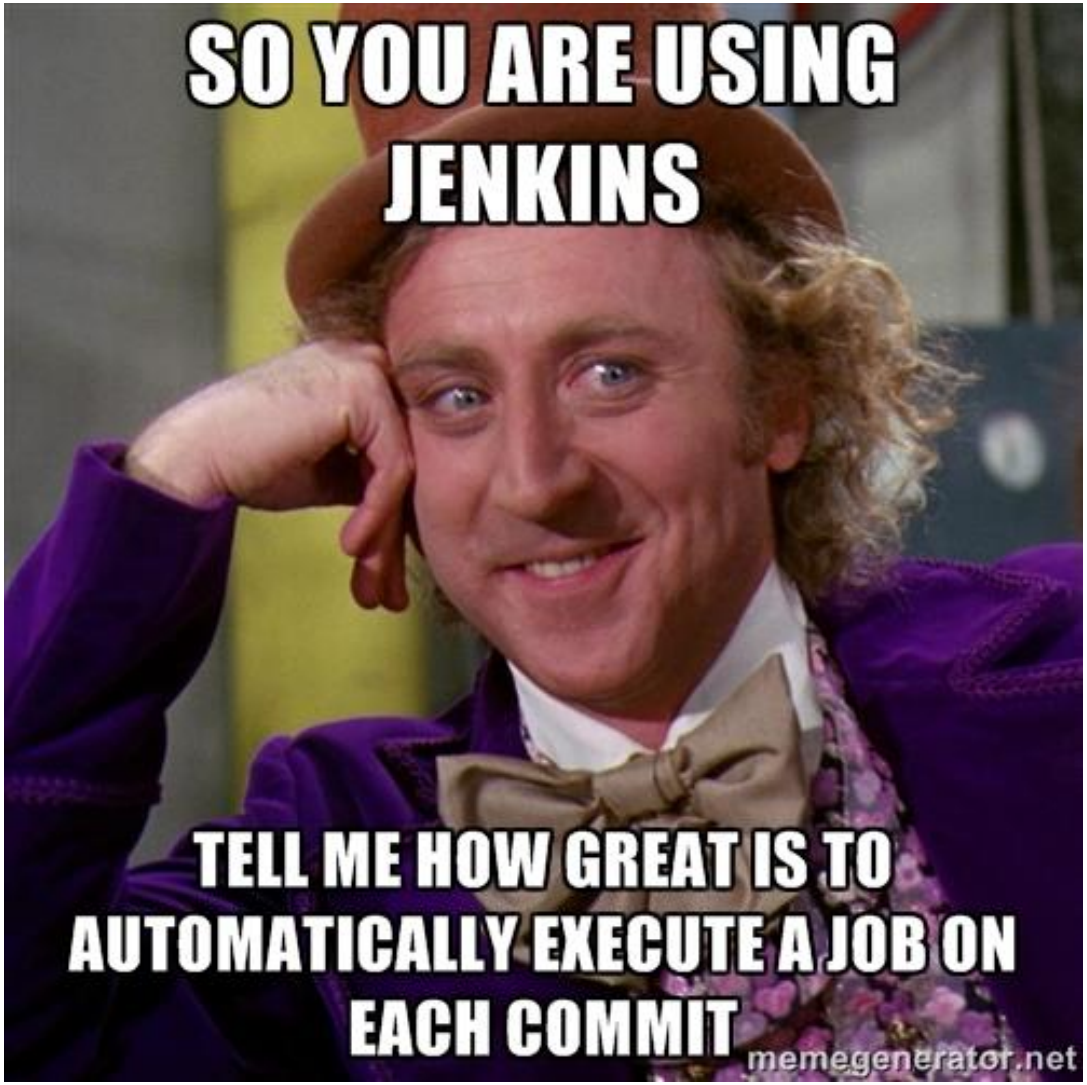
Verification workflow in practice



Based on still from Willy Wonka & the Chocolate Factory,
Source: memegenerator.net

Summary

http://go.cern.ch/**7L9h**
http://cern.ch/**plcverif**

Summary

- “Formal verification is not relevant to industry.” **FALSE**!

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Summary

- “Formal verification is not relevant to industry.” **FALSE**!

- First steps to **apply formal verification** to PLCs
  - **Interesting bugs** found (*with joint effort*)
  - **Critical parts** can be checked
  - **Complementary** to testing

http://go.cern.ch/**7L9h**
http://cern.ch/**plcverif**

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Summary

- "Formal verification is not relevant to industry." **FALSE**!
- First steps to **apply formal verification** to PLCs
  - **Interesting bugs** found (*with joint effort*)
  - **Critical parts** can be checked
  - **Complementary** to testing
- Still long way to go
  - Improving the **performance**
  - **Formal specification**

http://go.cern.ch/**7L9h**
http://cern.ch/**plcverif**

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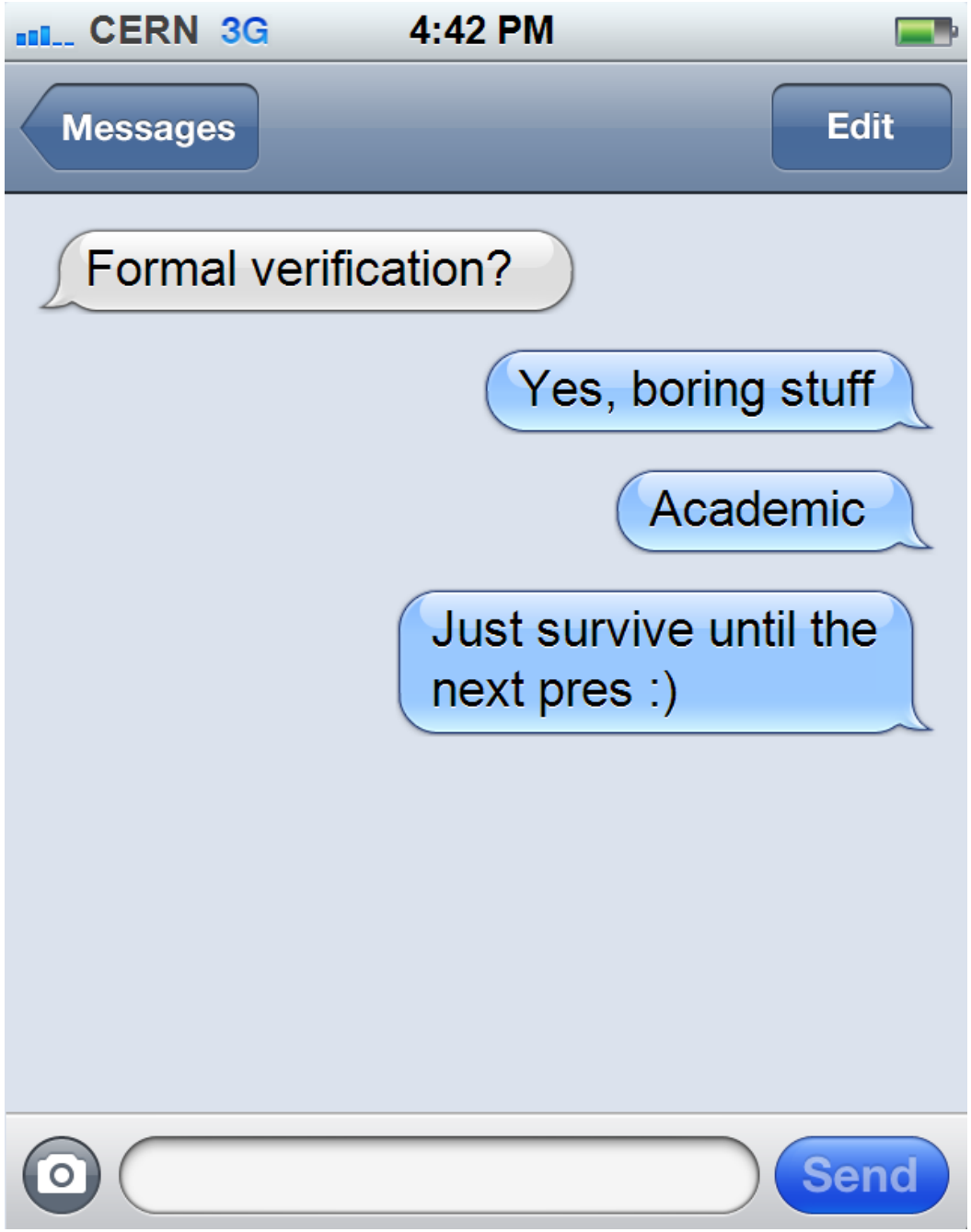
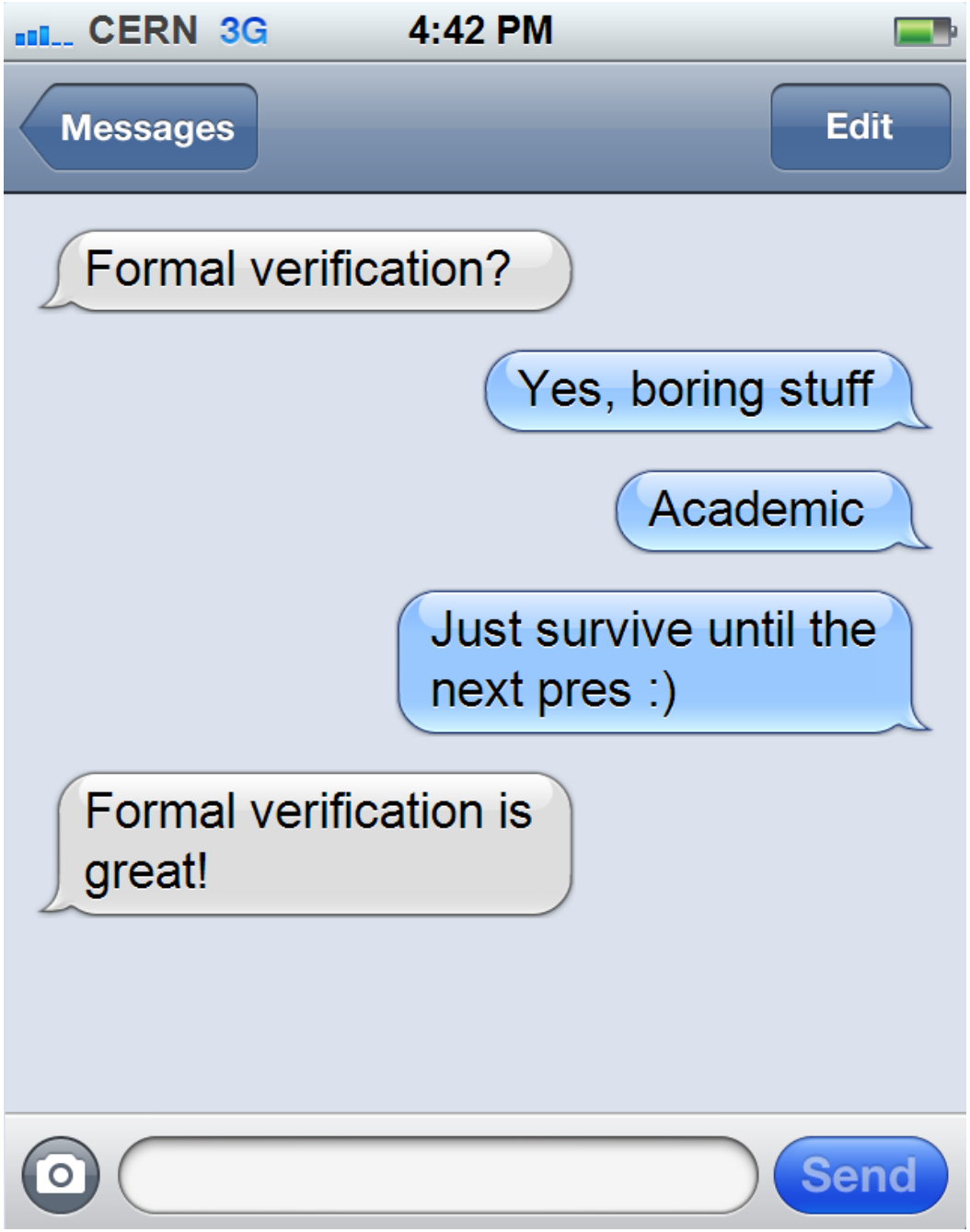


Source: http://www.iphonetextgenerator.com/



Source: http://www.iphonetextgenerator.com/

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