BPIX Module Qualification

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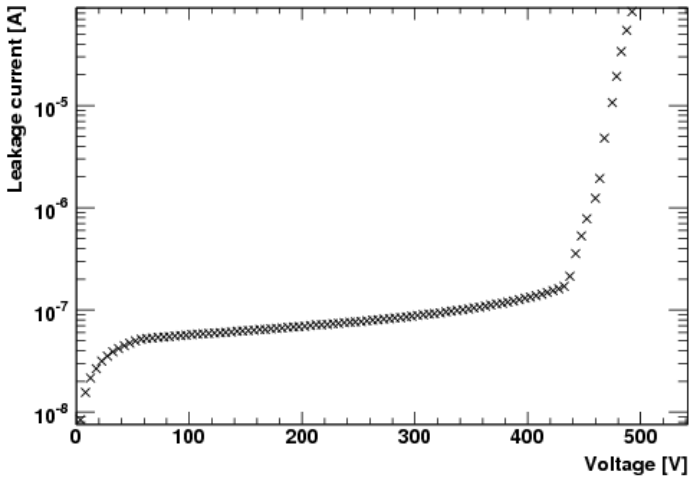
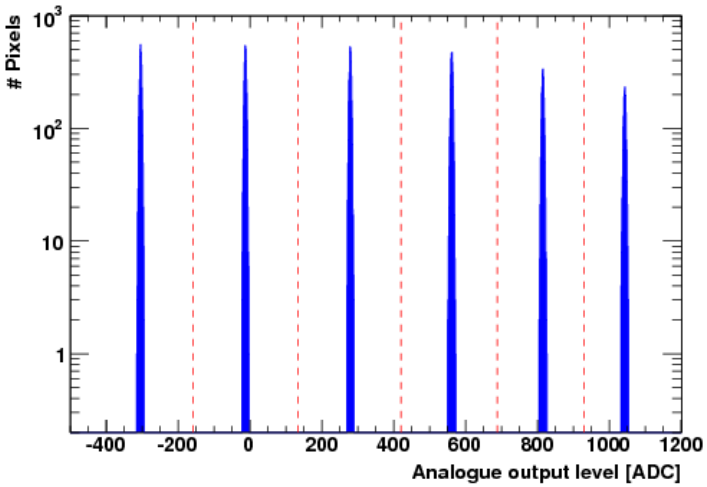
Module test classifications (FullTest & ShortTest)

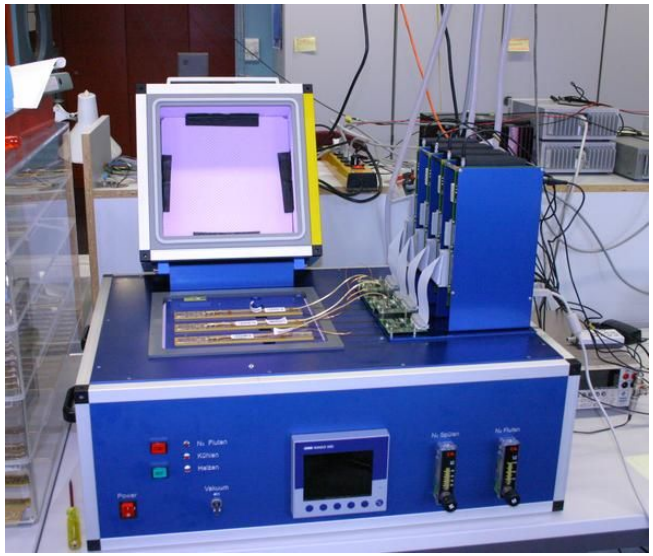
- Start-up adjustments
  - Analog current setting
  - Threshold and delay settings
  - Analog levels setting
- Functionality tests
  - Verification of pixel readout
  - Check bump bonding quality
  - Functionality of 4 trim bits
- Performance tests
  - Pixel noise measurements
  - Sensor IV curves / current at 100&150V
- Calibrations
  - Find separation between address levels
  - Calibration of pulse height
  - Threshold unification (trimming)
  - Internal signal calibration (with X-rays)

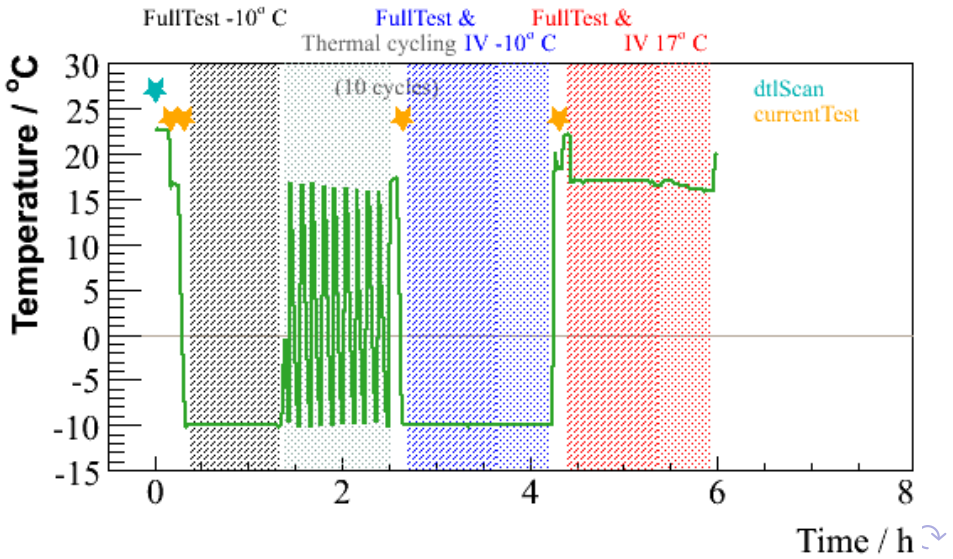




Testing set up and procedure

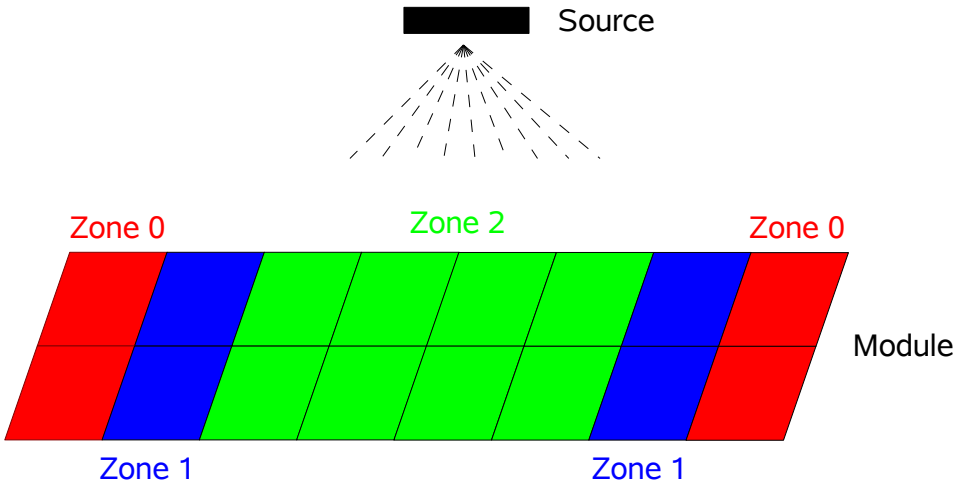
- Challenges
  - Huge number of channels: $5 \div 6 \times 10^7$
  - 29 DACs per ROC
  - Temperature dependence: -10°C / +17°C
- Test set up
  - Programmable cooling box
  - 4 modules at a time
  - Castom built test-boards with FPGA
- Procedure
  - Start-up adjustments
  - Full Test at -10°C
  - 10 thermal cycles
  - Full Tests and IV at -10°C & +17°C
  - Short Tests at -10°C & +17°C before module assembling





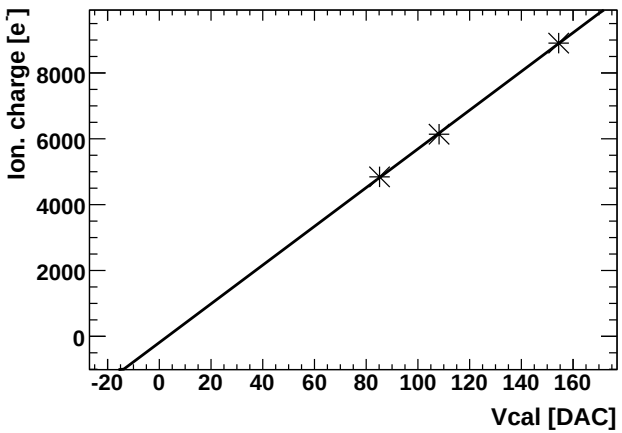
X-ray test

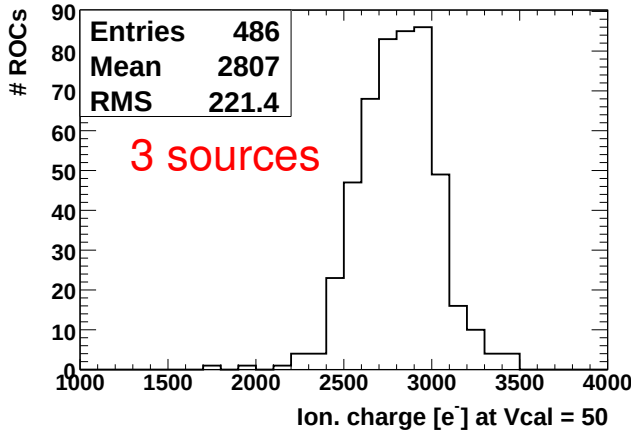
- Twofold purpose:
  - test module response to the injected charge into Si sensor
  - calibrate internal signal used for the trimming (setting threshold)
- X-ray source:
  - Primary source: Americium-241
  - Targets: Mo(4844 e^-), Ag(6139$^-$), Ba (8906 e^-)
  - Random trigger, stretched bunch-crossing
- Test setup:

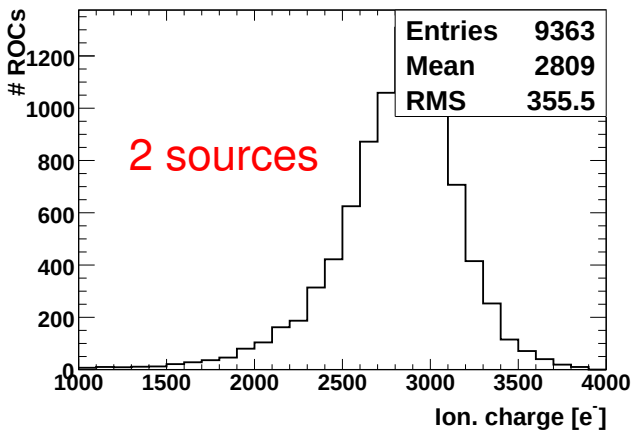


X-ray calibration

- On average 1 Vcal DAC corresponds to 66 e^-
- The mean offset at Vcal=0 is around -420 e^-
- Trimming with Vcal=50 corresponds to threshold of 2800 e^-
- For calibration use
  - if available, results for individual ROC from 3 sources
  - otherwise, mean from 2 sources average over module

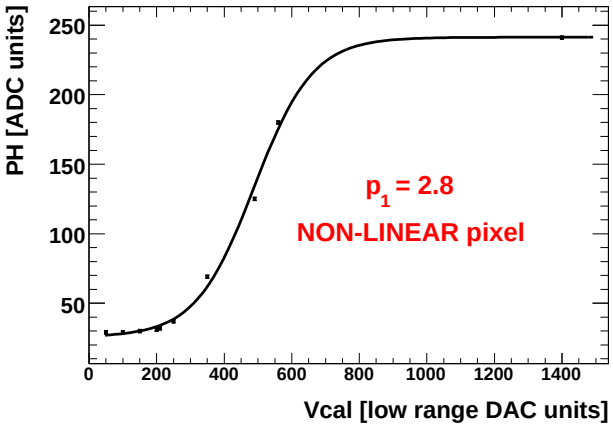


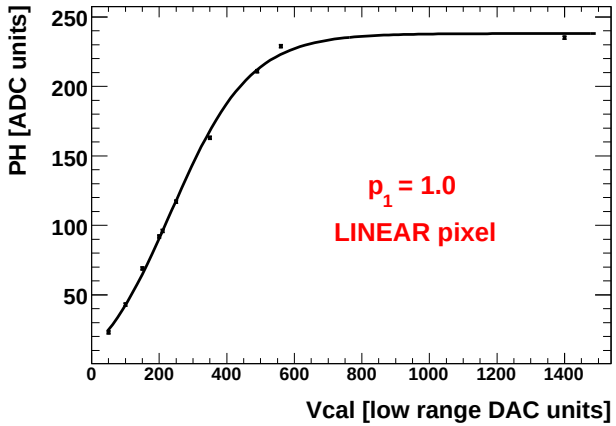


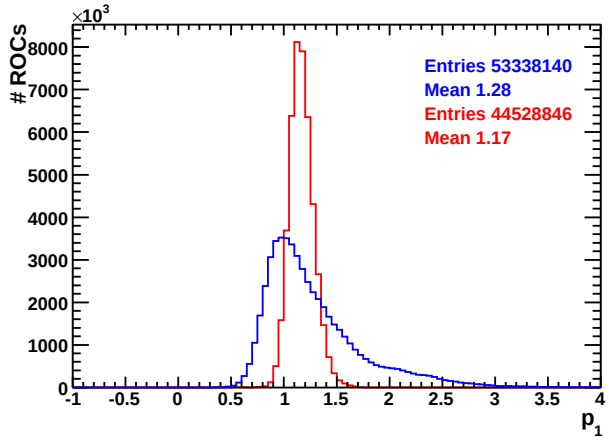


DAC optimization

- Several DACs have been optimized to set:
  - Analog and digital currents
  - Digital levels of TBM and ROC (Ultra Black)
  - Thresholds and delays
  - Pulse height ADC range and linearity
- Example: Pulse height linearity
  - Fit function: $y = p_3 + p_2 \cdot tanh(p_0 \cdot x - p_1)$



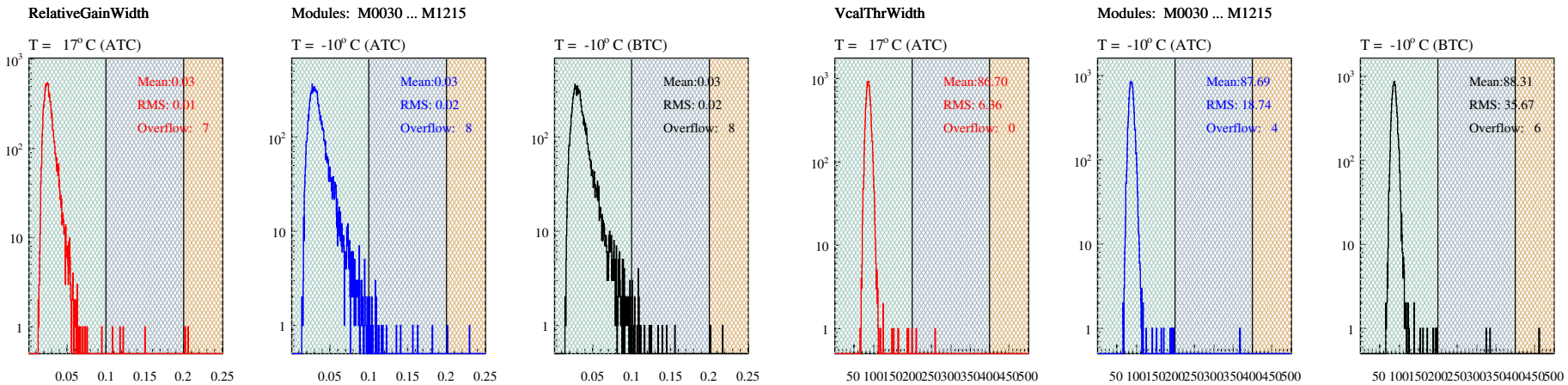




Grading

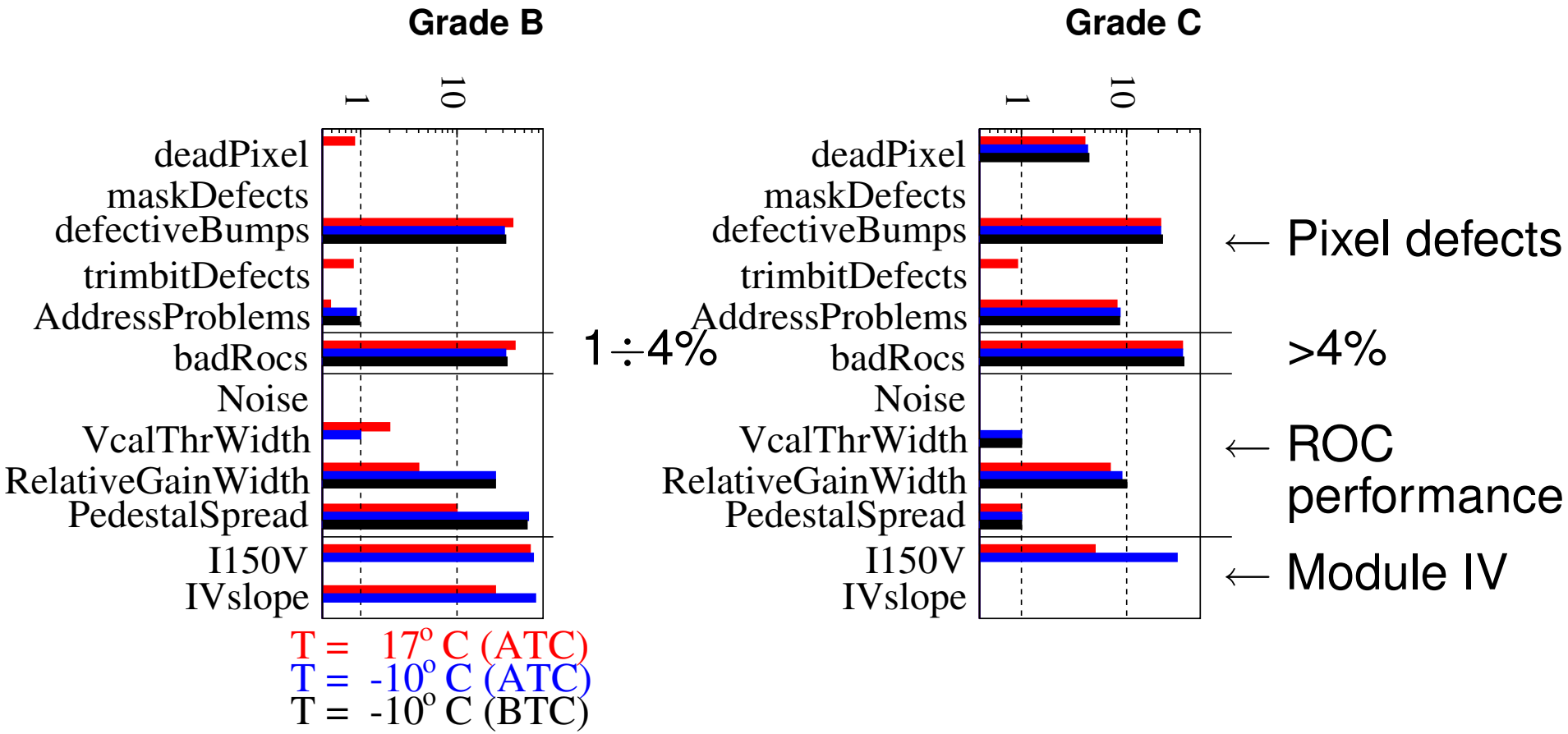
	Pixel	Mask	Noise	Gain	Pedestal	Thr.	I^{meas}_{+17}(150V)	I^{calc}_{-10}(150V)
A	$\leq$ 1%	0	$\leq 500e^-$	$\leq$ 10%	<2.5ke^-	<200e^-	<2μA	<3μA
B	$\leq$ 4%	0	$\leq 1000e^-$	$\leq$ 20%	<5.0ke^-	<400e^-	<10 μA	<15μA
C	$>$ 4%	$\geq$ 1	$\geq 1000e^-$	$>$ 20%	>5.0ke^-	>400e^-	>10μA	>15μA

- Pixel defects/chip
- Mask: permanent readout
- Noise in e^-
- Relative Gain width
- Pedestal spread in e^-
- Vcal Threshold Width in e^-
- I^{meas}_{+17}(150V): measured leakage current at $+17°$
- I^{calc}_{-10}(150V): recalculated leakage current at $-10°$



Production quality

Chip Failures



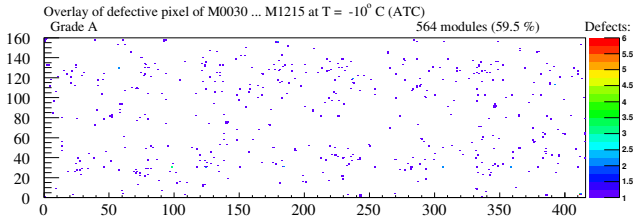
Production summary

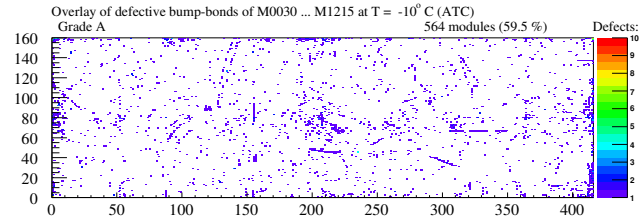
948 modules tested (827 full/ 121 half)

- 565/161 graded as A/B → 88% ‖ 87/23 → 91%
- 101 graded as C → 12% ‖ 11 → 9%

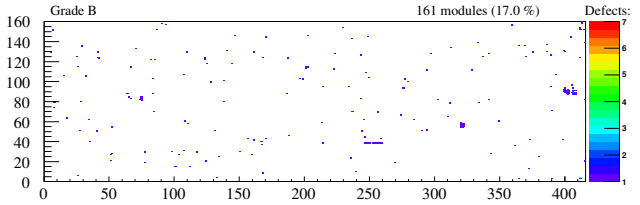
Overlay of modules tested at T = -10^{o} C (ATC)

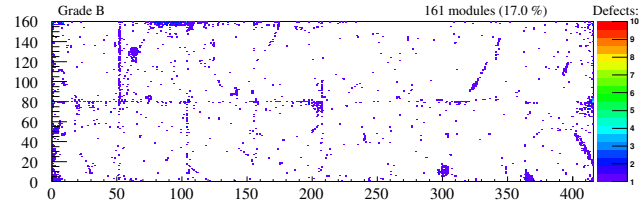
Final Grade A (564 modules)





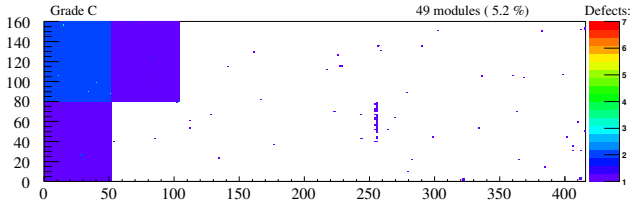
Final Grade B (161 modules)

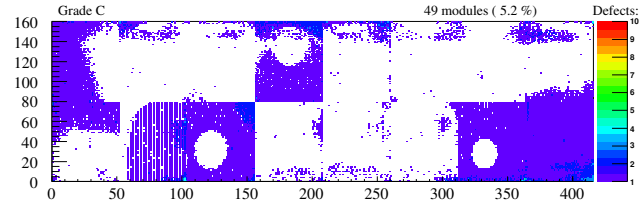




} 48.3M pixels

Final Grade C (49 modules)





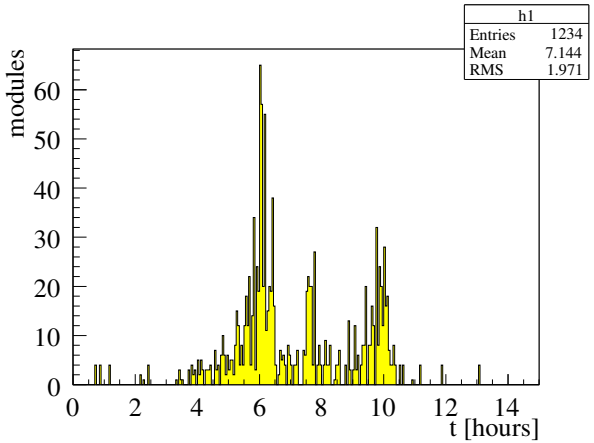
3.3M pixels

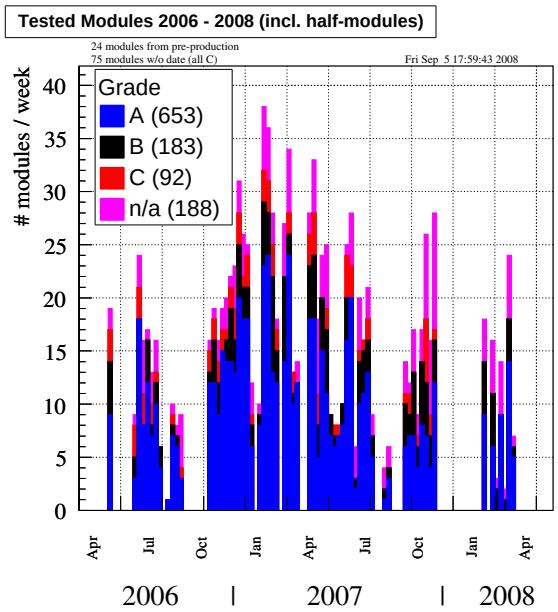
Dead pixels

Dead bumps

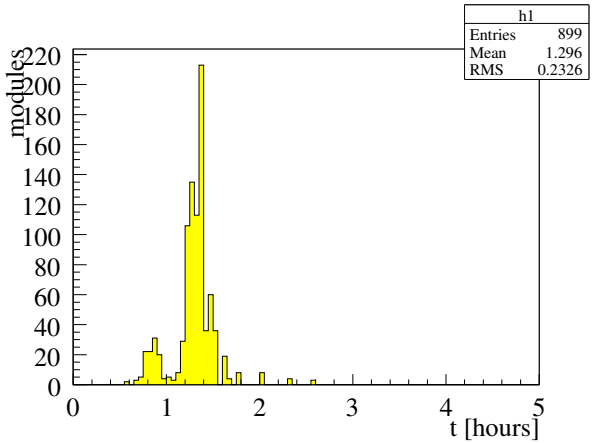
Production in time

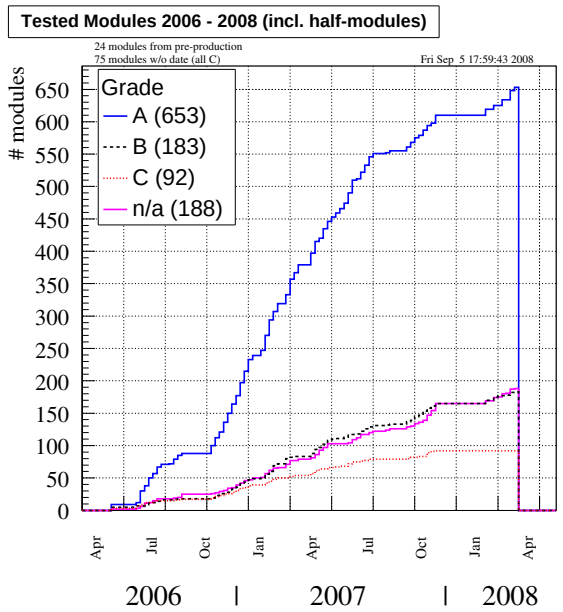
Full tests





Short tests (w/o x-ray)





Summary

- About 1220 bare modules (sensor+ROCs) built
  - 260 (20%) regected at this level, $\sim$80% due to high current
  - Other defects: ROC, HDI, bump-bonding
- 948 modules tested: 90% grade A/B, 10% grade C
  - after thermal cycling: $\sim$20 graded C (high current)
  - after accepted at -10°C rejected at +17°C: $\sim$20 modules (high current)
  - after Short Test: $\sim$40 modules rejected (mostly due to high current)
  - after X-ray: $\sim$10 modules rejected ($\geq$ 1 ROC not 'see' hits)
- Manpower and time
  - Manpower: 2 physicists and 3 PhD students (all $\sim$ 50%)
  - Time: 1.5 years: learning, test development and SW + 2 years of testing
- Crucial items
  - Automatic test procedure and grading
  - Second test setup (cooling box) required
  - DB is a must component: to keep track module test results and logistic
  - All experts in one place!