Software and Commissioning of the CMS Pixel Detector

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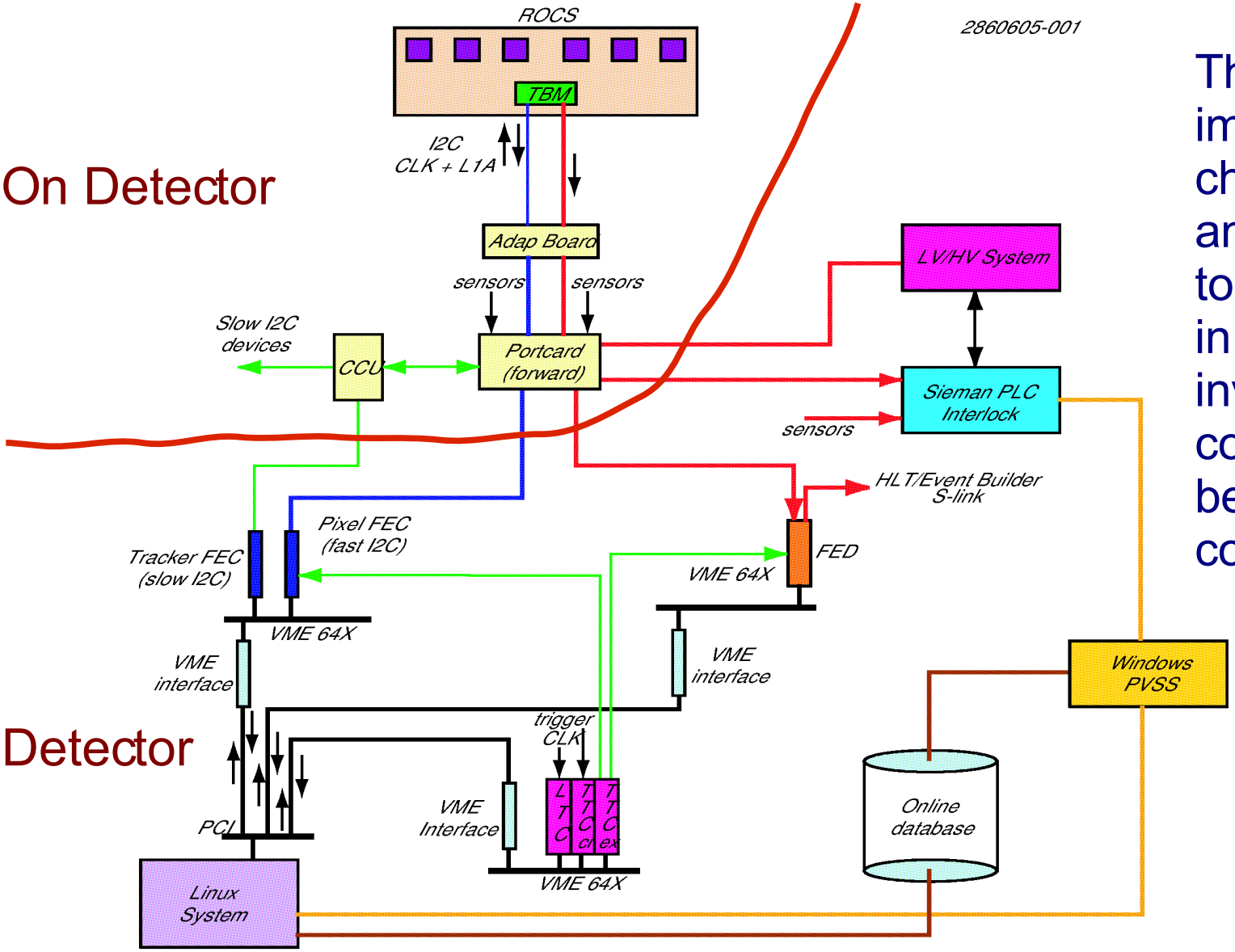
Outline:

- The CMS pixel detector and DAQ
- Some issues

Pixel Control and Readout

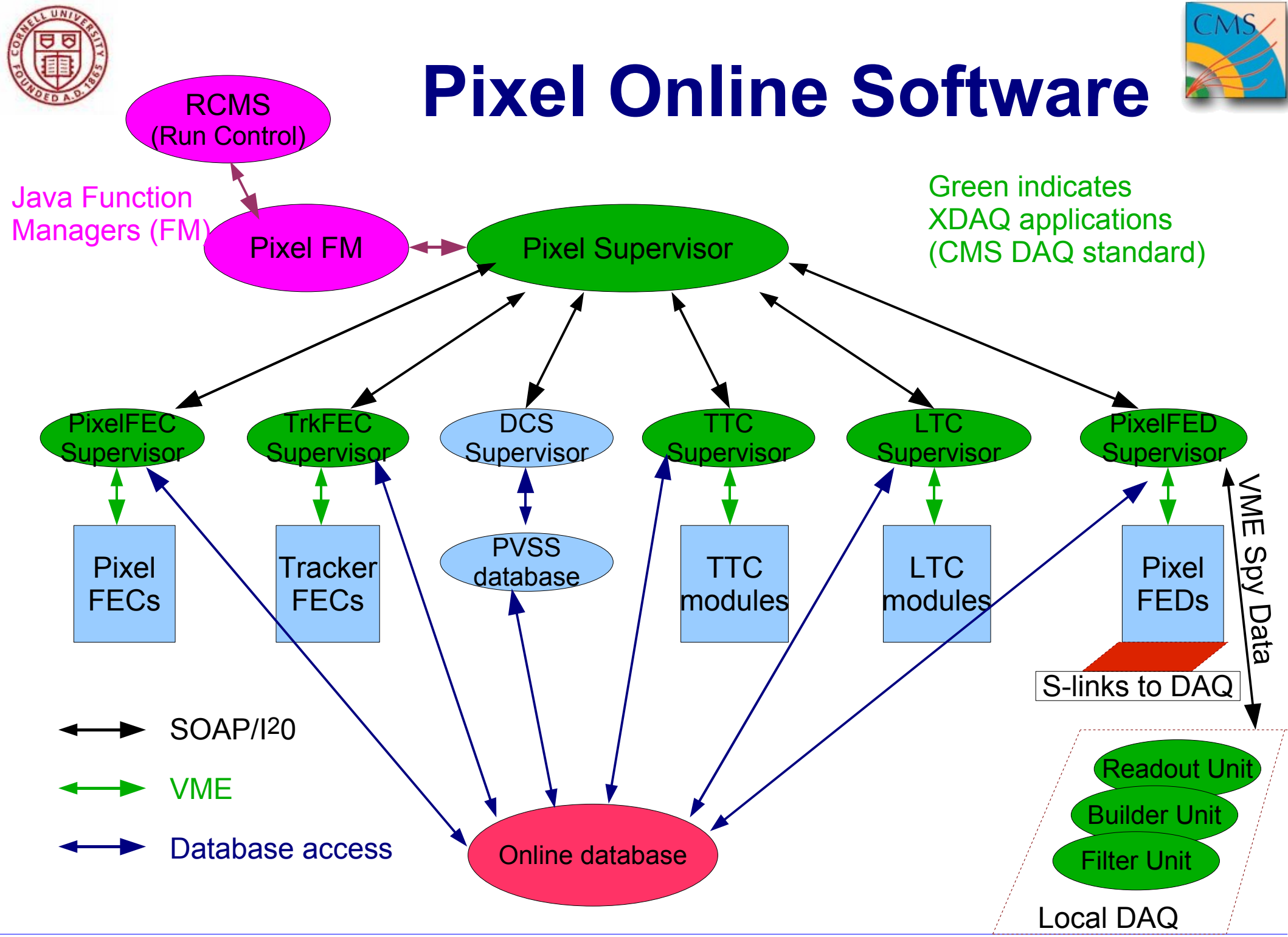
On Detector

Off Detector



This design implies that charge injection and readout has to be controlled in software and involves communication between different computers.

Pixel Online Software



Finding an Operational Point

- In order to be able to configure and read out data a large number of settings has to be determined

  Delay settings for 40MHz communications

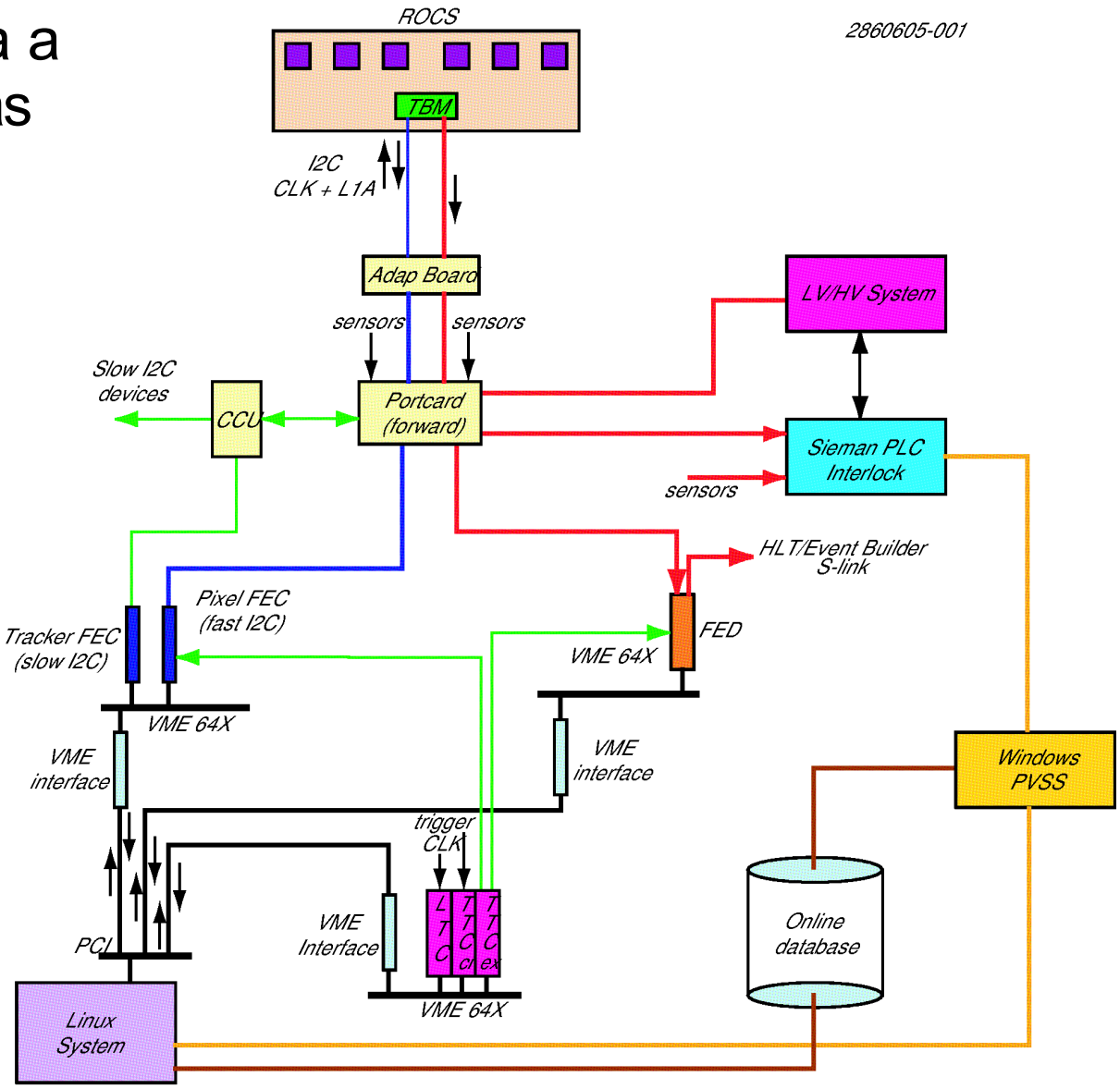
  ROC settings:
  Timing, Pulse Height,
  Gain settings, Linearity.

  TBM Gains

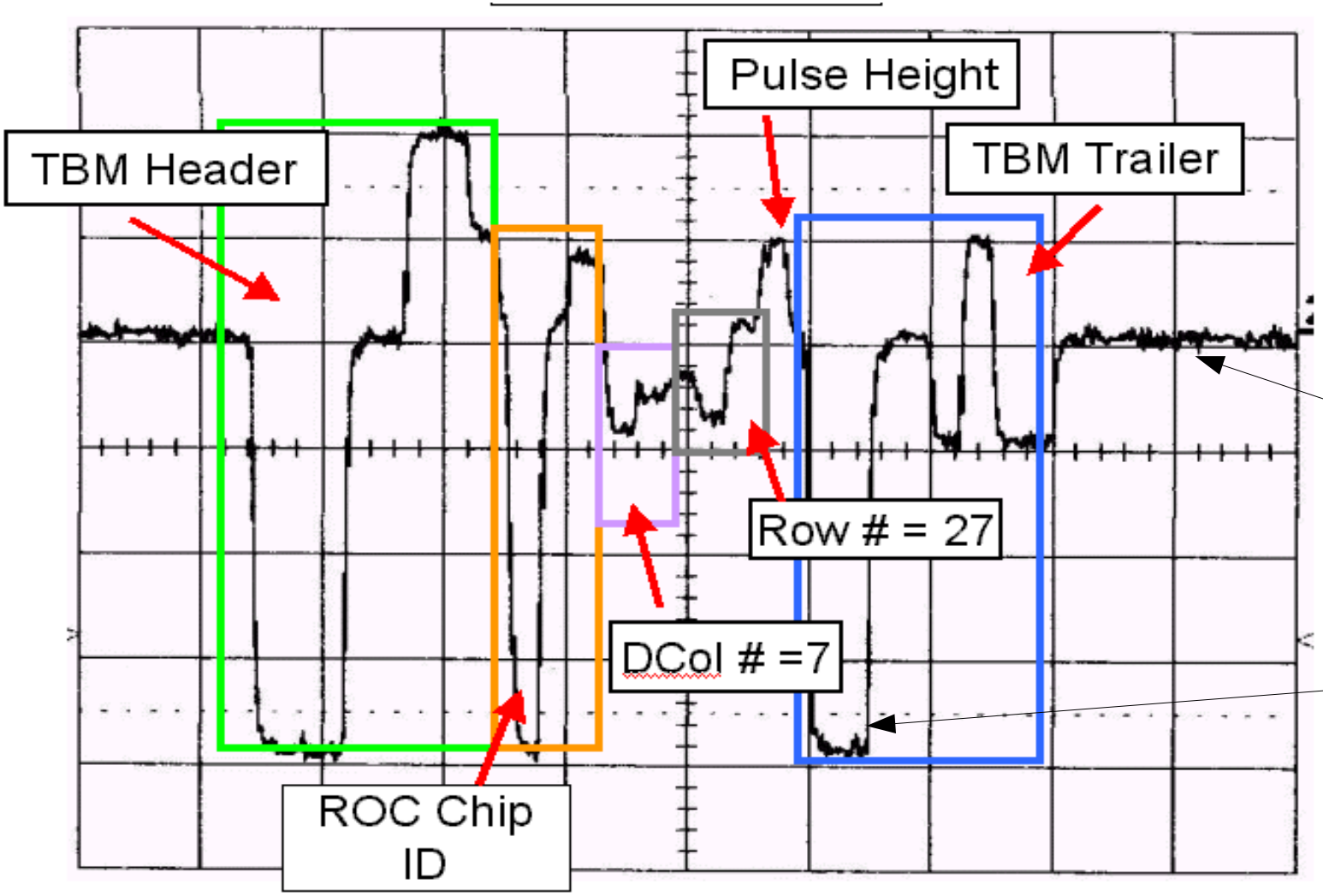
  AOH bias and gain

  Address levels in the FED
  +ADC phase adjustment

- Many adjustments for the analog communication
  - Go digital for readout?



Analog Optical Readout

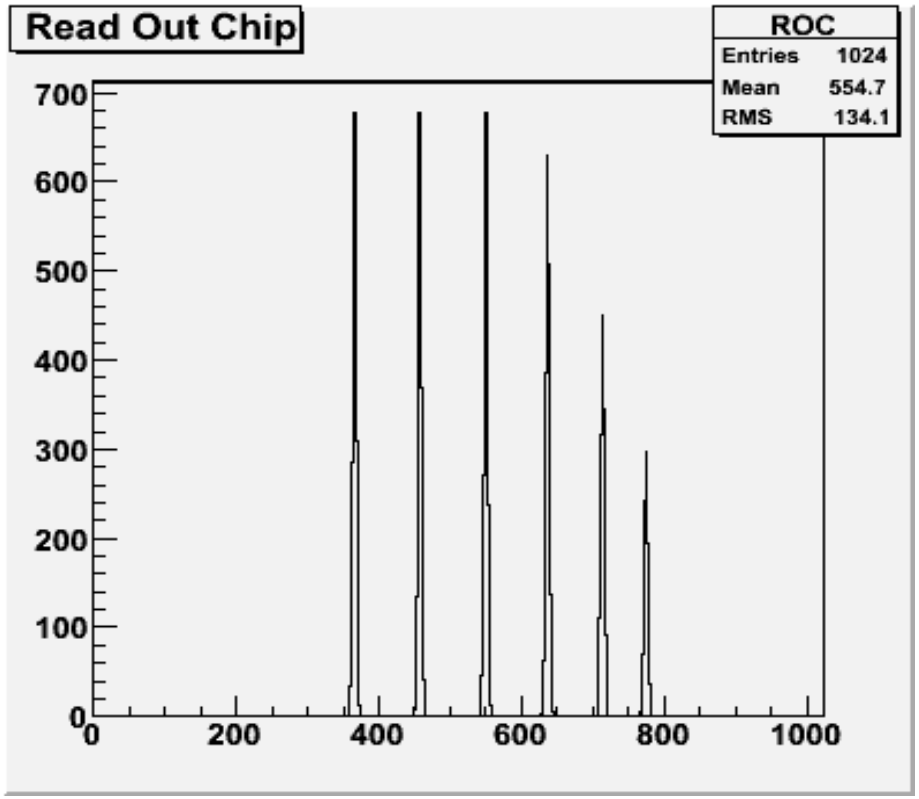


- FrontEnd Driver (FED) digitize and decode this package

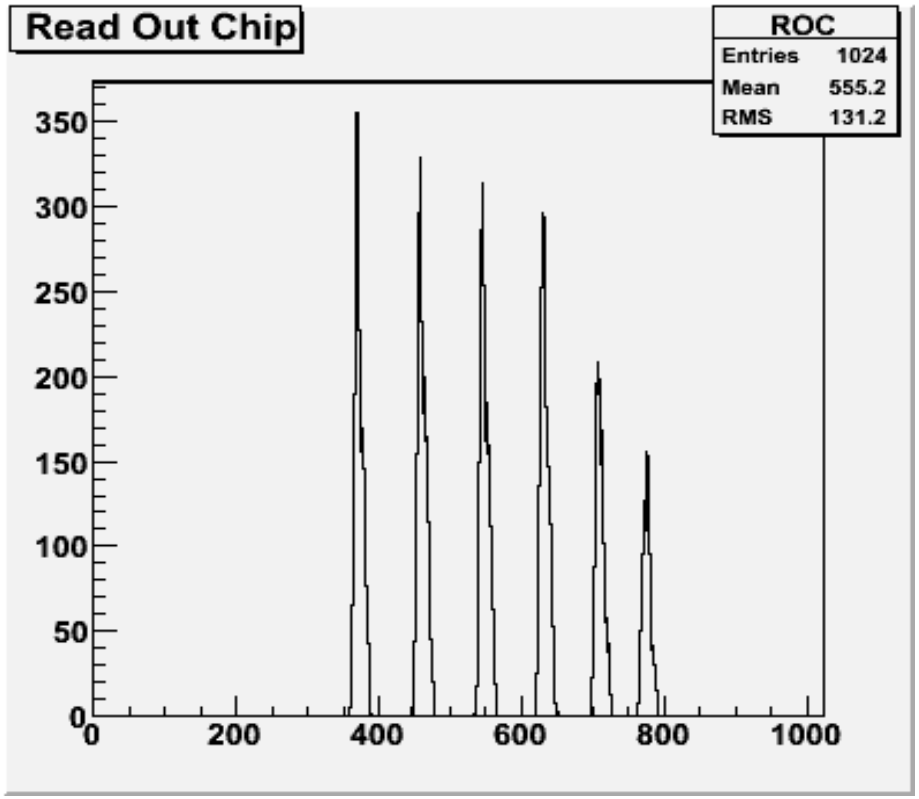
Address Levels

- Clean address levels are crucial to decode the pixel address

Good separation: rms is ~2.5 ADC



Poor separation: rms is >5 ADC

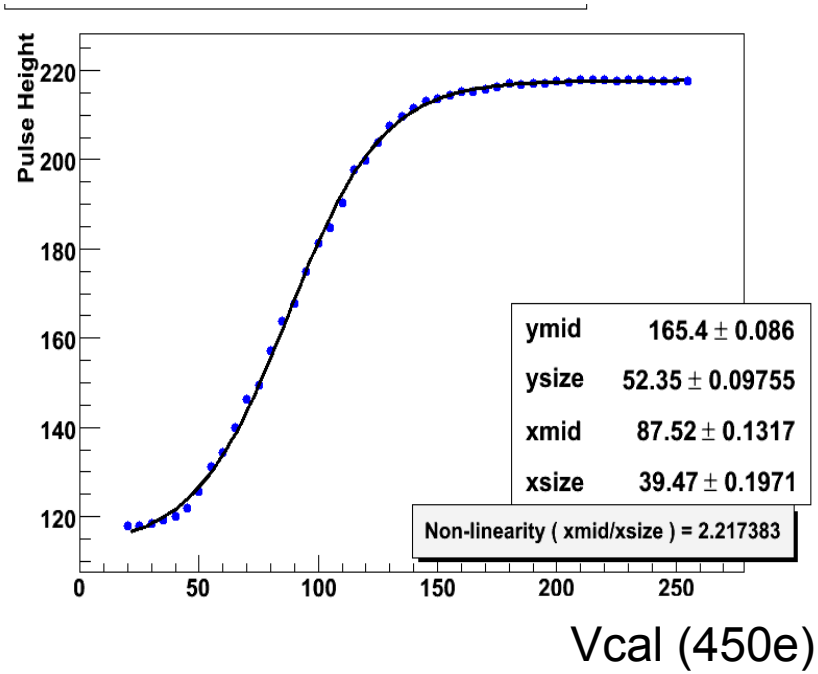


Even with the worse separation on some channels we can separate the different levels

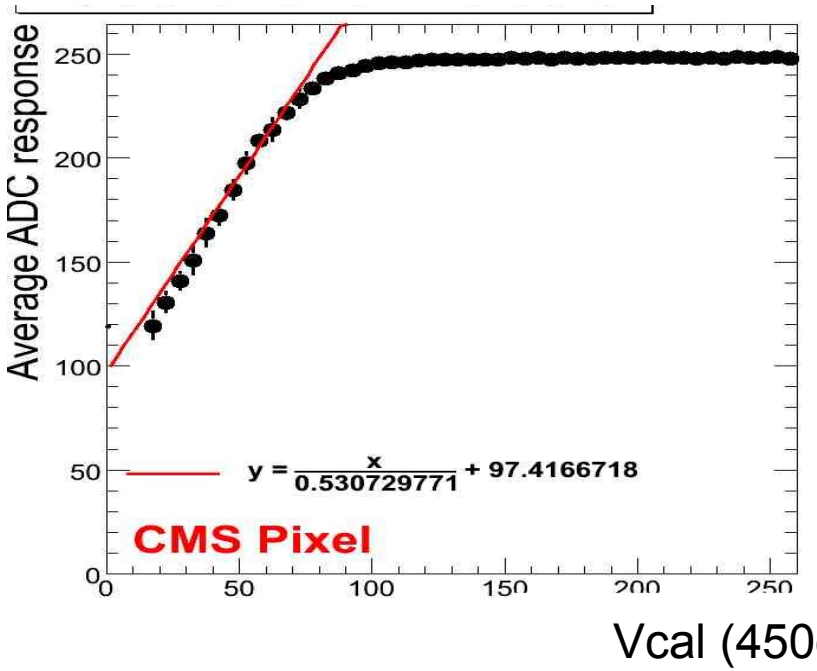
Optimizing ROC DACs

- In module testing and qualification during the production many of the ROC parameters have been tested.
- Again during the commissioning we have repeated these tests with the online software calibrations to determine these settings.
  - Below is an example for the linearity (Vsf adjustment)

Before tuning



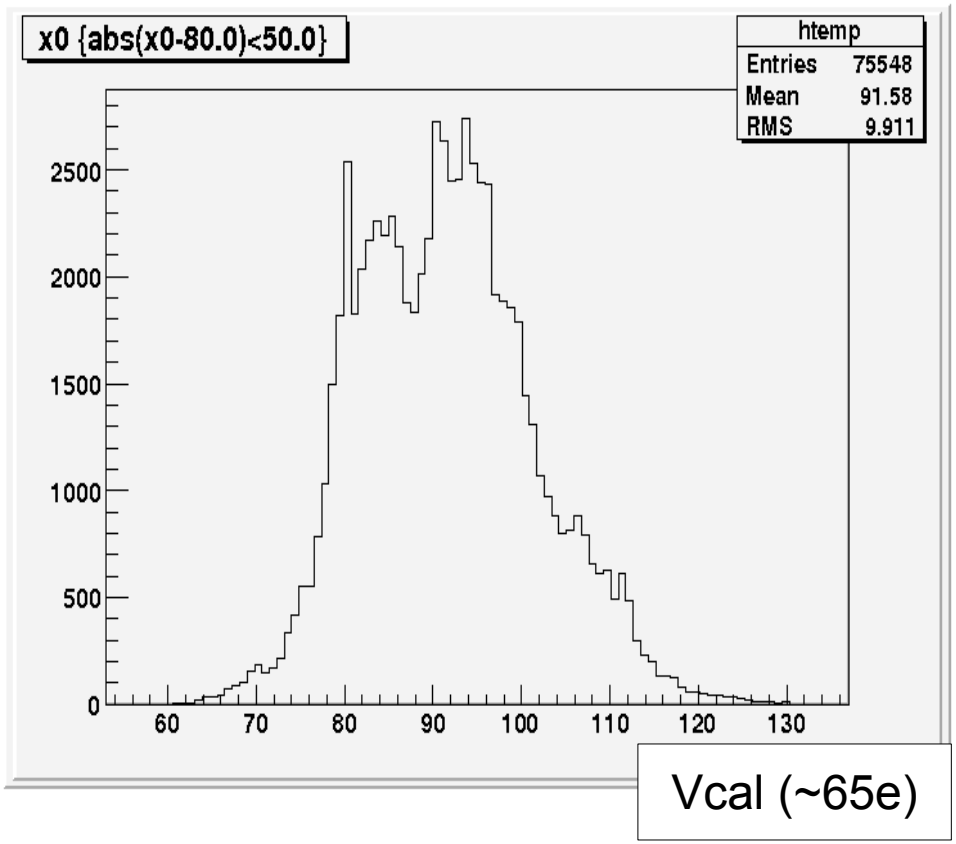
After tuning



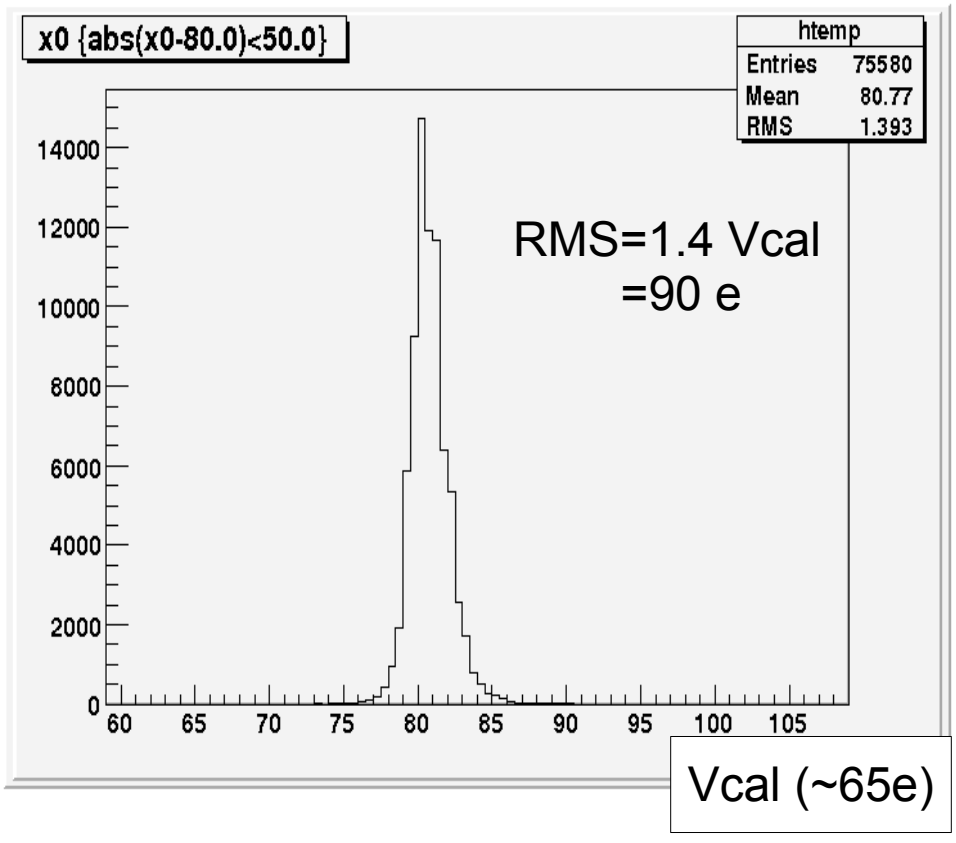
Trimming

- We have developed an iterative method to determine the trim bits and ROC DAC settings that control the threshold.
- We can move the threshold for all pixels in a ROC using the VcThr DAC.
  - Thresholds down to ~60 works for all ROCs.

Before trimming



After trimming



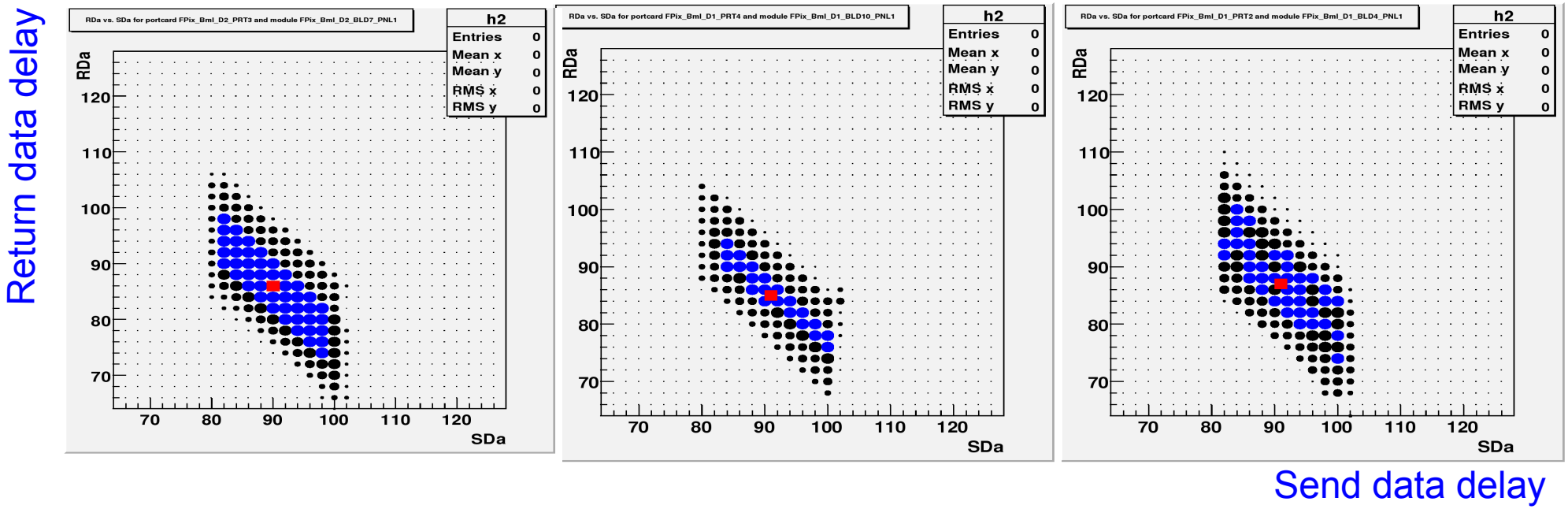
Configuration

- The 40 MHz protocol for configuring the the frontends has worked.
  - We can configure the full detector in less than 60s. (Assuming that the low voltage was turned on.)
- There are some features of this protocol that could have been made easier. Some wishes:
  - Actually reading back registers of the ROC.
  - More robust return data from transmissions.
    - FPix has problems with return data on some channels
    - BPix don't check return data as timing would need to be different for different modules.

40 MHz Readback

- Very small region of return data that works (blue points)

Good region | Small region | `Swiss cheese`



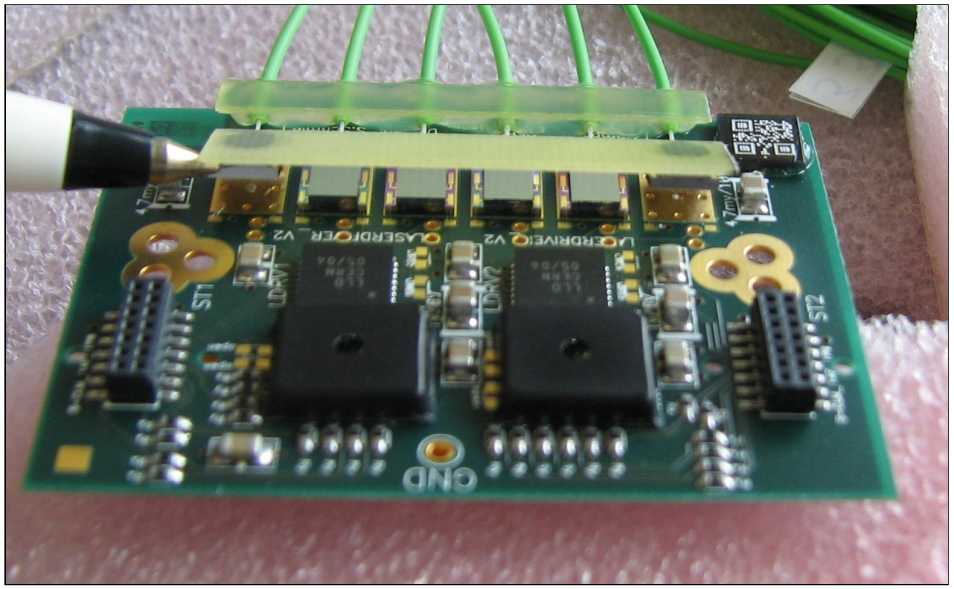
- The failure rate is small and there are some fixes that we are considering implementing:
  - Retry failed transmission – in the FEC firmware
  - The problem with the failure is (almost certainly) in the return data. A different algorithm for decoding the return data in the mFEC is being investigated.

Analog Readout

- The ROC and TBM produces a serial output that encodes the hits on one channel (8 to 24 ROCs).
- The pixel address is encoded using six distinct address levels.
  - These are separated by ~80 ADC counts.
- The AOH (Analog Optic Hybrid) is very temperature sensitive. We measure a change of ~45 ADC counts per degree C.
  - We can not keep the temperature stable to about 1 degree C
- The FED that digitizes the data from the ROCs applies a correction, offset, to take out the temperature variations.
  - This (digitial) correction determines a correction to apply to the ADC value in order to keep the baseline at a fixed value.
  - The baseline is the level when no data is transmitted.
- This correction has to be determined only when no data is transmitted. The logic for this has proven to be difficult to get right.
  - Several fixes to FED firmware to address these issues.

Analog Readout

- FPix as no direct cooling of the AOH. This will probably be addressed in a future shutdown.
  - The AOH temperature runs about 20 degree C above ambient temperature for the FPix detector.
  - After turning on the detector take ~15 min to get to thermal equilibrium where baseline is stable.
- BPix has a thermal connection to the cooling pipes for the detector.
- In addition the AOHs are very fragile. Both FPix and BPix destroyed (broke wirebonds) while handling them.

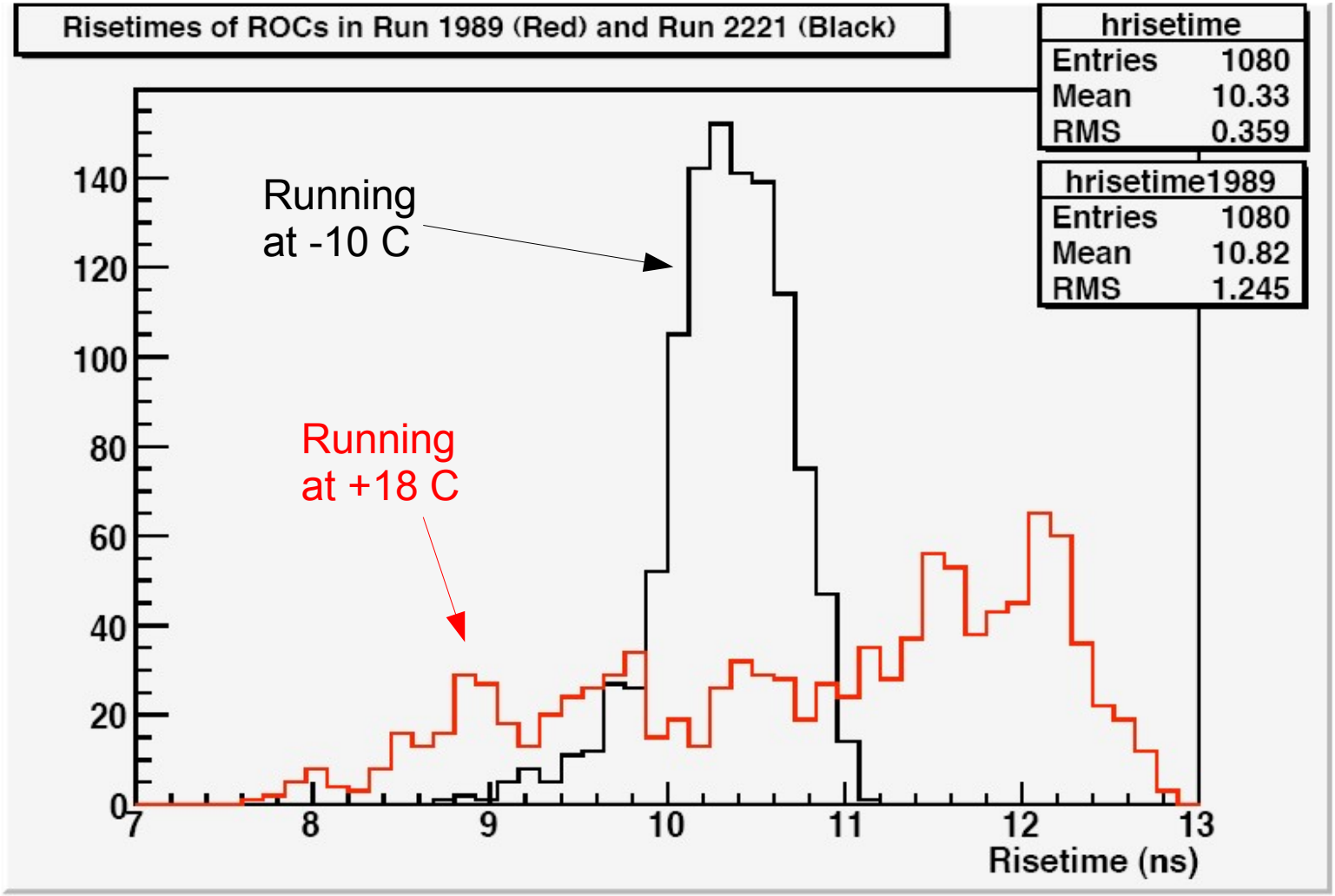


Address Level Separation

- Non-optimal phase used for FED ADC sampling
  - Typically have to pick late point to allow for rise/fall time of signal.
  - In FPix the timing is is slightly different on different plaquettes on a given panel. But we have only one phase setting for all ROCs
- ROC rise time. We found some ROCs to be slower than others. The slow ROCs improve at low temp (-10 C). This was in particular a problem in one FPix half cylinder. Still need to correlate this with production of modules and components. (Next page.)
  - ROC DAC settings have a very minor impact on the rise time.
- Sometimes poor address levels are correlated with a large RMS of the black level. This is often improved by cleaning the fibers.
- Other cases are not yet understood. Tends to affect all ROCs, so likely not a ROC related issue. But TBM, portcard, AOH could cause this.

ROC Rise Times

- All 1080 ROCs on one FPix half cylinder
  - Different types of modules need different timing.



Conclusions

- 40 MHz serial protocol works.
  - Fast configuration.
  - Return data checking not fully reliable (yet).
- Analog chain
  - Temperature sensitive
  - Address level separation
- Readout and control separated
  - This is the CMS DAQ model