PAUL SCHERRER INSTITUT

PSI

Design studies of a low power serial data link for a possible upgrade of the CMS pixel detector

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Pixel Replacement/Upgrade Discussion Meeting

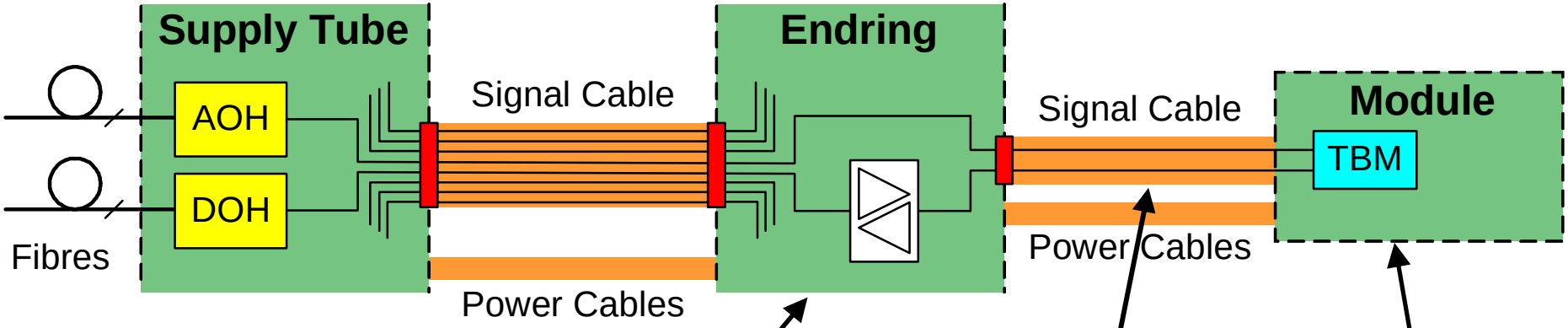
Motivation

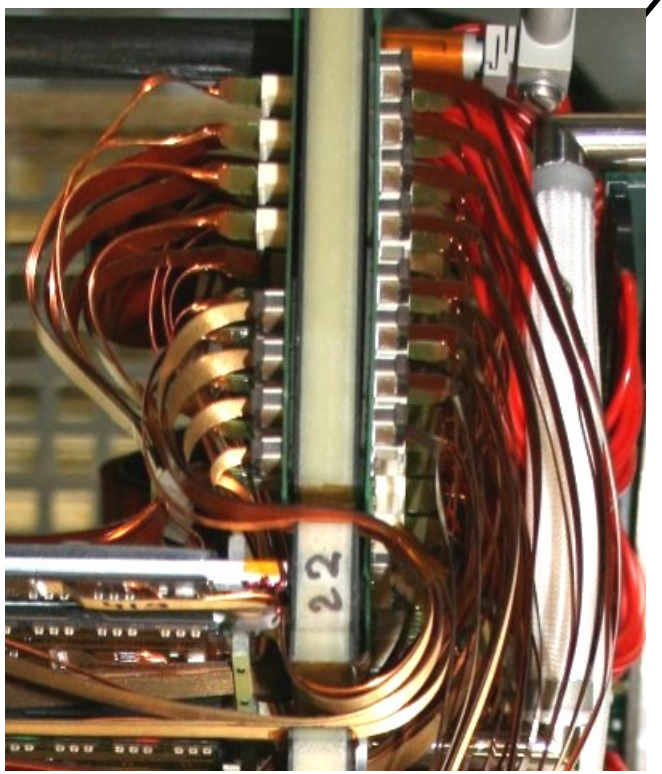
Communication link between detector (pixel module) to outside the tracker volume (BPIX supply tube) with

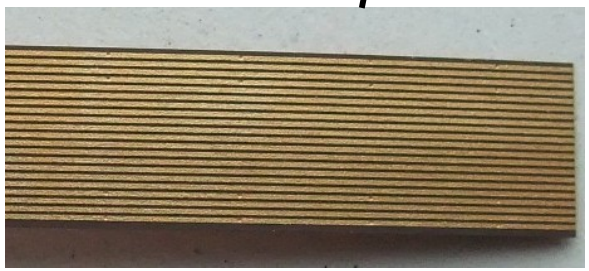
- minimal material budget → micro twisted pair (unshielded)
- minimal power consumption → low voltage swing → differential
- minimal wiring effort (# cables) → serial data link
- 160 or 320 Mbit/s (4x or 8x LHC clock)
- 1…2 m cable length

What is possible ?

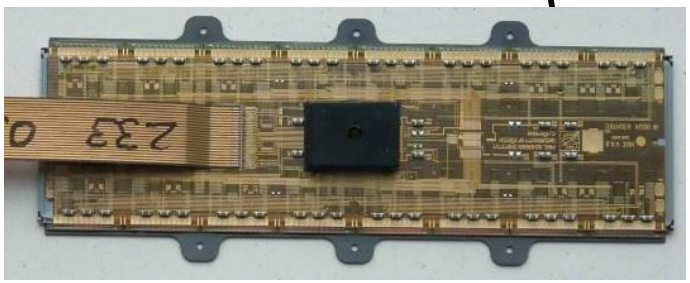
Existing Data Link in CMS Pixel Detector





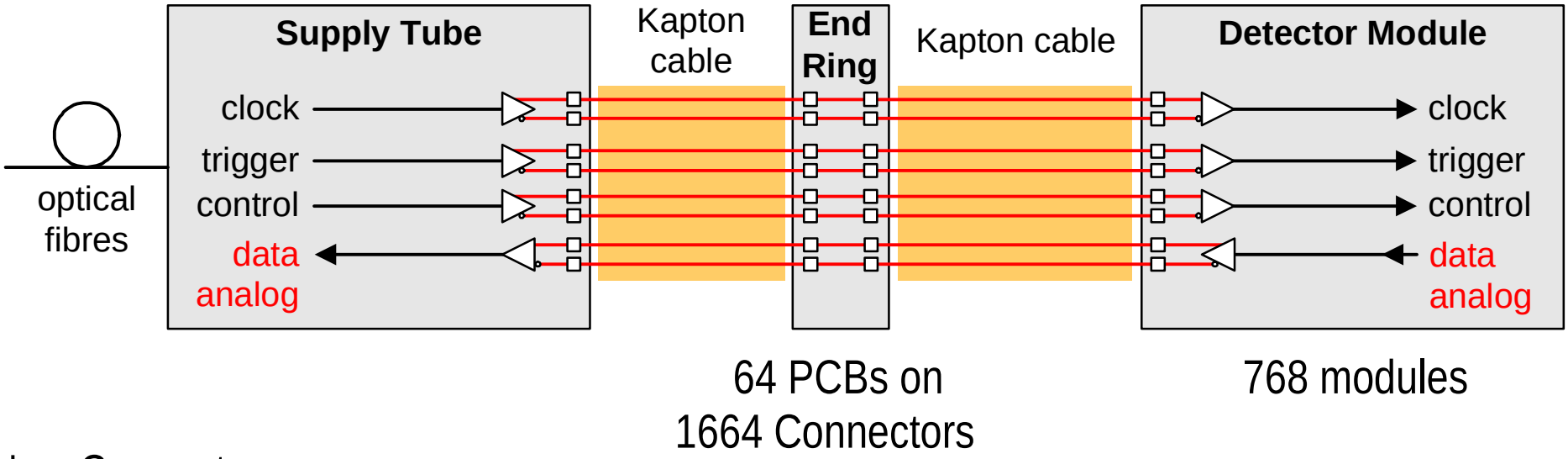


Kapton cable with 21 traces and ground plane

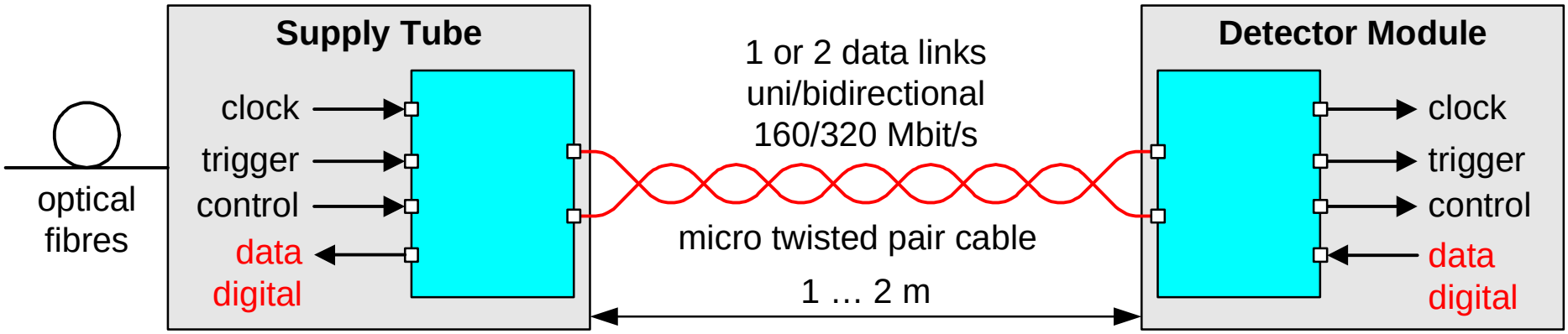


Comparison to a possible new Concept

Existing System in CMS Pixel Detector

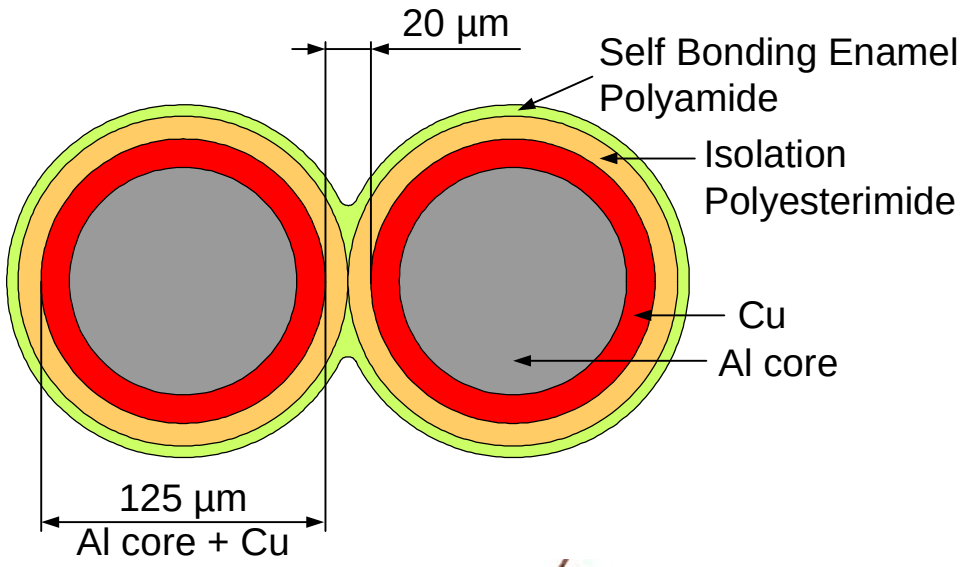


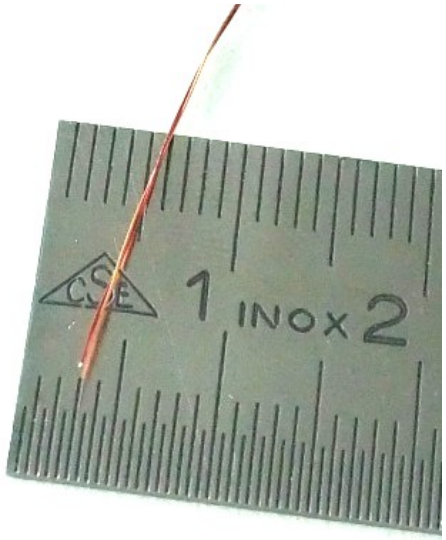
New Concept



Micro Twisted Pair Cable

cross section





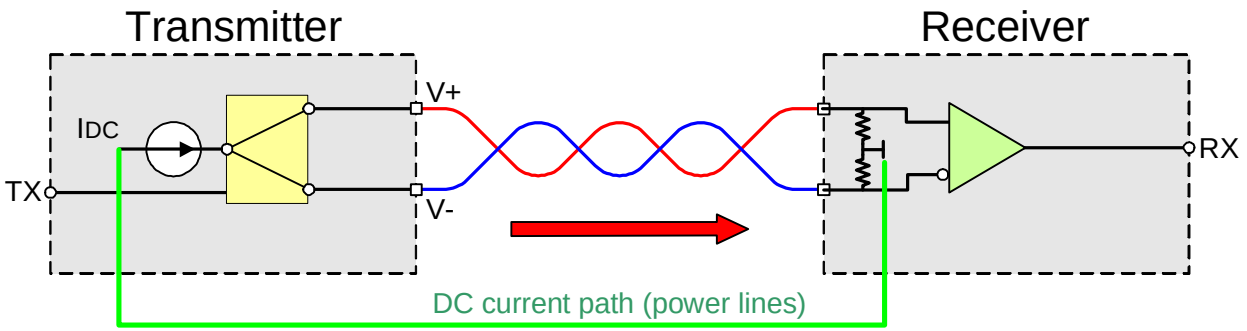
First Choice:

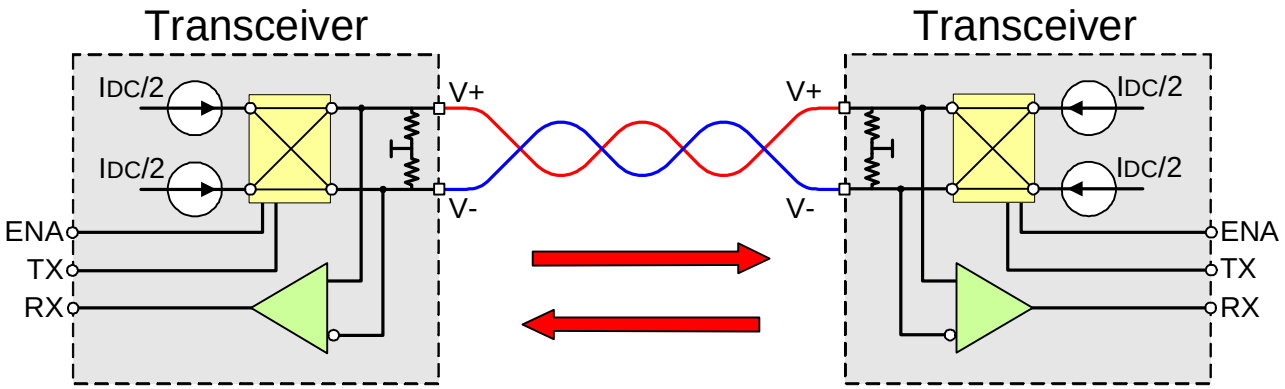
- twisted pair self bonding wire
- 125 µm wire diameter (4um Cu)
- 10 mm per turn

Electrical characteristics:

- Impedance: 50 Ohms (very low)
- v = 2/3 c_0 (5 ns/m)
- C = 100 pF/m, L=250 nH/m
- R_{DC} = 2.3 Ohm/m
- Skin deepth = 8.5 µm @ 100 MHz
- R = 8.5 Ohm/m @ 100 MHz
- 50% power loss (2 m cable)

Data Link Configurations



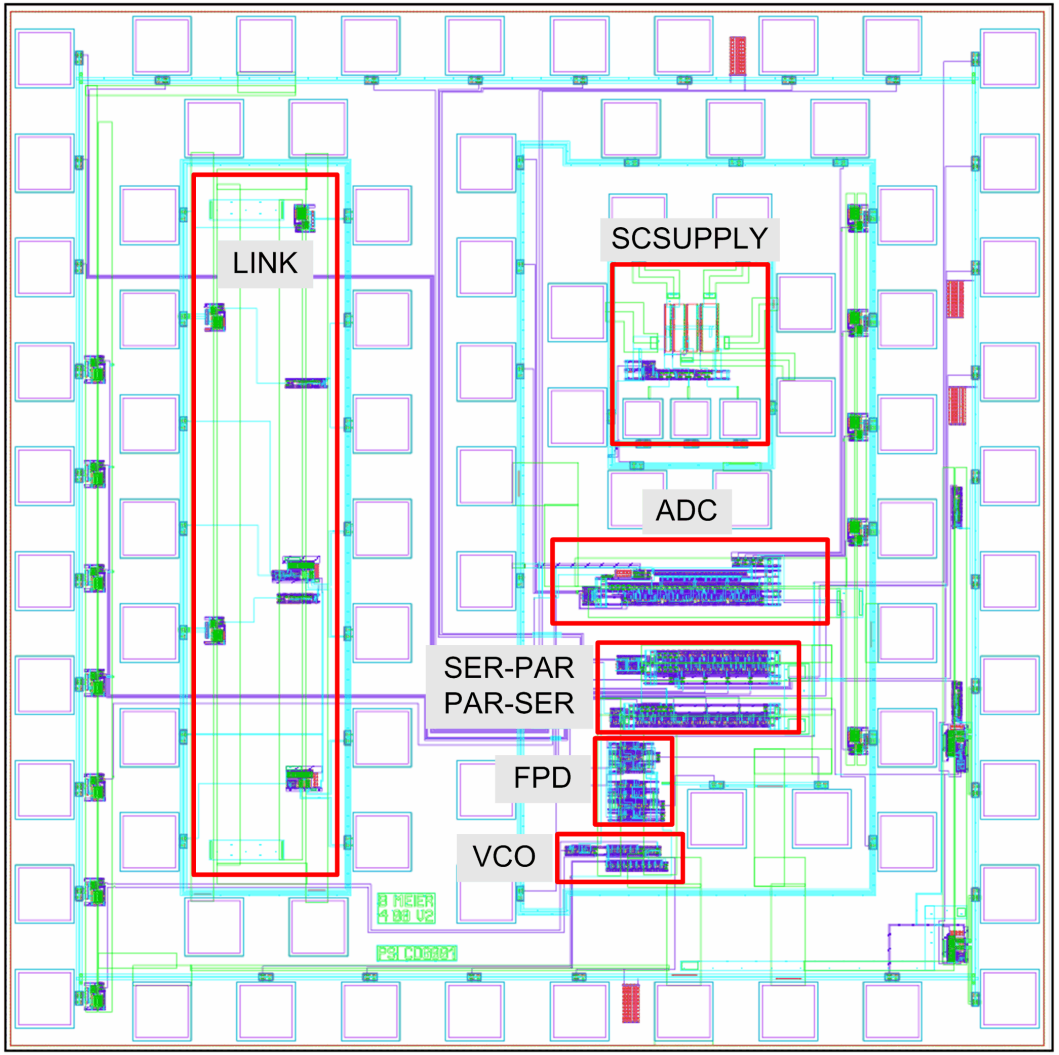


- Differential Current Driver (LCDS) from CMS Pixel
- rise time < 400 ps
- DC loop closed over power lines
- uni/bidirectional
- for test: output signal adjustable with IDC

Logic Levels

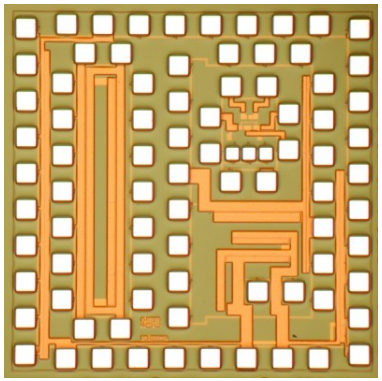
	V+	V-	diff	sum
L	0	IDC	-IDC	IDC
H	IDC	0	+IDC	IDC
high Z	IDC/2	IDC/2	0	IDC

Test Chip Layout

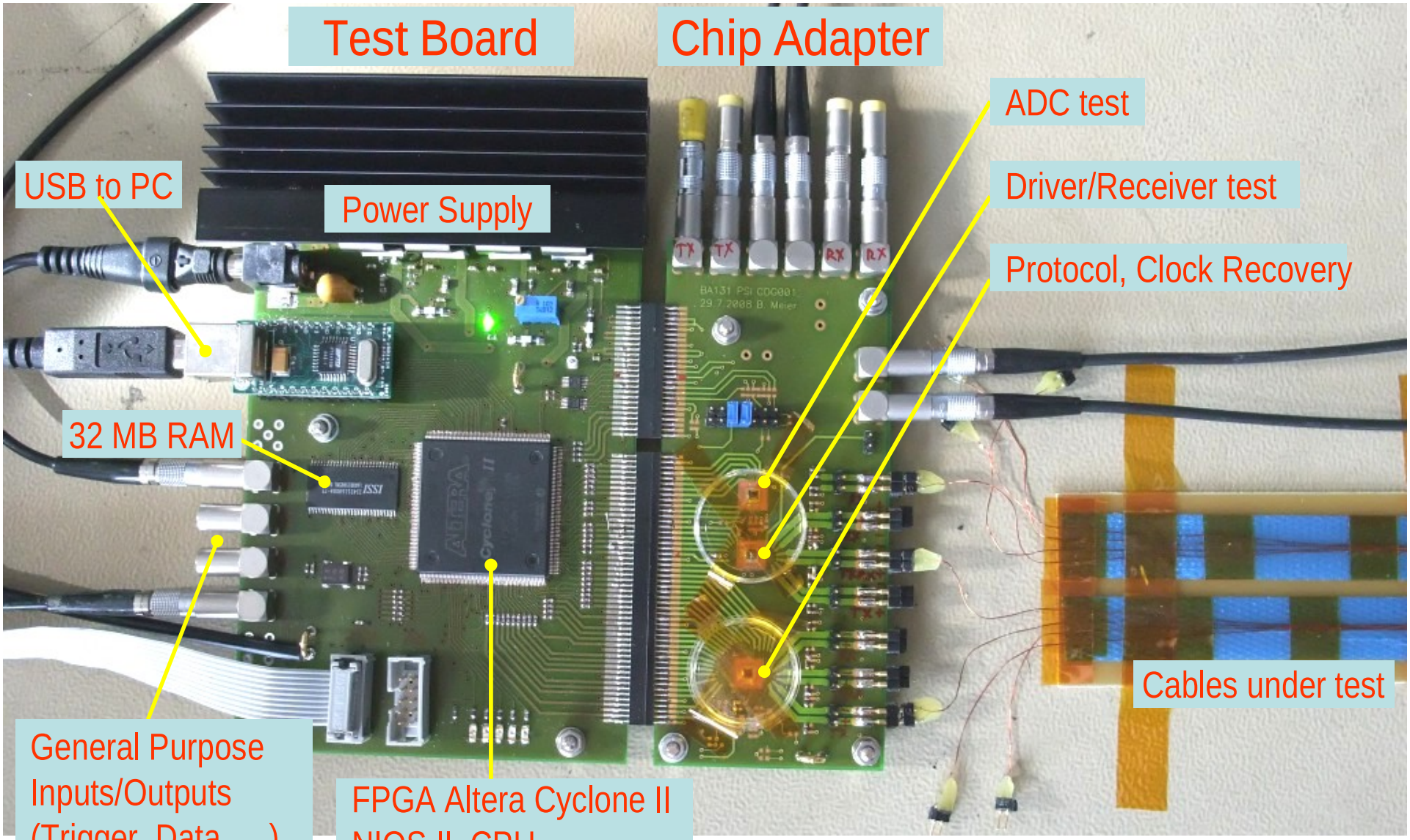


Design of a first test chip
(PSI Chip Design Core Team)

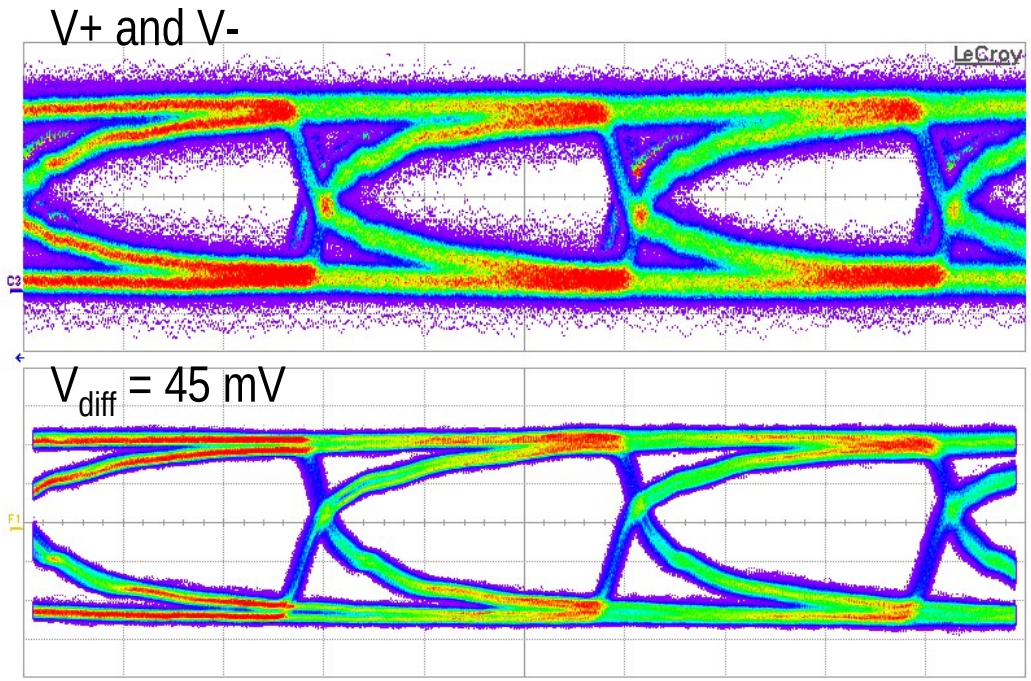
- Size: 2 x 2 mm
- Technology: 250 nm CMOS IBM
  same as CMS Pixel ROC
- radiation hardness design
- CERN MPW submitted in April 2008
- design time was 4 weeks



Chip Test System

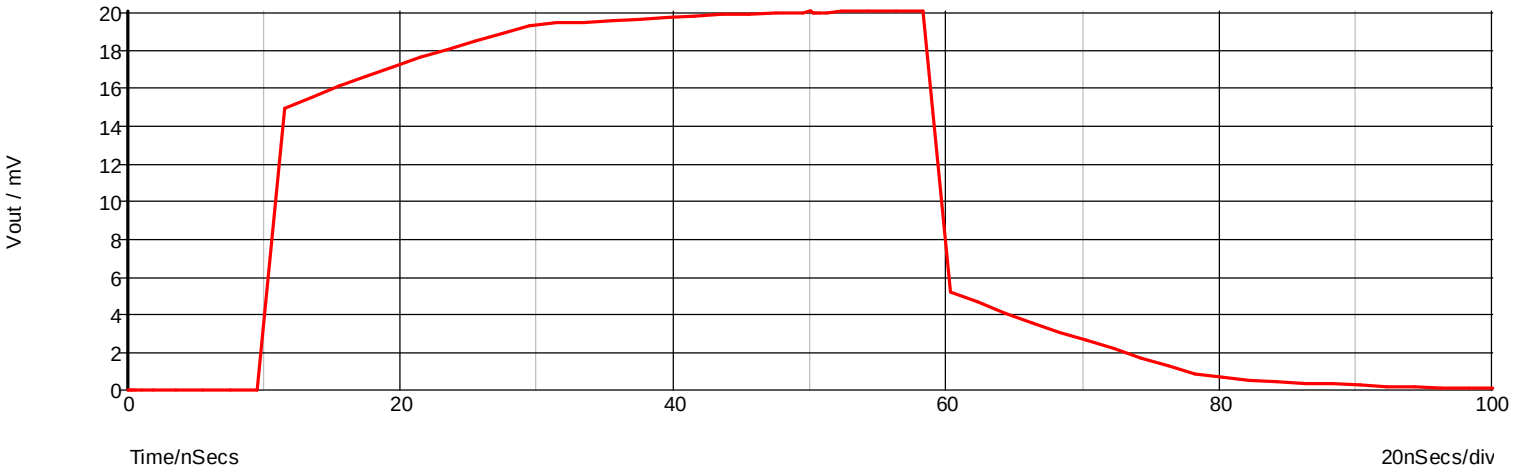


Loss Effects at 160 Mbit/s

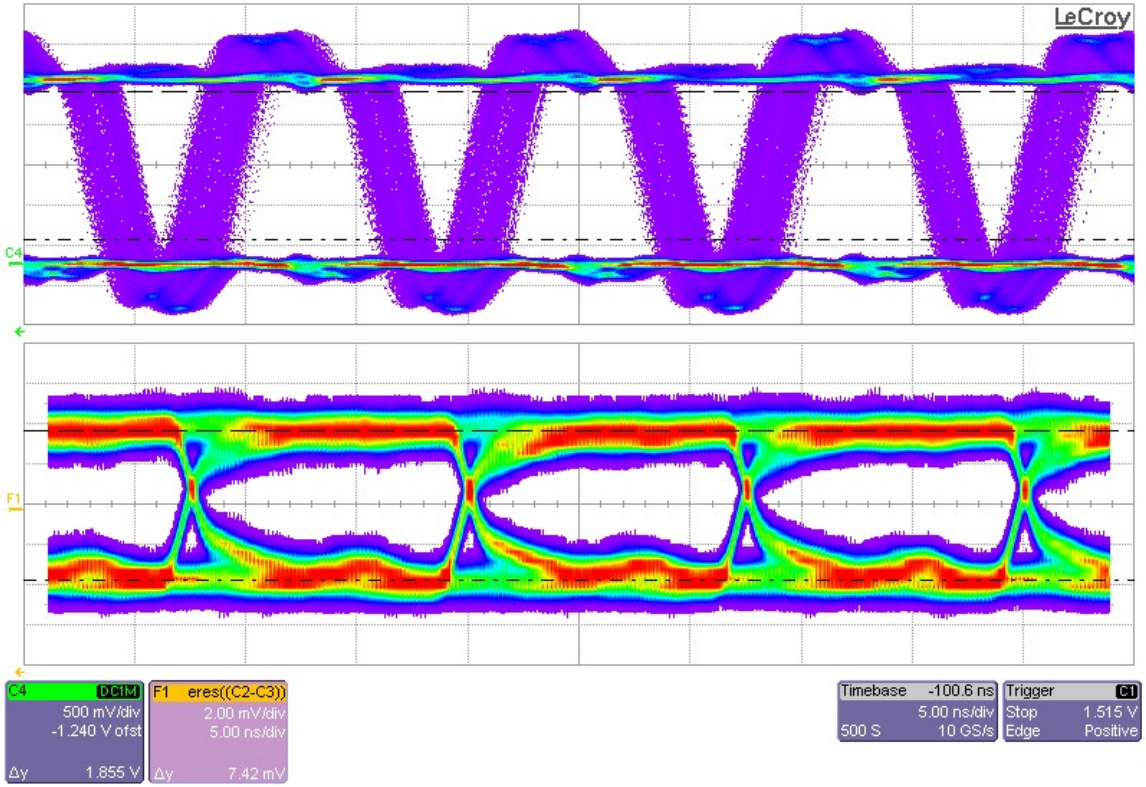


- Line length: 2 m
- Lossy line effects visible (rising and falling edges)
- Line in the RC (low frequency) and LC (high frequency) region

Fast and slow region in rising/falling edge as a result of the lossy line



Bit Error Rate Measurements



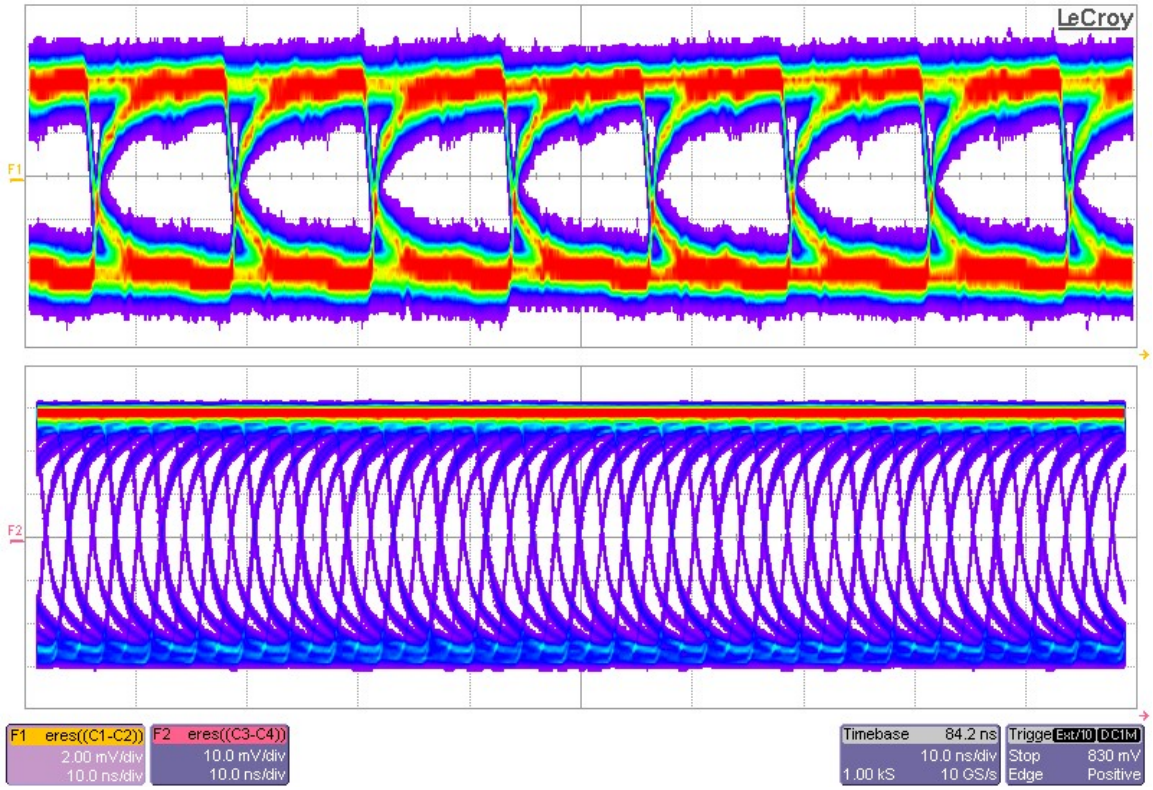
Receiver output signal

V_{diff} = 7.4 mV @ 80 Mbit/s

Scope bandwith limited to 1 GHz

- 80 Mbit/s and 160 Mbit/s
- Bit Error Rate < 10^{-11}
- Receiver design error (time asymmetry) → amplitude at receiver > 35 mV @ 160 MHz

Crosstalk



V_{diff} = 9 mV @ 80 Mbit/s

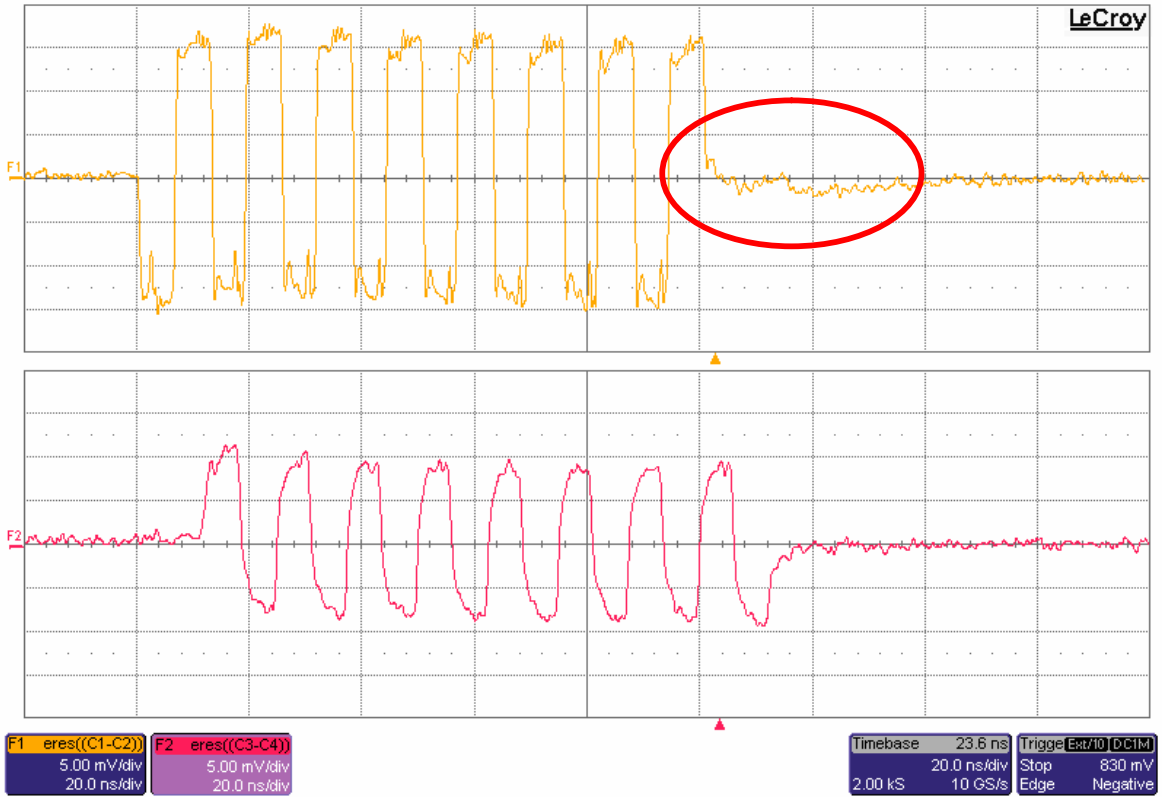
Scope bandwith limited to 1 GHz

parallel line signal (asynchronous)

V_{diff} = 56 mV

- 80 Mbit/s and 160 Mbit/s (with higher level)
- No difference in bit error rate visible with/without disturbing signal
- very robust for crosstalk (twisted cable, high capacitance cable)

Tranceiver switching Time

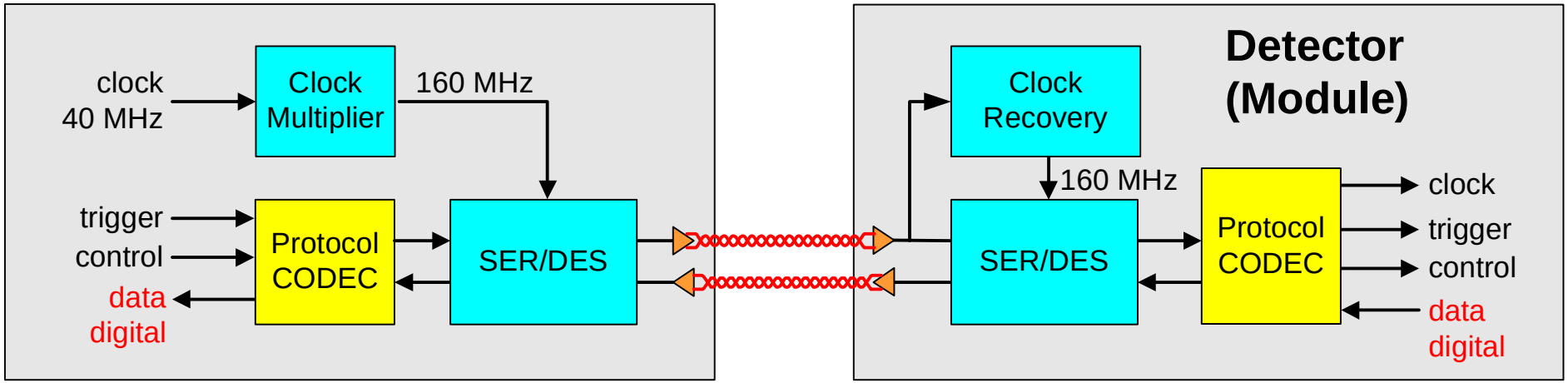


V_{diff} = 27 mV at transmitter

V_{diff} = 18 mV at receiver (line end)

- Data direction switching at 160 Mbit/s
- Line length: 2 m
- minimal delay for line stabilization (less than 1 signal round trip in a 2 m line)

Data protocol



Implemented on the Chip (blue)

- Clock multiplier (PLL)
- Clock recovery (PLL)
- Serializer/Deserializer SER/DES

To implement on the FPGA (yellow)

- Bit coding
- Protocol

Different cable configuration

- 1 cable, bidirectional ↔
- 2 cables, unidirectional → ←
- 2 cables, bidirectional ↔ ↔

Conclusions, Outlook

- 160 Mbit/s is tested
- Less than 10 pJ per bit
- Power for module data link: 2.4 mW (+PLL) new, 26 mW existing
- No crosstalk problems, it is possible to bundle the unshielded cable

- Tests with 320 Mbit/s
- Tests with other wires
- Clock recovery, PLL, VCO
- Run different data protocols (data packets)