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The Silicon Vertex Detector of the Belle II Experiment (12' + 3')

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The Belle II experiment at the SuperKEKB flavor factory will operate at an unprecedented luminosity of $8 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$, which is about 40 times larger than its predecessor Belle experiment. The vertex detector is composed of two-layer DEPFET pixel detector (PXD) and four-layer double-sided silicon microstrip detector (SVD). To achieve a precise vertex position determination and excellent low-momentum tracking, even under the high background and high trigger rate of 10 kHz, the SVD employs several innovative techniques. In order to minimize the parasitic capacitance in the signal path, 1,748 APV25 ASIC chips, which readout signals from 224k strip channels, are directly mounted on the ladders with the novel Origami concept. The analog signals from APV25 are digitized by an FADC system and sent to the central DAQ and also to online tracking system based on SVD hits to provide the region of interests to PXD in order to reduce the data size of PXD to achieve the required bandwidth and data storage space. In this talk, we present the design principles and construction status of the Belle II SVD.

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