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High Luminosity LHC Pixel Readout Test Chip and RD53A Prototype Plans (12' + 3')

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A pixel readout test chip called FE65-P2 has been fabricated on 65nm CMOS technology and tested with and without bump bonded sensors. FE65-P2 contains a matrix of 64 x 64 pixels on 50 micron by 50 micron pitch, designed to read out a bump bonded sensor. The goals of FE65-P2 are to demonstrate excellent analog performance, isolated from digital activity well enough to achieve 500 electron stable threshold, and radiation hard to at least 500Mrad, and to prove the novel concept of isolated analog front ends embedded in a flat digital design, called "analog islands in a digital sea". Each analog island is completely surrounded by digital circuitry, which is generated by automated place and route tools and will therefore be different around every island. FE65-P2 is about 4mm x 3mm and was produced in a multi-project run. Matching sensors are bing produced by several labs/manufactures, including Stanford, FBK, and Hamamatsu, and will be single-die bump bonded to FE65-P2. Results of these hybrid assemblies before and after irradiation and in test beams are expected to be available for ICHEP.
Experience from FE65-P2 chip and hybrid assemblies will be applied to the design for a large format readout chip, called RD53A, to be produced in a wafer run in early 2017 by the RD53 collaboration. The status of RD53A will also be covered.

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