R&D on analog and digital r/o electronics for large LAr TPC detectors for neutrino and astroparticle physics experiments

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ETHZ, 3rd CHIPP Neutrino Meeting, 18/11/2008

Swiss Institute of Particle Physics

Historical background

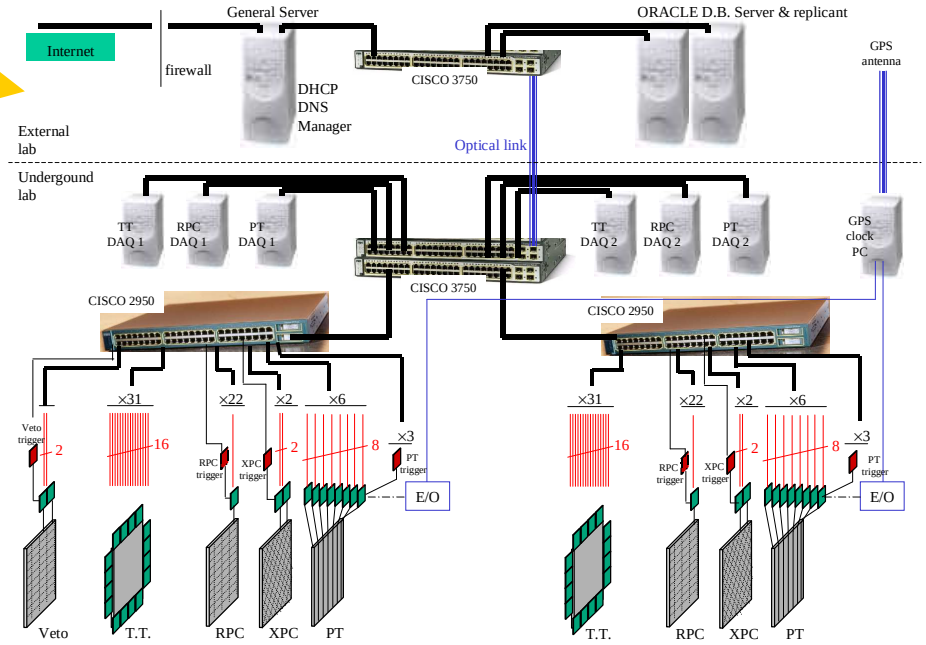
At IPN Lyon we started an R&D program to develop a modern low cost readout for LAr TPC detectors

➢In Lyon there was already experience from the development of the electronics for the digital readout and DAQ for OPERA.
➢Also experience in the development of analog F.E. electronics for L3,CMS,ILC.

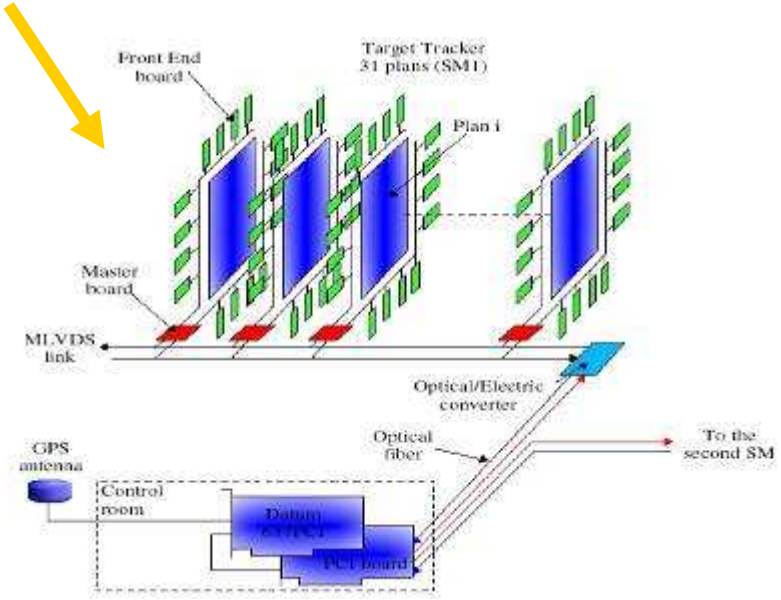
- DAQ development in OPERA : "smart sensors" concept
  - Independent common interface : processor board (FPGA+32-bits CPU+FIFO) on a standard Ethernet network
  - Triggerless system
  - External clock (+GPS) to synchronize local fine counters
  - Standard distributed software (CORBA)
  - 1200 sensors (PMT, RPC, drift tubes) taking data since mid-'06
- Local expertise in analog electronics
  - Long terms R&D on CMS FPPA + tests of the MGPA
  - Imaging applications ASIC design (pre-amplifier) to start the R&D and gain expertise on cryogenics.

OPERA readout structure

DAQ structure based on a Gigabit Ethernet network (1200 nodes) :



Clock distribution system for event time stamp using the GPS clock:



Heart of the DAQ system : Mezzanine ~150 eur/piece

- used in all subdetectors DAQ
- contains CPU (embedded LINUX), memory, FPGA, clock receiver and Ethernet

TT board containing ADC, DAC, HV, test pulse system ~180 eur/unit

RPC controller board

HPT/TDC board

Starting motivation: update the ICARUS design, reduce costs, improve performance
→ Develop the electronics for the 2Km LAr detector for T2K, O(10K channels).

- Appealing to handle in a coherent way both the analog and digital part of the project
- This R&D has a general orientation and interest for future applications of LAr TPCs (astro-particle physics, neutrino factories etc …) for the low cost readout of hundreds of Kchannels (Glacier, Laguna, T2K phase II)

- Activity started in January 2007 → R&D on readout electronics for the LAr TPC including both the analog front-end (cold electronics) and digital readout:

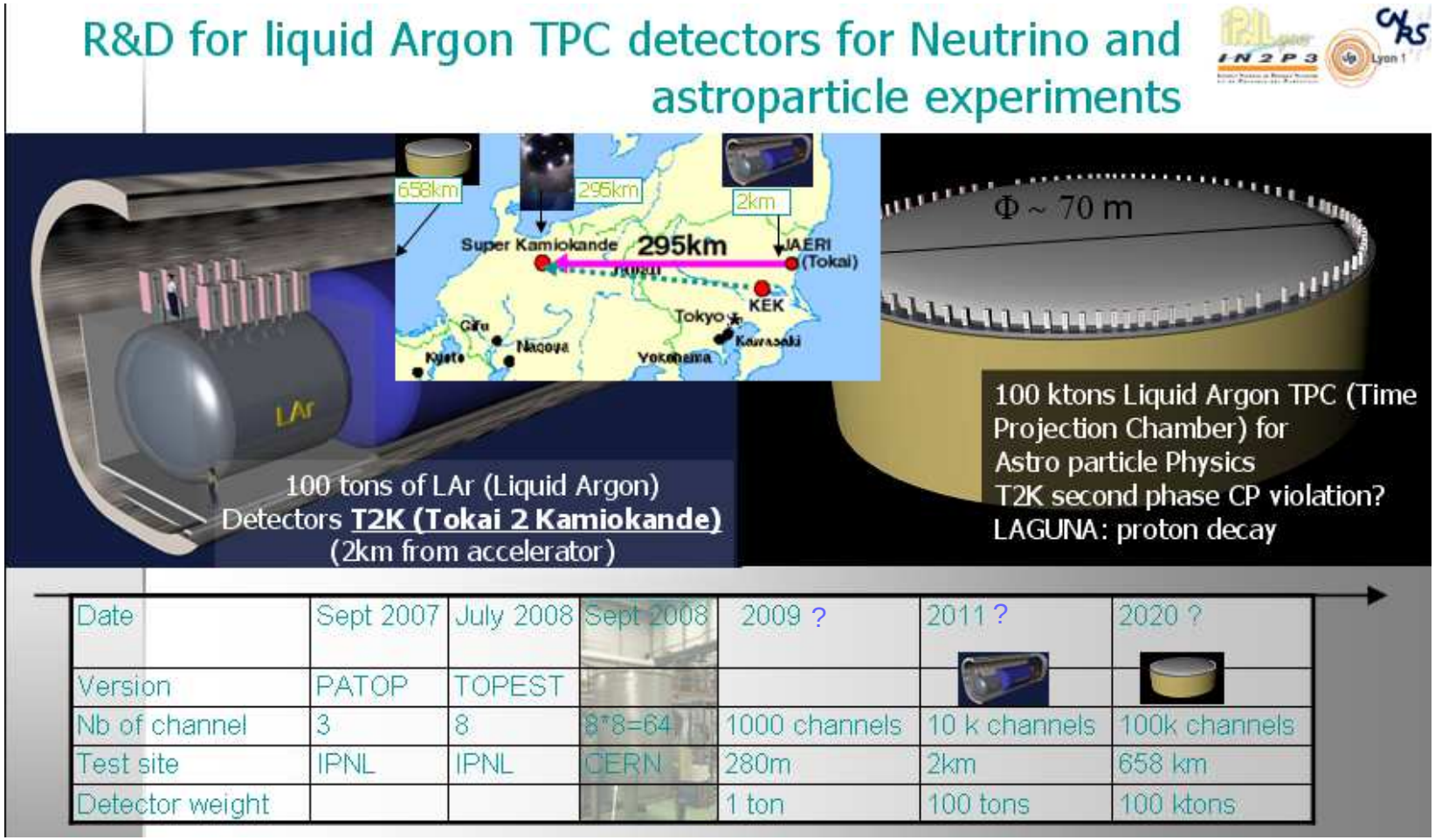
✓ R&D on a analog ASIC preamplifier working at cryogenic temperature for the charge readout of the LAr TPC
→ASIC preamp at low temperatures

✓ R&D on the Gigabit Ethernet readout chain + network time distribution system PTP (IEEE1588)

Lab tests up to now, tests on LAr prototypes to be started now in collaboration with ETHZ/Bern

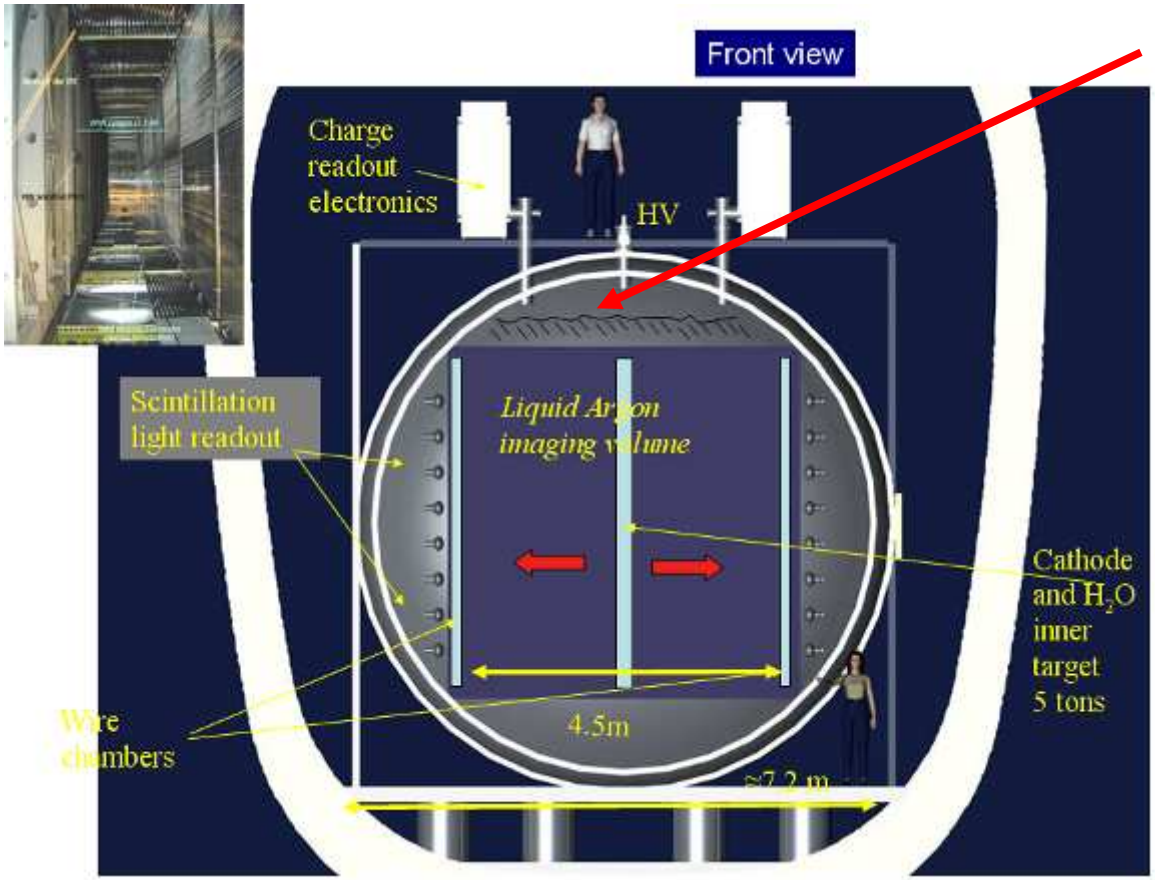
LAr R&D for T2K (IPNL-ETHZ-BERN-KEK- …):

✓Started with the 2KM LAr detector (+ Glacier)
✓2008 additional motivations in view of the T2K phase II



Date	Sept 2007	July 2008	Sept 2008	2009 ?	2011 ?	2020 ?
Version	PATOP	TOPEST				
Nb of channel	3	8	8*8=64	1000 channels	10 k channels	100k channels
Test site	IPNL	IPNL	CERN	280m	2km	658 km
Detector weight				1 ton	100 tons	100 ktons

"Small" 1ton prototype at 280m (neutrino cross sections)
2KM LAr detector (Proposal submitted by the T2K collab. Jparc PAC June/07)
100Kton detector for T2K phase II and astro-particle physics (also connected to EU program LAGUNA)



Gas phase ~100K

LAr detector at 2Km for T2K: analog and digital electronics (10K channels)

→ to be reoptimized following specific requirements (wire geometry, drift time, beam trigger) and reduced in cost starting wrt the one developed for ICARUS

→Development of analog FE ASIC at cryogenic temperatures, integrate power switching

Expected signal: ~ 15000 electrons (3mm m.i.p.)
ICARUS: Equiv. Noise charge: (350 + 2.5 x C_{in}) electrons = 1200 el.

Advantages of cold electronics:

- **Remove cables and their capacitance increasing Cd → lower noise**
- **Exploit intrinsic noise reduction at low T (minimum around 110K)**
- **Large scale integration and costs reduction (1~1.5 eur/ch)**

→ Better S/N increasing the physics performance and allowing to optimize also the detector granularity

Started with expertise at IPNL on low noise analog electronics but no experience in cold electronics → acquire expertise (of general validity)

Step 1) (2007) Validate simulations not guaranteed at low temperature

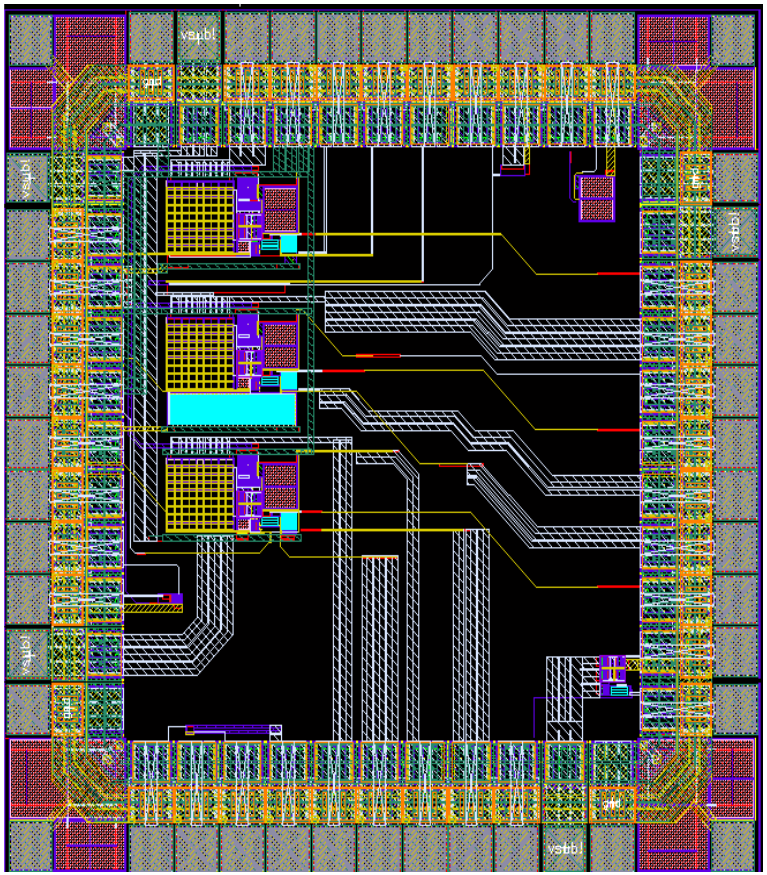
a) Tests on the already available Immotep preamp at low temperature (compare with simulations), problems with phase margin

b) First version of the preamp (PATOP) folded-cascode ASIC CMOS 0.35um

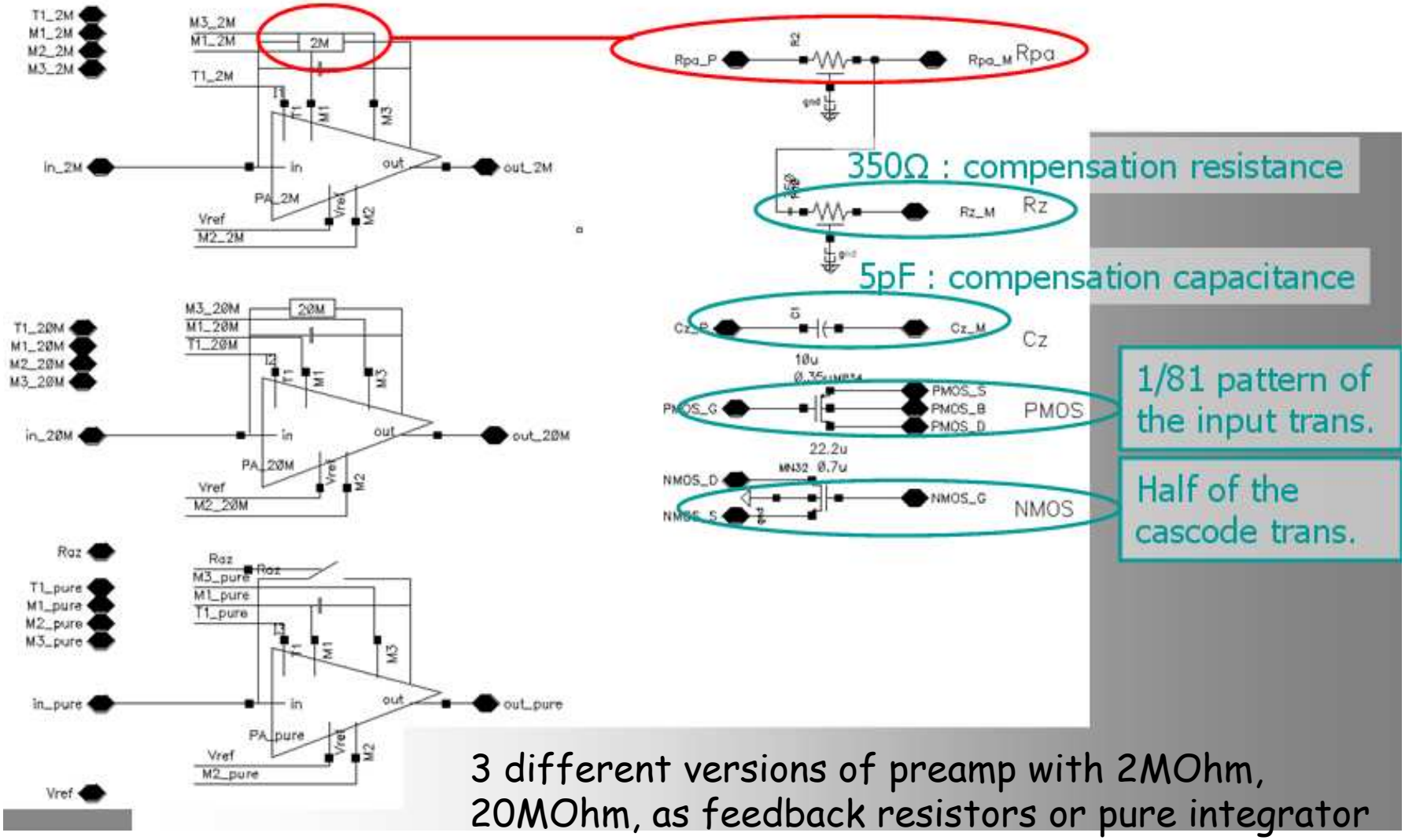
Multi-Project Circuit (CMP)
Foundry run (25 June 2007)
Techno AMS C35B4C3.

Several channels to be used for components characterization.

→ About 1000 e- ENC at 110K with Cd=250pF (-30% wrt room temperature 1500 e-)

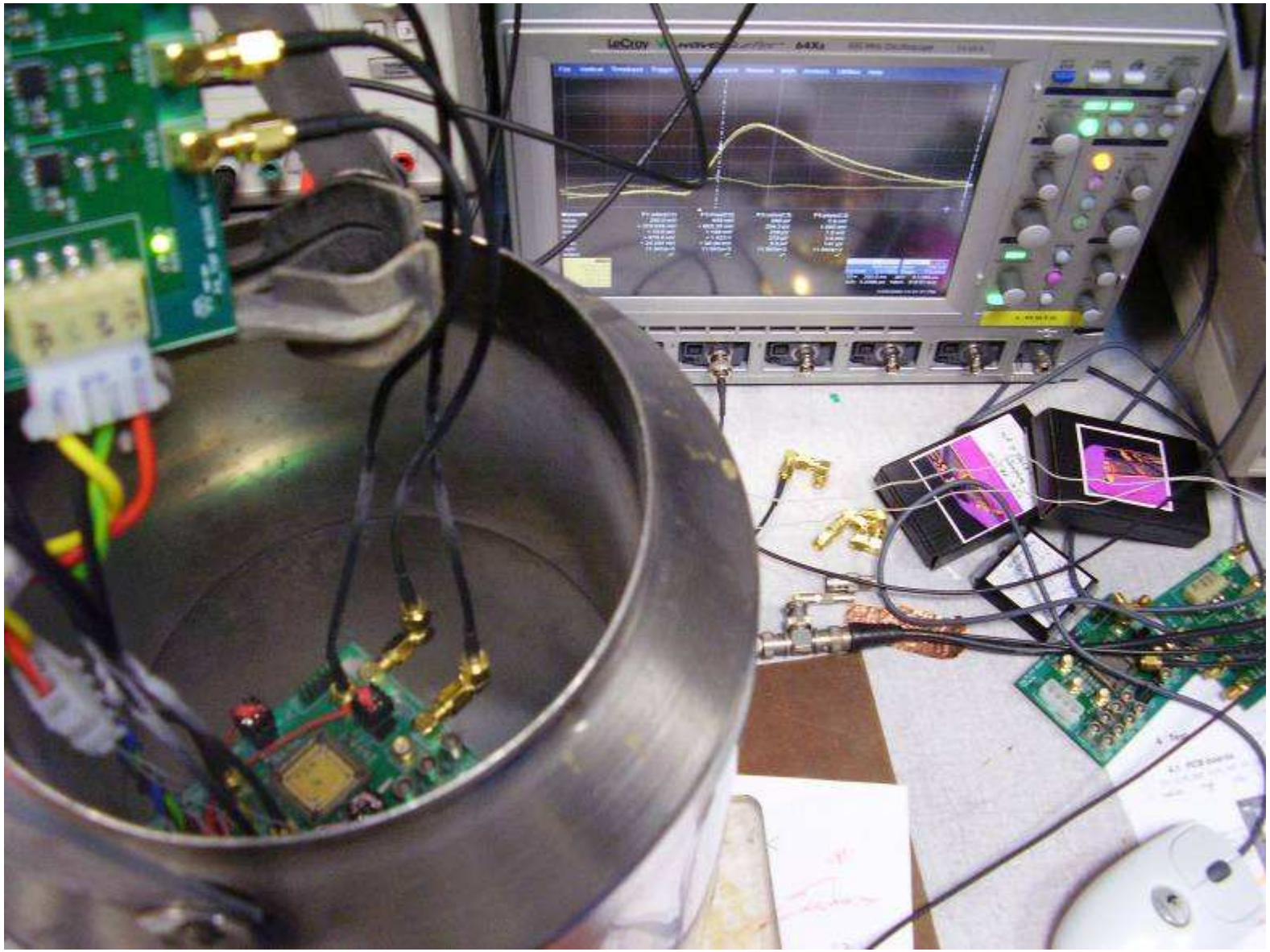


Inside PATOP test chip



3 different versions of preamp with 2MOhm, 20MOhm, as feedback resistors or pure integrator with a switch

Test setup in Liquid Nitrogen N2 @ 77K



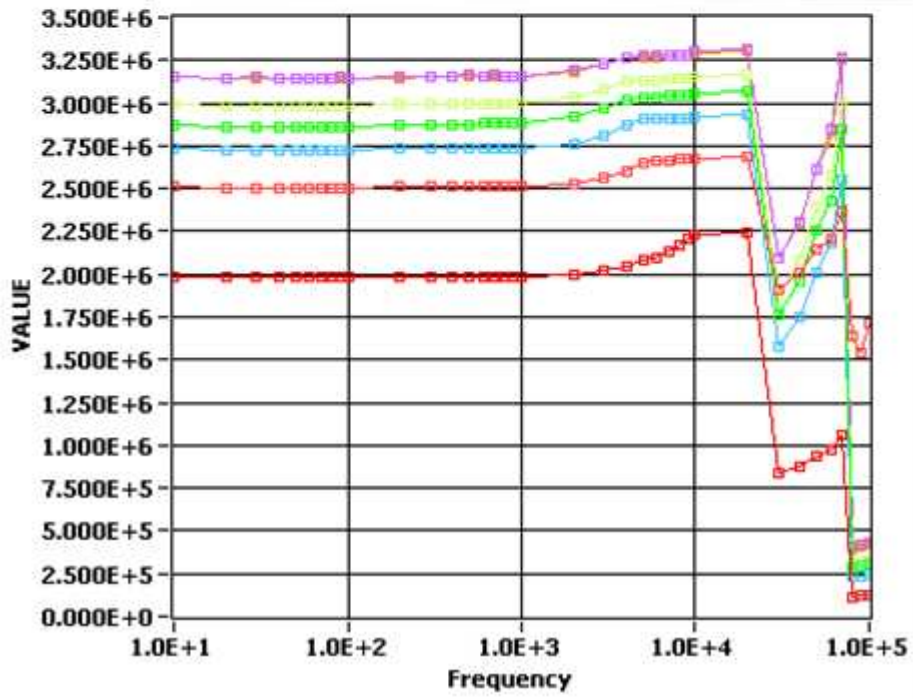
Resistance for various temperature

$$\frac{R(T)}{R(T0)} = 1 + TCR1(T - T0) + TRC2(T - T0)^2$$

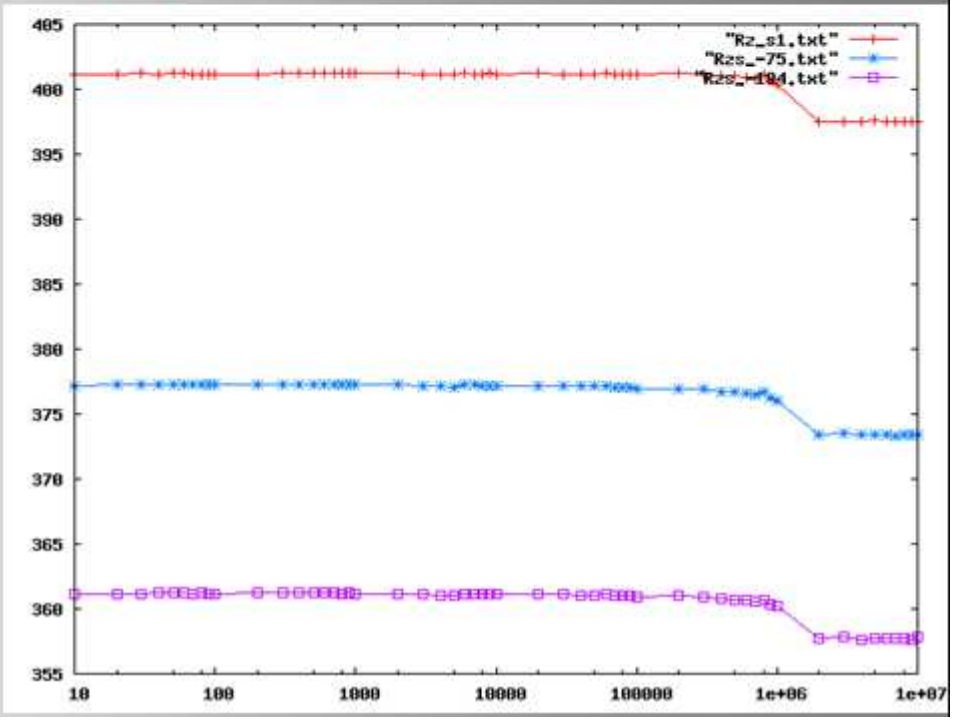
T0 27°C	RT0		TCR1 ($10^{-3}\Omega/K$)	TCR2 ($10^{-6}\Omega/K$)
	spec.	exp	exp	exp
rpoly2	350Ω	400Ω	0.70	1.17
rpolyhc	2MΩ	1.8MΩ	-2.37	5.70

Measured Using a QuadTech 7600 RLC meter

Rpolyhc 2MΩ ambiant to -196°C

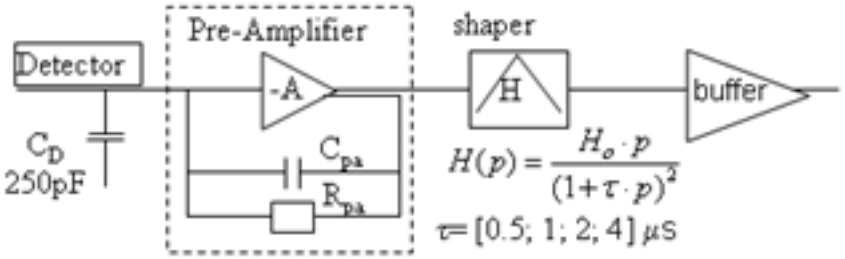


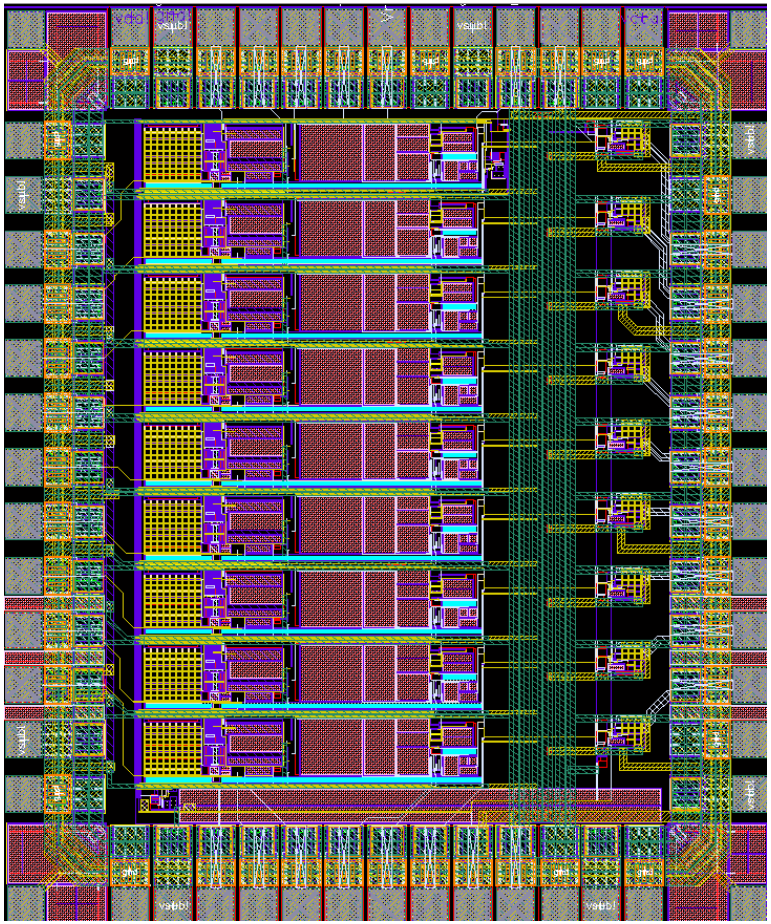
Rpoly2 350Ω ambiant to -196°C



Step 2) (2008) on the basis of the experience acquired during the first phase, new version (TOPEST) integrating also the shaper+buffer, 8 channels + single components for characterization.

Received at the end of July 2008. Tests at IPNL. Typical total gain 7.5 mV/fC, 40 mip dynamic range.





- **selectable:**
  feedback capacitance (500 fF-1 pf)
  feedback resistor (2 – 10 MΩ)
- **selectable shaping times (0.5 – 4 µs range)**
- **power switching on-off**

Step 3) (End 2008), detector tests 64 channels:

study noise vs track reconstruction as a function of angles and shaping times

Status of the cold ASIC R&D

✓Validation of simulations and components characterization as a function of T (results presented at the Wolte-08 conference), behaviour under control in the range [-200 C, -40 C]

✓The preamplifier works following expectations as far performances and reliability are concerned

✓More complete version including shaper + buffer under test, 8 channels, suitable for equipping a small Lar TPC test setup and study the effects on tracks reconstruction

→Finalize in 2009 an optimized version to equip a large number of channels for Lar TPC detectors
ADC integration ?

Digital development for LAr R/O

✓ R&D on the Gigabit Ethernet readout chain + network time distribution system PTP (IEEE1588)

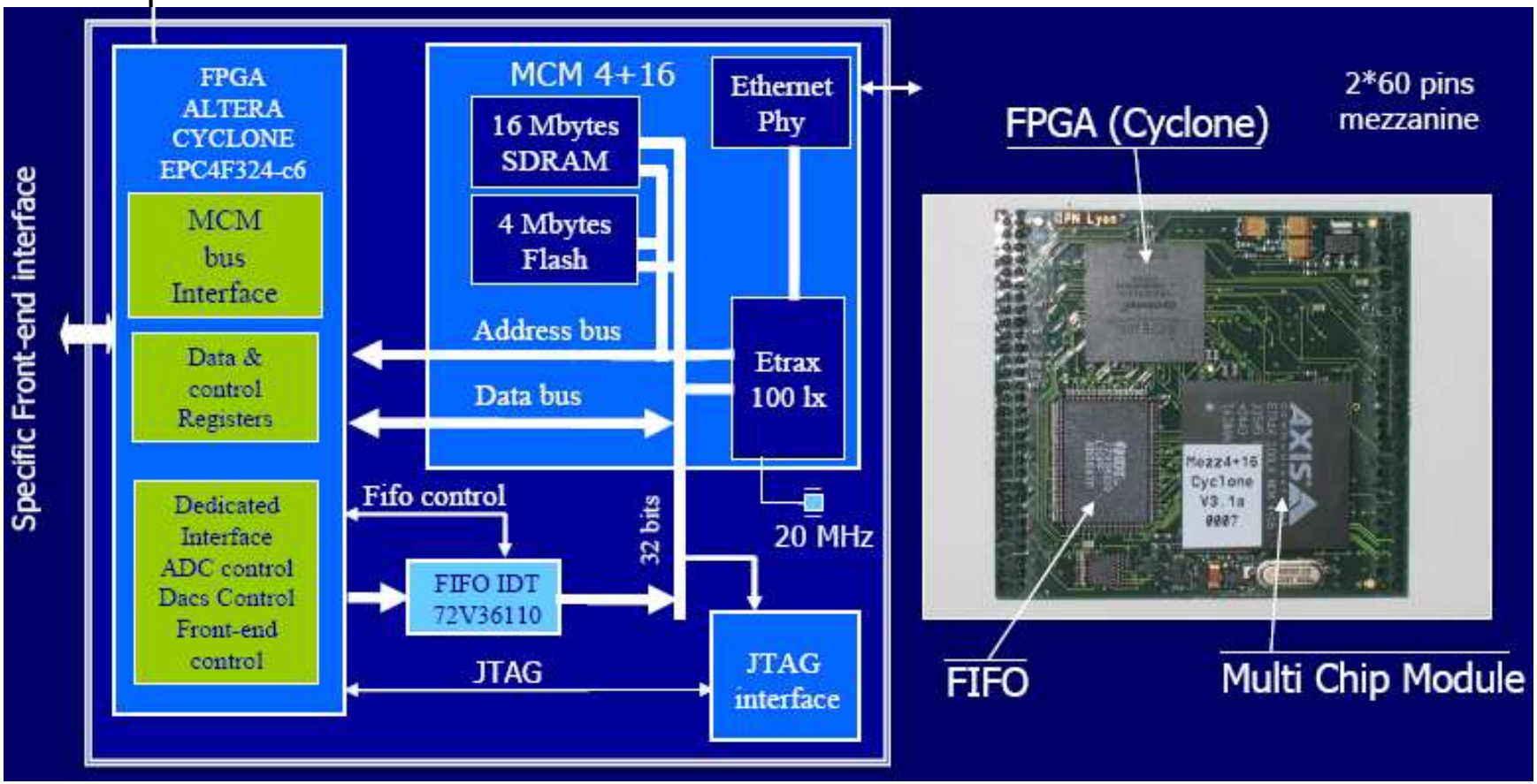
→ evolution and valorization of OPERA experience:

- Reduce Microprocessors market dependence
- Network stack in hardware to free the CPU
- Performance upgrade -> Gigabit Ethernet
- Simplify synchronization of distributed sensors

- Softcore processors (NIOS II)
- Network offload engine
- Gigabit Ethernet
  - form factor following micro-TCA standard form
- IEEE 1588 for synchronization
  - Improved PTP standard (IEEE 1588)

Also of interest for PTP R&D at 1ns level,
PTP collaboration with CERN + others

Embedded processor OPERA mezzanine



- The Etrax 100 lx is a 32 bits RISC microprocessor clocked at 100 MHz
- An embedded linux operating system / Application based on CORBA
- FPGA and FIFO are seen as memory peripherals.
- FPGA includes dedicated front-end interface (readout sequencer(ADC), serial interface (DAC) …)

NIOS II KIT ADC demonstrator 8 channels

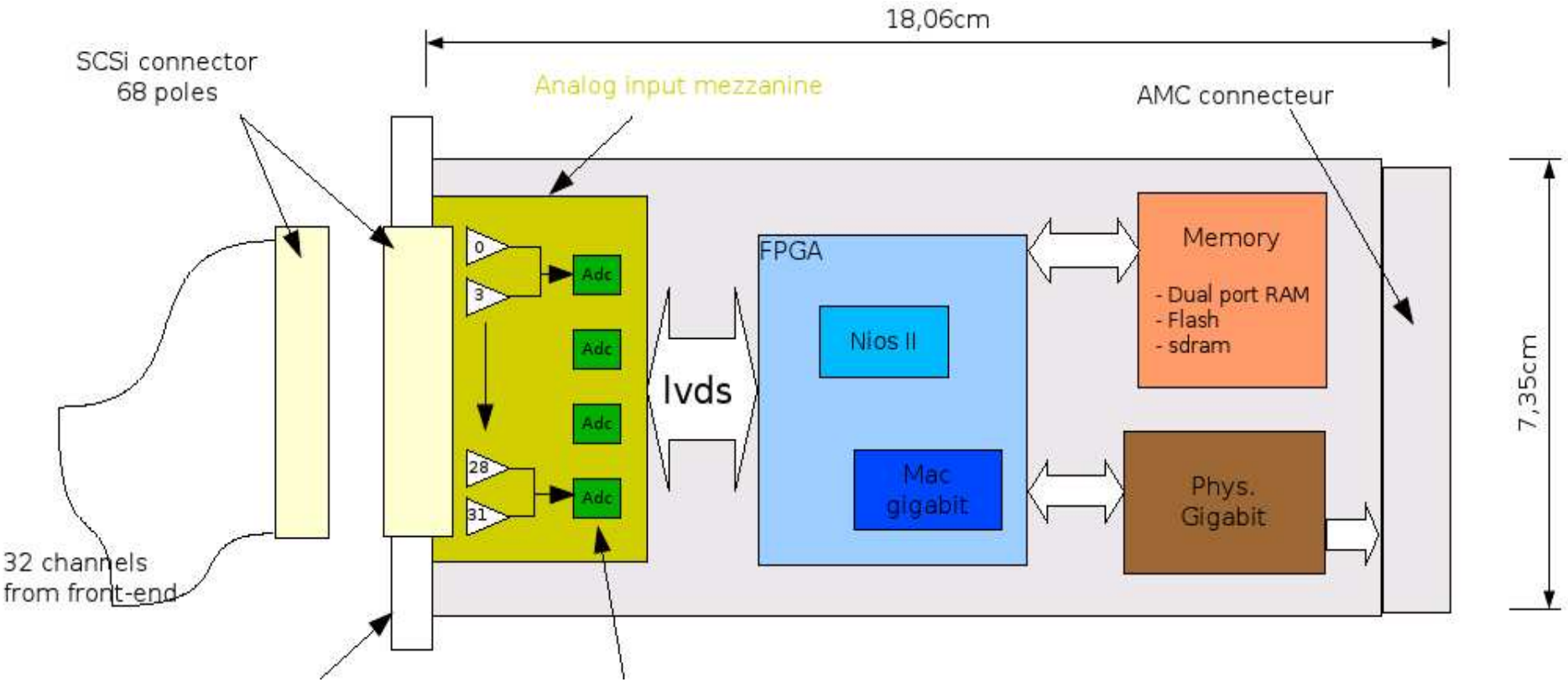
Phy Gigabit Ethernet

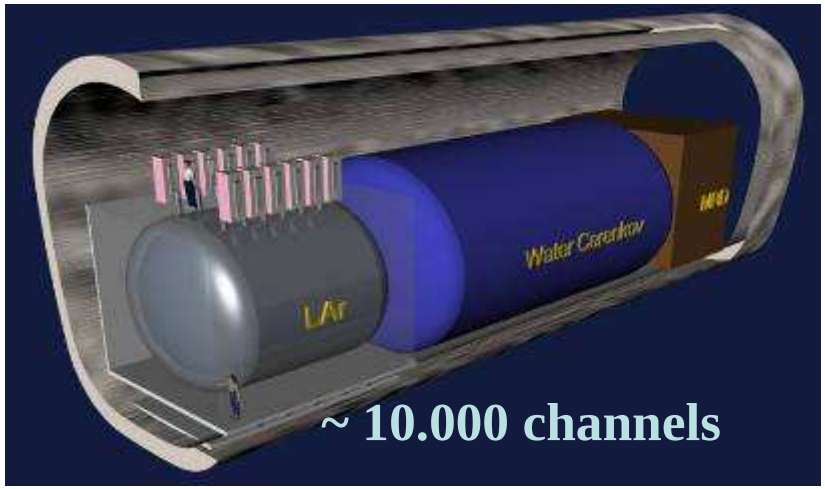
Maximum data UDP transfert =>
114 Mbyte/s (912 Mbit/s) achieved

8 channels ADC board
1.5 MHz / 10 bits

GOAL:

- Developing a TCA board hosting a F/E mezzanine (32 ch)
- 1st version independent from any micro-processor



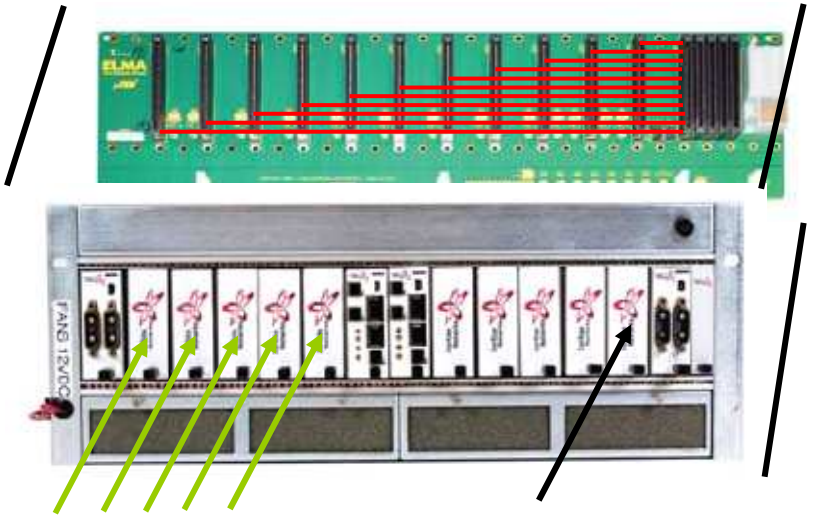


- ADC 10 bits @ 2.5 Msps (continuous sampling)
- 2 buffers / channel (working in Ping-pong mode)
- Buffer depth (6250 samples @ 2.5 ms drift time)
- Each channel is auto-triggerable (1 Hz trigger)

DAQ architecture based on µTCA

- Custom AMC module:
  - 32 ADC channels
  - Gigabit Ethernet output through the backplane

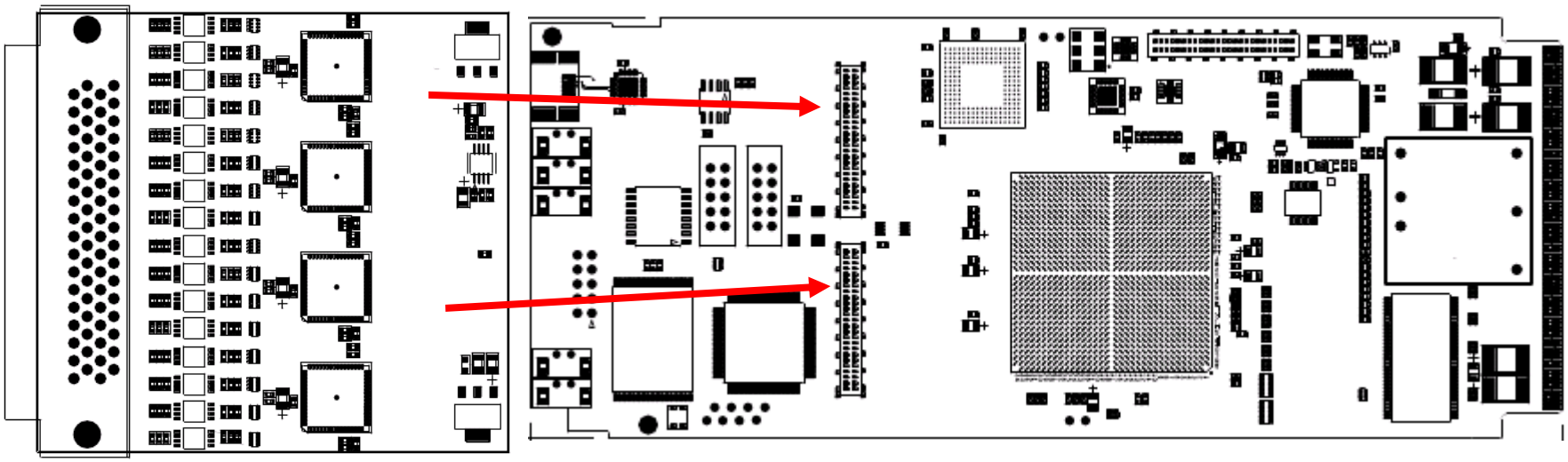
9 slots – dual star
Gigabit Ethernet on backplane



This will result in 34 µTCA racks (9 slots)

Production status of the micro-TCA board

- Design completed
- Full adaptation to ATCA standard
- 1st prototypes being produced to match the ASIC schedule

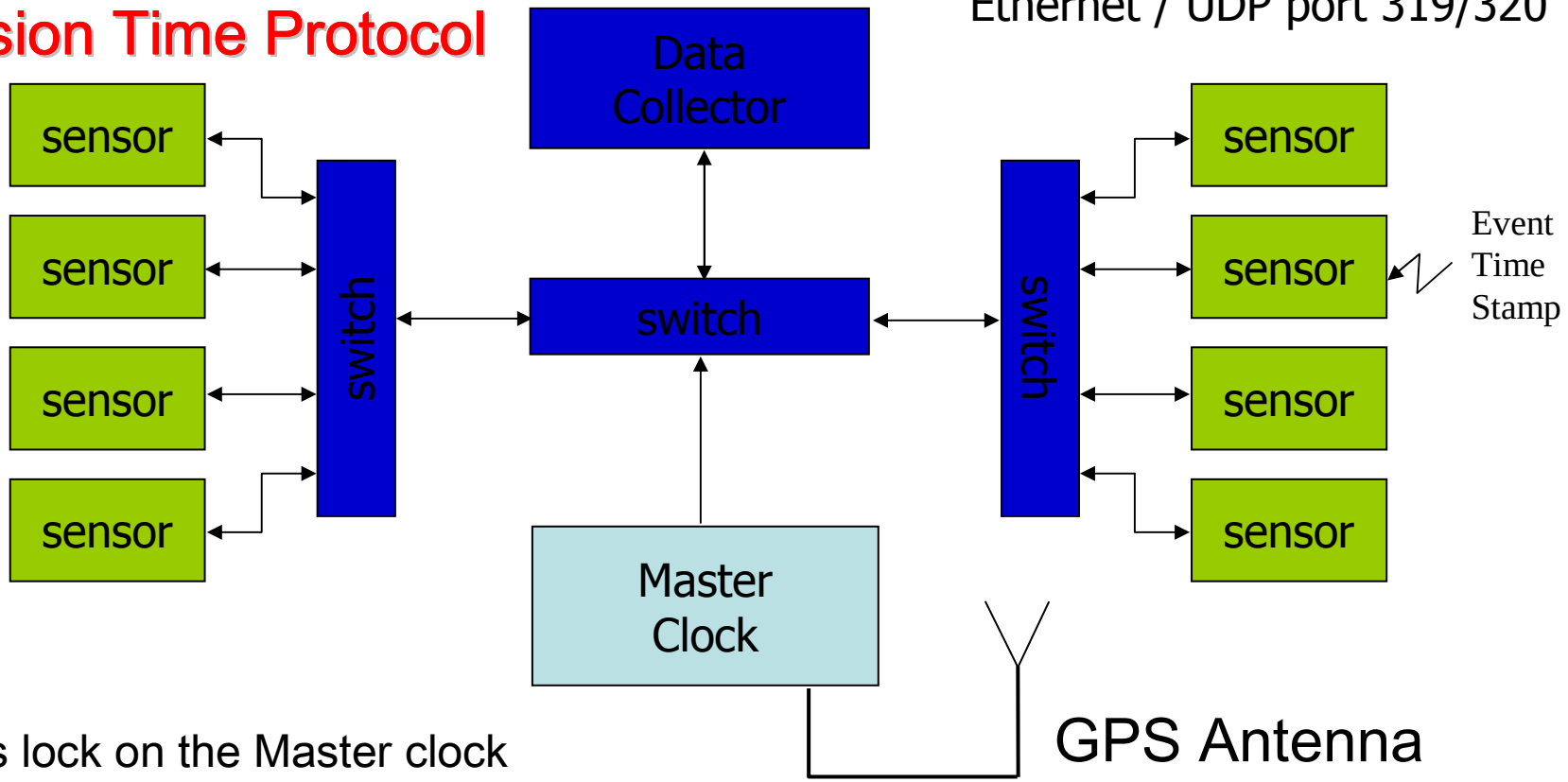


ADC mezzanine

R&D in Network based DAQ systems : Synchronization issues

IEEE 1588 standard
Precision Time Protocol

Ethernet / UDP port 319/320

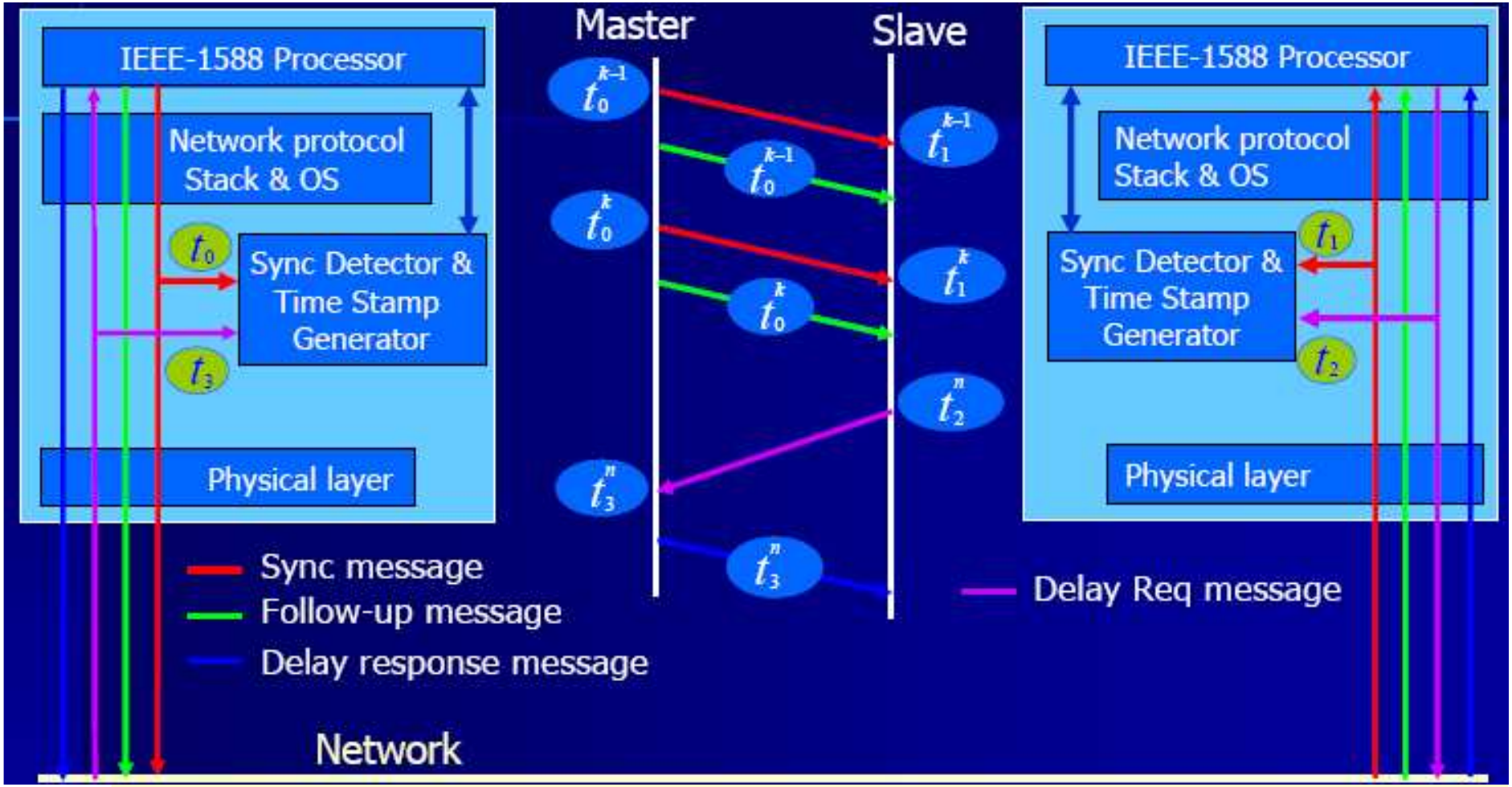


Sensors lock on the Master clock with a few 10 ns accuracy achievable with PTP-optimized switch.

Redundant masters are possible

IEEE 1588 standard
Precision Time Protocol

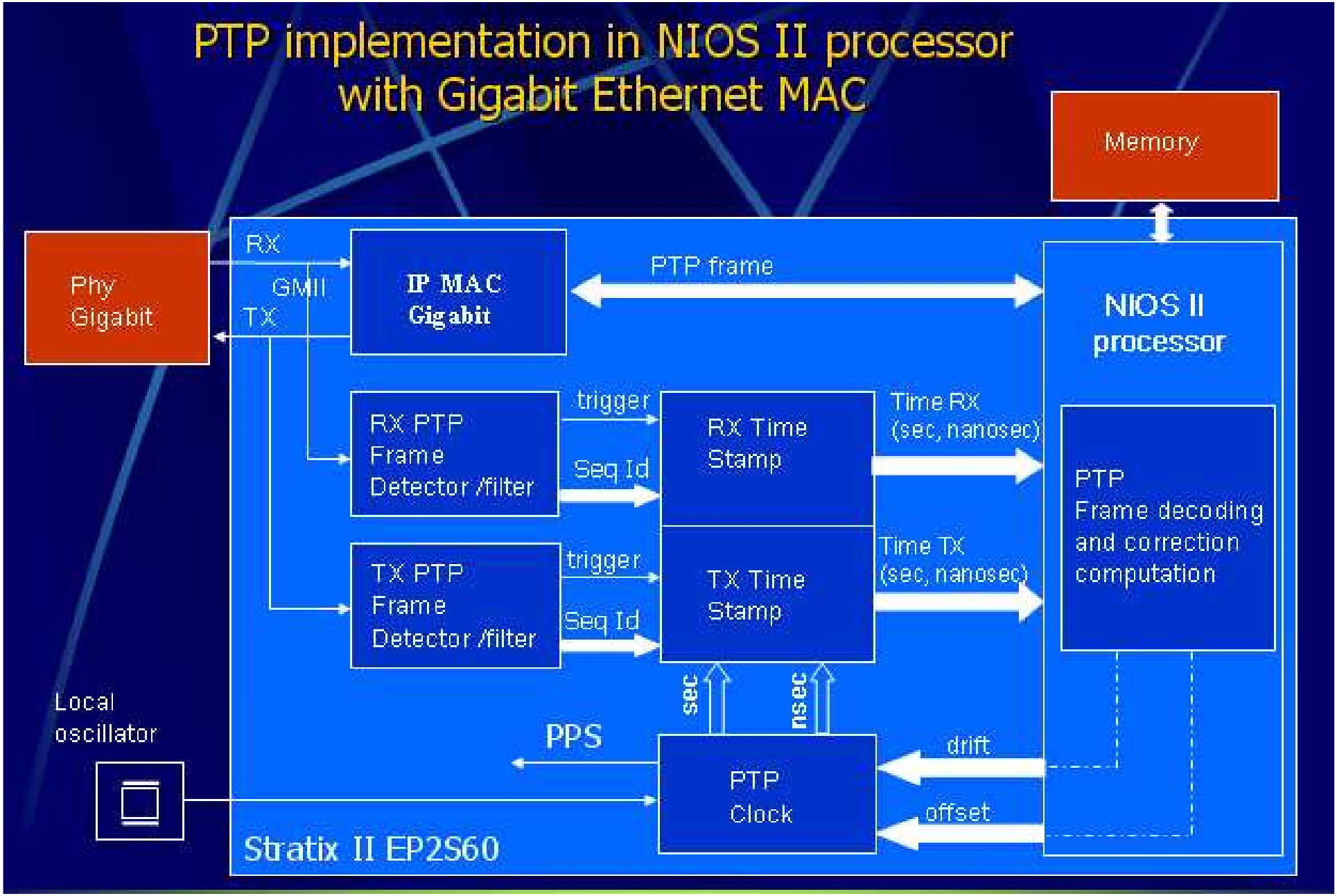
http://ieee1588.nist.gov/

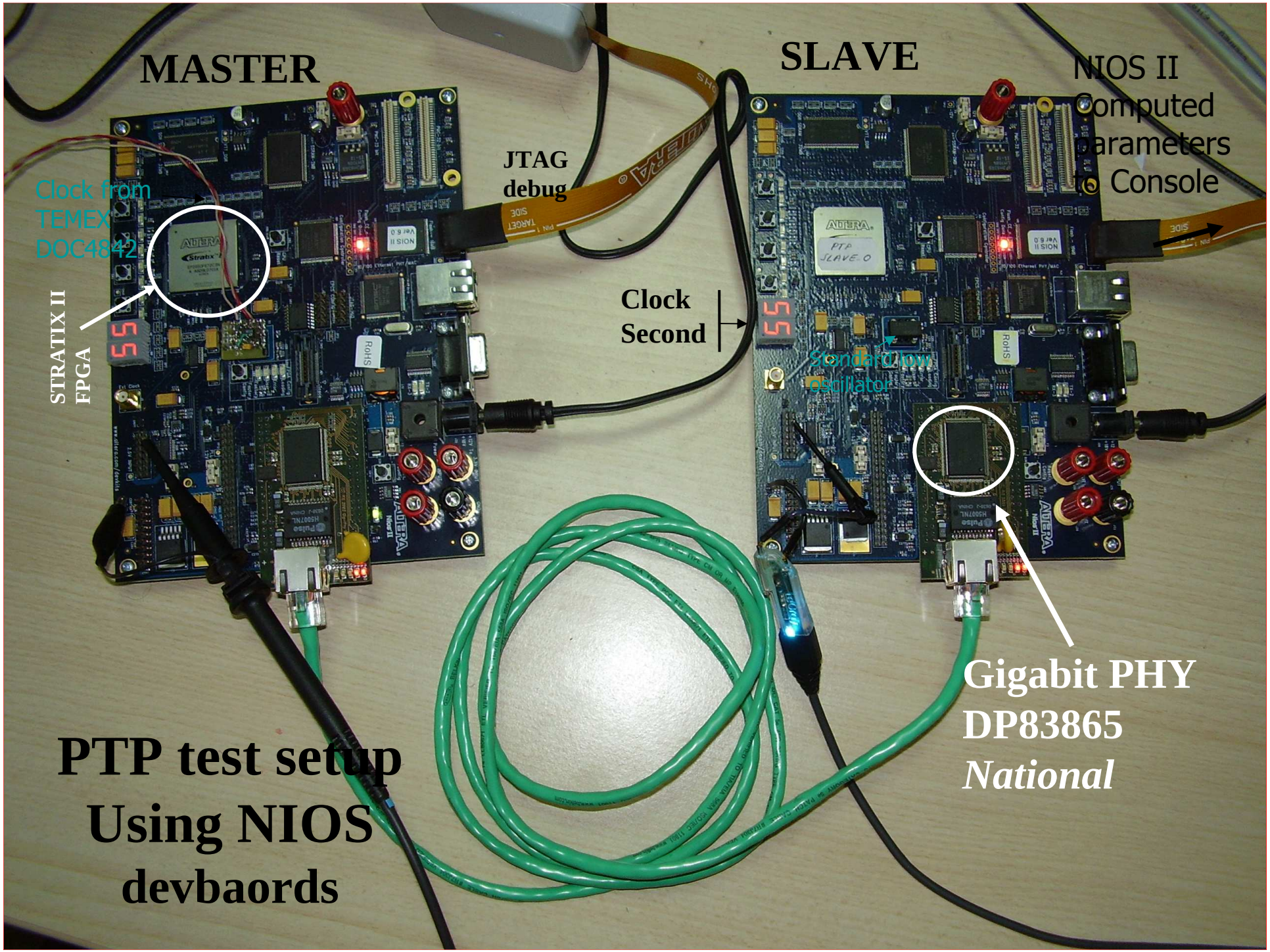


$$drift=\frac{(t_1^k-t_1^{k-1})-(t_0^k-t_0^{k-1})}{t_1^k-t_1^{k-1}}$$

$$delay=\frac{(t_1^k-t_0^k)+(t_3^n-t_2^n)}{2}$$

$$offset=(t_1^k-t_0^k)-delay$$


PTP implementation in NIOS II processor with Gigabit Ethernet MAC
Memory
Phy Gigabit
RX
GMII
TX
IP MAC Gigabit
PTP frame
NIOS II processor
RX PTP Frame Detector /filter
trigger
Seq Id
RX Time Stamp
Time RX (sec, nanosec)
PTP Frame decoding and correction computation
TX PTP Frame Detector /filter
trigger
Seq Id
TX Time Stamp
Time TX (sec, nanosec)
sec
nsec
Local oscillator
PPS
drift
offset
PTP Clock
Stratix II EP2S60

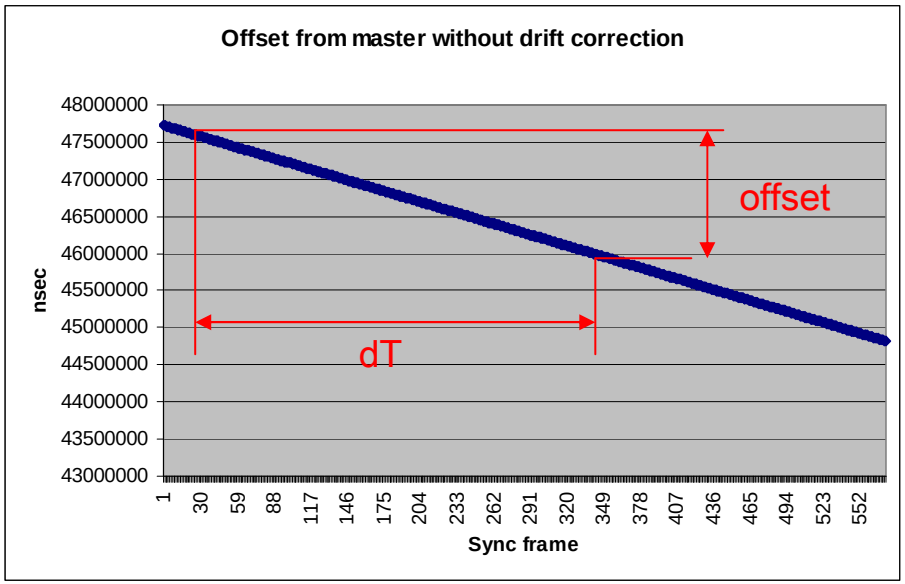

MASTER
SLAVE
NIOS II
Computed
parameters
to Console
JTAG
debug
Clock from
TEMEX
DOC4842
STRATIX II
FPGA
Clock
Second
Standard low
oscillator
Gigabit PHY
DP83865
National
PTP test setup
Using NIOS
devbaords

OFFSET and DRIFT on SLAVE relative to MASTER

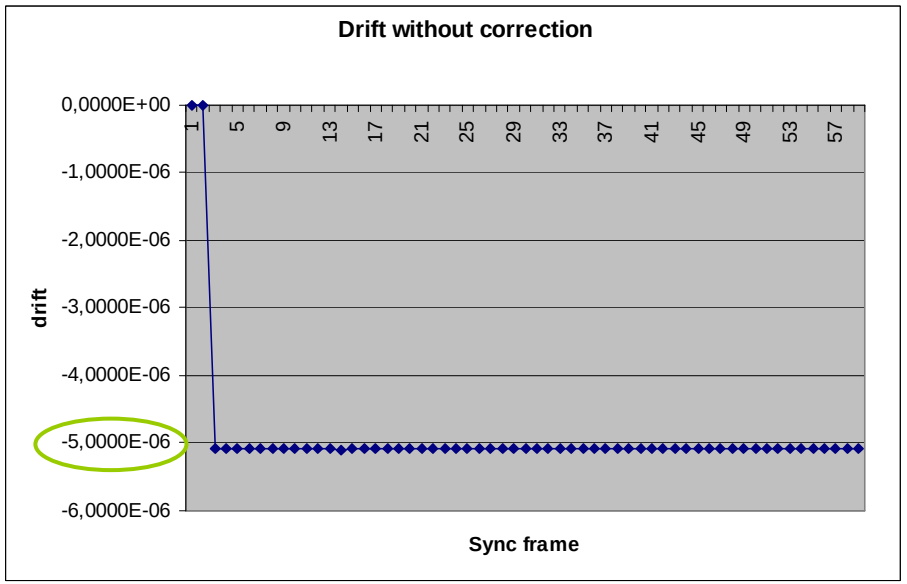
Observed without correction

Computed by NIOS microprocessor from PTP time stamps

OFFSET (clock shift)



DRIFT (clock period difference)

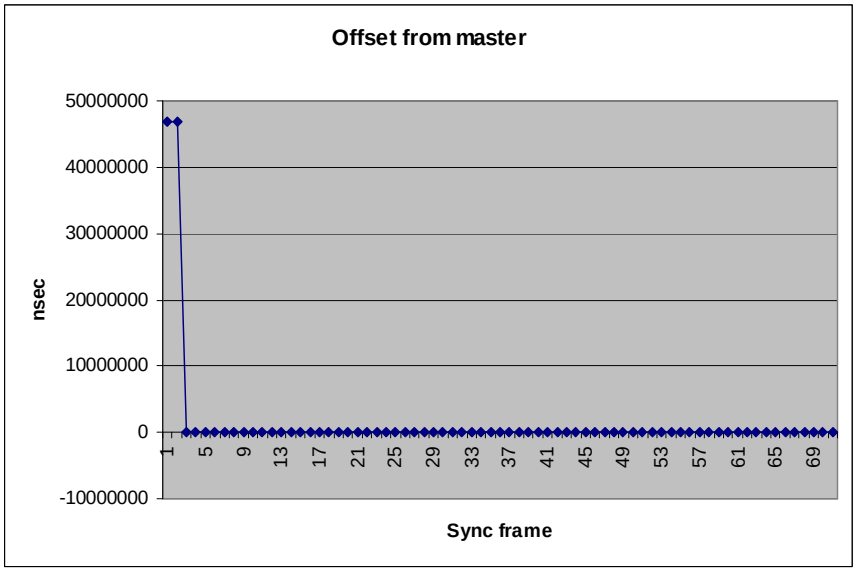


$$drift = \frac{offset}{dT} = -5ppm$$

$$drift = \frac{(t_0^k - t_0^{k-1}) - (t_1^k - t_1^{k-1})}{t_1^k - t_1^{k-1}}$$

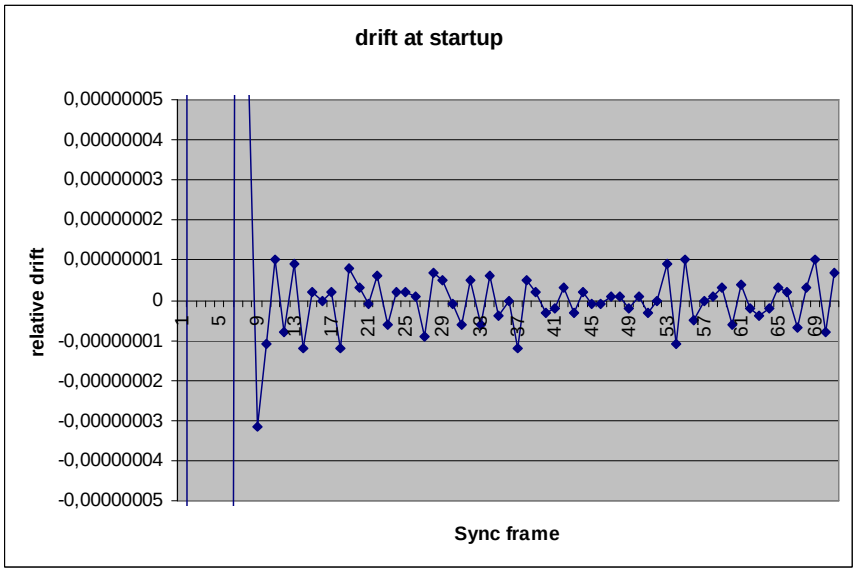
OFFSET and DRIFT with correction

OFFSET (clock shift)



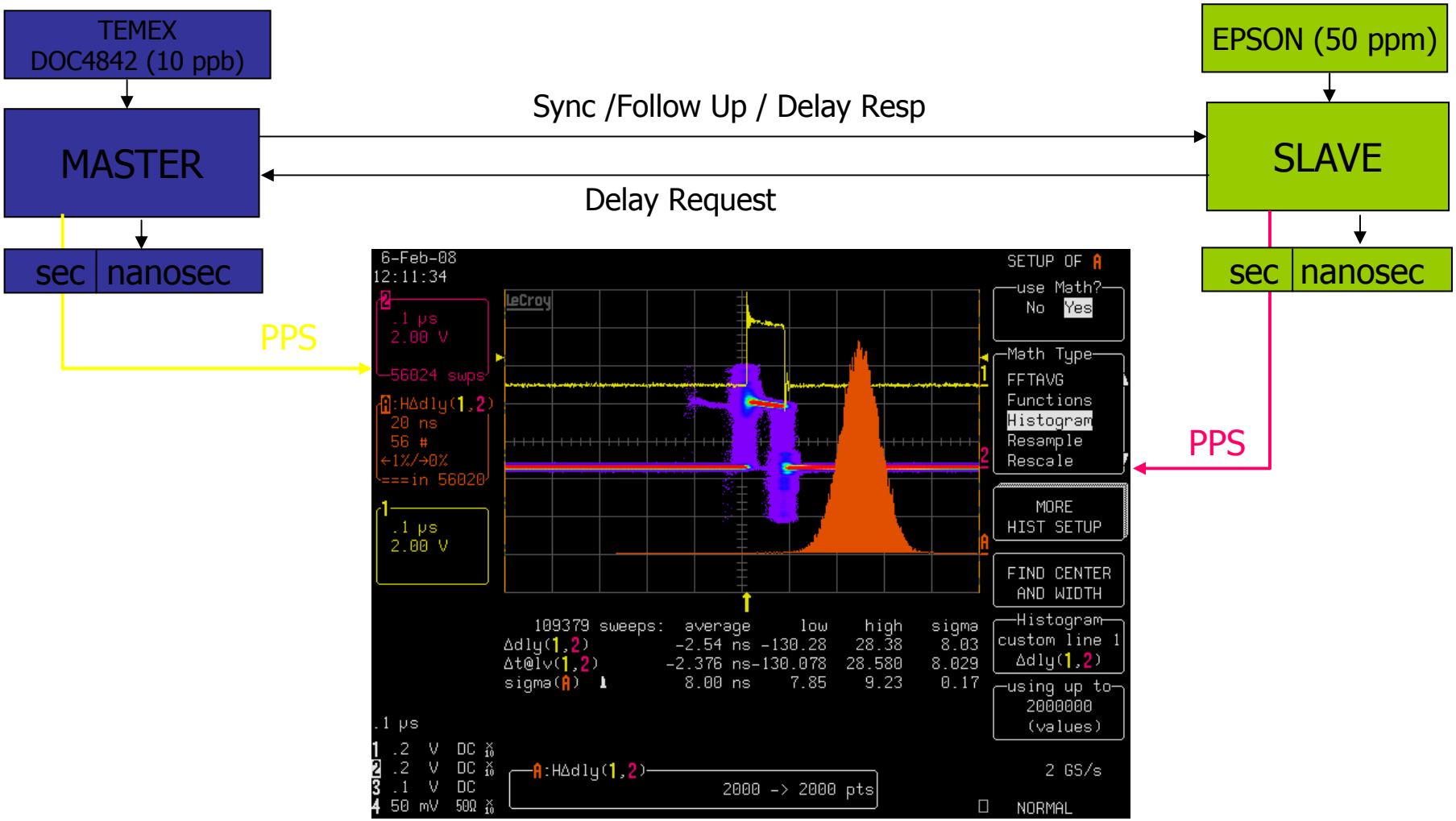
|offset| < 20 ns

DRIFT (clock period difference)



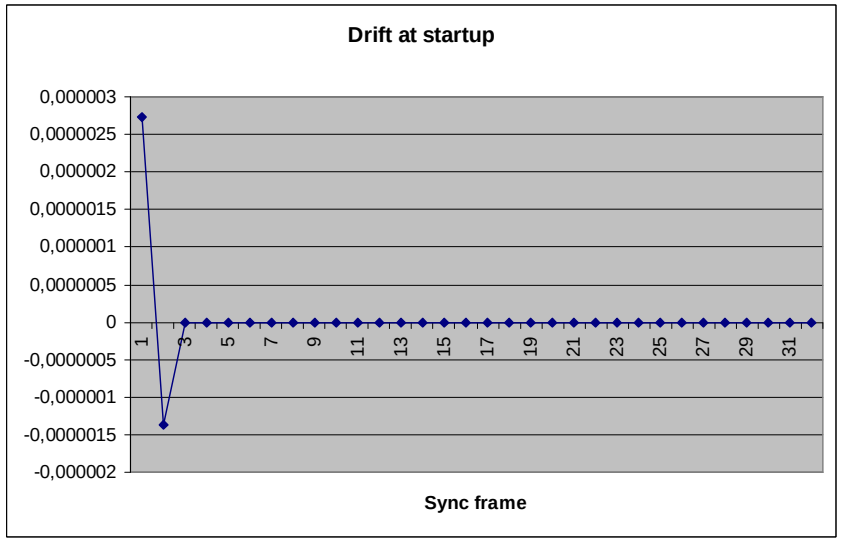
Drift = +/- 10 ppb
(+/-10 ns per 1 sec)

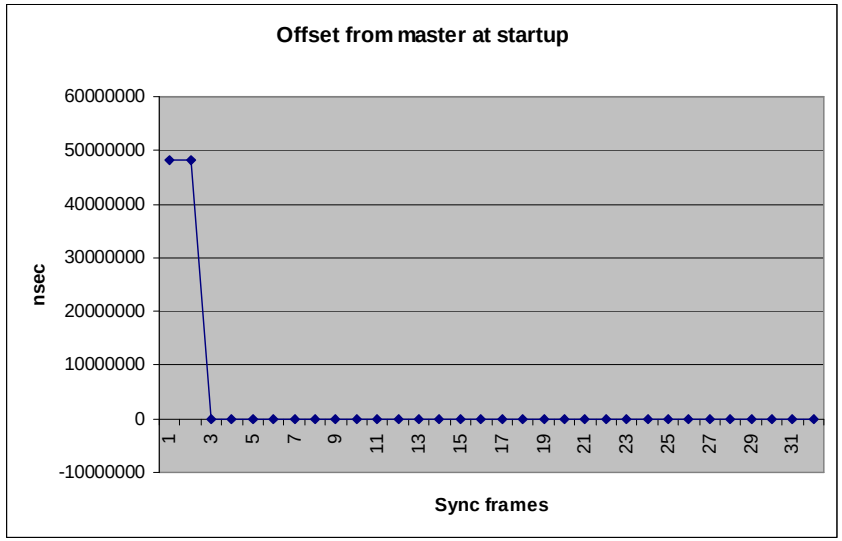
hardware measurement (PPS)

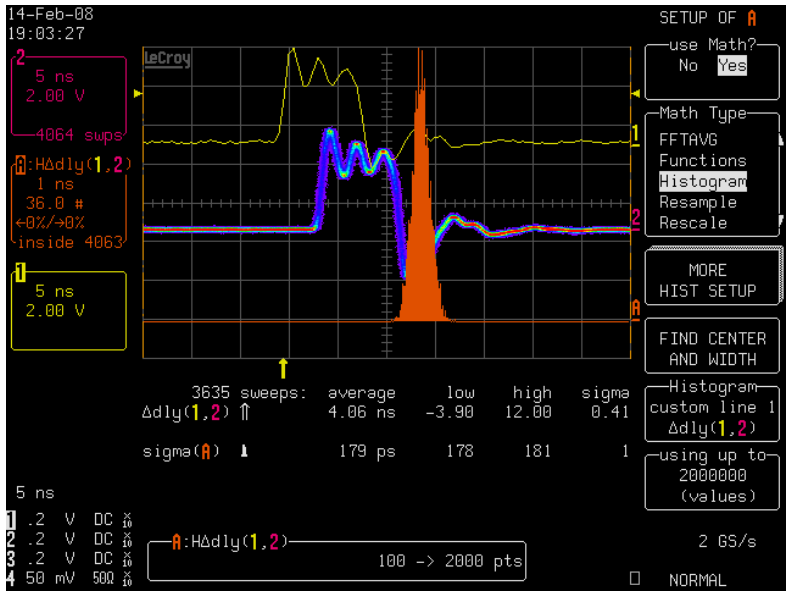


PPS synchronization
8.74 ns rms
(point to point without network trafic)

Optimization specific to gigabit Ethernet







PPS jitter (master vs. slave) ~ 180 ps (point to point without trafic)

The Offset correction is limited by the time stamp resolution. The use of TDC could improve this results.

A collaboration has been started to study a specific switch and to validate this concept in a more complex network topology

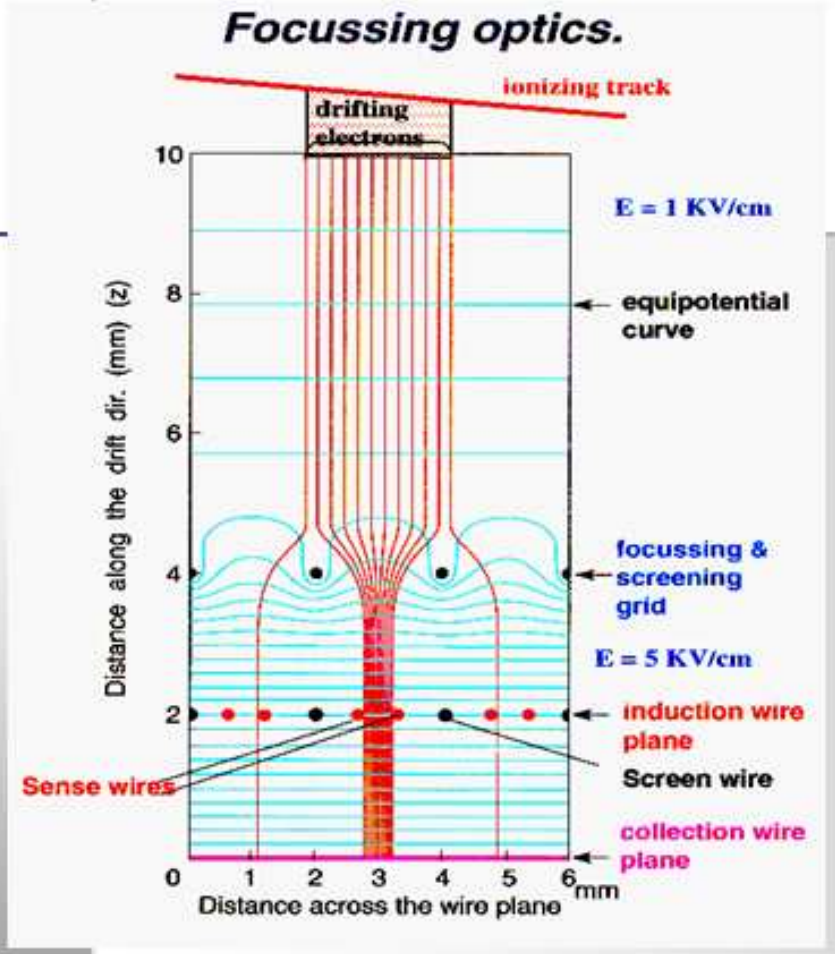
Conclusions:

- ASIC at cryogenic temperature under development (2^{nd} iteration under test).
- Upgrades of the "smart sensors" DAQ system (larger rates, standardized synchronization, better use of CPU) embedded in the digital R/O development.
- Prototype versions under design & test. Ready for tests on LAr TPC soon.

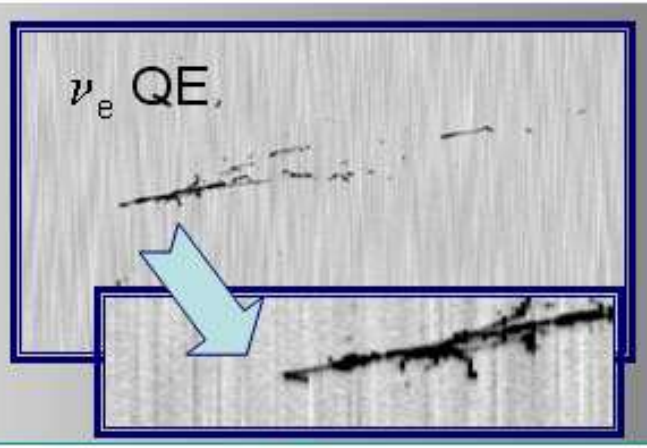
Spares

R&D on the analog FE

Charge collection in LAr



- Detection with a system of wires of primary ionization drifted in ultra-pure LAr by induction or collection, at minimum ~ 18000 electrons per channel
- No charge amplification at the level of the detector → low noise preamp
- 400 ns sampling to reconstruct the drift time and the amount of charge
- 3D image reconstruction with several planes of wires + drift time

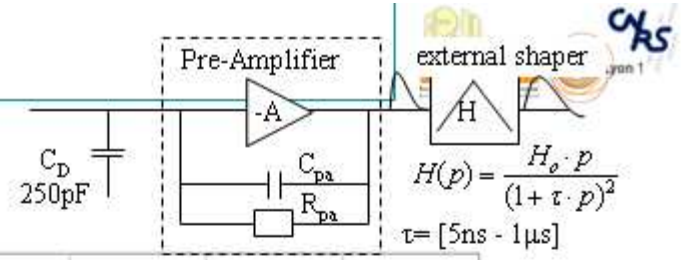


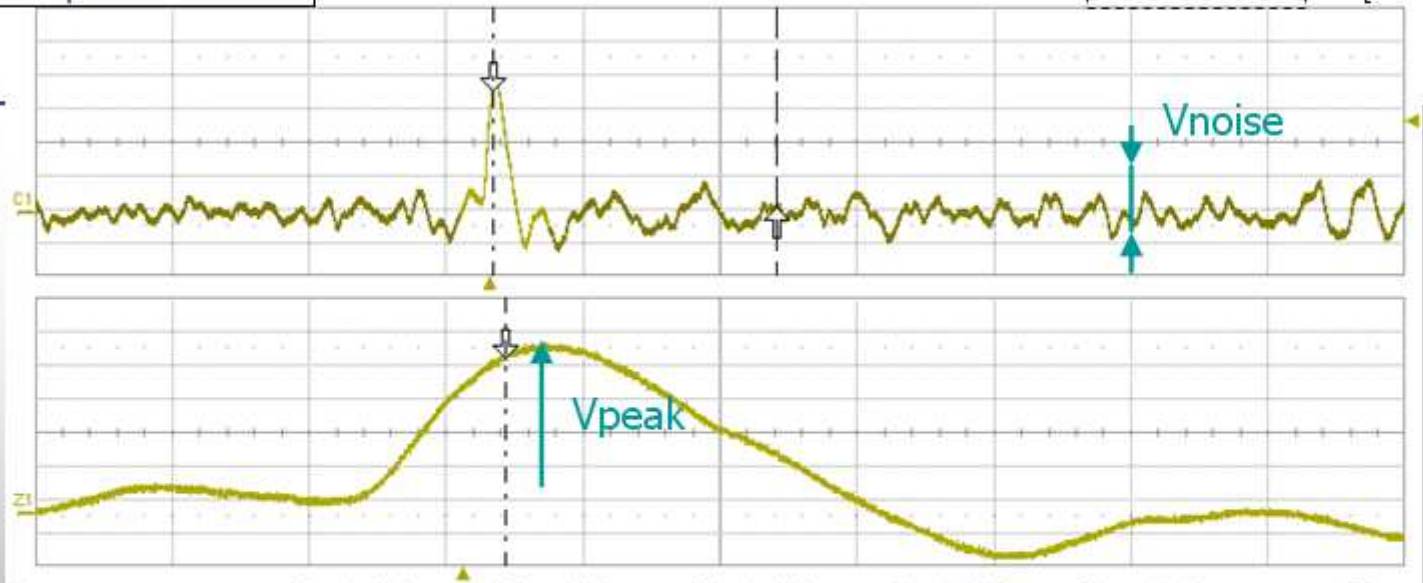
- Multichannel 3fC to 120fC (0.5μs pulse) pre-amplifier
- 1000 e- ENC with **250pF** Detector capacitance

Typical 3fC input charge signal

$$ENC = \frac{Qin * Vnoise}{q * Vpeak}$$

,q=1.6 10^{-19}





Measure	P1:sdev(C1)	P2:max(C1)	P3:sdev(C3)	P4:pkpk(C3)	P5:max(Math)	P6:- - -
value	51.3 mV	400 mV	262 µV	2.6 mV	397.0 mV	
mean	49.528 mV	407.38 mV	257.9 µV	2.394 mV	396.976 mV	
min	43.0 mV	333 mV	245 µV	2.1 mV	397.0 mV	
max	56.0 mV	483 mV	273 µV	2.9 mV	397.0 mV	
sdev	2.518 mV	27.19 mV	5.5 µV	141 µV	---	
num	167	167	207	207	1	
status	✔	✔	✔	✔	✔	

C1 DC50
100 mV/div
-211.0 mV
↓ 379.2 mV
↑ -34.8 mV
Δy -414.0 mV

Z1 zoom(C1)
79 mV/div
650 ns/div
↓ 368.8 mV
↑ ---
Δy ---

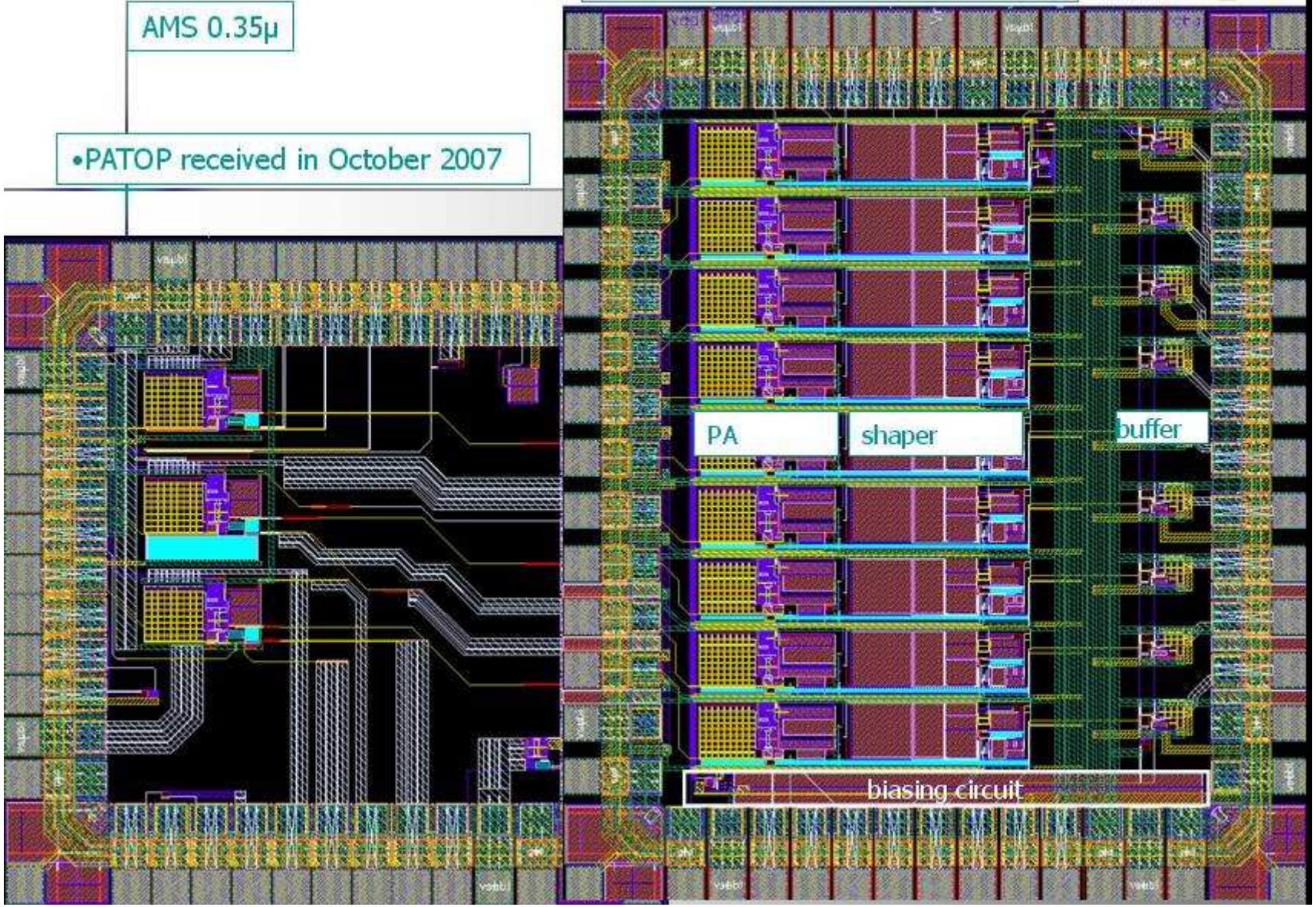
Timebase -16.8 µs
10.0 µs/div
250 kS 2.5 GS/s
X1= 200.0 ns ΔX= 20.6996 µs
X2= 20.8996 µs 1/ΔX= 48.3101 kHz

Trigger C1 DC
Auto 270 mV
Edge Positive

Two Test chip versions

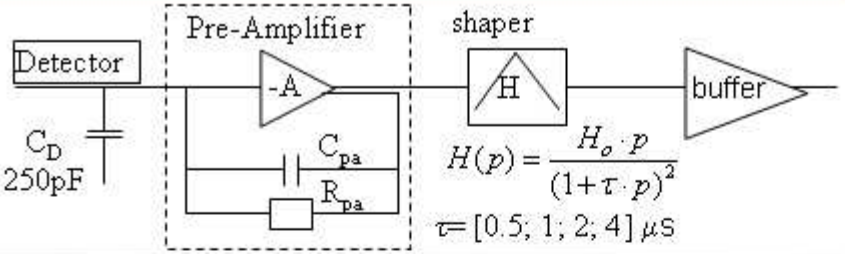
AMS 0.35µ

- PATOP received in October 2007
- TOPEST expected for mid-july 2008

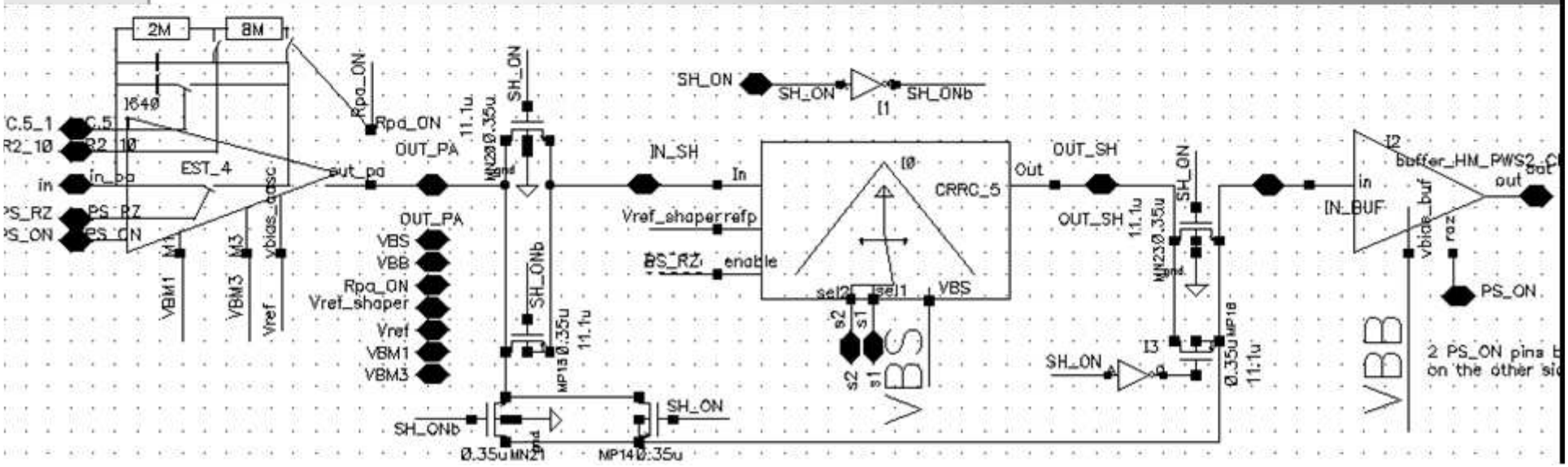


Second version : TOPEST

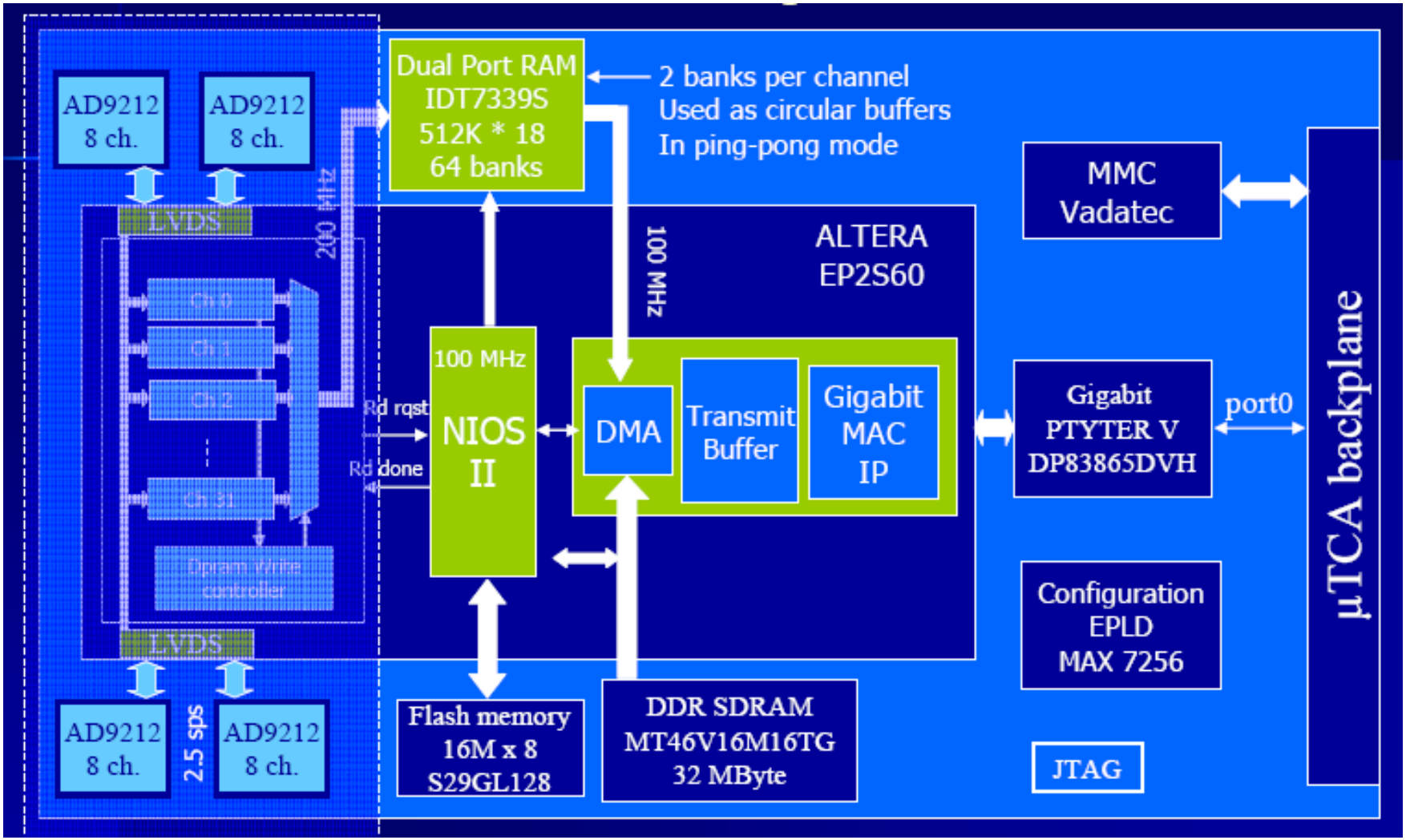
- Semi-configurable circuit:
  - Rpa = [0; 2; 10]MΩ
  - T = [0.5; 1; 2; 4] µs
  - Cpa = 0.5pF or 1pF
  - Power switching mode
    - ON-OFF



Gain : 1/0.5 * 0.85 * 4.4 =>
Gtotal = 7.5mV/fC



32 ADC channels AMC (µTCA) board with NIOS II and Gigabit MAC



(114 Mbytes /sec achieved in UDP)