Rad-hard electronics developments

The GBT-based Expandable Front-End (GEFE)

Manoel Barros Marin (on behalf of the GEFE team)

Beam Instrumentation
Technical Board
(09/09/2015)

BE-BI-QP

Rad-hard electronics developments

The GBT-based Expandable Front-End (GEFE)

Outline:

- Introduction
- The GEFE board
- Application examples
- Status
- Summary & Outlook

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Introduction (1 of 5)

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The GEFE team

- Andrea Boccardi
- Christophe Donat Godichal
- Jose Luis Gonzalez
- Thibaut Lefevre
- Tom Levens
- Balint Szuk
- Manoel Barros Marin

Acknowledgements

- Pedro Leitao & other colleagues from my old group PH-ESE
- Juan Boix Gargallo, Thierry Bogey and the rest of my section (BE-BI-QP)
- Tullio Grassi (PH-UCM)
- Slawosz Uznanski, Andrea Vilar Villanueva & other colleagues from TE-EPC
- Felix Andreas Arnold, Stephane Burger & other colleagues from BE-BI-PM
- Frank Locci, Stefano Magnoni, Erik Van Der Bij & other colleagues from BE-CO
- Bartosz Przemyslaw Bielawski & other colleagues from BE-RF
- Markus Brugger, Salvatore Danzeca & other colleagues from EN-STI and RadWG
- Special thanks to Fernando Carrio Argos (PH-UAT) for his simulations of GEFE's Power Distribution Network

Introduction (2 of 5)

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What is the GBT-based Expandable Front-End (GEFE)

Introduction (2 of 5)

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What is the GBT-based Expandable Front-End (GEFE)

- **General purpose** FPGA-based radiation tolerant board

Target Total Ionizing Dose (TID): up to 75 krad

- Rad-Hard **FPGA ProAsic3** (ACLA3PE3000-FGG896) from Microsemi
- Features different components of the **GBT-Versatile Link** ecosystem from **CERN PH-ESE**
- **Optical** & **Electrical** interfaces
- **Upgradable**:
  - FPGA Mezzanine Card (**FMC**) High-Pin Count (**HPC**) connector
  - 2x **GPIO connectors** (24 & 13 user I/Os respectively)
- **Flexible schemes for:**
  - Clocks
  - Resets
  - FPGA programming
  - Slow Control (SC) E-link
  - Power

Introduction (3 of 5)

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Our motivation

Introduction (3 of 5)

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Our motivation

Common
Digital Front-End
for
Beam Instrumentation

Introduction [3 of 5)

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Our motivation

Common
Digital Front-End
for
Beam Instrumentation

This is a big CHALLENGE

Introduction (4 of 5)

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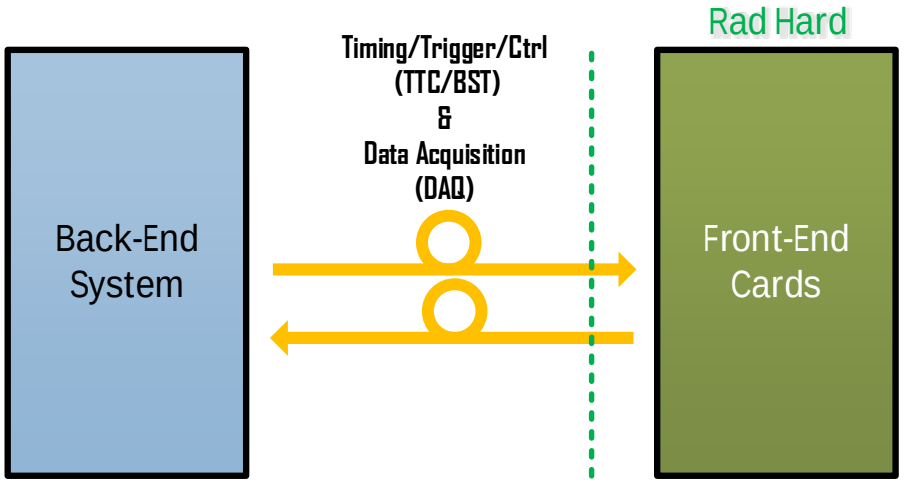
Why a common Digital Front-End?

Why a common Digital Front-End?

- Similar architecture in different beam instrumentation projects



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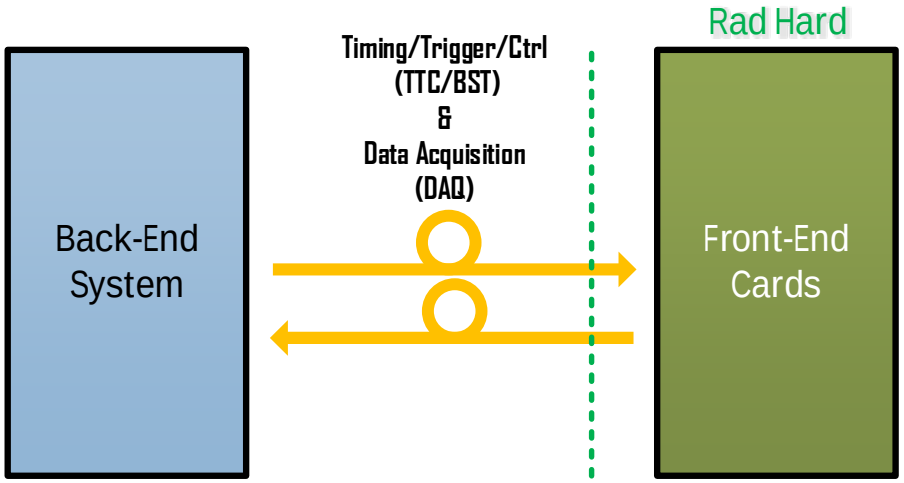
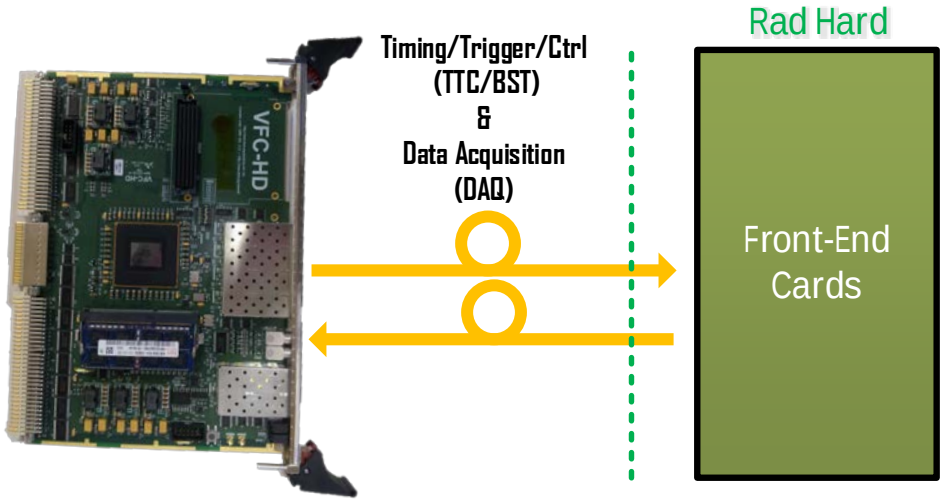


- New Back-End systems in beam instrumentation already unified

VFC-HD



Introduction (4 of 5)

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Why a common Digital Front-End?

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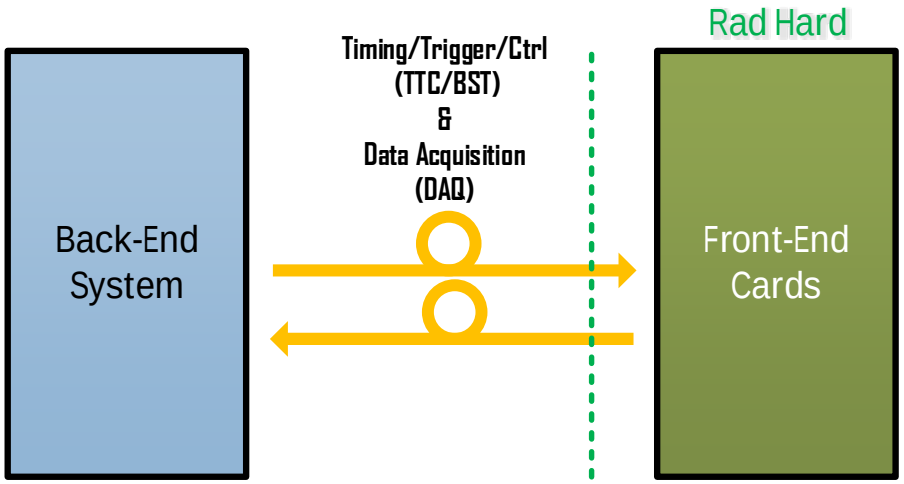

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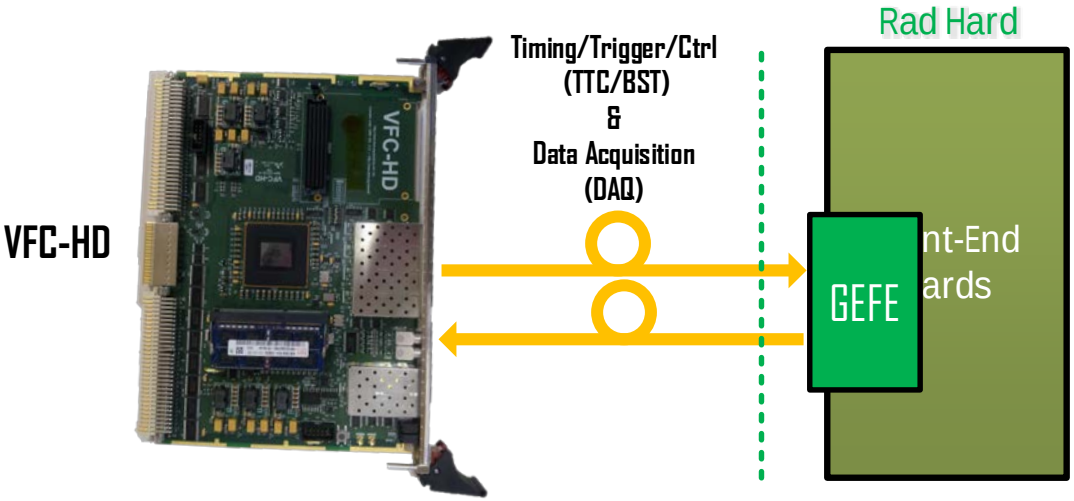

Introduction (4 of 5)

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Why a common Digital Front-End?

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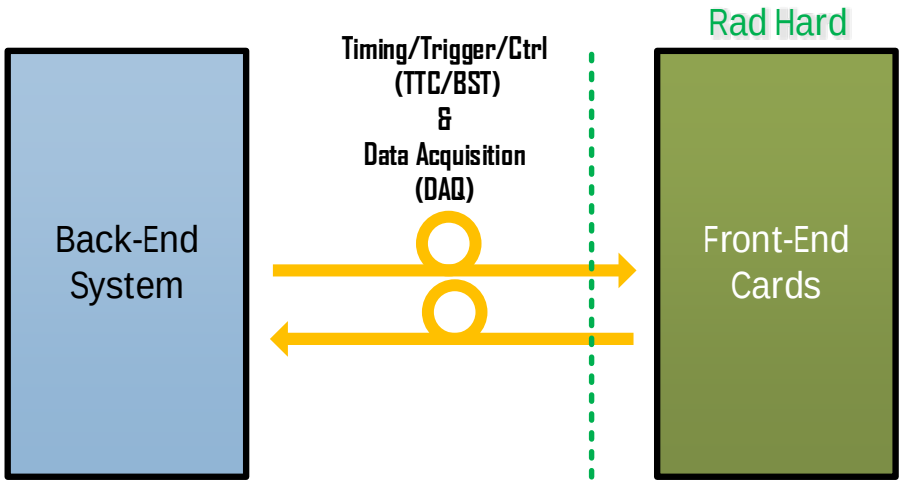

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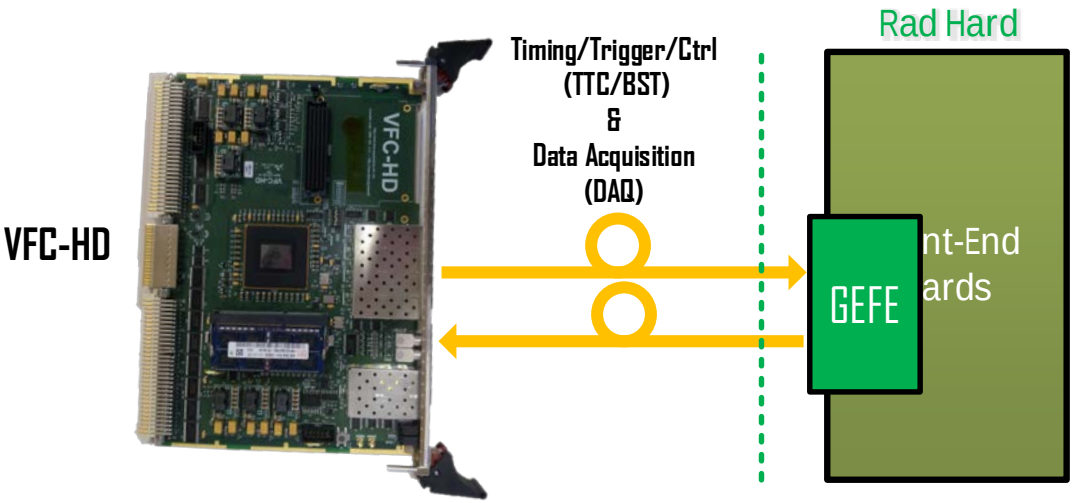

Facilitates:
- Design & Implementation
- Maintenance
- etc.

Introduction (5 of 5)

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Our approach

Introduction (5 of 5)

Our approach

After evaluating the different options…

Introduction (5 of 5)

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Our approach

- **The GEFE board**
  - Follow typical procedures for rad-hard electronic devices (e.g. simple design, rad-hard components)
  - Use advise about radiation hardness from other groups (e.g. TE-EPC, BE-CO, RadWG, etc.)
  - Use of active components already qualified in terms of radiation hardness:
    - GBT-Versatile Link ecosystem (VTRx, GBTx, etc.)
    - Microsemi ProAsic3 FPGA
    - Other active components (BJT, Schmitt-Trigger, etc.)

Reports from:
- PH-ESE (CERN)
- TE-EPC (CERN)
- RadWG (CERN)
- ESA
- REDW (IEEE)
- etc.

Introduction (5 of 5)

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Our approach

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Reports from:
- PH-ESE (CERN)
- TE-EPC (CERN)
- RadWG (CERN)
- ESA
- REDW (IEEE)
- etc.

- **The GEFE community**
  - Regular meetings with the different teams
  - Specifications (User Guide)
  - Open HardWare Repository (OHWR) Wiki
  - Updates through email lists:
    - Email list for all GEFE community: gefe@ohwr.org
    - Email list for GEFE community from CERN only: gefe-community@cern.ch

Rad-hard electronics developments

The GBT-based Expandable Front-End (GEFE)

Outline:

- Introduction
- **The GEFE board**
- Application examples
- Status
- Summary & Outlook

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GEFE board (1 of 9)

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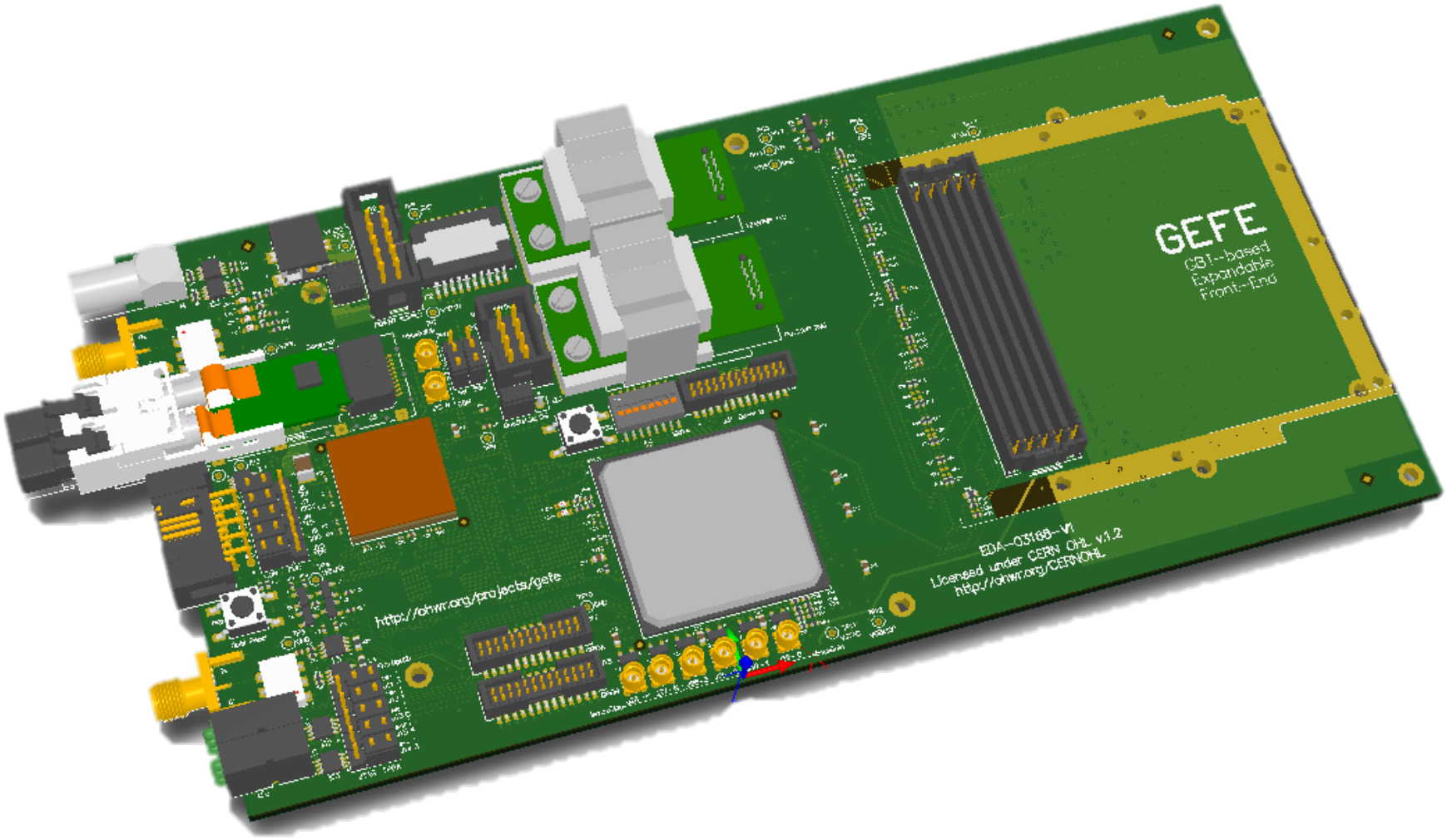
The GEFE at a glance



GEFE board (2 of 9)

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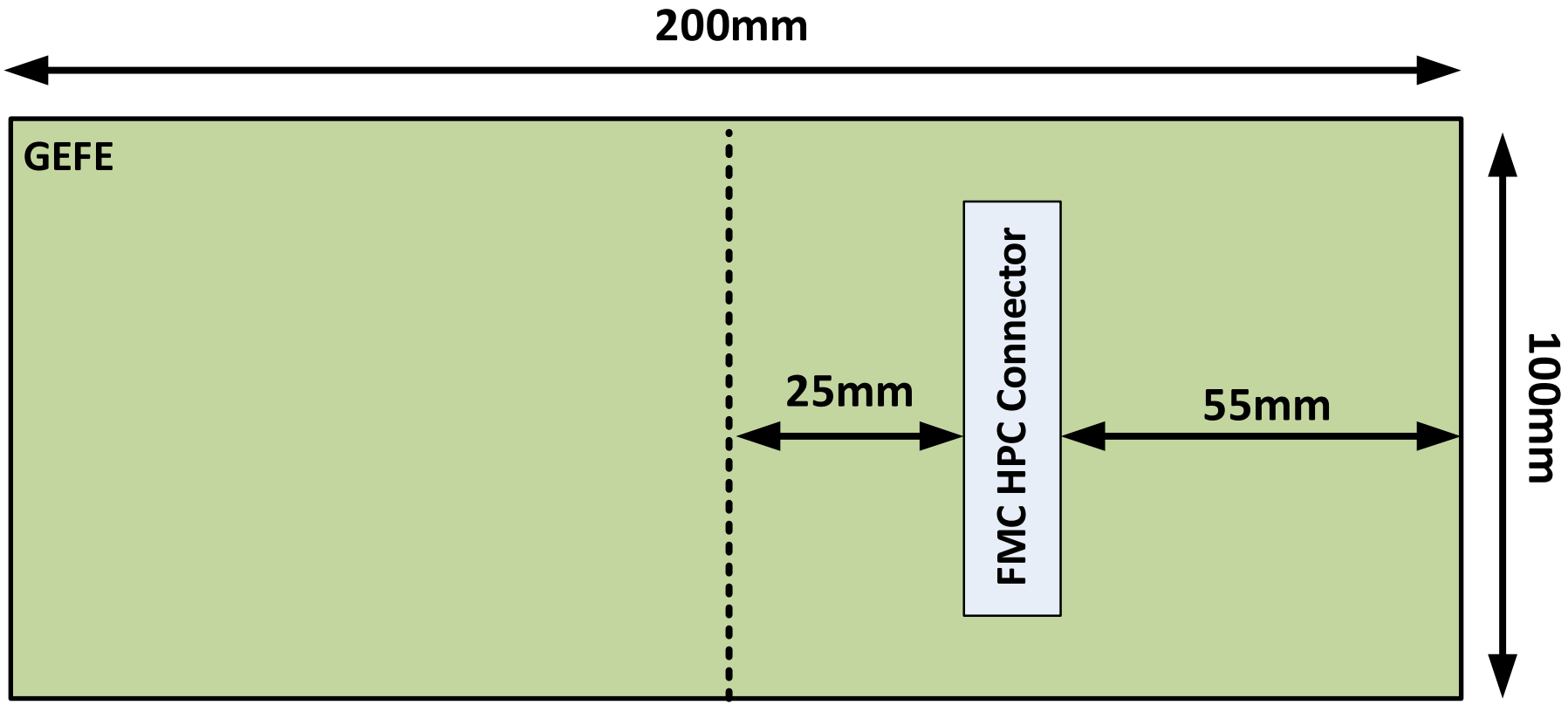
The GEFE at a glance



GEFE board (3 of 9)

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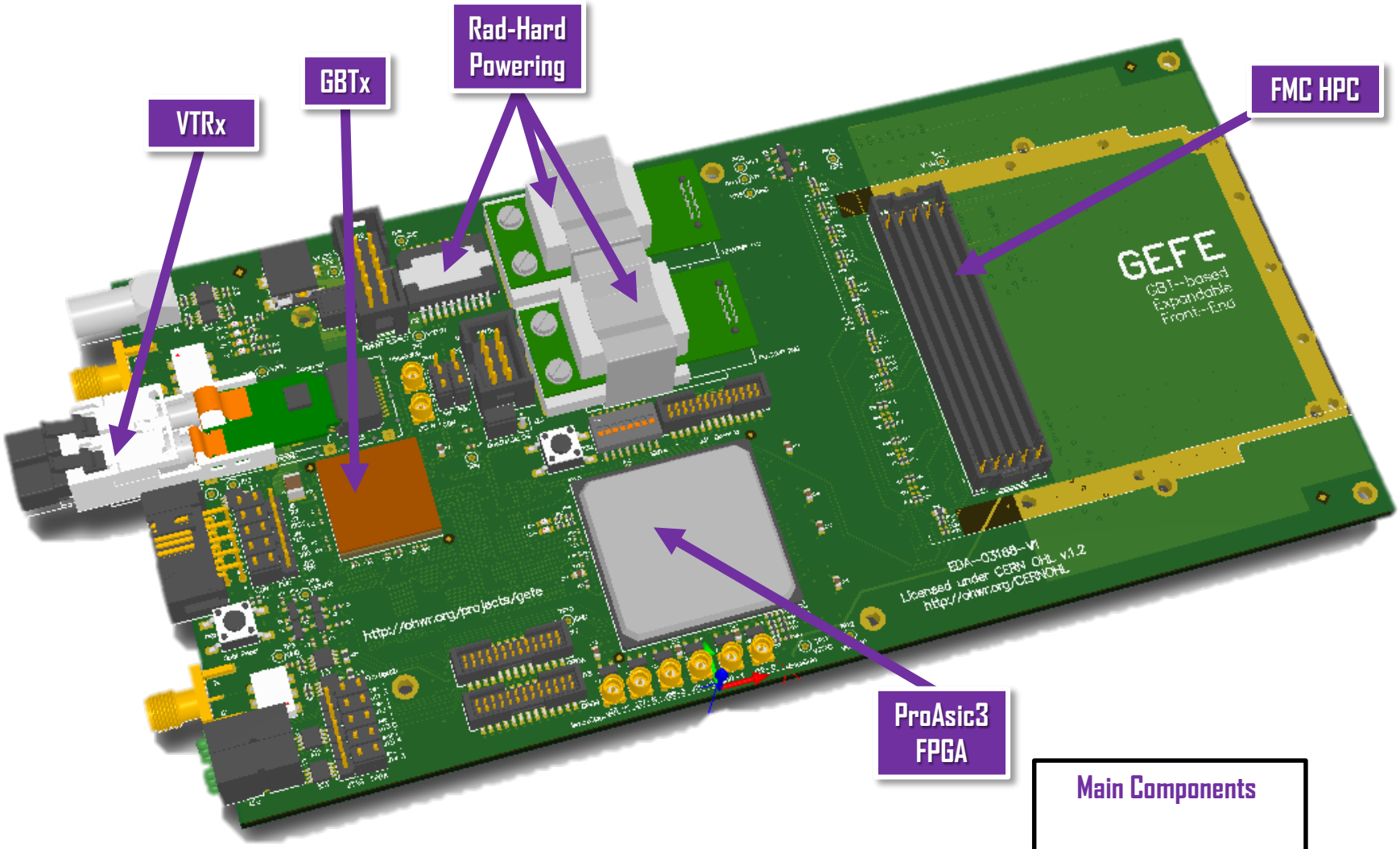
The GEFE at a glance



Main Components

GEFE board (4 of 9)

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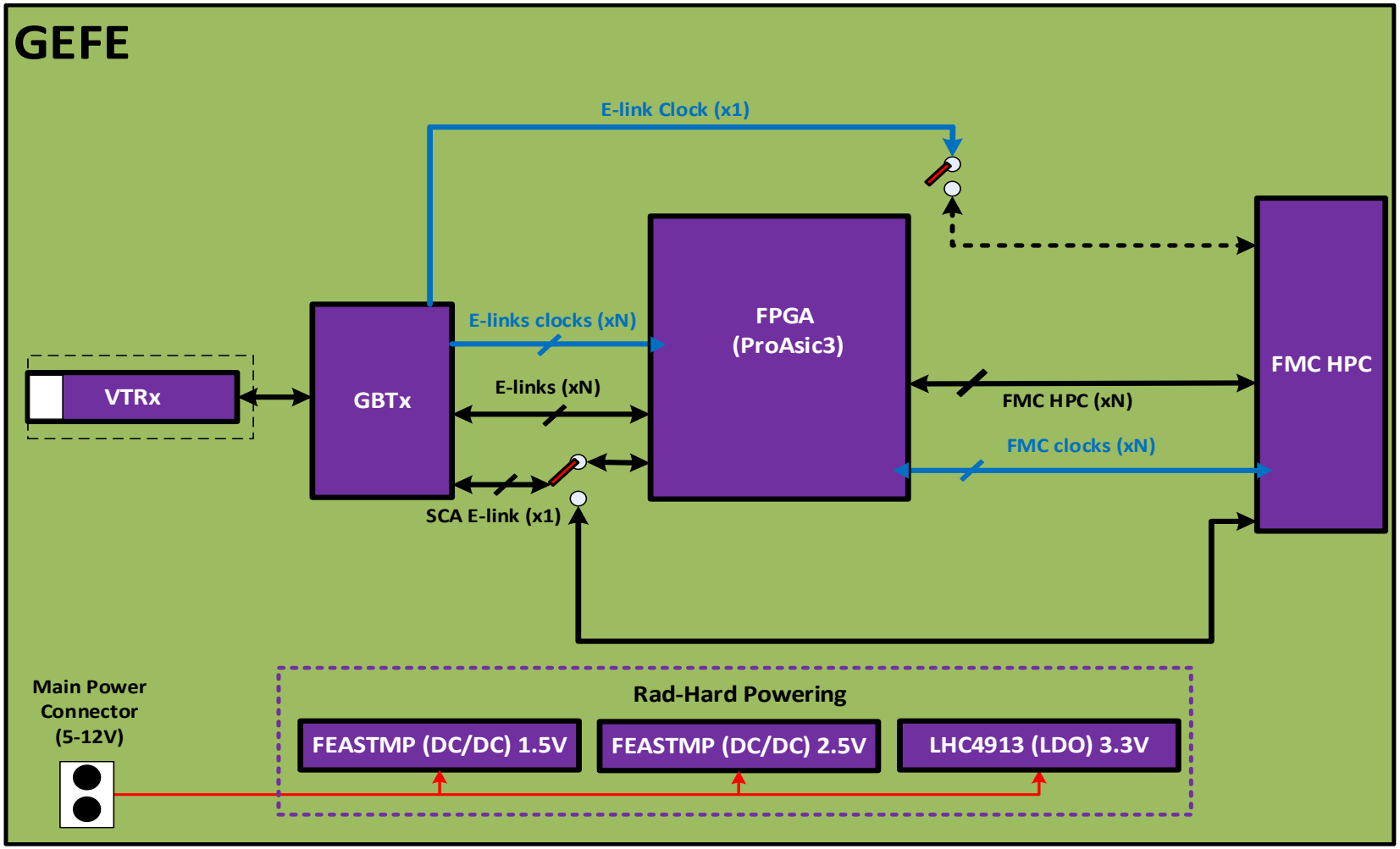
The GEFE at a glance



Main Components

GEFE board (5 of 9)

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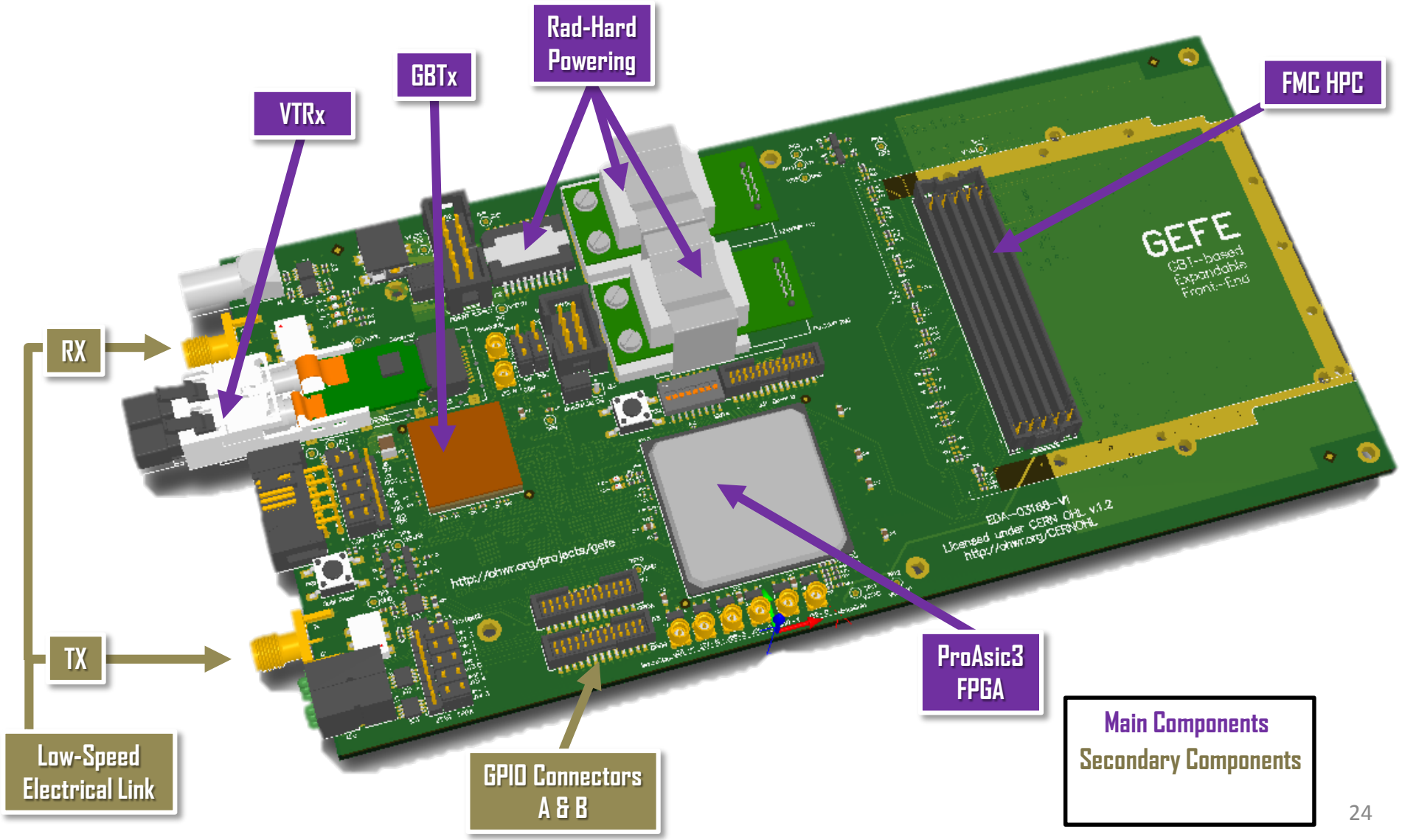
The GEFE at a glance



GEFE board (6 of 9)

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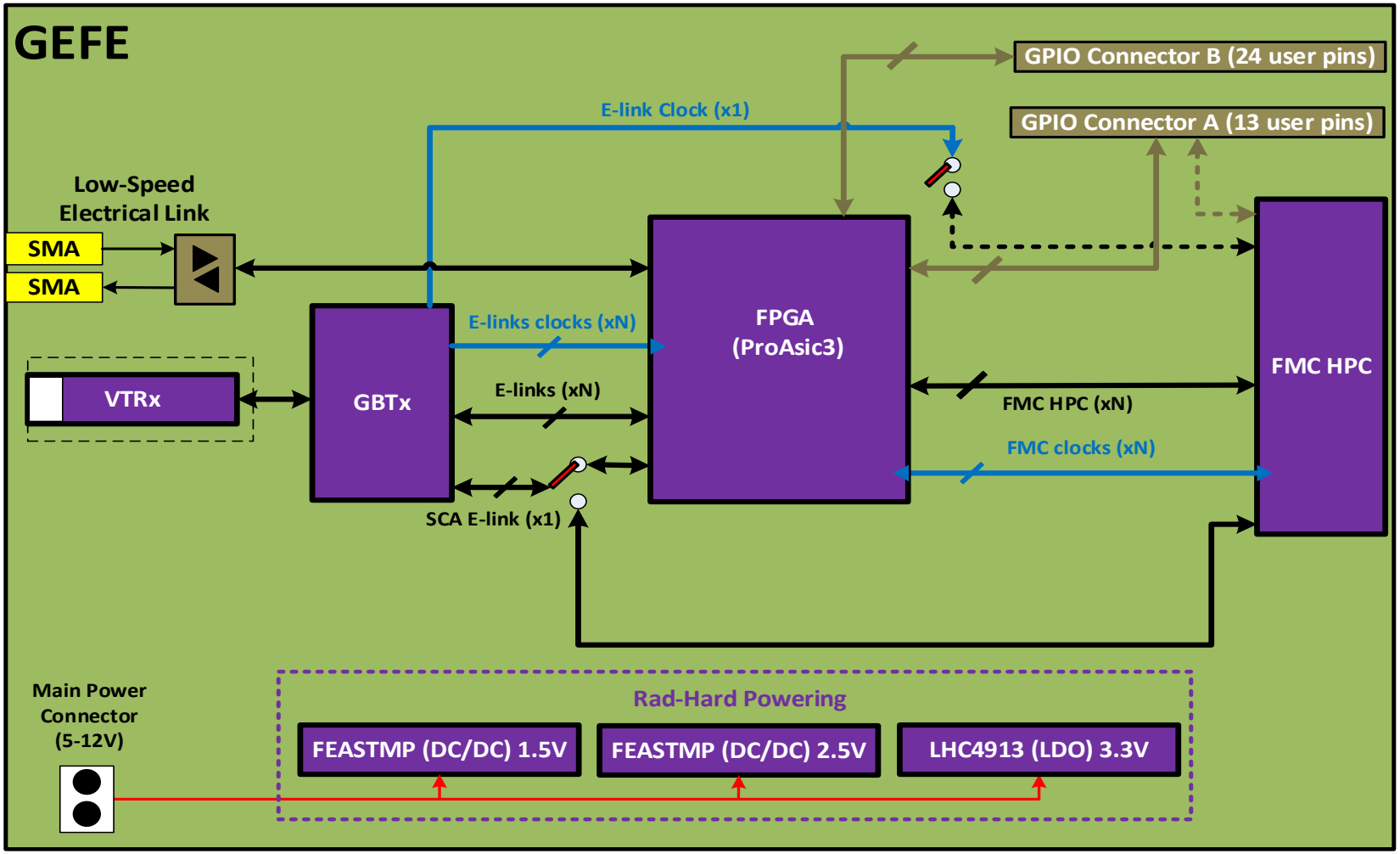
The GEFE at a glance



GEFE board (7 of 9)

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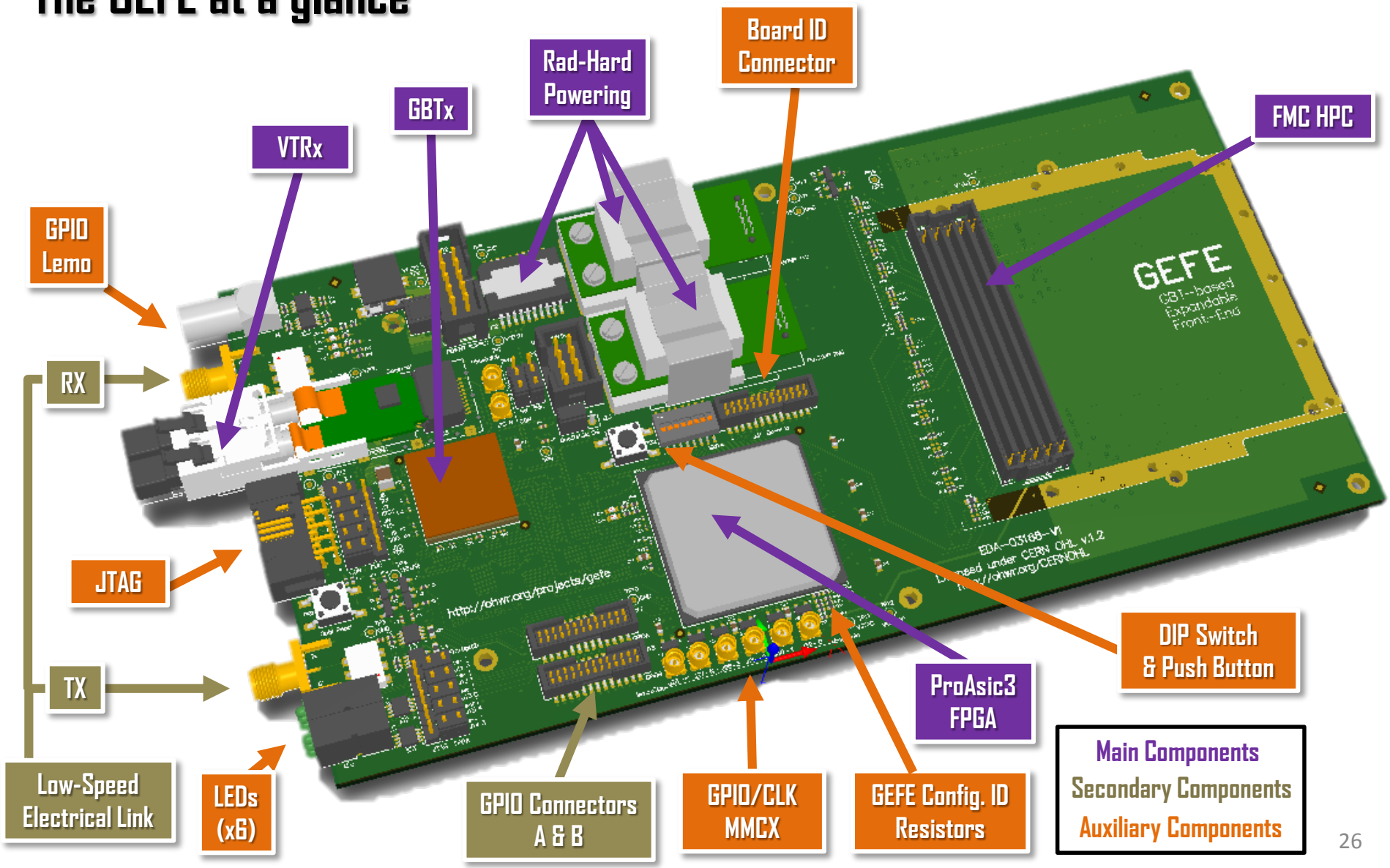
The GEFE at a glance



GEFE board (8 of 9)

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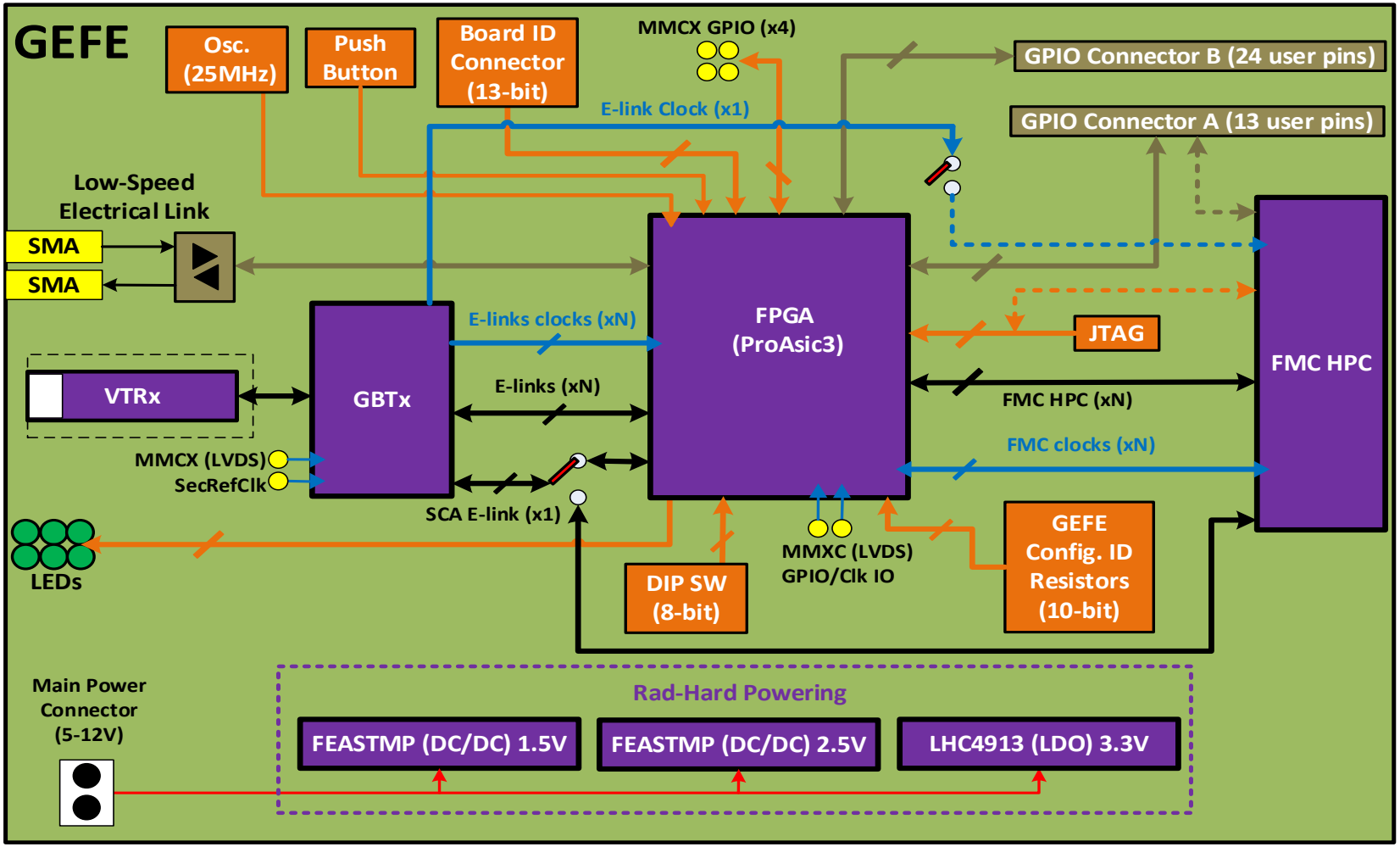
The GEFE at a glance



Main Components Secondary Components Auxiliary Components

GEFE board (9 of 9)

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Radiation Hardness

Qualified up to 75 krad
Qualified bellow 75 krad
Not Qualified

Active Component	Description	Tested	Max. Radiation Levels
VTRx	Optical Transceiver	YES	up to 50 Mrad 2x10^15 n/cm²
GBTx	Multi Gigabit Transceiver	YES	up to 100 Mrad 1.40x10^7 p/cm²
FPGA (ProAsic3)	A3PE3000-FGG896	YES	up to 300 krad LET of 55MeVcm²/mg 1*10^7 p/cm²
FEASTMP	DC/DC Regulator	YES	up to 200 Mrad(Si) 5.0x10^14 n/cm²
LHC4913	LDO Regulator	YES	up to 500 krad 2.0*10^7 p/cm²
SN74LVC2T45DCTT	Dual-Bit Dual-Supply Bus Transceiver	YES	x > 50 krad(Si) x > 9.31*10^11 p/cm²
BST82	N-CHANNEL MOSFET with Diode	YES	x > 27.1 krad(Si) 6.0x10^11 p/cm²
SN65LVDS2DBVR	High-Speed Differential Line Receiver	NO	
SPXO018077	Crystal Oscillator (25MHz)	NO	
BAV99	High Speed Switching Diode	NO	

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Application Examples (1 of 2)

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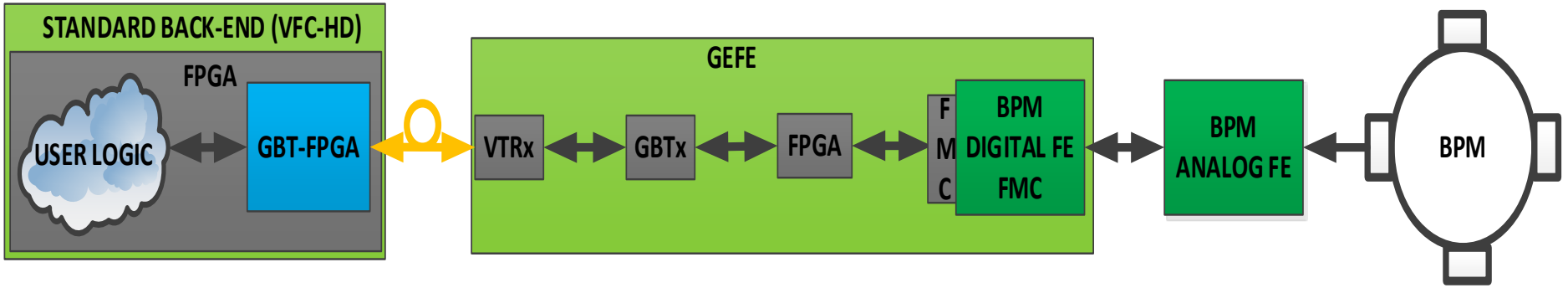
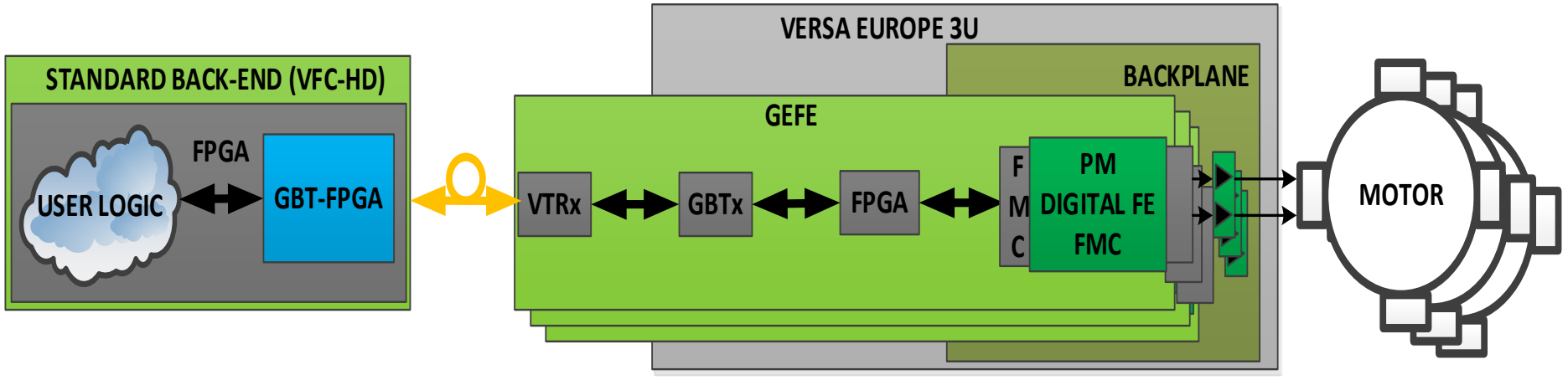
Multi-Orbit POsition System SPS (MOPOS SPS) (BE-BI-QP)



Motor Controller with Optical Interface (MCOI) (BE-BI-PM)



Application Examples (1 of 2)

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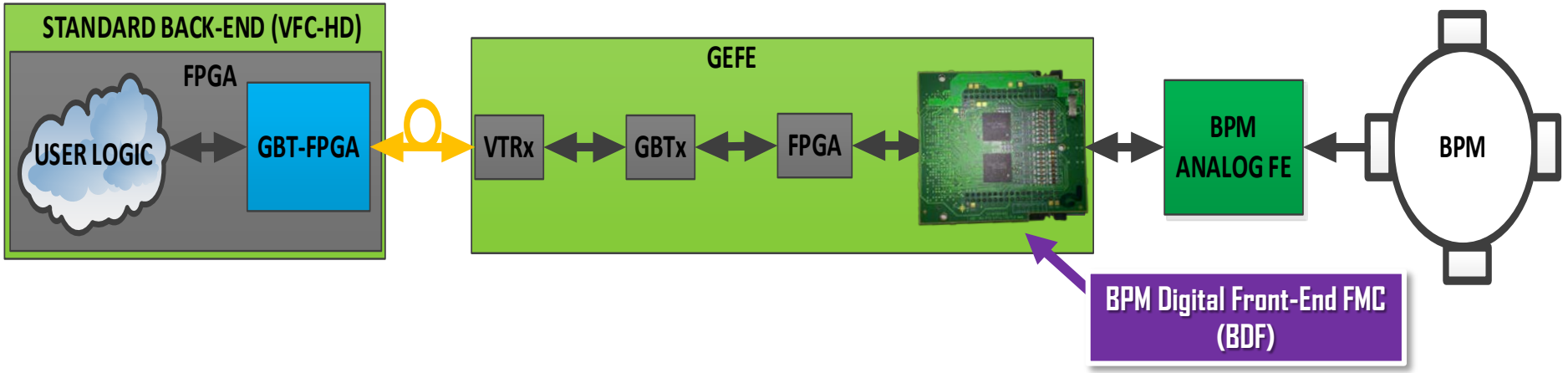
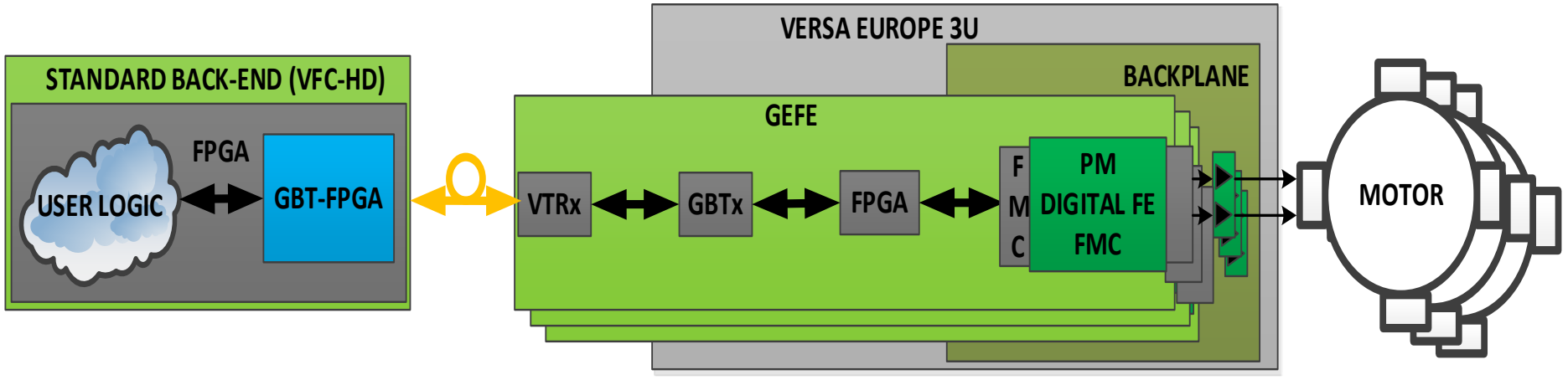


Motor Controller with Optical Interface (MCOI) (BE-BI-PM)



Application Examples (1 of 2)

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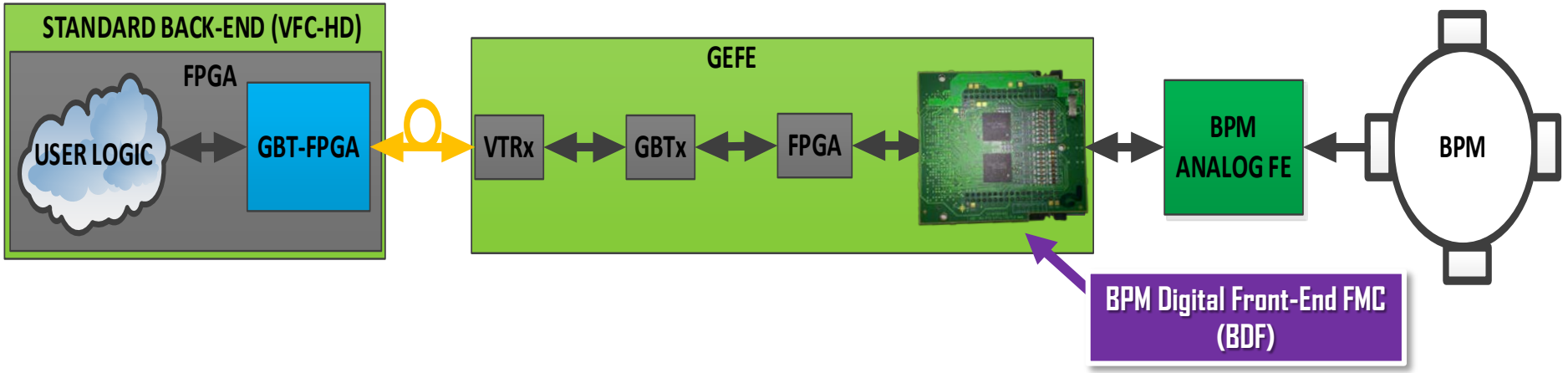

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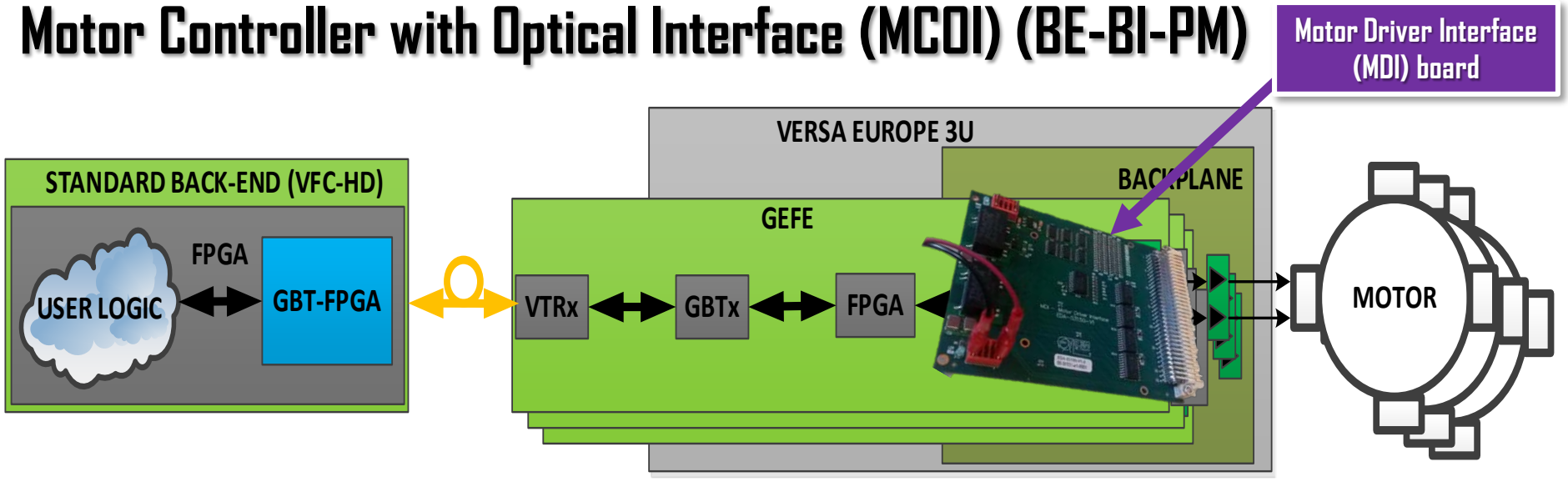

Application Examples (2 of 2)

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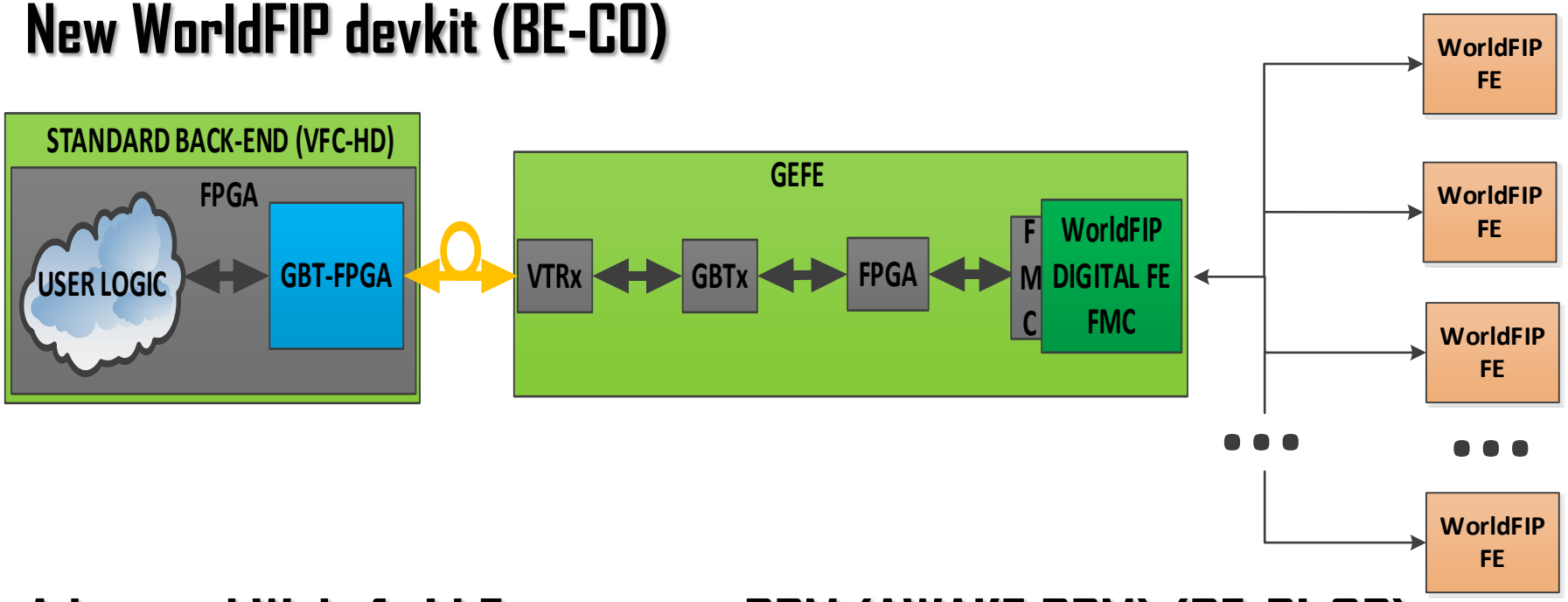
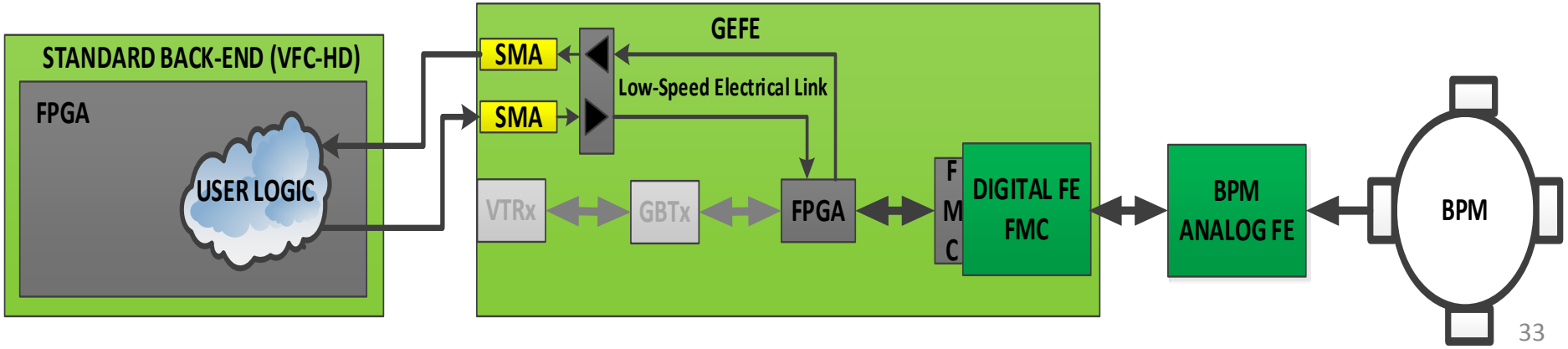
New WorldFIP devkit (BE-CO)



Advanced Wakefield Experiment BPM (AWAKE BPM) (BE-BI-QP)



Rad-hard electronics developments

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Status (1 of 2)

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The GEFE board

- Design of GEFE v1 finished
- 4 PCBs already fabricated
- 2 prototypes of GEFE v1 foreseen by the end of next week (week 38)
- Radiation hardness qualification required for:
  - Active components not qualified up to 75 krad
  - The full GEFE board

Status (2 of 2)

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The GEFE community

- Increasing the number of members
- Specification in version 0.8.5 (may be used as User Guide)
- Open HardWare Repository (OHWR) Wiki and Email List
- Projects in the GEFE community:
  - New Multi-Orbit POsition System SPS (MOPOS SPS) (BE-BI-QP): Requested 300 pieces
  - Advanced Wakefield Experiment BPM (AWAKE BPM) (BE-BI-QP): Requested 30 pieces
  - Motor Controller Optical Interface (MCOI) (BE-BI-PM): Requested 25 pieces
  - CLIC Acquisition and Control Module (CLIC-ACM) (BE-CO): Interested
  - New WorldFIP devkit (BE-CO): Interested
  - Function Generator Controller Lite (FGClite) (TE-EPC): Interested
  - Beam Wire Scanners (BE-BI-BL): Interested
  - CHARM test board (EN-STI): Interested

Rad-hard electronics developments

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Summary & Outlook (1 of 2)

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Summary

Common Digital Front-End for Beam Instrumentation

Target Total Ionizing Dose (TID): up to 75 krad

- **The GEFE board**
  - General purpose FPGA-based radiation tolerant board
    - Rad-Hard FPGA ProAsic3 (ACLA3PE3000-FGG896) from Microsemi
    - Features different components of the GBT-Versatile Link ecosystem from CERN PH-ESE
    - Optical & Electrical interfaces (FMC HPC, etc.)
  - 2 prototypes of GEFE v1 expected by the end of next week (week 38)
- **The GEFE community**
  - Increasing the number of members
  - Specifications in version 0.8.5 (may be used as User Guide)
  - Open HardWare Repository (OHWR) Wiki and Email Lists
  - Several projects (More than 350 pieces requested)

Summary & Outlook (2 of 2)

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Outlook

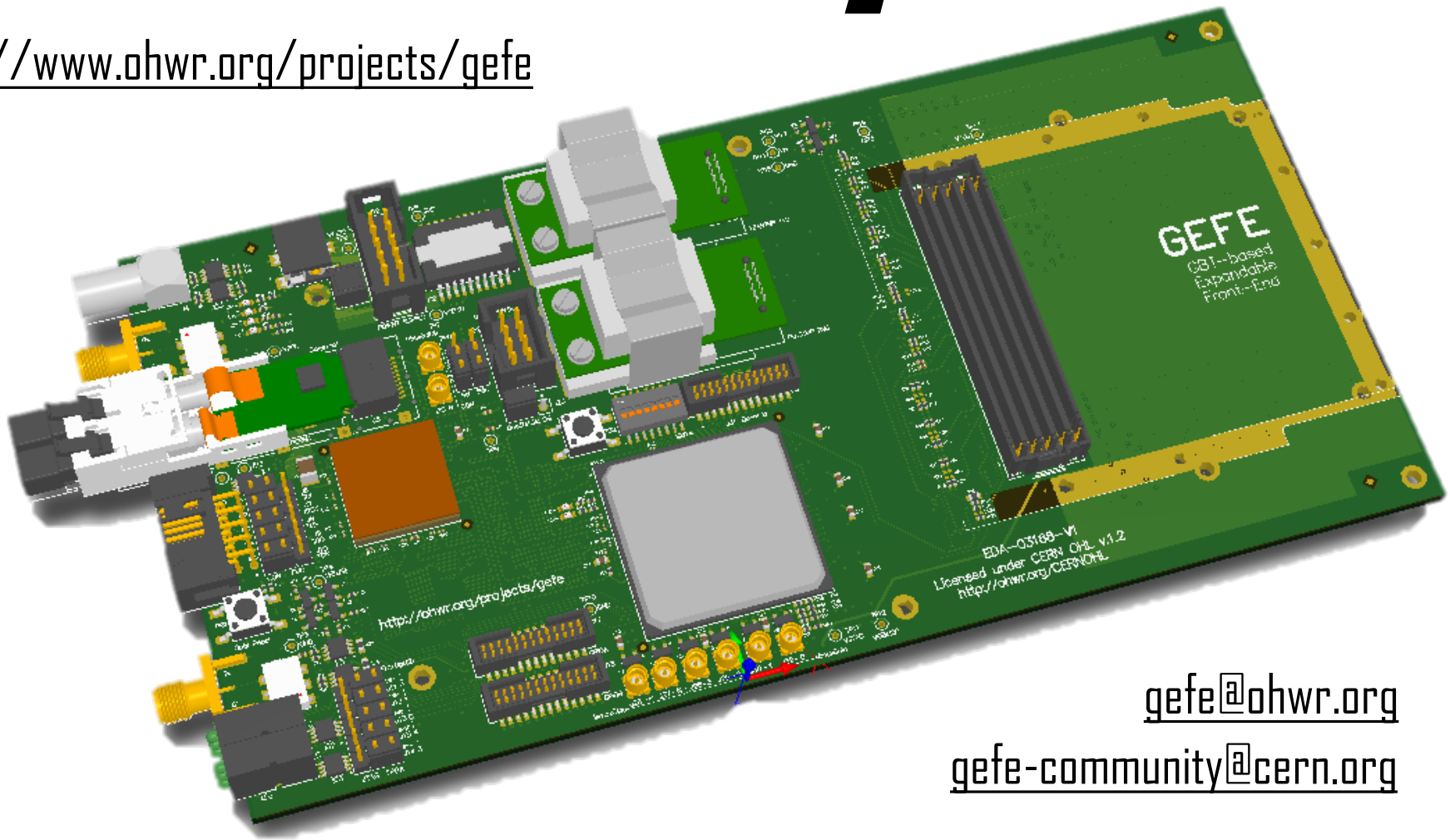
- **The GEFE board**
  - Validity test of the first 2 prototypes of GEFE v1 (October 2015)
  - Radiation hardness qualification of:
    - Active components of GEFE v1 not qualified up to 75 krad (Second half of 2015)
    - Prototype of GEFE v1 (First half of 2016)

    Ph.D. Student (Christophe Donat Godichal) in charge of the radiation tests
  - Design and implementation of a fully automated test bench for production testing (First half of 2016)
  - Production stage (First half of 2017)

- **The GEFE community**
  - Increase the number of members
  - Organise periodical meetings
  - Update specifications after assembly of first GEFE v1 prototypes
  - Update Open HardWare Repository (OHWR) Wiki
  - Organise production of GEFE for the different projects

Thank you

http://www.ohwr.org/projects/gefe



gefe@ohwr.org

gefe-community@cern.org

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References

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- The GEFE project web page: http://www.ohwr.org/projects/gefe
- The VFC-HD project web page: http://www.ohwr.org/projects/vfc-hd
- The GBT project web page: https://espace.cern.ch/GBT-Project/default.aspx
- The GBTx ASIC manual: gbtxManual.pdf
- The VTRx application note: Application Note V2.4.pdf
- FEASTMP project web page: http://project-dcdc.web.cern.ch/project-dcdc/
- ST LHC4913 data sheet: http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/documents/LHC4913.pdf
- ANSI/VITA specifications web page: http://www.vita.com/Specifications
- Microsemi web page: http://www.microsemi.com/
- Microsemi ProAsic3E FPGA Fabric user's guide: PA3E_UG.pdf
- Microsemi ProAsic3E Flash Family FPGAs datasheet: PA3E_DS_v14.pdf
- Microsemi application note AC380: LPF_AC380_AN.pdf

GEFE board

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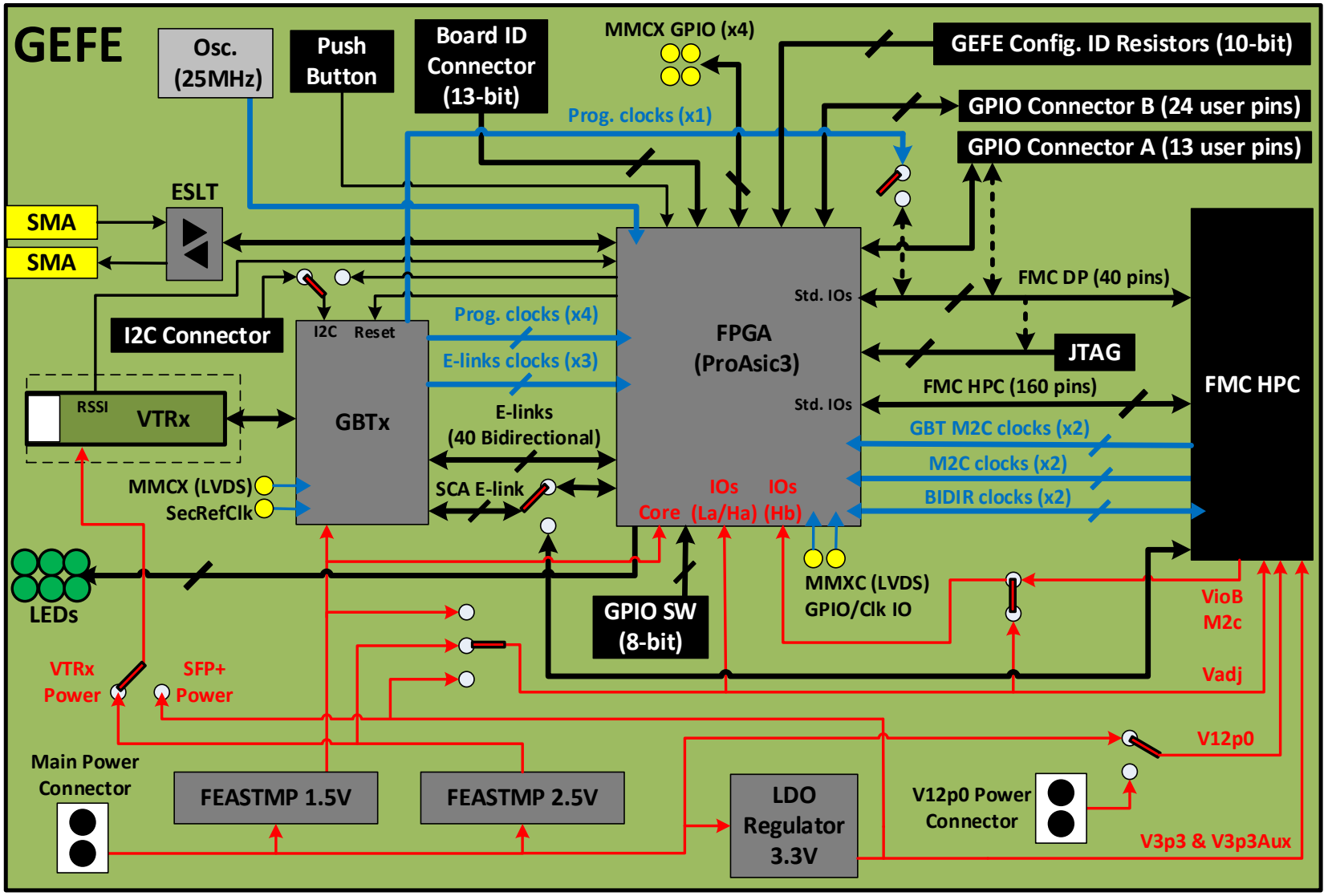
Detailed Block Diagram



GEFE board

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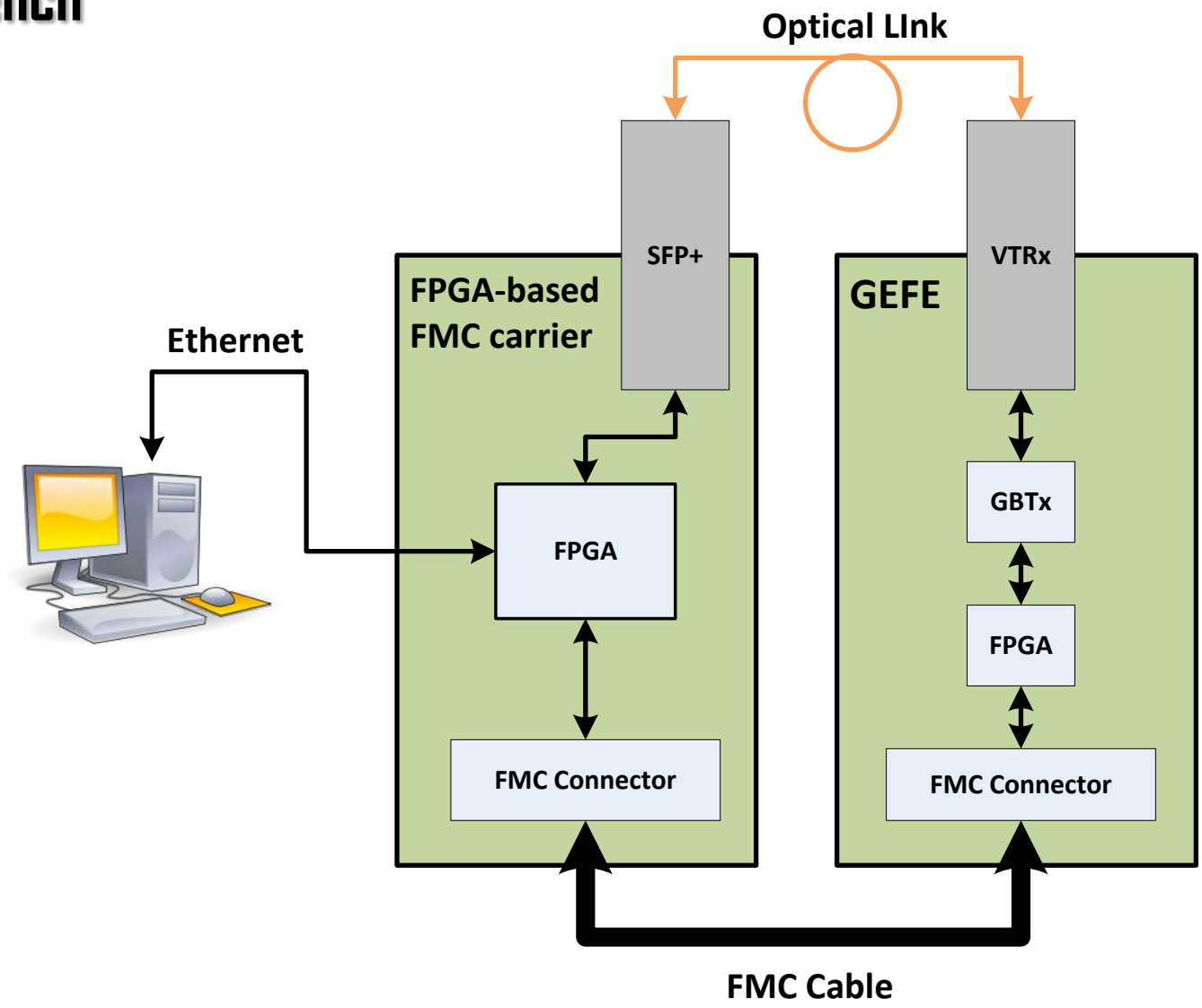
Test Bench



GEFE board

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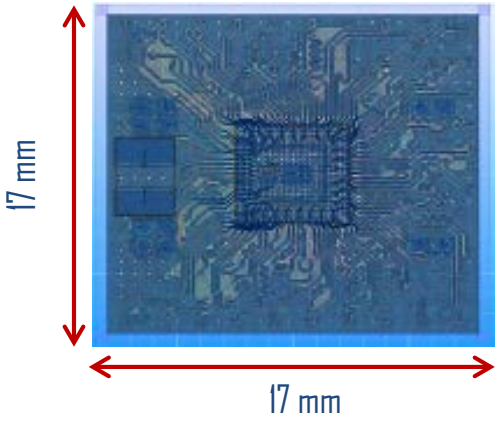
VTRx & GBTx

- **Main components of the new "Rad-Hard Optical Link for Experiments"**
- **Widely used at CERN (Experiments & Accelerators) and External institutions (Desy, etc.)**
- **Developed at CERN by PH-ESE**
- **VTRx**
  - Rad-Hard Optical Transceiver
  - Bidirectional Link at 4.8 Gbps (Versatile Link)
- **GBTx**
  - Rad-Hard ASIC
  - Single Electrical Link with VTRx at 4.8 Gbps
  - Multiple Electrical Links with Front-End Electronics (E-Links)
    - 40 Links @ 80 Mbps
    - 20 Links @ 160 Mbps
    - 10 Links @ 320 Mbps

VTRx

GBTx ASIC



GEFE board

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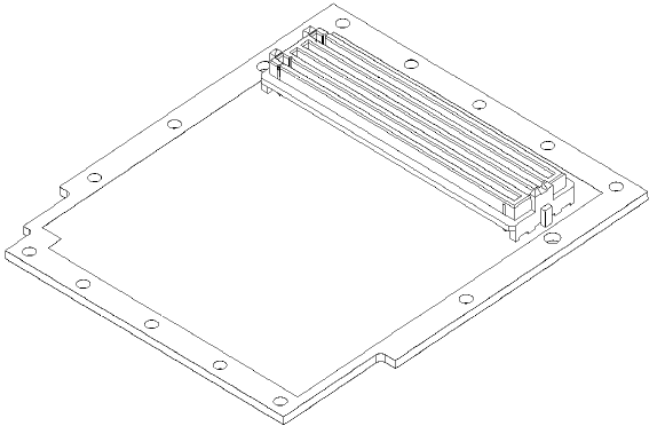
Particularities of the FMC connector in GEFE

- High-pin count (HPC) socket
- Accessible from the rear of the board
- The different control signals of the FMC standard are supported
- The targeted user-specific I/O data rate is up to 700 Mbps
- Up to 160 Single-Ended (or 80 Bidirectional) user-specific I/Os
- 6 differential clock lines (4 inputs and 2 bidirectional)
- The high-speed lanes (DP) connected to user-specific I/Os
- Special functions of DP lanes:
  - Direct SC e-link between GBTx and the FMC HPC connector
  - FPGA programming by JTAG master (e.g. SCA) placed on FMC
  - Direct signals from GPIO connector A to FMC HPC connector

Single width conduction cooled FMC Module



BDF

GEFE board

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FPGA (ProAsic3)

Microsemi

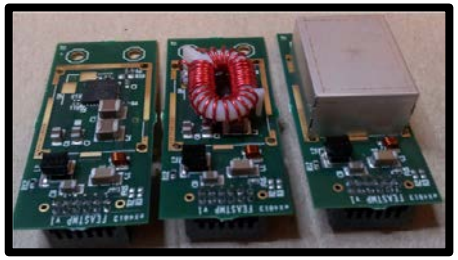
ProASIC3E	A3PE3000
System Gates	3,000,000
Equivalent LEs	35K
VersaTiles (D-Flip-Flop)	75,264
RAM kbits (1,024 bits)	504
4,608-Bit Blocks	112
FlashROM Bits	1,024
Secure (AES) ISP[2]	Yes
Integrated PLLs in CCCs[3]	6
VersaNet Globals	18
I/O Standards	Pro
I/O Banks (+JTAG)	8
Maximum User I/Os	620
Typical Static / Flash*Freeze Power (mW) at V_{CC}=1.2 V	3.30
Single-Ended I/Os / Differential I/O Pairs	
FG896	620/310

GEFE board

BE-BI-QP

Powering

FEASTMP



Features

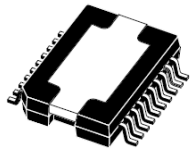
- Input voltage range 5 to 12V
- Continuous 4A load capability (dependent on output power level, limited to 10W)
- Available in different output voltage versions from 0.9 to 3.3V (minimum achievable with the FEAST ASIC 0.6V)
- Synchronous Buck topology with continuous mode operation
- High bandwidth feedback loop (150KHz) for good transient performance
- Over-Current protection
- Input under-voltage lockup
- Over-Temperature protection
- Power Good output
- Enable Input
- Fast acting fuse in series at the input of the module to protect the line in case of module failure
- EMC: conducted noise compatible with Class-B CISPR11 requirements
- Shielded to make it compatible with operation in close proximity (1cm) to sensitive detector systems
- Radiation tolerant: TID up to >200Mrad(Si), displacement damage up to 5e14n/cm^2 (1MeV-equivalent), no destructive SEEs up to >30MeVcm^{2}mg^{-1}, SEFI (reset) cross-section in a 230MeV proton beam ~ 2.8e^{-13} cm^2
- Magnetic field tolerance in excess of 40,000 Gauss

LHC4913 SERIES

3A POSITIVE LOW DROP VOLTAGE REGULATOR WITH INHIBIT FUNCTION

ADVANCE DATA

- LOW OUTPUT CAPACITANCE: 1µF
- LOW DROP VOLTAGE:
  0.5V @ I_O=1A
  1.5V @ I_O=3A
- OVERTEMPERATURE PROTECTION
- OVERCURRENT PROTECTION
- OUTPUT SHORT CIRCUIT MONITORING, SIGNALLED BY TTL OUTPUT
- ON/OFF EXTERNAL CONTROL BY MEANS OF TTL COMPATIBLE INPUT
- ADJUSTABLE CURRENT LIMITATION PROTECTS OUTPUTS FROM DAMAGING SHORTCIRCUITS
- REMOTE SENSING OPERATION



PowerSO-20 slug-up

GEFE board

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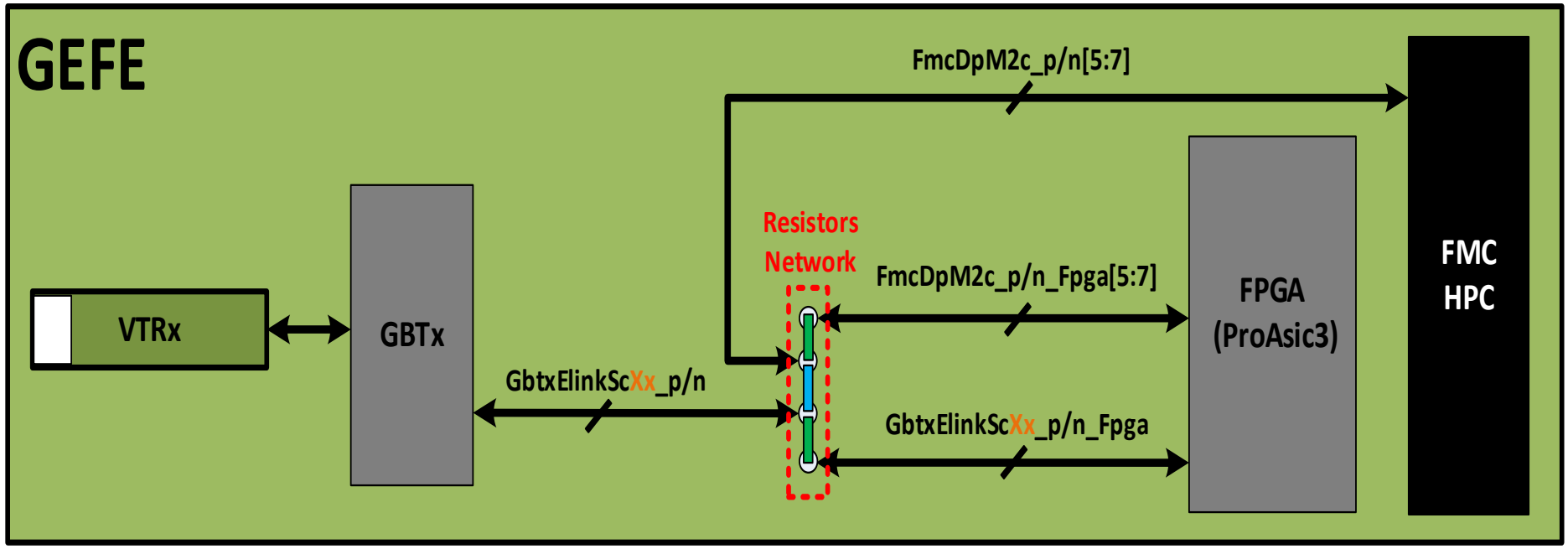
Slow Control (SC) E-Link

- Single E-link @ 80 Mbps



GEFE board

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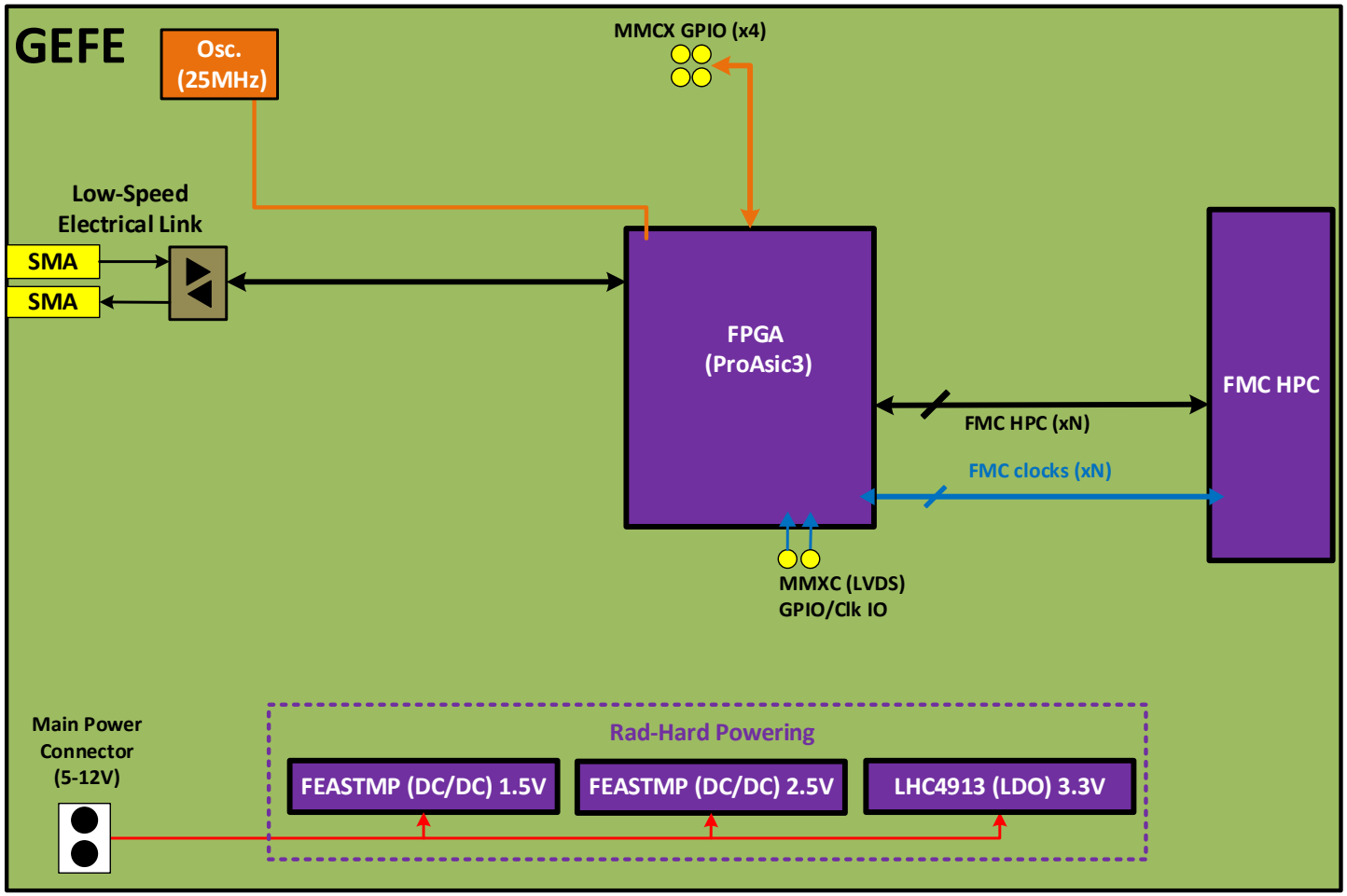
Low-Speed Electrical Link

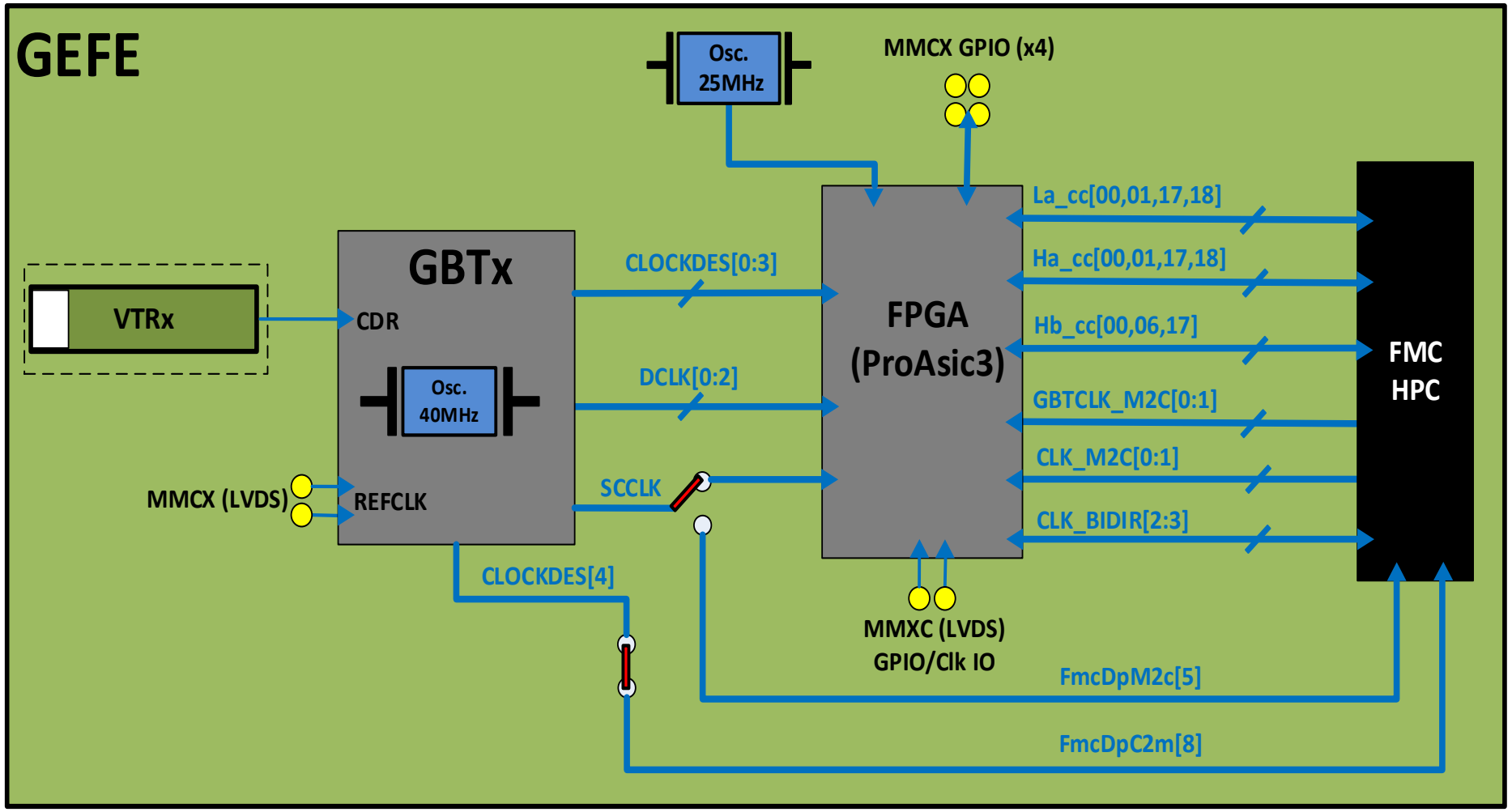
- Tested up to 10 Mbps over 2 Km of coper cable



GEFE board

BE-BI-QP

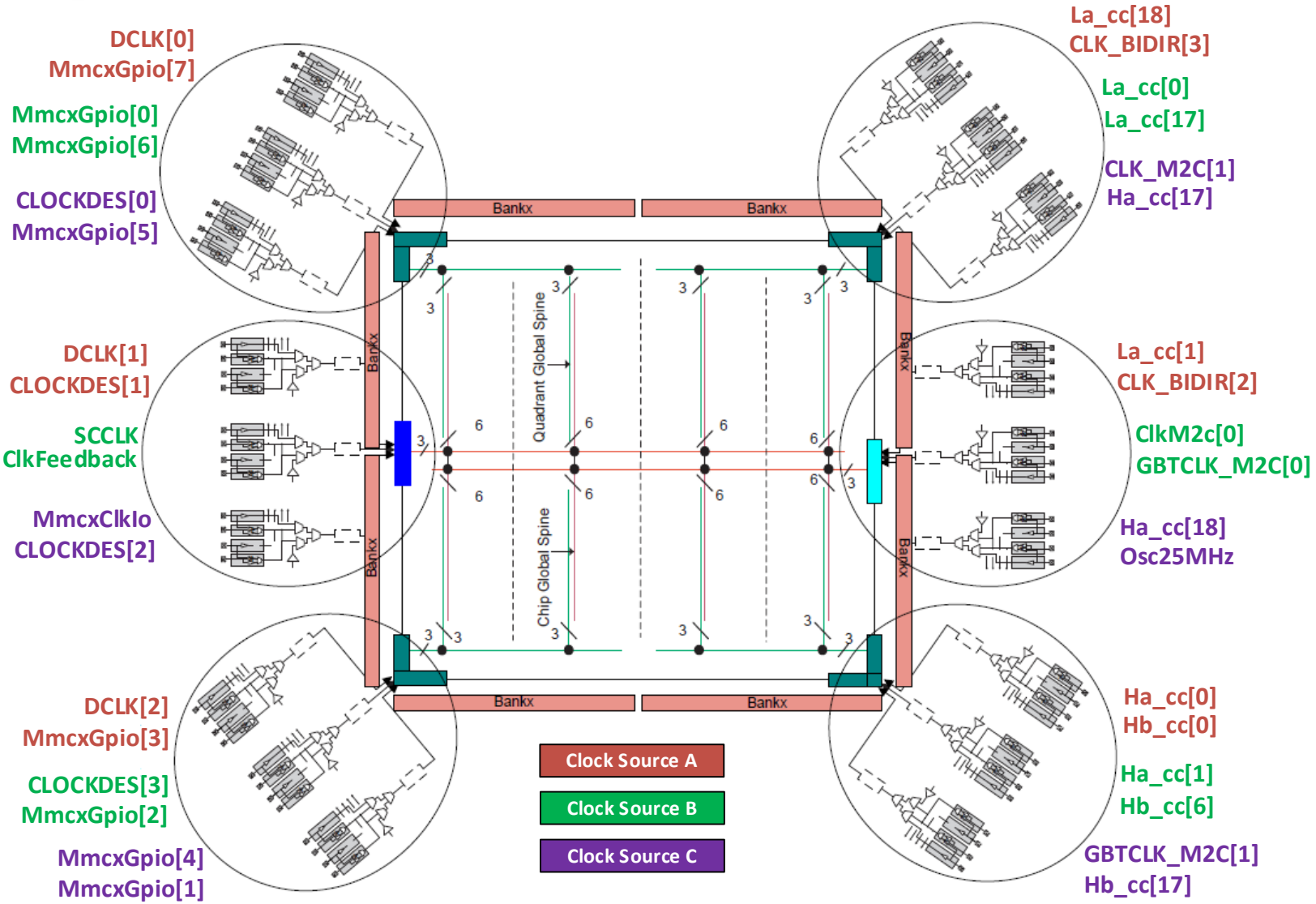
Clocking Scheme (1 of 2)



GEFE board

BE-BI-QP

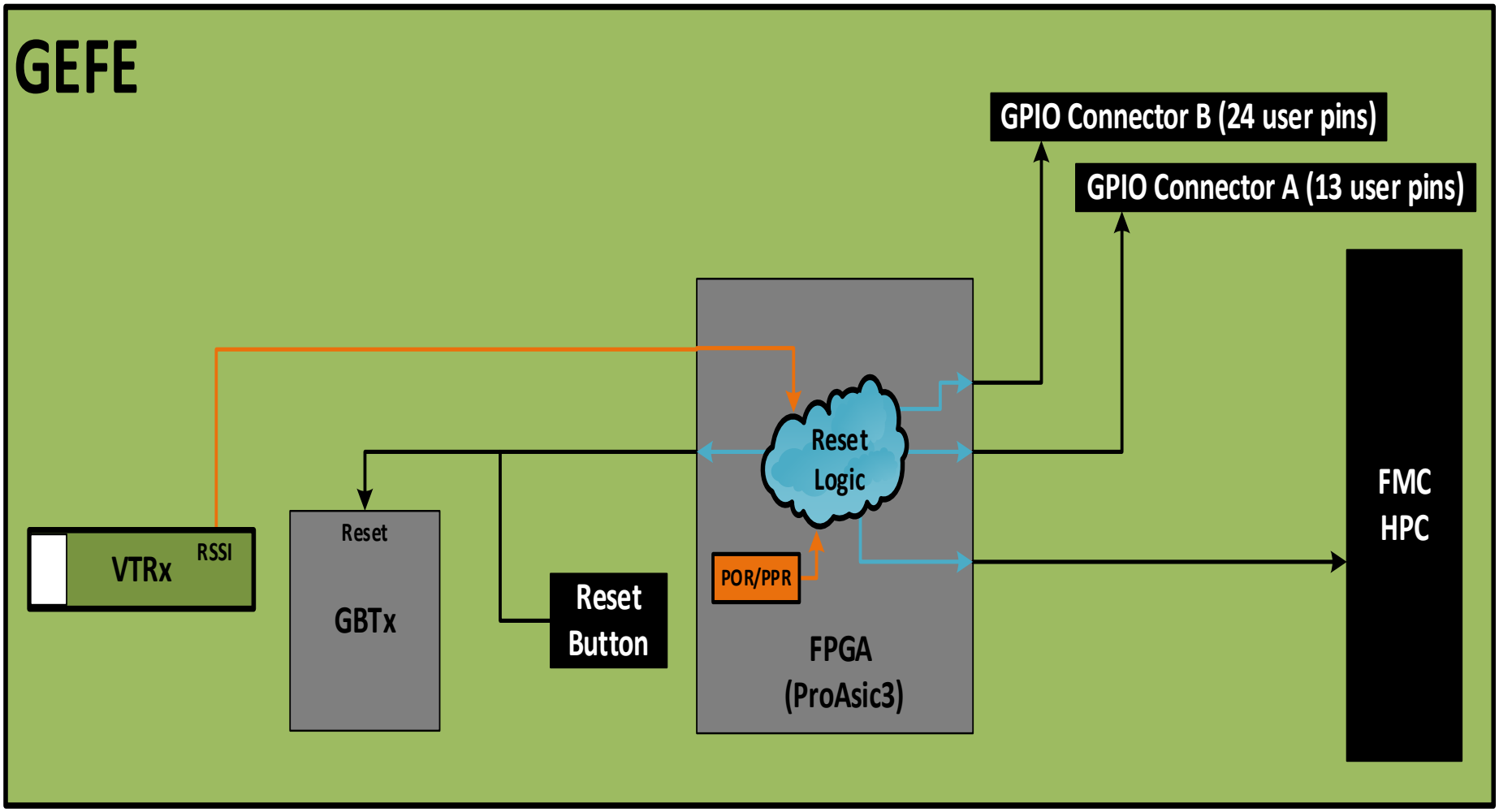
Clocking Scheme (2 of 2)



GEFE board

BE-BI-QP

Resets Scheme



GEFE board

BE-BI-QP

FPGA Programming Scheme