VFC-HD

PROJECT STATUS AND OUTSTANDING ISSUES @ SEPTEMBER 2015

BI VME FMC Carrier Project

VFC

2 LPC MEZZANINES

2 XILINX FPGAS

2 SRAMS

1 DDR CHIP

STATUS: DEBUGGED BUT OBSOLETE

High Speed ADCs

VFC-HPC

1 ***HPC*** MEZZANINES

1 ALTERA FPGA

2 SRAMS

4 APPLICATION SFPS

STATUS: DEBUGGED BUT OBSOLETE

High Volume Data

VFC-HD

1 HPC MEZZANINES

1 ALTERA FPGA

1 ***DDR3*** SO-DIMM

4 APPLICATION SFPS

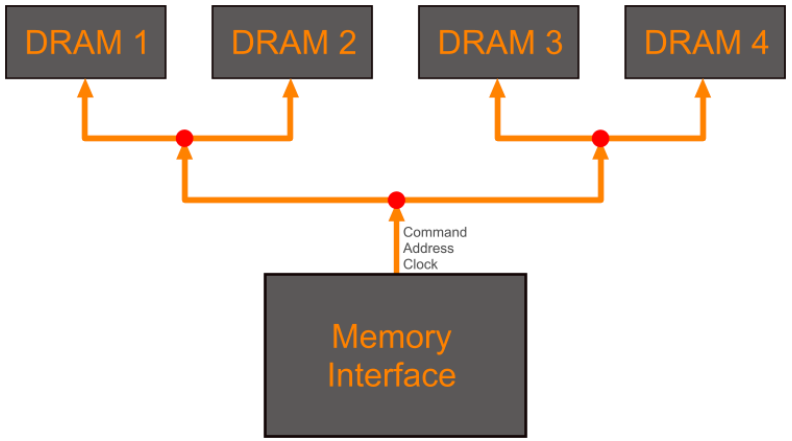
STATUS: REDESIGN NEEDED

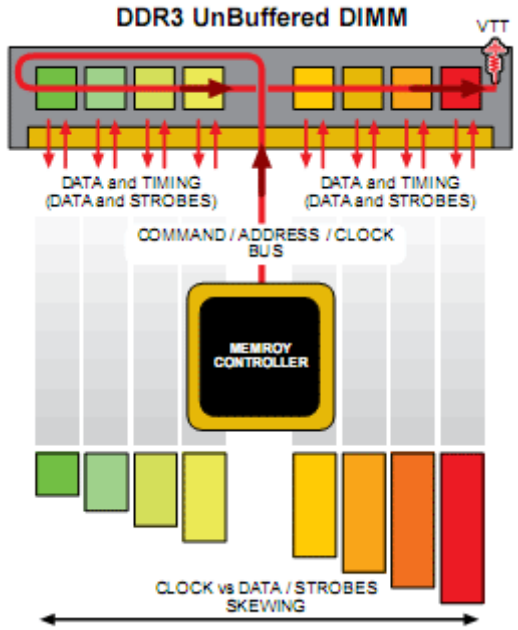
VFC-HD: the DIMM problem

ARRIA V GX and GT models support DDR3 chips interfaces but not in DIMM modules due to the fly by topology.

The default solution is to use single chip interfaces. Multi chip configurations are possible but should use a balanced tree layout in a pseudo DDR2 configuration and require extensive board simulation.

DDR2 Balanced tree structure





Single chip interface

- Simplest layout
- Advised in the ARRIA V datasheet
- Respect the DDR3 connections specs
- We can implement up to 2 fully **independent** 16bit interfaces (DLL/PLL sharing!)
- Chips from the same family of the one used by Altera for their dev kit are still in production (2Gb)
- Pin compatible chips with 1.35V interfaces (can run in 1.5V compatibility mode) exists with 2 and 4 times the density
- New chips with double die are in production with 8 times the density

Multi chip 64bit interface

- 2 times more memory than the single chip solution but in a single interface
- More complex layout
- Non DDR3 standard (Altera suggest a pseudo DDR2 balanced tree configuration and extensive board simulation)
- Can be copied by a dev kit (that implement a only partially balanced tree trying to simplify the layout)
- Implemented as 4x 16bit chips
- Chips from the same family of the ones used in the dev kit are still in production
- *Same upgradability options as for the single chip*

Multi chip 72bit interface

- *Same consideration as for the 64 bit interface but it requires an additional 8bit chip*
- The 8 extra bit would be used for error detection in the stored data
- The 8bit and the 4 16bit must be matched in latencies and depth
- The 8bit of the family chosen from Altera is no more in production: need to go for 1.35V in compatibility mode since the beginning

Summary

Single chip interface:

- 512MB in 2 independent interfaces
- Simple layout
- Require FW effort to have the 2nd interface running (clock resources sharing)

Multi chip interfaces

- 1GB
- More complex layout requiring extensive simulation but can be copied by a dev kit mimicking the layout
- Can be implemented as extended interface (72 instead of 64 bits) but:
  - Require the use of chips with 8 and 16 bit wide interfaces but matched in speed and depth
  - The 8 bit matching the 16bits used by Altera is already out of production requiring the immediate jump to DDR3L chips running in 1.5V compatibility mode

All the above can be upgraded to x2 and x4 times the memory using DDR3L in compatibility mode and to x8 using DDR3L dual die chips

We could foresee the passage to 1.35V interfaces just planning properly the PS and voltagereferences