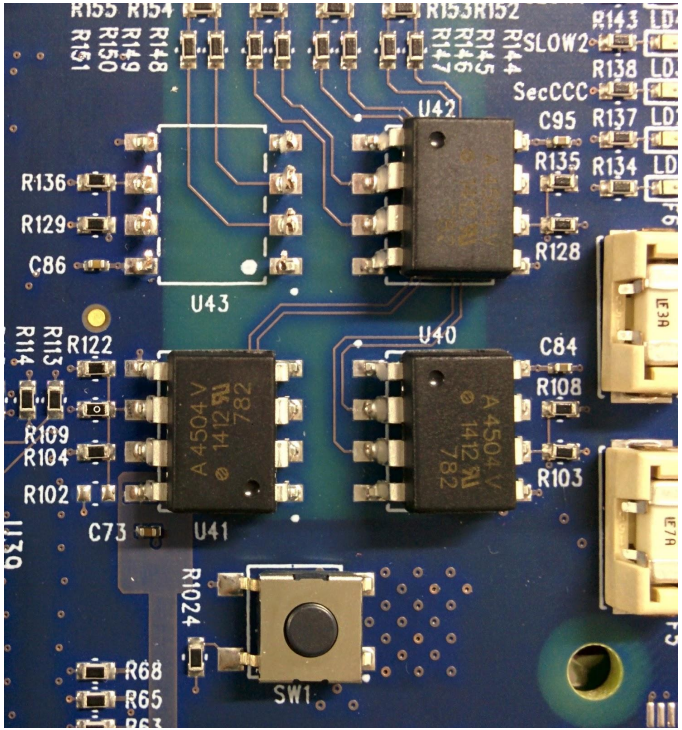
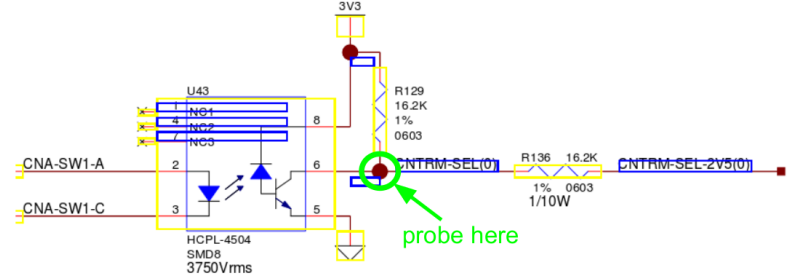
ngCCM Update

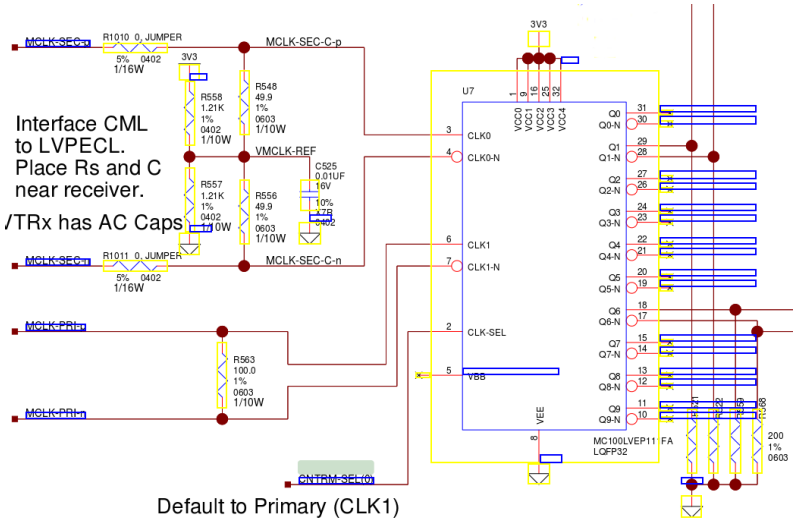
Joseph Mariano

27-08-2015

Optocoupler Removal







Default to Primary (CLK1)

Optocoupler Removal

- Optocoupler U43 has been removed on all boards
- All boards passed post removal testing:
  - Confirm logic high (avg. 2.68V) at indicated probe point
  - Test ngCCM registers using ngccm server
    - CNTRM-SEL(n) status registers added to confirm SW1 status

```
Checking the counting room switch statuses...
*********************************************
SW1: 1
SW2: 1
SW3: 1
SW4: 1
```

Summary of ngCCMs: Installation Candidates

18 ‘flawless’ ngCCMs:

- 08-01/001
- 01-02/005
- 03-02/006
- 02-03/011
- 05-01/012
- 09-04/013
- 09-02/014
- 05-02/016
- 01-01/017
- 10-02/018
- 06-04/020
- 10-04/021
- 02-04/022
- 02-01/023
- 06-02/024
- 04-04/025
- 06-01/026
- 03-03/027

Saw some errors on secondary link at UMD test stand. This is well explained by fiber perturbation during testing and no errors were seen during undisturbed 24 hour tests.

Currently at UVA with Stephen Goadhouse.

Summary of ngCCMs: Backups

3 ‘backup’ ngCCMs:

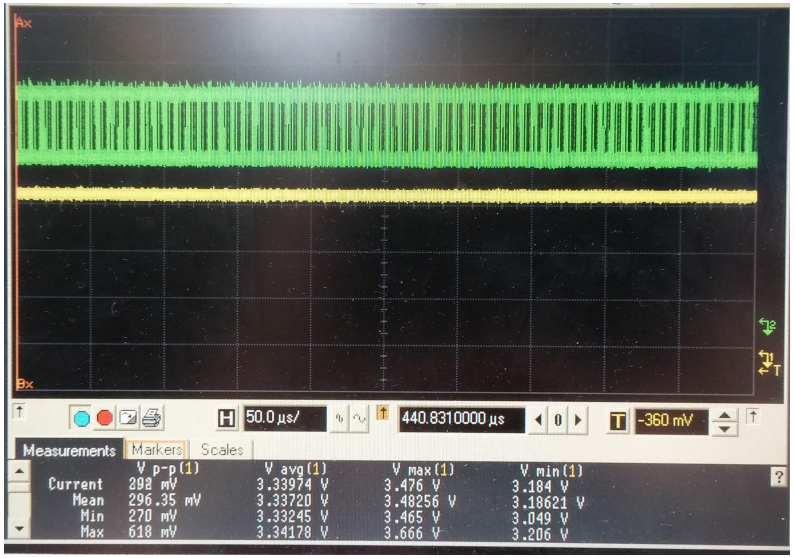
- 01-03/004
  - Consistently failed to communicate with the GLIBv2 on an alternate test stand at UMD. Cause of the issue undetermined. We have not been able to reproduce the problem and the board consistently communicates with the GLIBv3 at 904.
- 07-04/008
  - Saw a small number of errors on the primary link at the UMD test stand. Again, this could be well explained by the fiber being disturbed during the test, but only 2 cards showed errors in the primary link. Additionally, the JTAG programming test failed on the first try, but was successful on subsequent attempts. Maybe due to the power-up order?
- 08-03/019
  - This was the other board to see errors on the primary link.

Summary of ngCCMs: Problem Boards

4 ‘flawed’ ngCCMs:

- 03-04/002
  - Intermittent communications with QIEs
    - Does not depend on QIE chip number or slot position
  - I2C data line should be ~3.3V when no signal is on the line and be pulled low for data
  - I2C data was found to be stuck low (~0.1V) for slots investigated (between 1 and 7)
  - Signals 1-7 are handled by one FGPA (Slow1) and signals 8-14 by another (Slow2)

ngCCM 03-04/002 continued...



- But, when I tried to probe slots 9-14, the problem had disappeared (on all slots!)
  - I'm monitoring to see if the issue comes back

Summary of ngCCMs: Problem Boards

- 08-04/007
  - Consistently fails the secondary link JTAG programming test as a master
    - Not the most important function, but this problem may be indicative of a larger undiscovered issue
- 08-02/009
  - The ngCCM temperature sensors are intermittent
  - Does not always establish a link with the GLIBv3 at 904
    - Fiber sometimes has to be re-plugged several times

Summary of ngCCMs: Problem Boards

- 09-01/010
  - Consistently failed the following tests at the UMD test stand:
    - IO
    - I2C
    - TEMP
    - Secondary IO (as master)
  - The board was able to pass all these tests as the slave in a secondary link
    - Maybe a problem with the mezzanine/motherboard connector?

Firmware Update

- I've received new firmware (2v06) with TMR enabled from Stephen
- I'm beginning to update and test the boards:
  - Confirm that communications with GLIBv3 are locked
  - Use ngccm server to write/read ngCCM & QIE registers
- No problems so far!
- Plan: Get all ngCCMs reprogrammed and tested by tomorrow (hopefully)

RefClk_Sel Issue

- During testing, I've been noticing that ~20% of the time (very rough estimate) when I power up an ngCCM I receive this error:

```
HF2-mezz_SERDES_REFCLK_SEL
    expected: 1
    received: 0
```

- This is (almost) always fixed by a power-cycle
- Question: Is this a definitive measure of which RefClk the mezzanine is using? I know that the FPGA grabs a clock only during a reset/power-on.
  - This does not always agree with the uart debugger output (2v05)

RefClk_Sel Issue continued...

- Another question: Does a ‘1’ in this register correspond to RefClk0?
  - The uart debugger output on 2v06 makes me think not… This would mean the ngCCM almost always powers up into RefClk1.
    - Then how did we observe the problem with RefClk0 at UMD?
  - Resetting the mezzanine FPGA consistently causes the register to go to ‘0’
- Maybe we should consider having RefClk0 hard-coded before installing the boards.