Simulation and optimisation of CCPD + CLICpix response

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CLICdp Vertex Meeting – October 7th 2015

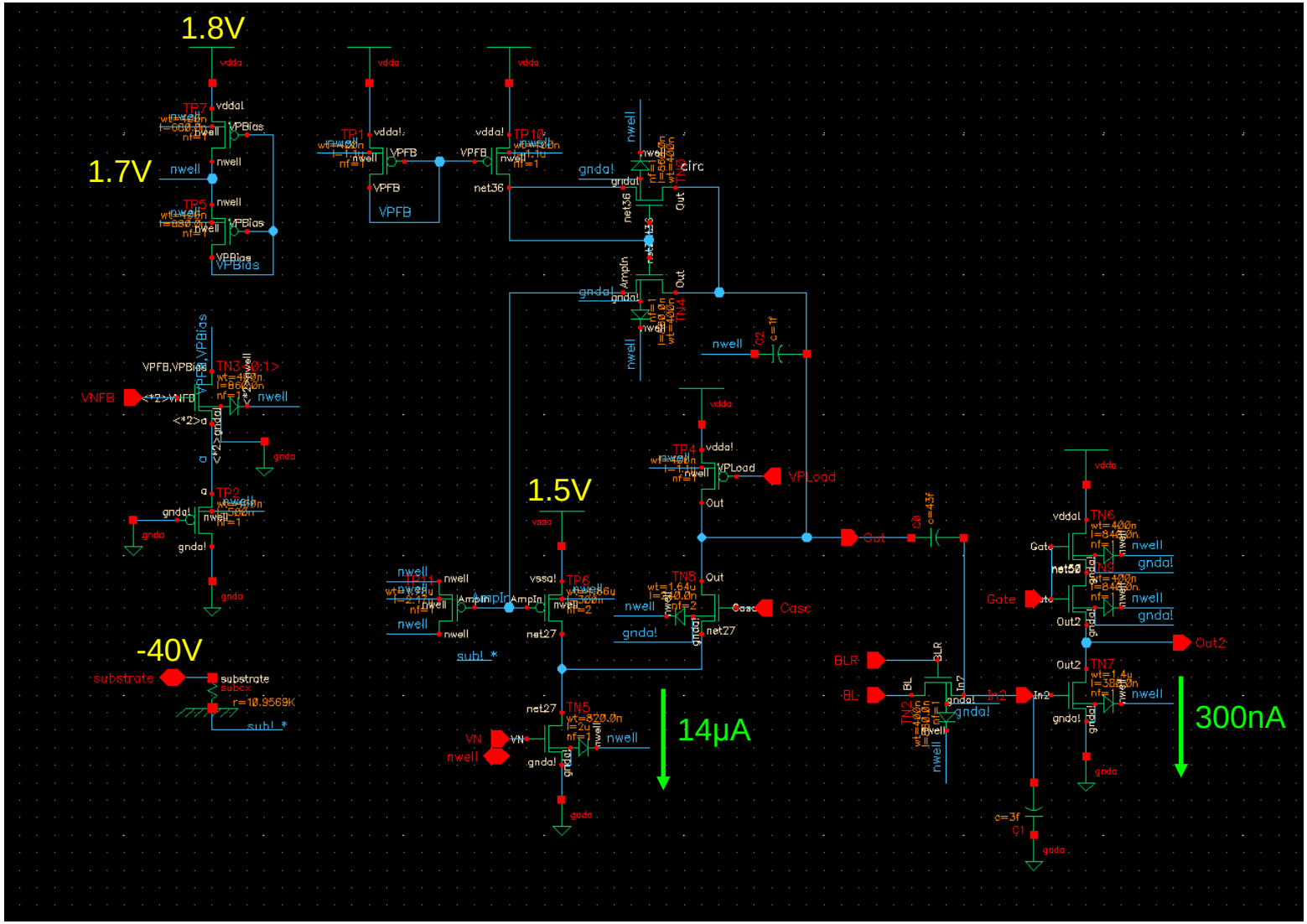
Introduction

- Iraklis Kremastiotis
- Doctoral Student, started September 2015
- Study, implementation and characterization of HV-CMOS sensors for a future vertex detector for CLIC
- Karlsruhe Institute of Technology (KIT)
- PH-ESE-ME

Outline

- CCPDv3 pixel schematic
- Coupling capacitance
- Simulation with CLICpix small-signal model
- Limitations
- Possible optimisations

CCPDv3 pixel schematic



CCPDv3 pixel schematic

- PMOS transistor used as coupling capacitor between the amplifier and the sensor (C ≈ 35fF)
- 2 amplification stages
- High-pass filter between 1st and 2nd amplification stage
- 7 control voltages:
  - 3 for the 1st amplification stage
  - 3 for the 2nd amplification stage
  - 1 for feedback and N-well biasing

1st stage amplifier

- Cascode stage with PMOS as input transistor
  - Biased at 14µA
- P+ diffusion at the output of the first stage acts as the parasitic capacitive feedback for the 1st stage amplifier
  - Charge gain of the amplifier is $\frac{1}{C_{FB}}$
  - Additional feedback due to parasitic capacitances between metal traces
  - Total feedback capacitance estimated ~1fF
- Parasitic feedback connects the output of the amplifier with the input prior to the coupling capacitor
  - Coupling capacitor is included in the feedback loop

1st stage amplifier

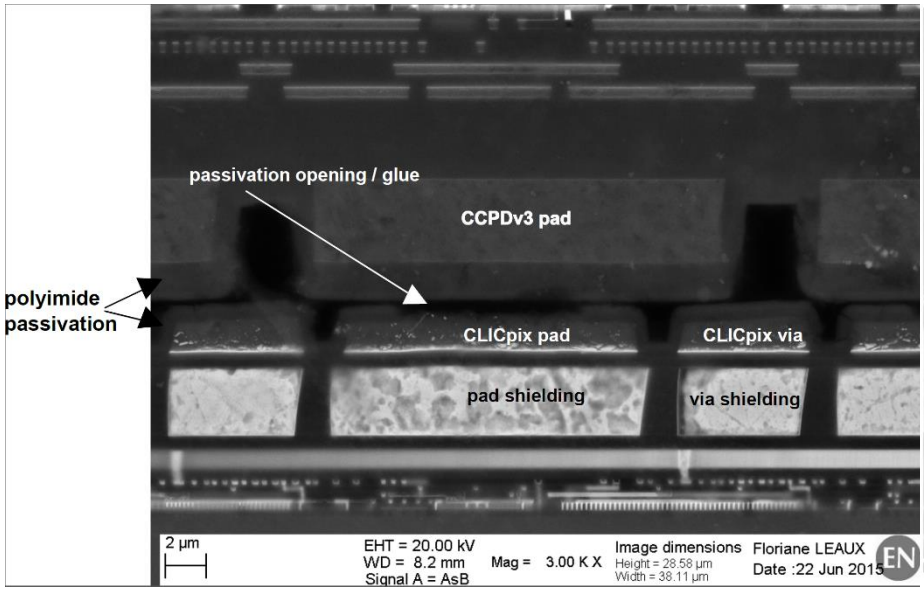
- NMOS transistor used as resistive feedback
  - Feedback transistor's current saturates for large positive output signals
  - Feedback resistance calculated as $\frac{1}{g_m}$ of the feedback transistor
- 3 control voltages (VN, VPLoad, Casc)

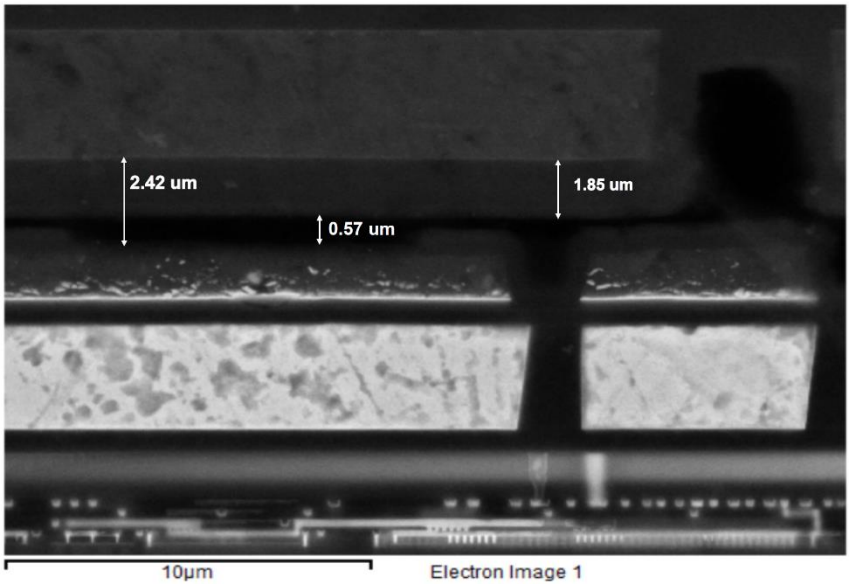
2nd stage amplifier

- NMOS common source
  - Biased at 300nA
- Open loop gain stage
- Peak-to-peak gain ~2
- Connected with 1st stage through a high-pass filter
  - 1 pole @ 430KHz
- 3 control voltages (Gate, BL, BLR)

Cross-section

- Assembly cross-section
- Distances used to estimate the coupling capacitance





Capacitance Calculation

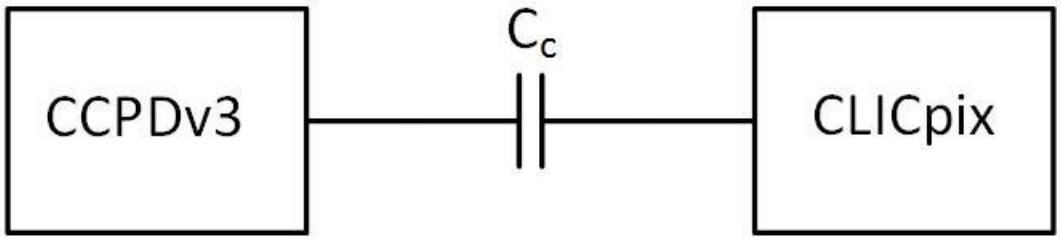
- Capacitance resulting from:
  - Polyimide passivation layer on the CCPD pads:
    - Thickness: ~1.85µm
    - Dielectric constant: 2.7 – 3.5
  - Epoxy glue:
    - Thickness: ~0.57µm
    - Dielectric constant: 2.5 – 6

- Using the above values, and for a pad area of $20*20\mu m^2$, the coupling capacitance is calculated as the series connected capacitance of the Polyimide and the Epoxy glue:

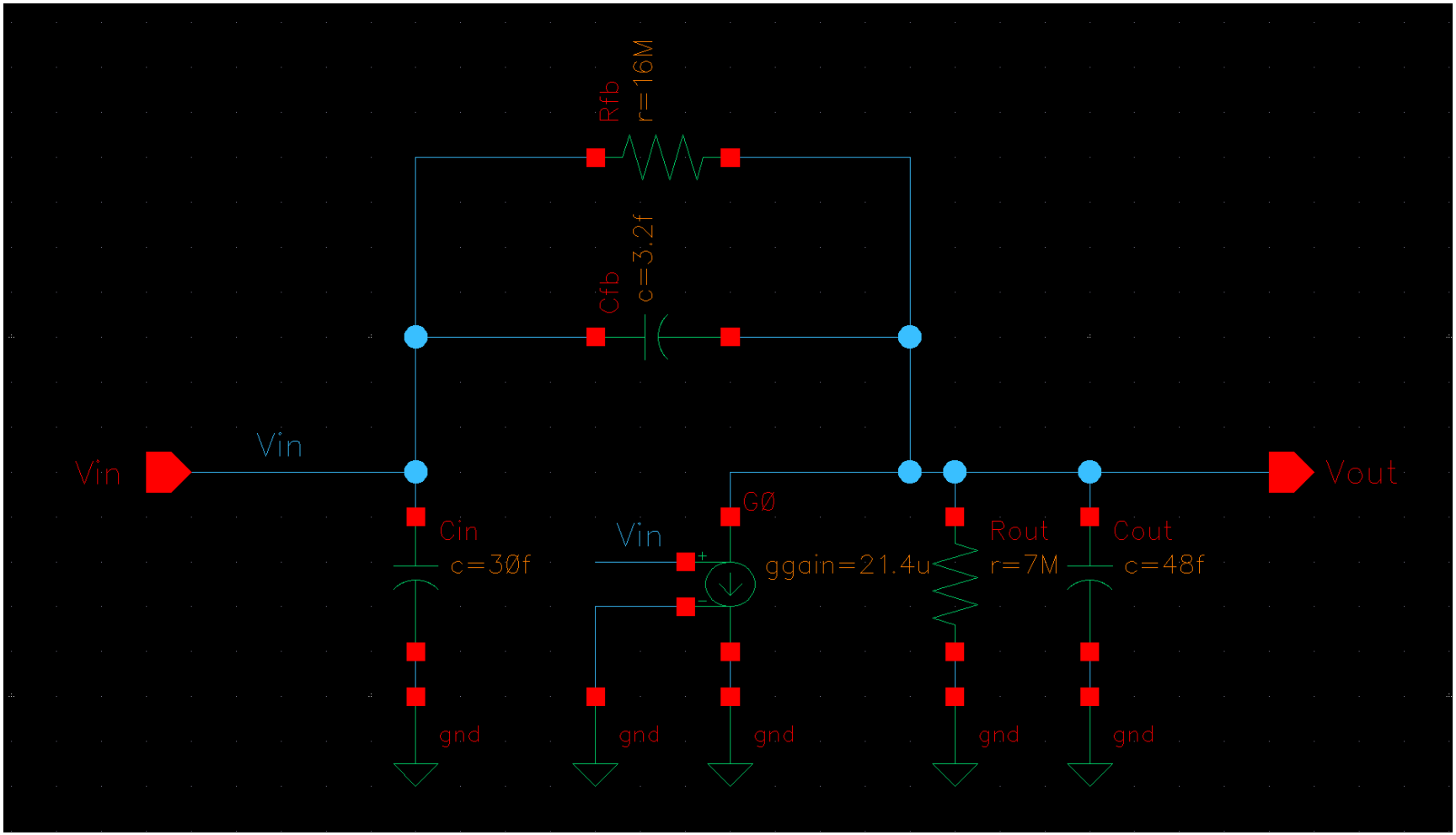
$$3.85fF < C_{coupling} < 5.65fF$$

Simulation with CLICpix

- Use of one CCPDv3 pixel, along with the bias block
- Connection with CLICpix through coupling capacitance
- Use of small-signal model of CLICpix (parameters provided by P. Valerio)



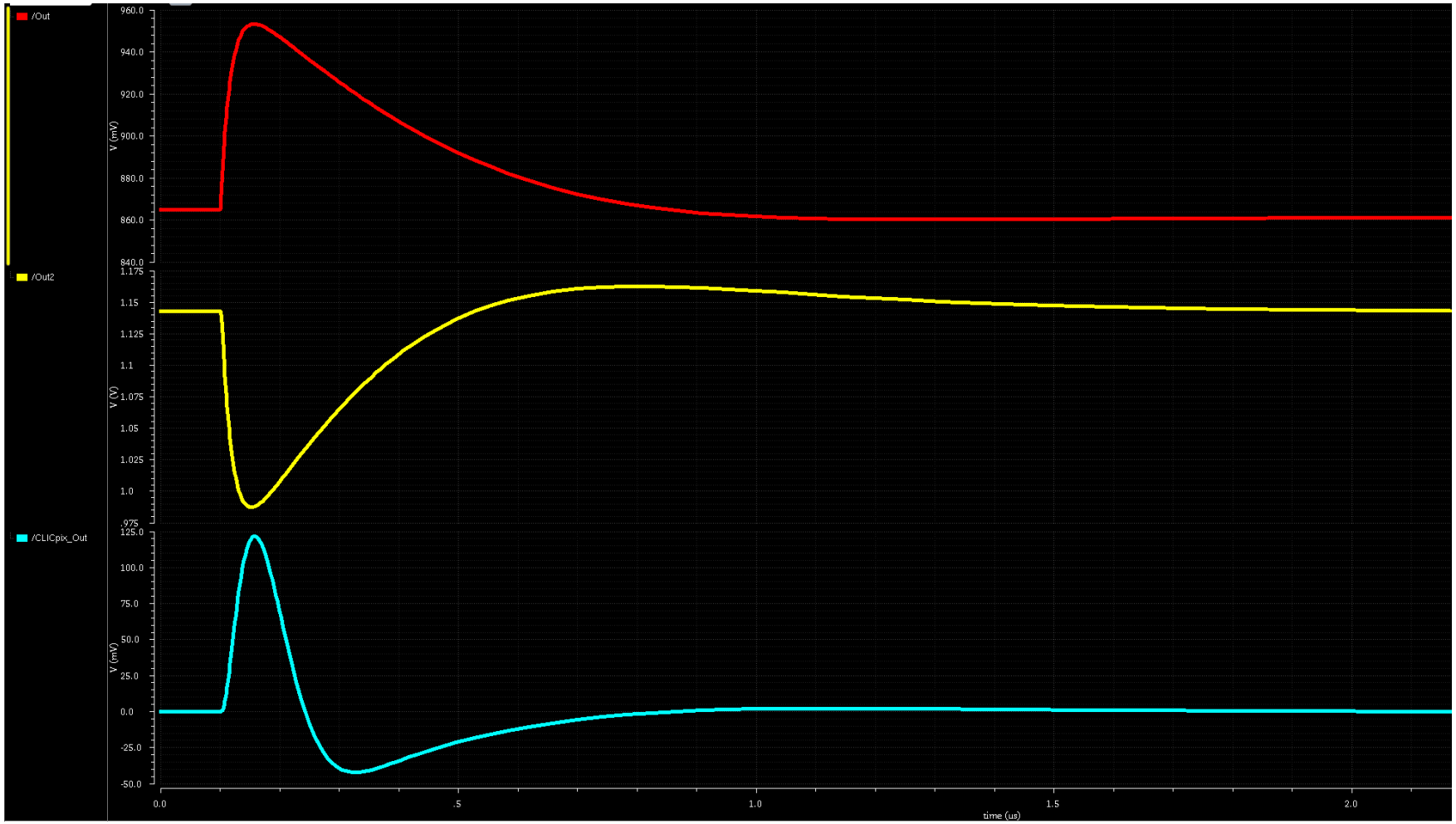
CLICpix small-signal model



Simulation Results

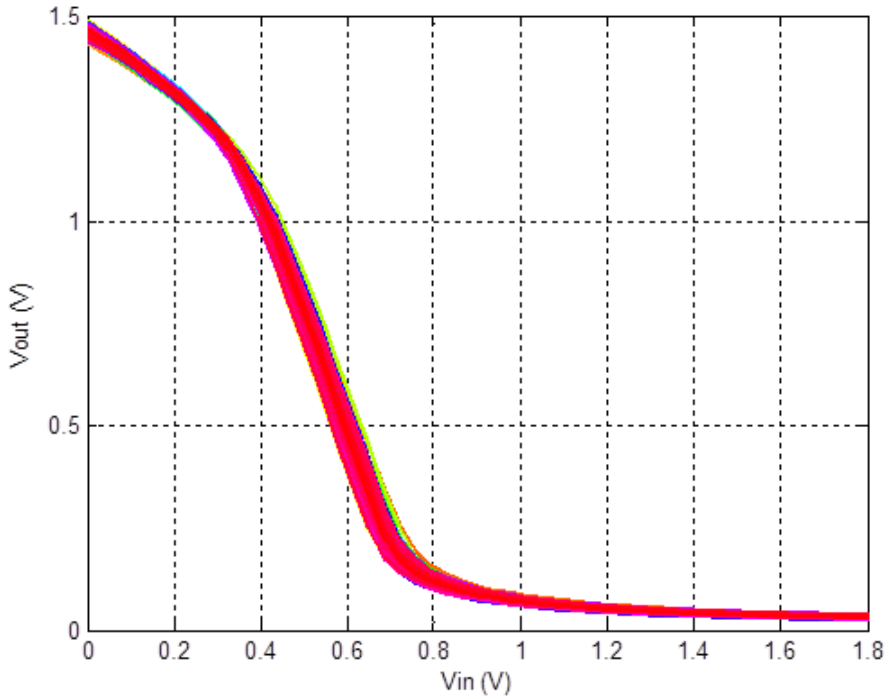
- Input pulse: 1ns*100nA
  - Equivalent to ~600e
- 1st stage:
  - p-p: 93mV
  - Rise time: 28ns
  - Fall time: 467ns
- CLICpix output:
  - p-p: 120mV
  - Rise time: 32ns
  - Fall time: 58ns
- N-well leakage current: 1nA
- Coupling capacitance: 4.5fF
- 2nd stage
  - p-p: 175mV
  - Rise time: 26ns
  - Fall time: 269ns

Simulation Results

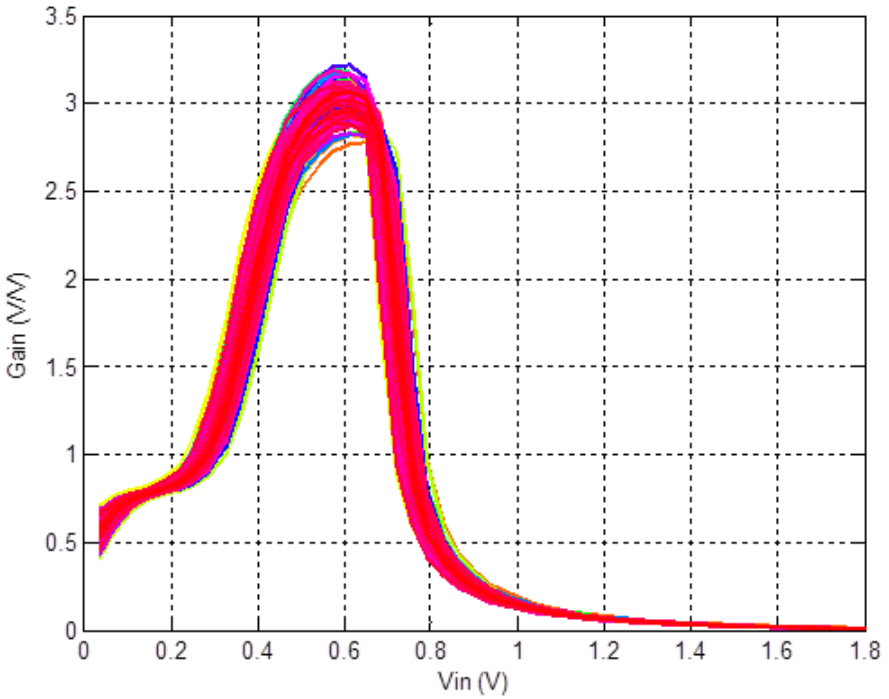


Monte Carlo analysis for 2nd stage

- Vout / Vin sampling

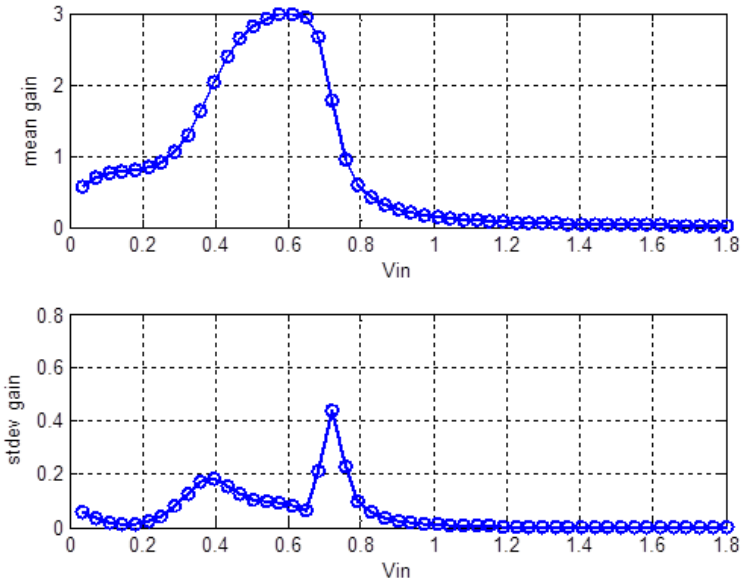


- Gain sampling



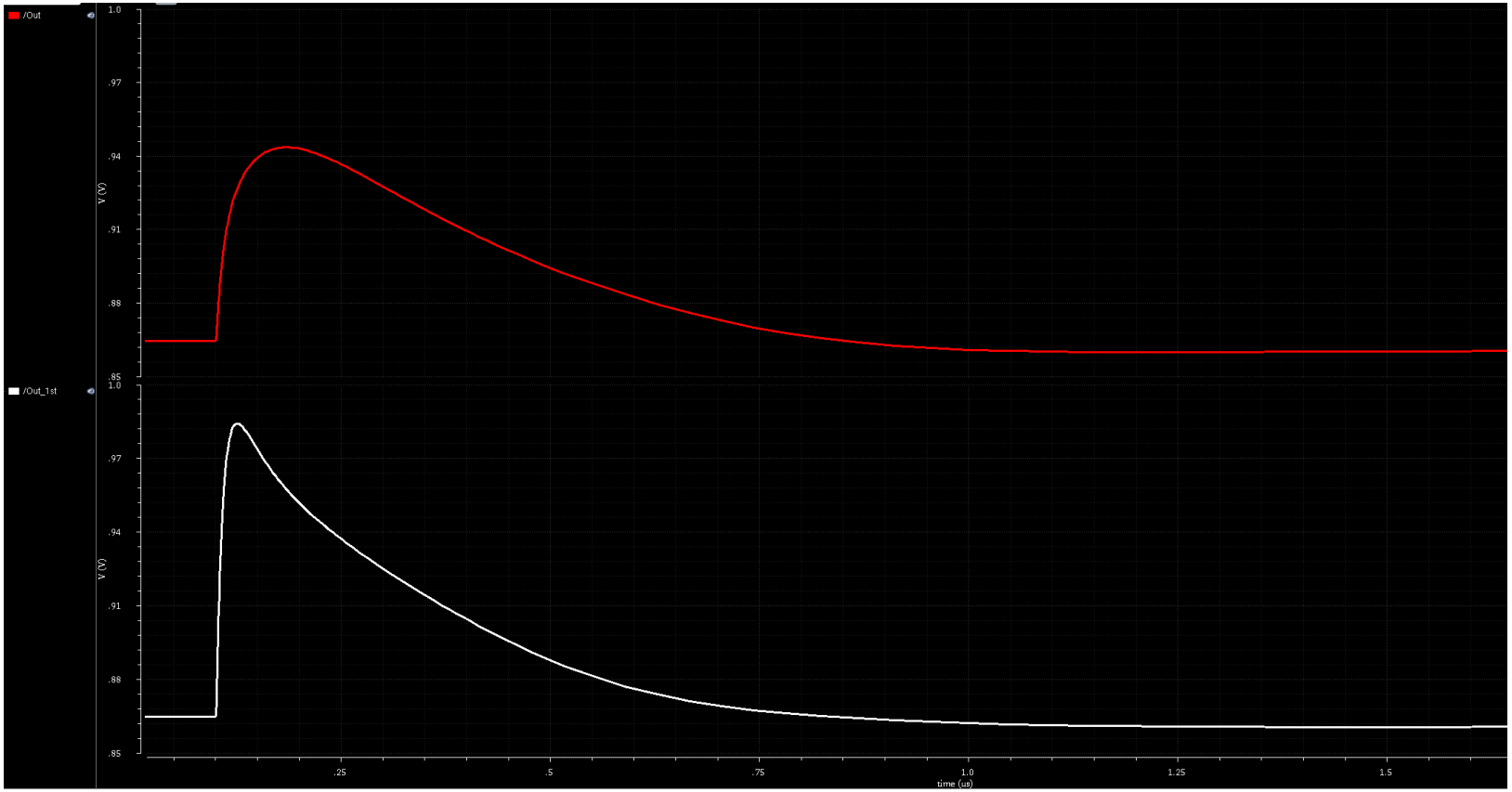
Monte Carlo analysis for 2nd stage

- High standard deviation at the points where the gain slope is high
- Results to low homogeneity between different pixels



Simulation without 2nd stage

- Output for the 1st stage of the pixel vs the 1st stage without the 2nd

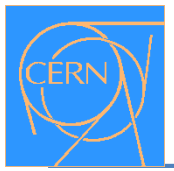


Limitations

- 2nd amplification stage:
  - Reduced homogeneity
  - Small contribution to gain or rise time
  - 3 extra control signals
  - Could be replaced by a source follower inside the feedback loop
- Deep N-well minimum spacing = 13.5 µm
- Every P+ diffusion is capacitively coupled to the N-well
  - Source of unwanted cross-talk

Future steps - possible optimisations

- Replacement 2nd stage of the amplifier with a source follower inside the feedback loop:
  - Improved homogeneity between different pixels
  - 1 control voltage instead of 3
  - To be simulated and compared with the existing version
- Noise simulations
- Measurement of the capacitance of the Epoxy glue
  - Extraction of dielectric constant
  - More precise estimation of the coupling capacitance
- Test pulsing in one pixel at a time (S. Kulis)
- Power pulsing of the matrix (S. Kulis)
- Improvement (redesign) of slow control interface (S. Kulis)
- Submission in early 2016
  - Engineering run with high-resistivity substrate (100 Ωcm)



Thank you!