HSIO II Development Platform Users Guide

Revision 3

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Revision History

Date	Version	Revision
12/01/2015	3	Production C03 version board photo for Fig 2
11/04/2015	2	Full update for first hardware batch release
11/11/2015	1	Updated Figure 2
11/11/2014	0	Initial release

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Introduction

The High Speed Input Output II, (HSIO II), development board is intended to provide signal processing capability for ATLAS pixel and strip tracker test setups. The basic platform is the Advanced Telecommunications Computing Architecture, (ATCA) form factor but intended for a more portable standalone bench setup and not to reside in an ATCA shelf. An interface board generally accompanies the HSIO that attaches to the Zone 3 connectors. The interface board is basically a Rear Transition Module, (RTM), as defined in the ATCA standard. This interface board provides specific connectors and buffering required to interface to front end detector electronics. The general idea is for the HSIO board to be a standardized design for processing data from the front end. The interface board is a much simpler board which provides the required connectivity to specific front end electronics. There is no need for installing the HSIO into an ATCA crate.

Features

- Xilinx Virtex 7 Artix
- USB 2.0 interface chips (FTDI FT232H) with host and peripheral ports
- Text display
- 10/100/1000 Ethernet Mac-PHY transceiver
- Onboard power regulators for all necessary voltages
- Power indicator LED and dip switch
- Two SFP+ Gigabit fiber/copper interface cages
- One QSFP Gigabit fiber interface cage
- Micron Tech. platform flash configuration storage device
- Headers for general purpose Input / Output, (IO)
- SMA and LEMO signal banks
- Oscillators at 125MHz, 312.5MHz
- Data Transport/Data Processing Module as a mezzanine, (DTM)
- TTL interface mezzanine

Additional Information

- Full schematics in PDF format and ViewDraw schematic format
- PC board layout in Pads PCB format
- Gerber files in *.pho and *.pdf for the PC board (There are many free or shareware Gerber file viewers available on the internet for viewing and printing these files)
- Documentation for the HSIO II is located at the following link.

  http://www.slac.stanford.edu/~djn/Atlas/HSIO_II/

- Documentation for the DTM is located at the following link:

  https://confluence.slac.stanford.edu/display/AIRTRACK/PC_248_101_19_C02

Additional Resources

- To find additional documentation, see the Xilinx website at: http://www.xilinx.com/literature/index/htm.
  - Xilinx 7 Series FPGA Overview, DS180
  - Xilinx Artix 7 Overview, DS190
  - Xilinx 7 Series FPGA Packaging and Pin-out, UG475

Xilinx 7 Series Configuration User Guide, UG47

- To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

  http://www.xilinx.com/support.

  A link to ATCA is listed below.

- http://en.wikipedia.org/wiki/Advanced_Telecommunications_Computing_Architecture

Block Diagram

Figure 1 below shows a block diagram of the board.

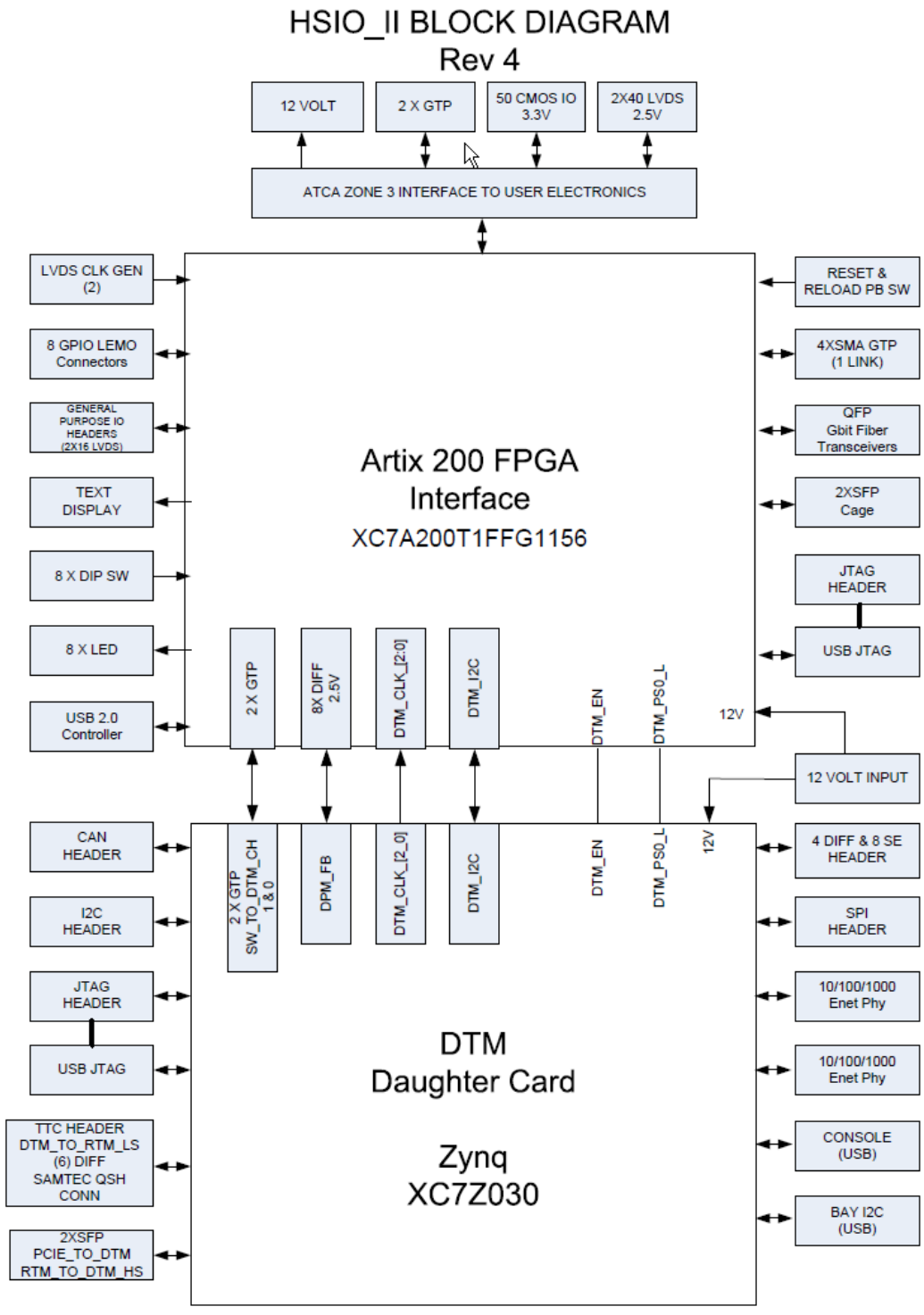

Figure 1 HSIO II Development Platform Block Diagram

Detailed Description

The HSIO II Development platform is shown in Figure 2.
These features/components are described in the subsequent sections of this document.

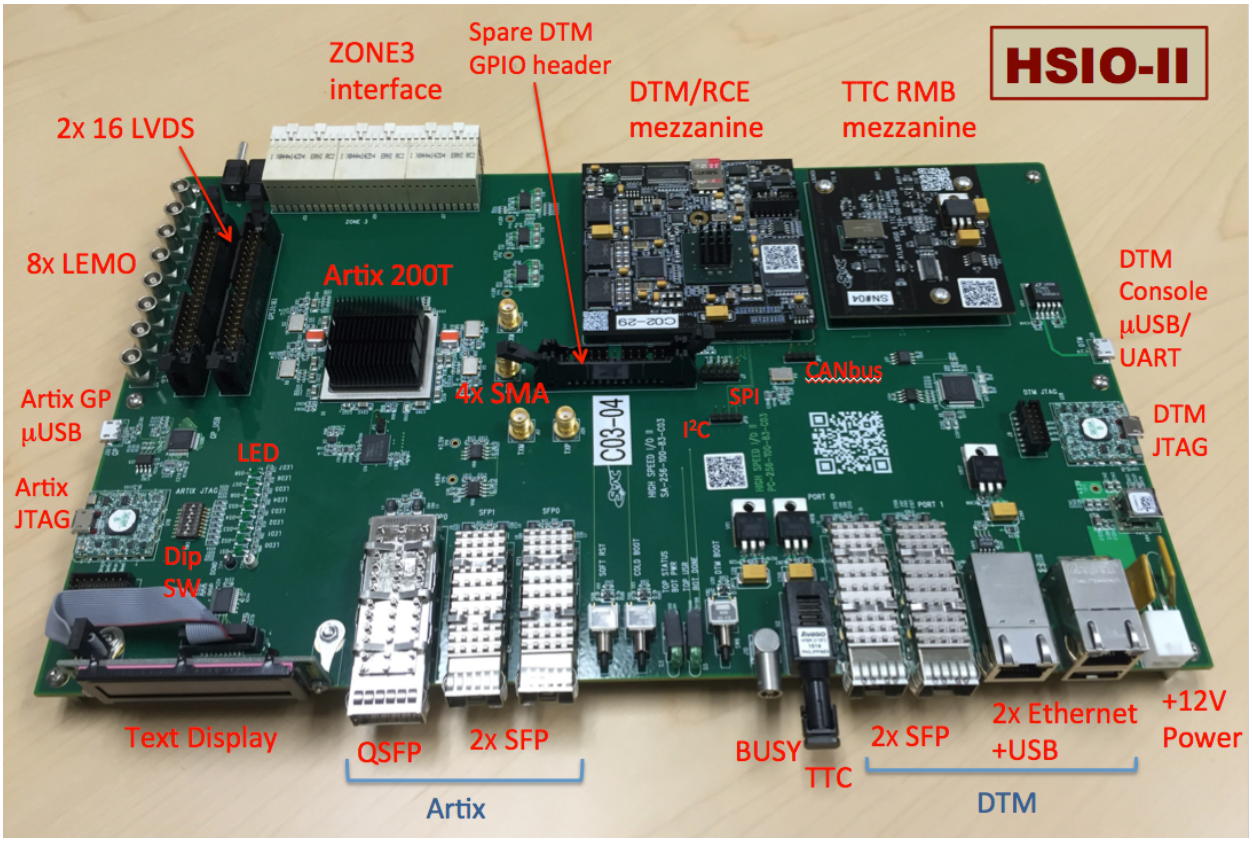

Figure 2 HSIO Development Platform (front view)

Xilinx Series 7, Artix FPGA

A Xilinx 7 series FPGA, XC7A200T is packaged in 1156 pin ball grid array.

Configuration

The board supports configuration in four modes: JTAG, Master Serial modes, Flash memory and direct *.bit FPGA load.

I/O Rails

The FPGA has 10 banks

Table 1: I/O Voltage Rail of FPGA Banks

FPGA Bank	I/O Voltage Rail
0	2.5V
12	3.3V
13	3.3V
14	2.5V
15	2.5V
16	3.3V
32	2.5V
33	2.5V
34	2.5V
35	2.5V
36	2.5V

Table 1 I/O Voltage Rail of FPGA Banks

Input Power Connector, Front right, JP2

The input power connector Molex Mini-Fit JR, type 5569 right angle PC mount, 4 pin connector. The input power requirement is +12V DC with at least 3.0Amp, which can be a typical 12V laptop supply. In case of very noise sensitive applications or heavy use of many MGTs, it is worth bearing in mind if a more heavy duty lab supply could serve the task better.

Pin Number	Value
1	+12V
2	+12V
3	RETURN
4	RETURN

Table 2 Power connector pin-out

Output Power Connectors

Output power is available on J2 and J3. These connectors are standard for the ATCA platform Rear Transition Module, (RTM). These connectors provide +12V DC up to 5 amperes. J2 is the return and J3 is the +12V DC power.

Power and FPGA Status Indicators

The lower LED of the two green LEDs indicates that the 3.3V is powered. The upper LED of the two is intended to be used for an FPGA status. The user must program this LED. Control of the status indicator is assigned to BANK 2, pin AJ20. Setting this pin to logic high will turn on this LED.

On-board Power Supplies

There are four groups of Power supply circuitry on the board. Refer to Figure 3 below.

(1) Output power is available on J2 and J3. These connectors are standard for the ATCA platform Rear Transition Module, (RTM). J2 and J3 provide +12V DC at 5 amperes. J2 is the return and J3 is the +12V DC power.

(2) The second group is the FPGA power, 3.3V, 2.5V, 1.8V, and 1.0V. The 3.3V and 1.0V are generated using switcher supplies. The 2.5V and 1.8V are linear regulators.

(3) The third group is the DTM module that generates 6.0V and uses the 3.3V power as well.

(4) The fourth group provides power to the high speed links, (GBTs). 1.2V and 1.0V supplies are switcher type located near the bottom of Zone 3 connectors.

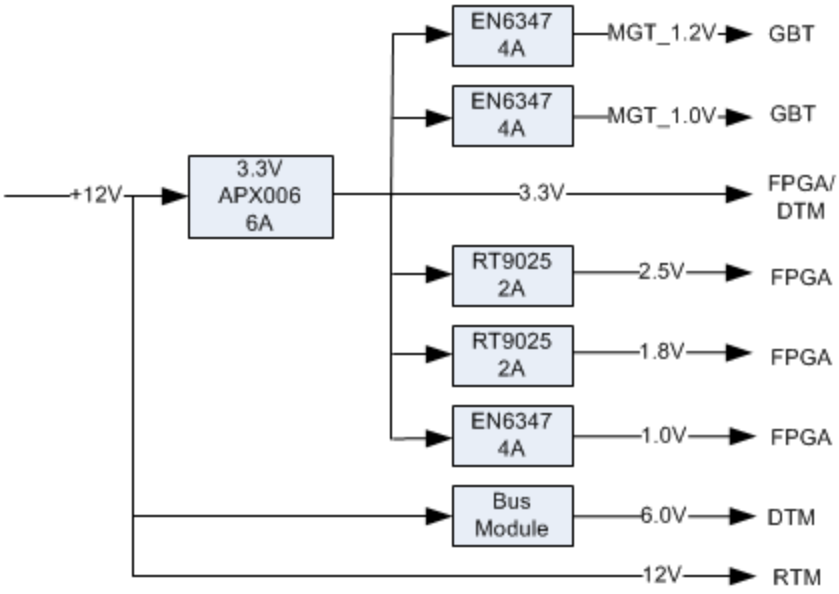

Figure 3 Power Supply Diagram

Oscillators

The HSIO II Development Platform has four crystal oscillators. Two oscillators feed the GTP bank 113, X3 and X9. X3 is a 250MHz oscillator and X9 is a 312.5MHz oscillator which is not normally loaded. Two oscillators feed the GTP bank 116, X5 and X10. X5 is a 250MHz oscillator and X10 is a 312.5MHz oscillator which is not normally loaded.

Artix, U1, Boot Push-Button Switches

There are two HSIO II boot switches, SW4 and SW5 located on the front panel. SW4 is used to reload the ARTIX FPGA, U1 from the Flash memory, (U14). SW5 is used to load the flash memory U14 and load U1 FPGA from the JTAG interface.

DTM, Boot Push-Button Switch

There is one switch, SW6, located on the front panel that sends a signal to the Artix FPGA, U1. U1 in turn generates the required I^2C signals which instruct the DTM to boot. The DTM boot SW6 connects to, (U1) pin G34. An external pull-up resistor is implemented.

User Dip Switch

SW3 is an eight position DIP switch, which are general purpose. The pins must be programmed with pull-up resistors in the pin definition file.

Switch Signal	FPGA Pin
DIP_SW0	AN6
DIP_SW1	AN9
DIP_SW2	AP9
DIP_SW3	AJ10
DIP_SW4	AK10
DIP_SW5	AP11
DIP_SW6	AP10
DIP_SW7	AL9

Table 3 Eight position DIP Switch Pin assignment

Artix, U1, Boot status LEDs

Two stacked LEDs provide the Artix status. The lower LED indicates that the 3.3V supply is on. The upper LED indicates the Artix FPGA boot status.

DTM, Boot status LED

There is one blue LED located near the front edge of the DTM that indicates the status of the DTM.

User LEDs

There are eight green LEDs, DS1-DS8, which are general purpose. The LEDs are lit using positive logic from U1 bank 32. The table below provides the LED name, signal name and pin-out.

LED Name	Switch Signal	FPGA Pin
LED0	LED0	AM9
LED1	LED1	AM11
LED2	LED2	AN11
LED3	LED3	AJ11
LED4	LED4	AK11
LED5	LED5	AL10
LED6	LED6	AM10
LED7	LED7	AL8

Table 4 Eight position LED Pin assignment

Artix FPGA Configuration

Two options exist for configuring the Artix FPGA, U1.

(1) The standard 14 pin header dongle interface, J32.

(2) USB JTAG interface U16 which is a Digilent JTAG SMT2 module. Please refer to the following link.
http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,395,1053&Prod=JTAG-SMT2

DTM FPGA Configuration

Three options exist for configuring the DTM FPGA.

(1) The standard 14 pin header dongle interface, J9.
(2) USB JTAG interface U28 which is a Digilent JTAG SMT2 module. Please refer to the following link.
http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,395,1053&Prod=JTAG-SMT2

(3) The DTM has an on-board SD card which stores the configuration.

USB 2.0 Port

The FT2232H, U26, with μUSB port J30, is a single channel USB 2.0 High Speed (480Mb/s) to UART/FIFO IC. Refer to the link below for configuring the port. The USB 2.0 port has a dedicated 12.0MHz crystal clock. Also an EEPROM is provided to give unique serial port numbers. The EEPROM is a Microchip 93LC46. Refer to FTDI web site for complete information.

http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT232H.pdf

Signal Name	FPGA Pin – BANK 16
USB1_A_D0	L23
USB1_A_D1	M24
USB1_A_D2	L24
USB1_A_D3	K23
USB1_A_D4	J23
USB1_A_D5	G24
USB1_A_D6	G25
USB1_A_D7	K25
USB1_A_RXF – LOW TRUE	J25
USB1_A_TXE – LOW TRUE	M25
USB1_A_RD – LOW TRUE	L25
USB1_A_WR – LOW TRUE	J24
USB1_A_SIWUA	H24

USB1_A_CLKOUT	L28
USB1_A_OE – LOW TRUE	K28
ACBUS7	J28
ACBUS8	H28
ACBUS9	J29

Table 5 USB 2.0 FPGA Pin-out

SFP+ Transceivers, Fiber/Copper

Two SFP+ interface module cages, U9 and U21 are provided. The recommended transceivers are AFBR-57R6AEZ from AVAGO Technologies.

http://www.avagotech.com/pages/en/fiber_optics/storage/4g_fibre_channel/afbr-57r6apz/

These devices interface to the Xilinx GTPs. The small form-factor pluggable (SFP) is a compact, hot-pluggable transceiver. It interfaces a network device motherboard to a fiber optic or copper networking cable. It is a popular industry format supported by many network component vendors.

Refer to the following link http://en.wikipedia.org/wiki/Small_form-factor_pluggable_transceiver

Below is a table of the pin-out interface between the FPGA and the SFP+ transceivers.

Bank	Signal Name Transceiver	Signal Name Xilinx	FPGA Pin
12	MOD1-SCL	SFP1_MOD1	AN33

12	MOD2-SDA	SFP1_MOD2	AP33
113	RD+	SFP1_RX_P	AJ13
113	RD-	SFP1_RX_M	AK13
113	TD+	SFP1_TX_P	AN13
113	TD-	SFP1_TX_M	AP13

Table 6 SFP+ Transceiver, U9, to FPGA Pin-out

Bank	Signal Name Transceiver	Signal Name Xilinx	FPGA Pin
12	MOD1-SCL	SFP0_MOD1	AN33
12	MOD2-SDA	SFP0_MOD2	AP33
113	RD+	SFP0_RX_P	AJ15
113	RD-	SFP0_RX_M	AK15
113	TD+	SFP0_TX_P	AL14
113	TD-	SFP0_TX_M	AM14

Table 7 SFP+ Transceiver, U21, to FPGA Pin-out

QSFP InfiniBand 4X QDR, QSFP Pluggable, Parallel Fiber-Optics Module

Description

The Avago Technologies AFBR-79Q4Z, U27, is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP Transceiver for QDR InfiniBand and proprietary applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnect applications. It integrates four data lanes in each direction with 40 Gbps aggregate bandwidth. QSFP can pass/drive 10Gbit but Artix only has GTP of 6-7Gbits/s. Each lane can operate at 10 Gbps up to 100 m using OM3 fiber. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 38-contact edge type connector. The optical interface uses an 8 or 12 fiber MTP® (MPO) connector. This module incorporates Avago Technologies proven integrated circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

Below is a table of the pin-out interface between the FPGA and the SFP+ transceivers.

Bank	Signal Name Transceiver	Signal Name Xilinx	FPGA Pin
12	SCL	QSFP_SCL0	AJ24
12	SDA	QSFP_SDA0	AL34
12	/RESET	QSFP_RST0	AM34
12	/MOD_SEL	QSFP_SEL0	AJ33
12	/INT	QSFP_INT0	AJ34
12	/MOD_PRS	QSFP_PRS0	AN34
12	LP_MODE	QSFP_LP0	AP34
213	TX1P	PGP0_TX_P	AN19
213	TX1N	PGP0_TX_M	AP19
213	RX1P	PGP0_RX_P	AL18
213	RX1N	PGP0_RX_M	AM18
213	TX2P	PGP1_TX_P	AN21
213	TX2N	PGP1_TX_M	AP21
213	RX2P	PGP1_RX_P	AJ19
213	RX2N	PGP1_RX_M	AK19
213	TX3P	PGP2_TX_P	AL22
213	TX3N	PGP2_TX_M	AM22
213	RX3P	PGP2_RX_P	AL20
213	RX3N	PGP2_RX_M	AM20
213	TX4P	PGP3_TX_P	AN23
213	TX4N	PGP3_TX_M	AP23
213	RX4P	PGP3_RX_P	AJ21
213	RX4N	PGP3_RX_M	AK21

Table 8 QFP+ Transceiver, U27, to FPGA Pin-out

GTP to SMA high speed link

One GTP link is interfaced to four SMA connectors, J17-J20, located on the main board.

Bank	Signal Name Transceiver	Connector	FPGA Pin
13	SMA_TX_P	J20	AN17
13	SMA_TX_M	J17	AP17
13	SMA_RX_P	J18	AJ17
13	SMA_RX_M	J19	AK17

Table 9 GBT Transceiver, J17-20, to FPGA Pin-out

Text Display

A NEWHAVEN DISPLAY is provided on the front panel, part number NHD-0220FZ-FSW-GBW-P-33V3. The link to the product is below.

http://www.newhavendisplay.com/nhd0220fzfswgbwp33v3-p-5161.html

The display is a 2x20 Character display, 3.3 VDD STN-GRAY, WHITE LED B/L 3V.

The display is driven by a 16-bit I^2C controller, PCA9535.

http://www.ti.com/lit/ds/symlink/pca9535.pdf

The I^2C control interface is on Artix FPGA bank 16. Table 16 provides the pin assignment. VHDL code for controlling the display is provided upon request.

BANK	Signal Name	FPGA Pin
16	FP_INIT	H31
16	FP_SDA	L34
16	FP_SCL	M26

Table 10 Front Panel Character Displays

General Purpose LEMO Connectors

Eight general purpose LEMO connectors are provided to users for functions such as triggers and interrupts. Bank 12 is hard wired to +3.3V. Bank 14 is hard wired to +2.5V.

BANK	Ref Designator	Signal Name	FPGA Pin
12	J21	LEMO_1	AL30
12	J22	LEMO _2	AM30
12	J23	LEMO _3	AL28
12	J24	LEMO _4	AL29
14	J29	LEMO _5	Y31
14	J28	LEMO _6	AA30
14	J33	LEMO _7	AB30
14	J34	LEMO _8	AB31

Table 11 LEMO Connector IO

Zone 3 IO Connections

There are three ATCA Zone 3 connectors, J25-J27, for user interface. Table 7 below shows the pin-out for J25 which consists of the four separate groups. The first group is for four Giga-bit/s fiber interfaces. The second group is a set of four LVDS global clock pairs. The third group is 80 LVDS pair signals.

BANK	FPGA Pin No.	Signal Name	Connector Pin No.		FPGA Pin No.	Signal Name
216	B23	RTM0_TX_P	J25-A1	J25-B1	A23	RTM0_TX_M
216	F21	RTM0_RX_P	J25-C1	J25-D1	E21	RTM0_RX_M
216	D22	RTM1_TX_P	J25-E1	J25-F1	C22	RTM1_TX_M
216	D20	RTM1_RX_P	J25-G1	J25-H1	C20	RTM1_RX_M
13	AD23	GPIO_0	J25-A3	J25-B3	AF34	GPIO_1
13	AG34	GPIO_2	J25-C3	J25-D3	AD33	GPIO_3
13	AD34	GPIO_4	J25-E3	J25-F3	AH33	GPIO_5
13	AH34	GPIO_6	J25-G3	J25-H3	AE33	GPIO_7
13	AF33	GPIO_8	J25-A4	J25-B4	AG32	GPIO_9
13	AH32	GPIO_10	J25-C4	J25-D4	*AE32*	GPIO_11
13	AF32	GPIO_12	J25-E4	J25-F4	AD31	GPIO_13
13	AE31	GPIO_14	J25-G4	J25-H4	AD30	GPIO_15
13	AE30	GPIO_16	J25-A5	J25-B5	AD28	GPIO_17
13	AD29	GPIO_18	J25-C5	J25-D5	AG31	GPIO_19
13	AH31	GPIO_20	J25-E5	J25-F5	AF29	GPIO_21
13	AF30	GPIO_22	J25-G5	J25-H5	AG29	GPIO_23
13	AG30	GPIO_24	J25-A6	J25-B6	AH28	GPIO_25
13	AH29	GPIO_26	J25-C6	J25-D6	AE28	GPIO_27
13	AF28	GPIO_28	J25-E6	J25-F6	AD26	GPIO_29

13	AE26	GPIO_30	J25-G6	J25-H6	AC26	GPIO_31
13	AC27	GPIO_32	J25-A7	J25-B7	AG27	GPIO_33
13	AH27	GPIO_34	J25-C7	J25-D7	AE27	GPIO_35
13	AF27	GPIO_36	J25-E7	J25-F7	AG26	GPIO_37
13	AH26	GPIO_38	J25-G7	J25-H7	AE23	GPIO_39
13	AF23	GPIO_40	J25-A8	J25-B8	AG24	GPIO_41
13	AH24	GPIO_42	J25-C8	J25-D8	AC24	GPIO_43
13	AD24	GPIO_44	J25-E8	J25-F8	AF25	GPIO_45
13	AG25	GPIO_46	J25-G8	J25-H8	AD25	GPIO_47
13	AE25	GPIO_48	J25-A9	J25-B9	AF24	GPIO_49
12	AL28	GC_IO_0_P	J25-A10	J25-B10	AL29	GC_IO_0_M
12	AJ28	GC_IO_1_P	J25-C10	J25-D10	AK28	GC_IO_1_M
12	AP29	GC_IO_2_P	J25-E10	J25-F10	AP30	GC_IO_2_M
12	AM29	GC_IO_3_P	J25-G10	J25-H10	AN29	GC_IO_3_M

Table 12 Zone 3 J25 Connector and FPGA Pin-out

BANK	FPGA Pin No.	Signal Name	Connector Pin No.		Signal Name	FPGA Pin No.
33	AG1	J26_LVDS_0_P	J26-A1	J26-B1	J26_LVDS_0_M	AH1
33	AD1	J26_LVDS_1_P	J26-C1	J26-D1	J26_LVDS_1_M	AE1
33	AH2	J26_LVDS_2_P	J26-E1	J26-F1	J26_LVDS_2_M	AJ1
33	AE2	J26_LVDS_3_P	J26-G1	J26-H1	J26_LVDS_3_M	AF2
33	AF3	J26_LVDS_4_P	J26-A2	J26-B2	J26_LVDS_4_M	AG2
33	AH3	J26_LVDS_5_P	J26-C2	J26-D2	J26_LVDS_5_M	AJ3
33	AF4	J26_LVDS_6_P	J26-E2	J26-F2	J26_LVDS_6_M	AG4
33	AD5	J26_LVDS_7_P	J26-G2	J26-H2	J26_LVDS_7_M	AD4
33	AH4	J26_LVDS_8_P	J26-A3	J26-B3	J26_LVDS_8_M	AJ4
33	AD3	J26_LVDS_9_P	J26-C3	J26-D3	J26_LVDS_9_M	AE3
33	AG6	J26_LVDS_10_P	J26-E3	J26-F3	J26_LVDS_10_M	AG5
33	AE5	J26_LVDS_11_P	J26-G3	J26-H3	J26_LVDS_11_M	AF5
33	AD6	J26_LVDS_12_P	J26-A4	J26-B4	J26_LVDS_12_M	AE6
33	AF7	J26_LVDS_13_P	J26-C4	J26-D4	J26_LVDS_13_M	AG7
33	AD9	J26_LVDS_14_P	J26-E4	J26-F4	J26_LVDS_14_M	AD8
33	AE8	J26_LVDS_15_P	J26-G4	J26-H4	J26_LVDS_15_M	AE7
33	AH7	J26_LVDS_16_P	J26-A5	J26-B5	J26_LVDS_16_M	AH6
33	AF9	J26_LVDS_17_P	J26-C5	J26-D5	J26_LVDS_17_M	AF8
33	AH9	J26_LVDS_18_P	J26-E5	J26-F5	J26_LVDS_18_M	AH8
33	AF12	J26_LVDS_19_P	J26-G5	J26-H5	J26_LVDS_19_M	AG12
34	W10	J26_LVDS_20_P	J26-A6	J26-B6	J26_LVDS_20_M	Y10
34	V9	J26_LVDS_21_P	J26-C6	J26-D6	J26_LVDS_21_M	V8
34	W9	J26_LVDS_22_P	J26-E6	J26-F6	J26_LVDS_22_M	W8
34	V7	J26_LVDS_23_P	J26-G6	J26-H6	J26_LVDS_23_M	V6
34	Y8	J26_LVDS_24_P	J26-A7	J26-B7	J26_LVDS_24_M	Y7
34	W6	J26_LVDS_25_P	J26-C7	J26-D7	J26_LVDS_25_M	Y6

34	W1	J26_LVDS_26_P	J26-E7	J26-F7	J26_LVDS_26_M	Y1
34	V2	J26_LVDS_27_P	J26-G7	J26-H7	J26_LVDS_27_M	V1
34	Y3	J26_LVDS_28_P	J26-A8	J26-B8	J26_LVDS_28_M	Y2
34	V3	J26_LVDS_29_P	J26-C8	J26-D8	J26_LVDS_29_M	W3
34	V4	J26_LVDS_30_P	J26-E8	J26-F8	J26_LVDS_30_M	W4
34	W5	J26_LVDS_31_P	J26-G8	J26-H8	J26_LVDS_31_M	Y5
34	AA5	J26_LVDS_32_P	J26-A9	J26-B9	J26_LVDS_32_M	AA4
34	AB5	J26_LVDS_33_P	J26-C9	J26-D9	J26_LVDS_33_M	AB4
34	AB2	J26_LVDS_34_P	J26-E9	J26-F9	J26_LVDS_34_M	AB1
34	AA3	J26_LVDS_35_P	J26-G9	J26-H9	J26_LVDS_35_M	AA2
34	AC2	J26_LVDS_36_P	J26-A10	J26-B10	J26_LVDS_36_M	AC1
34	AC4	J26_LVDS_37_P	J26-C10	J26-D10	J26_LVDS_37_M	AC3
34	AA8	J26_LVDS_38_P	J26-E10	J26-F10	J26_LVDS_38_M	AA7
34	AC7	J26_LVDS_39_P	J26-G10	J26-H10	J26_LVDS_39_M	AC6

Table 13 Zone 3 J26 Connector and FPGA Pin-out

BANK	FPGA Pin No.	Signal Name	Connector Pin No.		Signal Name	FPGA Pin No.
35	M7	J27_LVDS_0_P	J27-A1	J27-B1	J27_LVDS_0_M	M6
35	N9	J27_LVDS_1_P	J27-C1	J27-D1	J27_LVDS_1_M	M9
35	N8	J27_LVDS_2_P	J27-E1	J27-F1	J27_LVDS_2_M	N7
35	W11	J27_LVDS_3_P	J27-G1	J27-H1	J27_LVDS_3_M	M10
35	P9	J27_LVDS_4_P	J27-A2	J27-B2	J27_LVDS_4_M	P8
35	P6	J27_LVDS_5_P	J27-C2	J27-D2	J27_LVDS_5_M	N6
35	N1	J27_LVDS_6_P	J27-E2	J27-F2	J27_LVDS_6_M	M1
35	M5	J27_LVDS_7_P	J27-G2	J27-H2	J27_LVDS_7_M	M4
35	R1	J27_LVDS_8_P	J27-A3	J27-B3	J27_LVDS_8_M	P1
35	N3	J27_LVDS_9_P	J27-C3	J27-D3	J27_LVDS_9_M	N2
35	P4	J27_LVDS_10_P	J27-E3	J27-F3	J27_LVDS_10_M	P3
35	P5	J27_LVDS_11_P	J27-G3	J27-H3	J27_LVDS_11_M	N4
35	R6	J27_LVDS_12_P	J27-A4	J27-B4	J27_LVDS_12_M	R5
35	T5	J27_LVDS_13_P	J27-C4	J27-D4	J27_LVDS_13_M	T4
35	R3	J27_LVDS_14_P	J27-E4	J27-F4	J27_LVDS_14_M	R2
35	U2	J27_LVDS_15_P	J27-G4	J27-H4	J27_LVDS_15_M	U1
35	T3	J27_LVDS_16_P	J27-A5	J27-B5	J27_LVDS_16_M	T2
35	U5	J27_LVDS_17_P	J27-C5	J27-D5	J27_LVDS_17_M	U4
35	R8	J27_LVDS_18_P	J27-E5	J27-F5	J27_LVDS_18_M	R7
35	R10	J27_LVDS_19_P	J27-G5	J27-H5	J27_LVDS_19_M	P10
35	L12	J27_LVDS_20_P	J27-A6	J27-B6	J27_LVDS_20_M	K12
35	G10	J27_LVDS_21_P	J27-C6	J27-D6	J27_LVDS_21_M	G9
35	K11	J27_LVDS_22_P	J27-E6	J27-F6	J27_LVDS_22_M	J11
35	H11	J27_LVDS_23_P	J27-G6	J27-H6	J27_LVDS_23_M	G11
35	L10	J27_LVDS_24_P	J27-A7	J27-B7	J27_LVDS_24_M	L9
35	K10	J27_LVDS_25_P	J27-C7	J27-D7	J27_LVDS_25_M	J10

35	J9	J27_LVDS_26_P	J27-E7	J27-F7	J27_LVDS_26_M	J8
35	H9	J27_LVDS_27_P	J27-G7	J27-H7	J27_LVDS_27_M	H8
35	L8	J27_LVDS_28_P	J27-A8	J27-B8	J27_LVDS_28_M	K8
35	G7	J27_LVDS_29_P	J27-C8	J27-D8	J27_LVDS_29_M	G6
35	K7	J27_LVDS_30_P	J27-E8	J27-F8	J27_LVDS_30_M	K6
35	H7	J27_LVDS_31_P	J27-G8	J27-H8	J27_LVDS_31_M	H6
35	G5	J27_LVDS_32_P	J27-A9	J27-B9	J27_LVDS_32_M	G4
35	J6	J27_LVDS_33_P	J27-C9	J27-D9	J27_LVDS_33_M	J5
35	F3	J27_LVDS_34_P	J27-E9	J27-F9	J27_LVDS_34_M	F2
35	L5	J27_LVDS_35_P	J27-G9	J27-H9	J27_LVDS_35_M	K5
35	H4	J27_LVDS_36_P	J27-A10	J27-B10	J27_LVDS_36_M	H3
35	J4	J27_LVDS_37_P	J27-C10	J27-D10	J27_LVDS_37_M	J3
35	L4	J27_LVDS_38_P	J27-E10	J27-F10	J27_LVDS_38_M	L3
35	H2	J27_LVDS_39_P	J27-G10	J27-H10	J27_LVDS_39_M	G2

Table 14 Zone 3 J27 Connector and FPGA Pin-out

General Purpose IO Connections

There are two general purpose IO connectors. The signals can be either LVDS or CMOS. Bank 32, 33, 34, 35, 36 are set to 2.5V. The connector is a standard 40 pin vertical ribbon cable connector with pin spacing of 0.1 inch.

Table 14 below shows the pin-out for P2. SP2 and SP6 are special purpose test points that the user can use for feeding power into the attached cable.

BANK	FPGA Pin No.	Signal Name	Connector Pin No.		Signal Name	FPGA Pin No.
33	AG10	GP_LVDS_0_P	P2-1	P2-2	GP_LVDS_0_M	AG9
33	AD11	GP_LVDS_1_P	P2-3	P2-4	GP_LVDS_1_M	AE11
33	AG11	GP_LVDS_2_P	P2-5	P2-6	GP_LVDS_2_M	AH11
33	AD10	GP_LVDS_3_P	P2-7	P2-8	GP_LVDS_3_M	AE10
		DGND	P2-9	P2-10	DGND	
34	AB7	GP_LVDS_4_P	P2-11	P2-12	GP_LVDS_4_M	AB6
34	AC9	GP_LVDS_5_P	P2-13	P2-14	GP_LVDS_5_M	AC8
34	AA10	GP_LVDS_6_P	P2-15	P2-16	GP_LVDS_6_M	AA9
34	AB10	GP_LVDS_7_P	P2-17	P2-18	GP_LVDS_7_M	AB9
		DGND	P2-19	P2-20	DGND	
35	U10	GP_LVDS_8_P	P2-21	P2-22	GP_LVDS_8_M	T10
35	U7	GP_LVDS_9_P	P2-23	P2-24	GP_LVDS_9_M	U6
35	T8	GP_LVDS_10_P	P2-25	P2-26	GP_LVDS_10_M	T7
35	U9	GP_LVDS_11_P	P2-27	P2-28	GP_LVDS_11_M	T9
		DGND	P2-29	P2-30	DGND	
36	K1	GP_LVDS_12_P	P2-31	P2-32	GP_LVDS_12_M	J1

36	H1	GP_LVDS_13_P	P2-33	P2-34	GP_LVDS_13_M	G1
36	M2	GP_LVDS_14_P	P2-35	P2-36	GP_LVDS_14_M	L2
36	K3	GP_LVDS_15_P	P2-37	P2-38	GP_LVDS_15_M	K2
		SP2	P2-39	P2-40	SP6	

Table 15 P2 General Purpose IO Connector

Table 22 below shows the pin-out for P3. SP3 and SP5 are special purpose test points that the user can use for feeding power into the attached cable.

BANK	FPGA Pin No.	Signal Name	Connector Pin No.		Signal Name	FPGA Pin No.
32	AN1	GP_LVDS_16_P	P3-1	P3-2	GP_LVDS_16_M	AP1
32	AK2	GP_LVDS_17_P	P3-3	P3-4	GP_LVDS_17_M	AK1
32	AM2	GP_LVDS_18_P	P3-5	P3-6	GP_LVDS_18_M	AN2
32	AL2	GP_LVDS_19_P	P3-7	P3-8	GP_LVDS_19_M	AM1
		DGND	P3-9	P3-10	DGND	
32	AN3	GP_LVDS_20_P	P3-11	P3-12	GP_LVDS_20_M	AP3
32	AK3	GP_LVDS_21_P	P3-13	P3-14	GP_LVDS_21_M	AL3
32	AN4	GP_LVDS_22_P	P3-15	P3-16	GP_LVDS_22_M	AP4
32	AJ5	GP_LVDS_23_P	P3-17	P3-18	GP_LVDS_23_M	AK5
		DGND	P3-19	P3-20	DGND	
32	AP6	GP_LVDS_24_P	P3-21	P3-22	GP_LVDS_24_M	AP5
32	AL4	GP_LVDS_25_P	P3-23	P3-24	GP_LVDS_25_M	AM4
32	AL5	GP_LVDS_26_P	P3-25	P3-26	GP_LVDS_26_M	AM5
32	AJ6	GP_LVDS_27_P	P3-27	P3-28	GP_LVDS_27_M	AK6
		DGND	P3-29	P3-30	DGND	
32	AK7	GP_LVDS_28_P	P3-31	P3-32	GP_LVDS_28_M	AL7
32	AM7	GP_LVDS_29_P	P3-33	P3-34	GP_LVDS_29_M	AM6
32	AJ8	GP_LVDS_30_P	P3-35	P3-36	GP_LVDS_30_M	AK8
32	AN8	GP_LVDS_31_P	P3-37	P3-38	GP_LVDS_31_M	AP8
		SP3	P3-39	P3-40	SP5	

Table 16 P3 General Purpose IO Connector

Data Transport Module (DTM)

The DTM is an optional pluggable module that provides on board CPU resources and TTC interface for the convenience of wider range of

applications. While the DTM has its own dedicated I/O ports of various kinds, there is also a communication bridge with substantial bandwidth between the HSIO II Artix FPGA and the Xilinix Zynq FPGA located on the DTM to share the processing and I/O resources on both sides. Refer to Figure 1.

Communication between the DTM and the Artix FPGA

DTM Present

The DTM sends a signal, “DTM_PS0_L”, to the Artix if the DTM is installed. This is a low true signal that is sensed on the Artix, Bank 15, pin R31, 2.5V CMOS input. The Artix responds by asserting the signal, ”DTM_EN_L”, which enables the DTM power.

DTM Reset

Two options are available to reset the DTM module. (1) A front panel USB port, U18, that can send the reset I^2C command. (2) The Artix FPGA can generate the I^2C reset command. This is selectable by four zero Ohm resistors, R103-R106.

Install R103, R104, and remove R105, R106 will select the USB port for configuring the DTM.

Install R105, R106, and remove R103, R104 will select the Artix interface, which is the default contract. The DTM is reset by the front panel switch, SW-6. The Artix senses this signal as low true, 3.3V CMOS input. The Artix, when sensing this signal low will initial an I^2C command that is sent to the DTM.

High speed links

Two high speed, multi Giga-bit, links between the Artix and Zynq FPGAs are provided.

Artix Interface			DTM Interface	
BANK	Signal Name	Artix FPGA Pin No.	Signal Name	DTM Connector Pin No.
116	HSIO_DTM0_TX_P	B13	HSIO_DTM0_TX_P	J8-1
116	HSIO_DTM0_TX_M	A13	HSIO_DTM0_TX_M	J8-3
116	HSIO_DTM0_RX_P	F13	HSIO_DTM0_RX_P	J8-2
116	HSIO_DTM0_RX_M	E13	HSIO_DTM0_RX_M	J8-4
116	HSIO_DTM1_TX_P	B13	HSIO_DTM1_TX_P	J8-5
116	HSIO_DTM1_TX_M	A13	HSIO_DTM1_TX_M	J8-7
116	HSIO_DTM1_RX_P	F13	HSIO_DTM1_RX_P	J8-6
116	HSIO_DTM1_RX_M	E13	HSIO_DTM1_RX_M	J8-8

Table 17 GTP High speed links

Low speed bus link

One bi-directional eight bit LVDS bus is provided between the Artix and Zynq FPGAs.

Artix Interface			DTM Interface	
BANK	Signal Name	Artix FPGA Pin No.	Signal Name	DTM Connector Pin No.
15	DTM0_FB_P	R26	DTM0_FB_P	J8-65
15	DTM0_FB_M	P26	DTM0_FB_M	J8-67
15	DTM1_FB_P	N26	DTM1_FB_P	J8-66
15	DTM1_FB_M	M27	DTM1_FB_M	J8-68
15	DTM2_FB_P	U25	DTM2_FB_P	J8-69
15	DTM2_FB_M	T25	DTM2_FB_M	J8-71
15	DTM3_FB_P	P24	DTM3_FB_P	J8-70
15	DTM3_FB_M	N24	DTM3_FB_M	J8-72
15	DTM4_FB_P	U26	DTM4_FB_P	J8-73
15	DTM4_FB_M	U27	DTM4_FB_M	J8-75
15	DTM5_FB_P	R25	DTM5_FB_P	J8-74
15	DTM5_FB_M	P25	DTM5_FB_M	J8-76
15	DTM6_FB_P	T27	DTM6_FB_P	J8-77
15	DTM6_FB_M	RR27	DTM6_FB_M	J8-79
15	DTM7_FB_P	N27	DTM7_FB_P	J8-78
15	DTM7_FB_M	N28	DTM7_FB_M	J8-80

Table 18 Eight bit LVDS Low speed bus

Clock Interface

One-three bit LVDS bus provides clocking synchronization between the DTM and the Artix FPGA.

Artix Interface			DTM Interface	
BANK	Signal Name	Artix FPGA Pin No.	Signal Name	DTM Connector Pin No.
15	DTM_CLK0_P	R30	DTM_CLK0_P	J8-49
15	DTM_CLK0_M	P30	DTM_CLK0_M	J8-51
15	DTM_CLK1_P	P28	DTM_CLK1_P	J8-50
15	DTM_CLK1_M	P29	DTM_CLK1_M	J8-52
15	DTM_CLK2_P	U29	DTM_CLK2_P	J8-53
15	DTM_CLK2_M	T29	DTM_CLK2_M	J8-55

Table 19 Three-bit Clock Interface

Communication between the DTM and external interfaces

Ethernet

Two Ethernet RJ-45 ports are provided on the front panel. These two ports are generated by the DTM module. BASE0 port connects to U17 RJ-45 and BASE1 connects to U18. Please refer to the DTM module user manual. The integrated 10/100/1000 gigabit Ethernet interface uses a Marvell 88E1111 transceiver.

CAN bus Header JP1

The CAN bus interface is a four pin header located on the main board. Pin 1 is “CAN_H”, pin 2 is “CAN_L”, and pins 3 and 4 are ground. The DTM interface is J8-10 for “CAN_H” and J8-12 for “CAN_L”. See link for more information

http://en.wikipedia.org/wiki/CAN_bus

I²C Header JP5

The I^2C interface is a three pin header located on the main board. Pin 3 is “SDA” pin 2 is “SCL”, pins 3 is ground. The DTM interface is J8-30 for “SDA” and J8-32 for “SCL”. See link for more information.

http://en.wikipedia.org/wiki/I%C2%B2C

Console USB

The console USB port of U19, with actual µUSB connection at J35, is used for the DTM Console UART signals. J8-22 is RX and J8-24 is TX of the DM connector J8. U19-16 provides CON_UART_TX and U19-17 provides interface to CON_UART_RX after U19 is properly programmed.

SPI Header J7

The SPI interface is a 10 pin header located on the main board.

http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus

SPI Header J7		DTM Interface J8	
PIN	Signal Name	Signal Name	DTM Connector Pin No.
1	SPI_OUT_MOSI	SPI_OUT_MOSI	J8-34
2	+3.3V		
3	GND		
4	SPI_OUT_SELECT0	SPI_OUT_SELECT0	J8-36
5	N/C		
6	SPI_OUT_SELECT1	SPI_OUT_SELECT1	J8-38
7	SPI_OUT_CLK	SPI_OUT_CLK	J8-33
8	SPI_OUT_SELECT2	SPI_OUT_SELECT2	J8-40
9	SPI_OUT_MISOI	SPI_OUT_MISOI	J8-35
10	GND		

Table 20 SPI Header Interface

2 Differential & 8 Single Ended signal header

Two differential LVDS signals and eight single ended CMOS 2.5V signals are provided on a 20 pin header P4. These signals have dedicated use when the DTM is running on a COB, but there is no corresponding need on HSIO-II so that these signals become available for general purpose use.

Header P4		DTM Interface J8	
PIN	Signal Name	Signal Name	DTM Connector Pin No.
1	GND		
2	GND		
3	BP_CLK0_IN	BP_CLK0_IN	J8-97
4	BP_CLK0_OUT	BP_CLK0_OUT	J8-98
5	BP_CLK1_IN	BP_CLK1_IN	J8-99

6	BP_CLK1_OUT	BP_CLK1_OUT	J8-100
7	BP_CLK2_IN	BP_CLK2_IN	J8-101
8	BP_CLK2_OUT	BP_CLK2_OUT	J8-102
9	BP_CLK3_IN	BP_CLK3_IN	J8-103
10	BP_CLK0_OUT	BP_CLK0_OUT	J8-104
11	GND		
12	GND		
13			
14			
15			
16			
17			
18			
19			
20			
21	DTM_IPM0_P	DTM_IPM0_P	J8-109
22	DTM_IPM1_P	DTM_IPM1_P	J8-110
23	DTM_IPM0_M	DTM_IPM0_M	J8-111
24	DTM_IPM1_M	DTM_IPM1_M	J8-112
25	GND		
26	GND		

Table 21 Header of spare differential and single ended signals to DTM.

SFP+ Transceivers, DTM Interface Fiber/Copper

Two SFP+ interface module cages, U10 and U11 are provided. The transceivers are AFBR-57R6AEZ from AVAGO Technologies.

http://www.avagotech.com/pages/en/fiber_optics/storage/4g_fibre_channel/afbr-57r6apz/

These devices interface to the Xilinx GTPs. The small form-factor pluggable (SFP) is a compact, hot-pluggable transceiver. It interfaces a network device motherboard to a fiber optic or copper networking cable. It is a popular industry format supported by many network component vendors.

Refer to the following link http://en.wikipedia.org/wiki/Small_form-factor_pluggable_transceiver

Below is a table of the pin-out interface between the FPGA and the SFP+ transceivers.

DTM J-8 Pin	Signal Name Transceiver	Signal Name Xilinx	FPGA Pin Artix Bank 12
	MOD1-SCL	DTM0_MOD1	AL32
	MOD2-SDA	DTM0_MOD2	AM32
J8-25	RD+	DTM0_RX_P	
J8-27	RD-	DTM0_RX_M	
J8-26	TD+	DTM0_TX_P	
J8-28	TD-	DTM0_TX_M	

Table 22 SFP+ Transceiver, U10, to DTM J8 Connector

DTM J-8 Pin	Signal Name Transceiver	Signal Name Xilinx	FPGA Pin Artix Bank 12
	MOD1-SCL	DTM1_MOD1	AJ31
	MOD2-SDA	DTM1_MOD2	AK32
J8-17	RD+	DTM1_RX_P	
J8-19	RD-	DTM1_RX_M	
J8-18	TD+	DTM1_TX_P	
J8-20	TD-	DTM1_TX_M	

Table 23 SFP+ Transceiver, U11, to DTM J8 Connector

Trigger & Timing Controller, (TTC), Interface

A TTC is implemented that is compatible with the current TTC in ATLAS detector. U2 is the fiber interface, HFBR-2119, and J10, LEMO connector, is the “BUSY” signal. The DTM interface is a daughter board which connects to J14, a Samtec QSH-020-01-F-D-DP-A-K, 40 pin header.