LAPP Electronics:

Evolution

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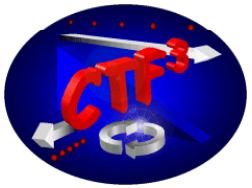
CERN - January 27th, 2009 - CTF3 Collaboration Technical meeting

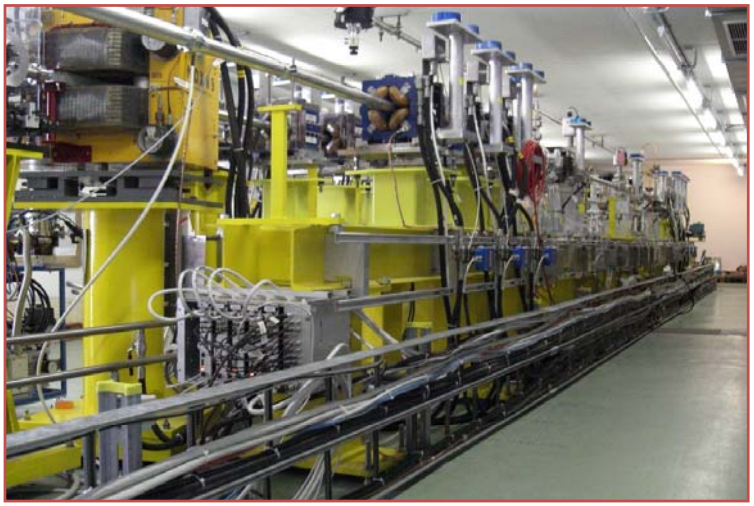


Today's schedule

- **Part1 : LAPP / CTF3 Installation**
  - Job done since last workshop
  - LAPP production
  - 2k9 Installation to be done with SP team
- **Part2 : LAPP / R&D research**
  - CLEX experiments & conclusions
  - Developments
  - Prototypes schedule

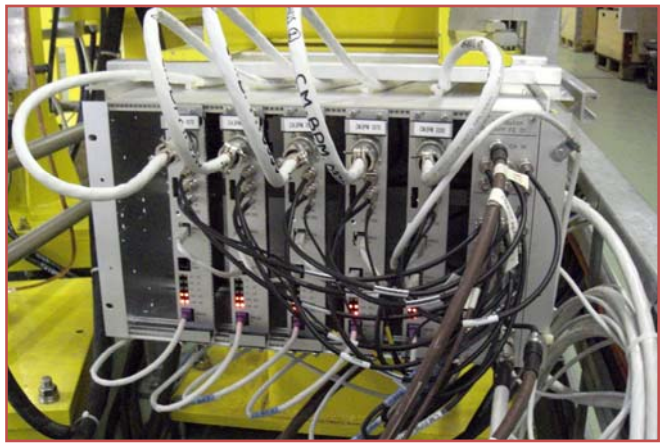
What is in CTF3 now ?!

- **47** Analog Modules
- **31** DFE boards / **8** Crates in CLEX-TL2 / Including all cables
  - ↳Started in 2008 spring
- **2** Frontend Servers



Under prod. and install

- **WHERE**
  - BP**S** acquisitions for **TBL** line
- **WHAT**
  - **15** DFE boards
  - **4** distribution boards
  - ↳**4** new crates
- **WHEN**
  - 1st week of April 09 ?
  - According to CTF3 project schedule



Under prod. and install

CTF3 - Shutdown 2008-2009 — 24.11.08

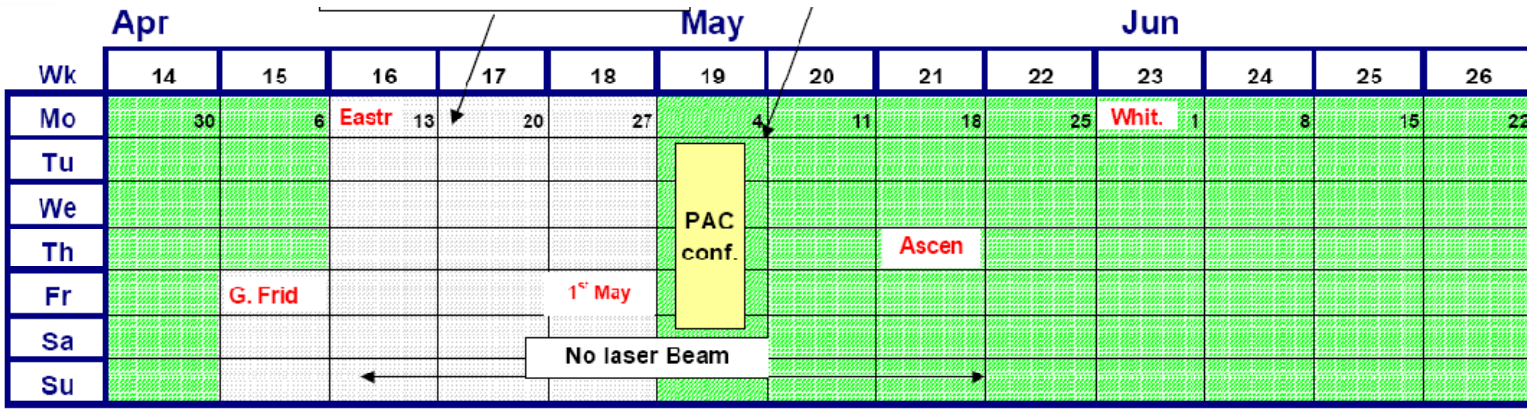
ID	Task Name	Duration
112		
113	TBL	1 day?
114	Install. Module prototype	1 day
115	Tracage geometres	1.5 days
116	Pose 8 poutres	8 days
117	Deplacement Dump	1 day
118	Tirage de cables ensemble elements	15 days
119	Delivery Q.	1 day
120	Install. 3 Q.+ table de reglage mover	2 days
121	Install. 13 Tables de reglage standart	3 days
122	Install. 13 Q.	3 days
123	Install. MTV	3 days
124	Connexion electrique elements	5 days
125	Alignement elements	5 days
126	Install. 16 BPS	5 days
127	Install. Vide	5 days
128	Install. Electr.BPS- LAPP/Barcelone	10 days
129		
130	Galerie	5 days
131	Pose alimentations PO	5 days

December 2008 | January 2009 | February 2009 | March 2009 | April 2009

49 50 51 52 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

01.12 08.12 15.12 22.12 29.12 05.01 12.01 19.01 26.01 02.02 09.02 16.02 23.02 02.03 09.03 16.03 23.03 30.03 06.04 13.04 20.04 27.04

19.02 19.02 | 26.01 27.01 | 27.01 06.02 | 07.01 07.01 | 23.02 13.03 | 23.02 | 24.02 25.02 | 26.02 02.03 | 03.03 05.03 | 06.03 10.03 | 11.03 17.03 | 18.03 24.03 | 25.03 31.03 | 01.04 07.04 | 01.04 14.04 | 16.02 20.02



Works with Spanish team

- **LAPP brings :**
  - **15** DFE board in 4 crates
- **SPANISH collaboration brings**
  - **15** BPS modules
  - **15** analog modules
- **To be defined with collaboration**
  - Production / Cabling analog links

46 Beam Position Signal Digitizers

+10% spares by April09

Fixed, and to be fixed

- **Hardware issue - “MARS” crate**
  - Signal integrity issue to be fixed during the next April shutdown
- **OASIS viewer Jitter problem**
  - Already fixed (?)
- **FESA processes crashes**
  - LAPP team working on / tests running now
- **Visualization background noise**
  - To be fixed by april09
- **LAPP Software optimizations for control**

LAPP R&D

- **Current developments**
  - Power Supplies and Calibration board
  - ADC Board : Optical linked evolution of DFE
  - Possible data processing on board
  - Network for data collection

Power Supplies and Calibration board

- **Autonomous 220Vac : relevant design issue for future CLIC architecture**
- **Linked to ADC board for timing**
- **Electric design simulations currently in progress**
- **Still to be discussed with the collaboration : amplitude and pulse length specs.**
- **Critical issues : radiations**

Pick a solution

	1st solution *Sept 2008*	2nd solution *Dec 2008*	3th solution *Jan 2009*
Tconv	**2** ns / 500 MHz	**5** ns / 200 MHz	**10** ns / 100 MHz
Res	12 bits	16 bits	16 bits
Dyn	2,0 Vpp	2,25 Vpp	2,25 Vpp

Powerless &
- 40% Price

Powerless &
- 20% Price

200 MHz or 100 MHz solutions easier to Implement & More reliable

2009/2010 Schedule

- **Specifications** to be confirmed
- 2 years dev: ~**3** men/year & ~**50k**€/year
- Labs prototypes – **Out Sept 2009**
- **Tests** in CTF3 accelerator foreseen
- Network study for **flexible** data collection (switch-like board)
- Possible **Acquisition Upgrade** for CTF3 (and CTF3+ ?) … if funding is approved and if it's working !!!

Thank you for your attention