Monolithic pixels for tracker upgrades

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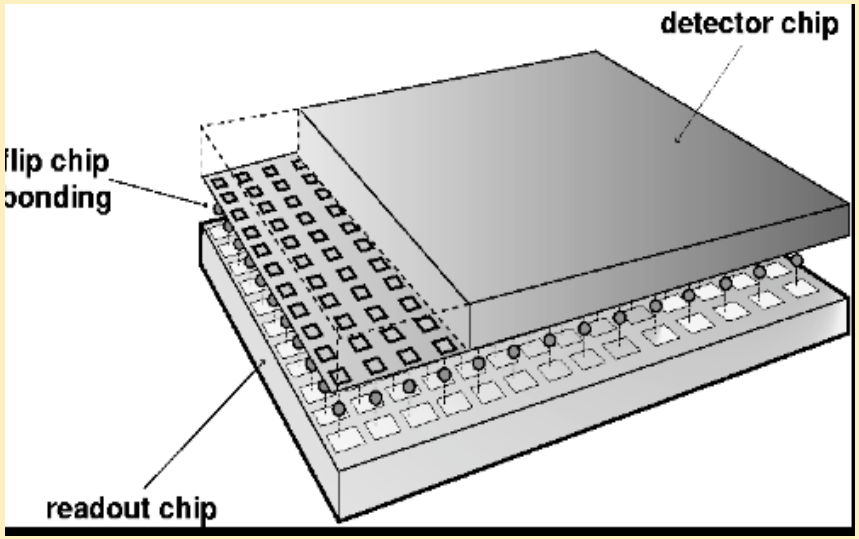
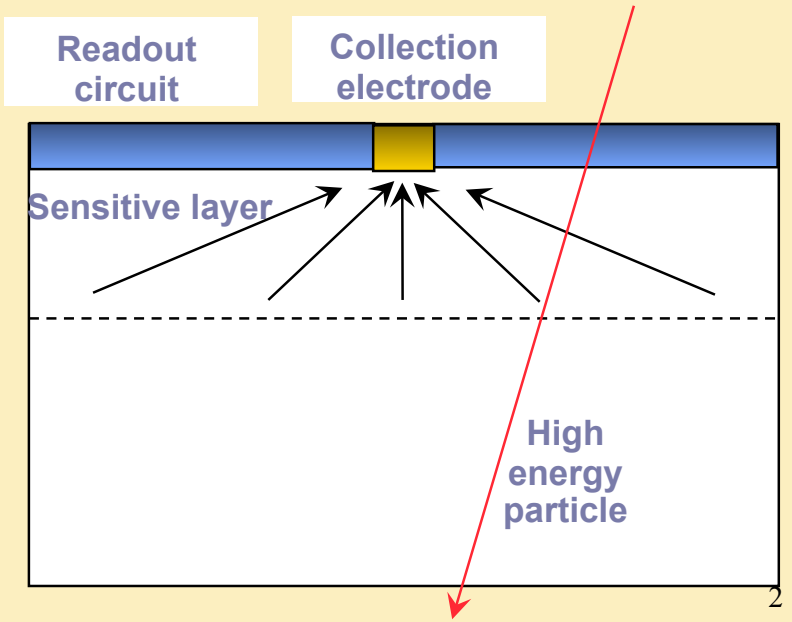
A monolithic detector in standard very deep submicron CMOS technology

- 'Traditional' monolithic detectors:
  - non-standard processing on very high resistivity substrate

  or
  - MAPS based with serial readout not necessarily compatible with future colliders, and with collection by diffusion very much affected by radiation damage
- Feedback from foundry that substrate sufficiently lowly doped is available in very deep submicron technologies (130 nm and beyond), 10 micron depletion no problem, strong perspectives to obtain more
- Is the first time there is an opportunity to integrate detector with very advanced standard CMOS





Monolithic in very deep submicron standard CMOS !

- Cost per unit area in production less than that of traditional silicon detectors
- Standard volume production (~ 20 square meter a day)
- Detector-readout connection automatically realized
- Low capacitance allows very favorable power – signal-to-noise ratios
- Very deep submicron allows power and speed advantages
- Allows innovative readout circuits
- Collection by drift (and higher doping level) will allow increased radiation tolerance

Very interesting for the LHC upgrades

Significant investment dominated by engineering run submissions
(90 nm or beyond !)

- Aiming for 10 mW per square cm or less with 100x100 micron elements for tracker upgrades
- Significant advantages beyond 130 nm (low k dielectrics in metallization)

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Very interesting for the LHC upgrades

Foundry proposed a way to obtain prototypes through MPW service

- Aiming for 10 mW per square cm or less with 100x100 micron elements for tracker upgrades
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Analog power

$$\text{Noise} \sim \frac{1}{\sqrt{gm}} \sim \frac{1}{I^{m}} \quad \text{where } m < 1/2 \qquad \text{Signal-to-Noise} \sim \frac{Q \times I^{m}}{C}$$

Weak dependence of the noise on current !

For constant signal to noise

Current I per channel :

$$I^{-m} \sim \frac{Q}{C} \quad \text{or} \quad I \sim (C/Q)^{2\ldots4}$$

Weak … Strong inversion

Segmentation

Number of elements N, C~1/N:

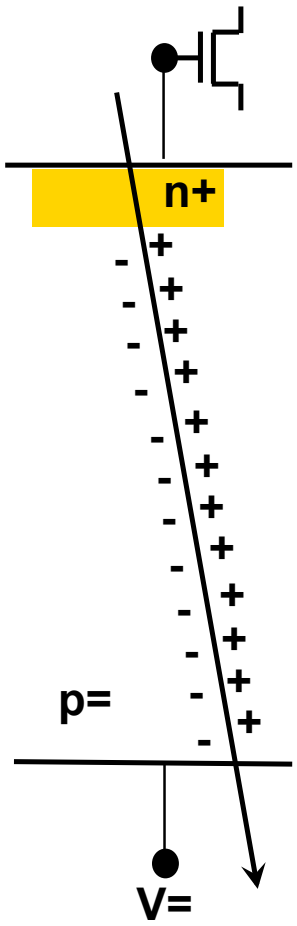
$$\text{Total analog Power} \sim N(C/Q)^{2\ldots4} \sim (1/N)^{1\ldots3}$$

Higher segmentation is (very) good

Decreased depletion layer thickness -> need to segment in proportion

Xd ÷ 2 -> C ÷ 2

Analog power



- 10 mW/cm^2 = 1 microW/(100x100 micron)
- Example: Basic element of 100x100 micron with 1 μA of current (so we split elements to optimize power to signal/noise ratio)
- Take transistor noise at 40 MHz BW

$$Veq \approx 0.16mV$$

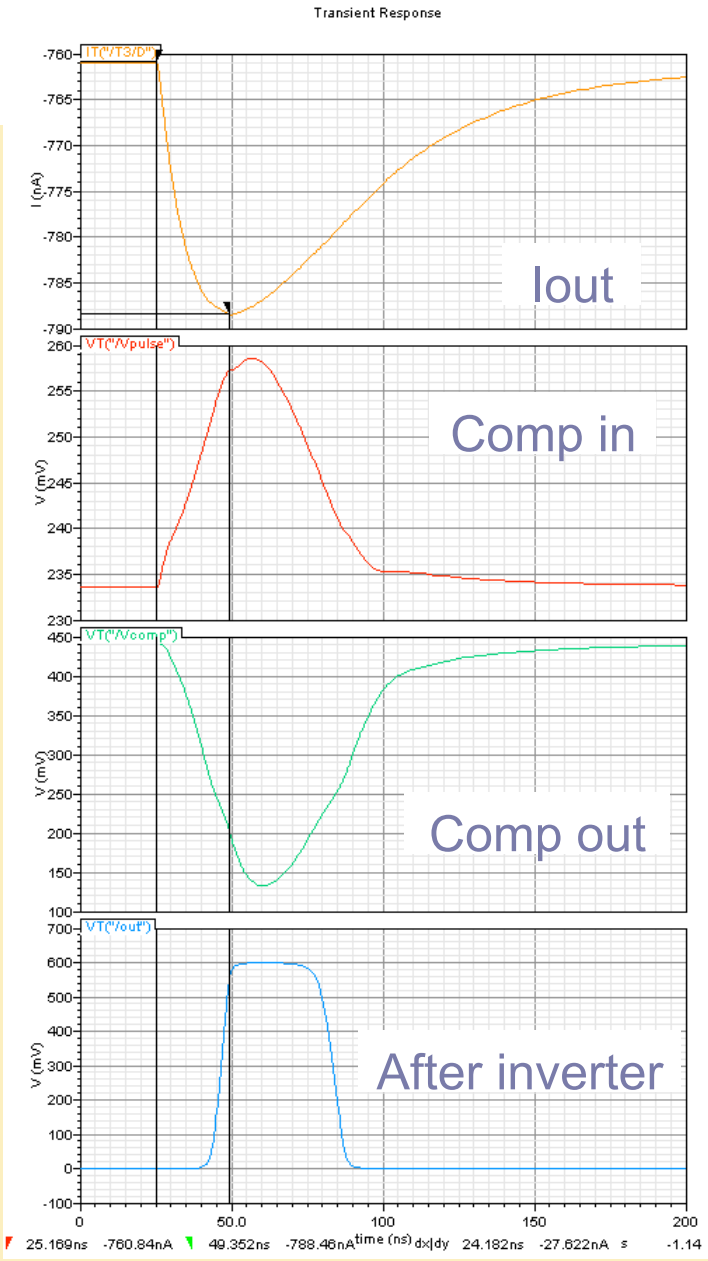
$$\frac{S}{N} = 25 \Rightarrow \frac{Q}{C} = 4mV \quad \boxed{= \frac{4\,fC}{1\,pF}} \quad \boxed{= \frac{0.4\,fC}{0.1\,pF}} \quad \boxed{= \frac{0.04\,fC}{10\,fF}}$$

Collection depth	**300 μm**	**30 μm**	**3 μm**

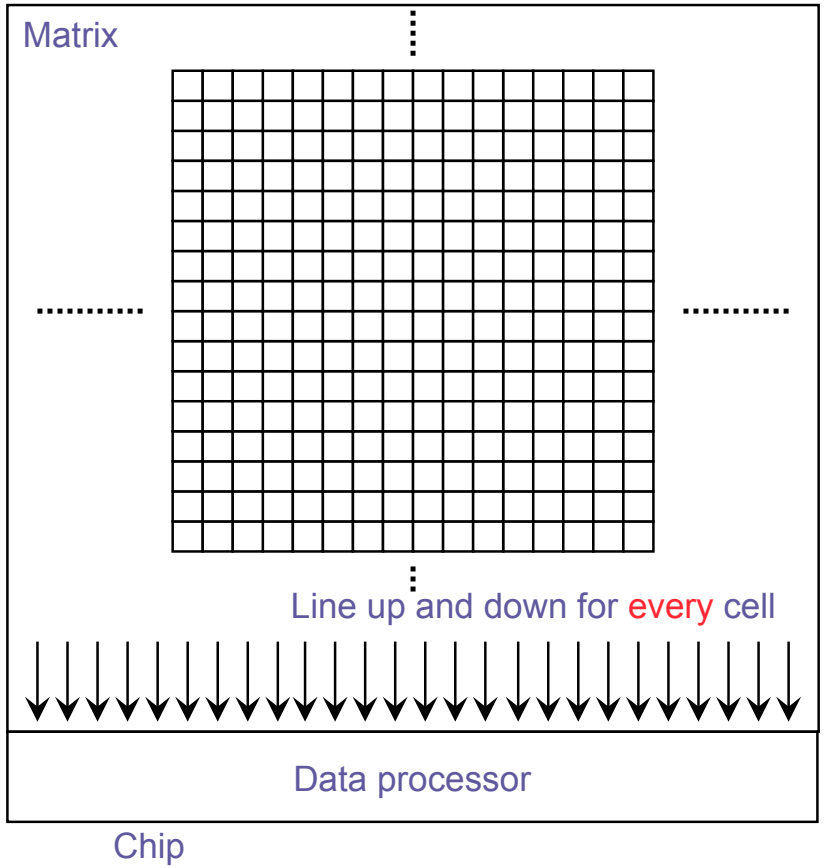
Could fit both monolithic and non-monolithic approach !

Front end for monolithic in 90nm

- 'Minimal' cell which sends current signal out: Use metal lines as capacitors in a current mode front end. Can have 10 000 elements per square cm (100 x 100 mm2 per element)
- Need fine metal pitch to create all the busses (one line per element !)
- Advantage: minimal activity/power consumption within matrix, but large data processor at the edge of the chip
- Simulations started:~ 900 nA for integrated amplifier – shaper + comparator
- Few modeling questions related to very deep submicron technology. Studied parasitic extraction to verify against measurements.
- Note: compared to present day pixel detectors important savings in power, but less S/N (maybe some of this can be recovered, depends on Q/C finally achieved)



Save analog power, how about digital ?

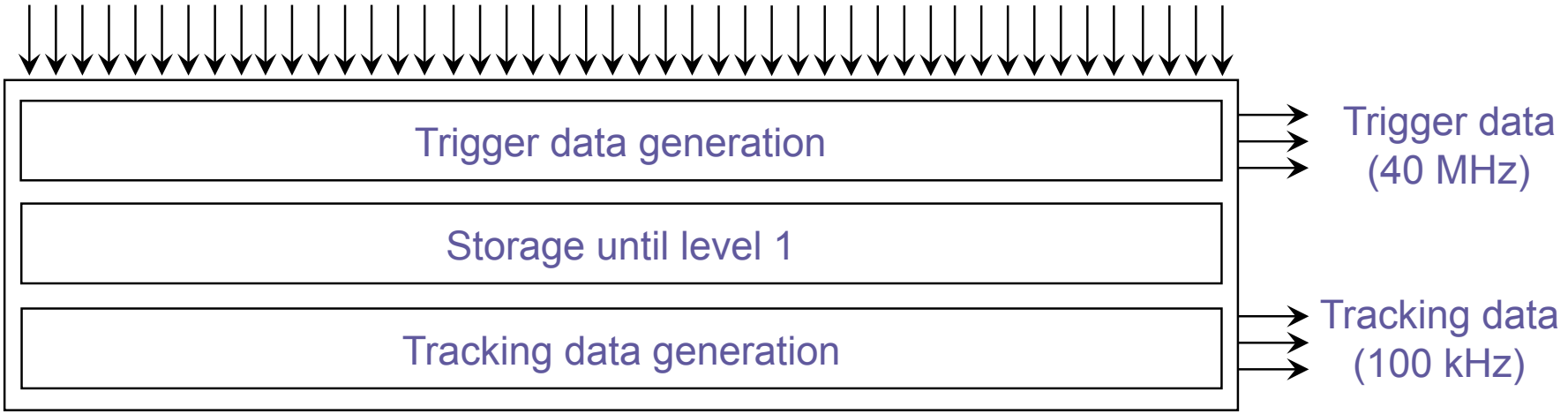


Challenge is efficient data processing at the edge of the chip and communication to the outside for trigger and tracking signals

Occupancy D. Abbaneo	Element 100x100 micron	Superelement 256x100x100 micron
PXB Layer 1	5.56E-03	1.42E+00
PXB Layer 2	2.41E-03	6.16E-01
PXB Layer 3	1.39E-03	3.55E-01
TIB Layer 1 int	3.39E-04	8.69E-02
TIB Layer 1 ext	2.82E-04	7.23E-02
TIB Layer 2 int	2.18E-04	5.58E-02
TIB Layer 2 ext	1.88E-04	4.82E-02
TIB Layer 3 int	1.28E-04	3.29E-02
TIB Layer 3 ext	1.14E-04	2.91E-02
TIB Layer 4 int	9.32E-05	2.39E-02
TIB Layer 4 ext	8.55E-05	2.19E-02
TOB Layer 1	5.94E-05	1.52E-02
TOB Layer 2	4.58E-05	1.17E-02
TOB Layer 3	3.54E-05	9.06E-03
TOB Layer 4	2.78E-05	7.11E-03
TOB Layer 5	2.57E-05	6.58E-03
TOB Layer 6	1.97E-05	5.05E-03

In the following some ideas on architecture – not final at all, would like to point out the thinking, do not want to give impression things are fully solved…

Data processor



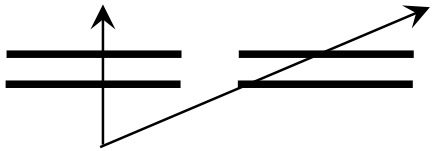
- Advantages of having all bits at the edge:
  - Can handle them in a programmable way
  - Do not need to distribute the clock to all elements (cannot would take a good fraction of 10 mW/sq cm), save power by not doing so

Strategy for trigger: example of compression of data, folding

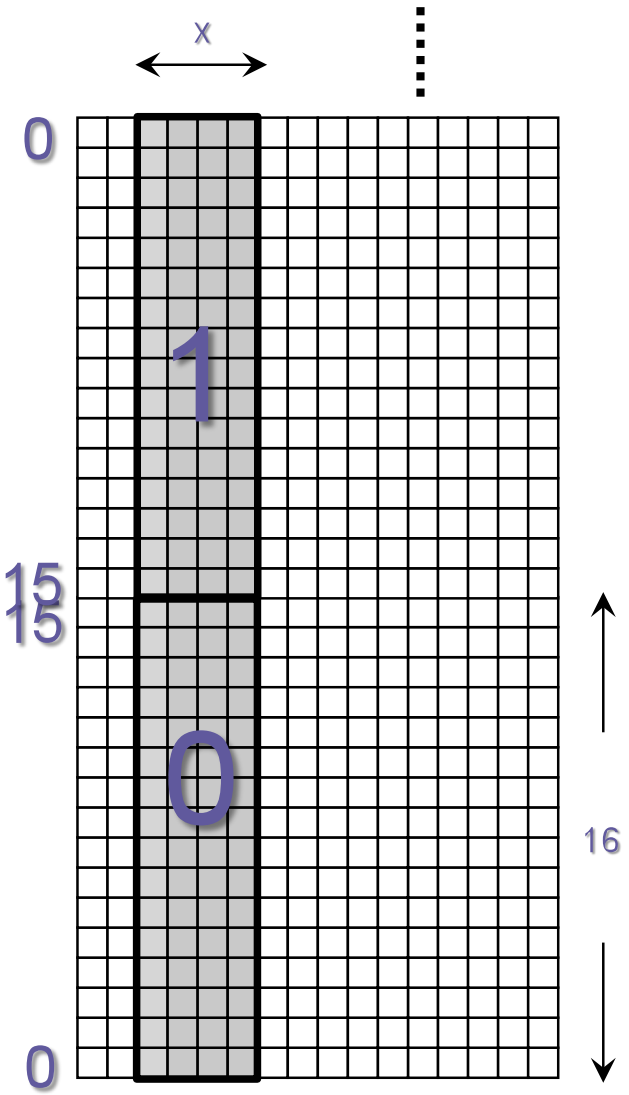
- Idea is to reduce data/number of outputs without big increase in activity in the bits while at the same time being robust in situtations of charge sharing/multiple hits
- Make column wider so that average occupancy in column =< 0.25, TOB6 128 wide, TOB1 16, TIB4 8, TIB1 2 , so in general x
- Do folding 256 -> 16+16 coordinates = per supercolumn 32*40Mbit/s = 1.28 Gb/s
- If 8 bit address, for one hit (no charge sharing, 4x less data, but no tolerance for charge sharing and double hits.
- Power: if local transmission in CMOS @ 40 MHz

Changing bits/hit*0.25*40 MHz*2pF < 40 uW

- Need programmable shift :



Stitching

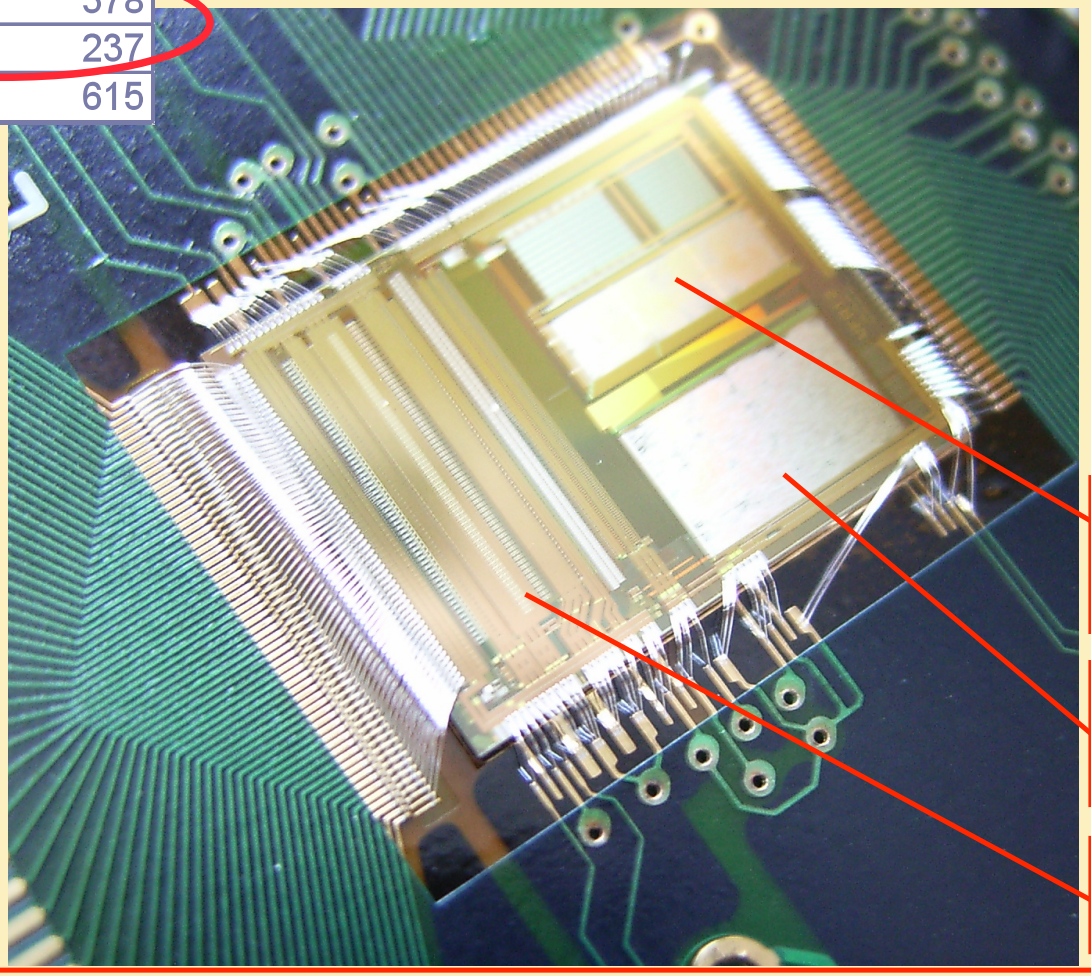


Digital power consumption: TOTEM VFAT chip

VFAT power consumption			
(mW)	Sleep	Run (nominal)	Run (max)
Analog	33	378	378
Digital	135	194	237
Total	168	572	615

VFAT sends digital data to GOH hybrid, which serializes and optically transmits this data

P. Aspell et al. TWEPP 2007



Designers :
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Jan Kaplon
Kostas Kloukinas
Pierre Chalmet

CERN C4i

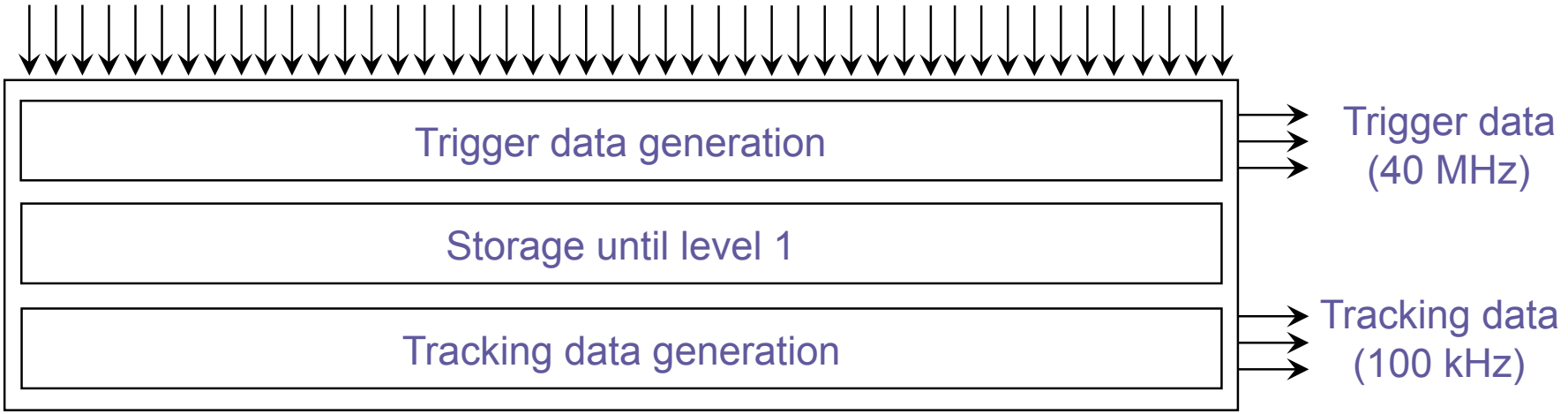
Data treatment and memories

Slow Control Registers

Frontend

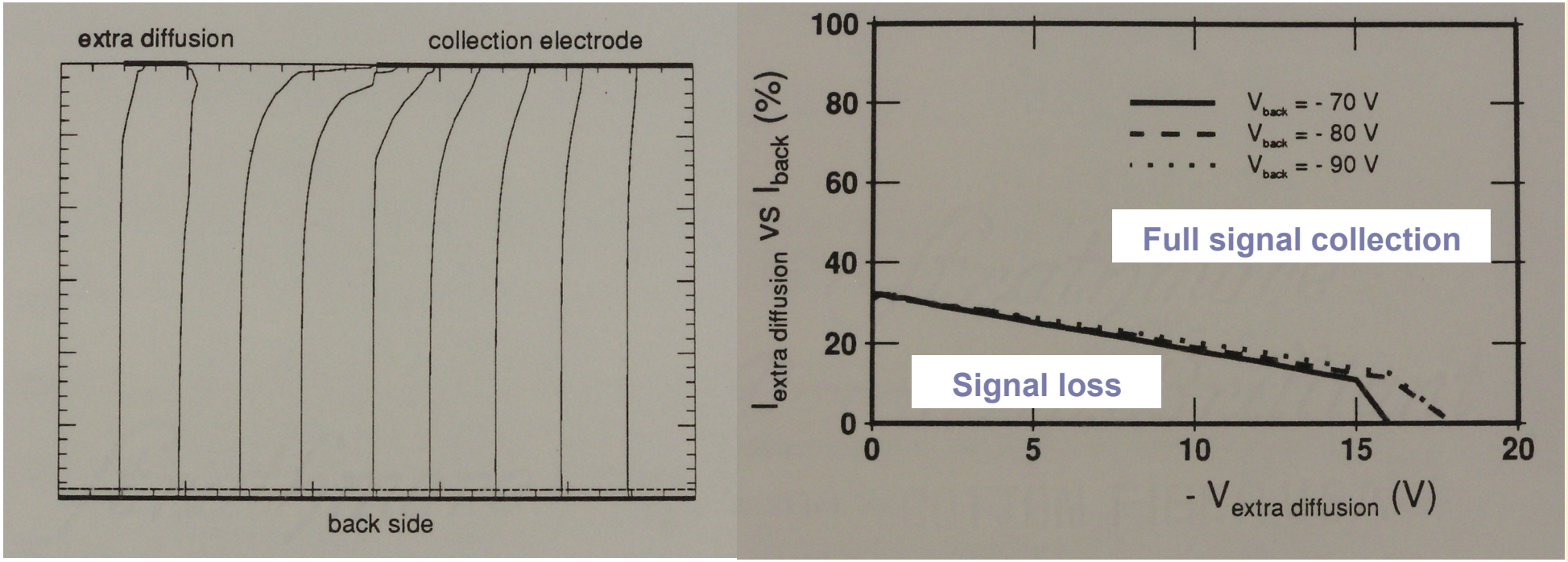
128 channels of tracking front end with digital storage and data transmission
8 programmable trigger outputs, designed for radiation tolerance

Storage until level 1



- Full memory for storage until level 1?
  - In principle space not prohibitive
  - In VFAT (TOTEM) ~2 mW/channel for this (including many whistles and bells)
  - Gain in technology max 20x, need much better than this:
- Need less than 1uW/channel (= 10 mW/sq cm)
  - Need encoding before writing into memory
  - Folding in Y yields a factor 8 (for this example), can look at X
  - Can ‘or’ channels, so reduce apparent segmentation

How about monolithic (integrate sensor and readout on one piece of silicon) ?



Should not lose the charge 'somewhere' in the readout circuitry: in the example extra diffusion collects charge from a considerable fraction of the substrate, on the right bias required to divert the flow lines

How about monolithic (integrate senor and readout on one piece of silicon) ?

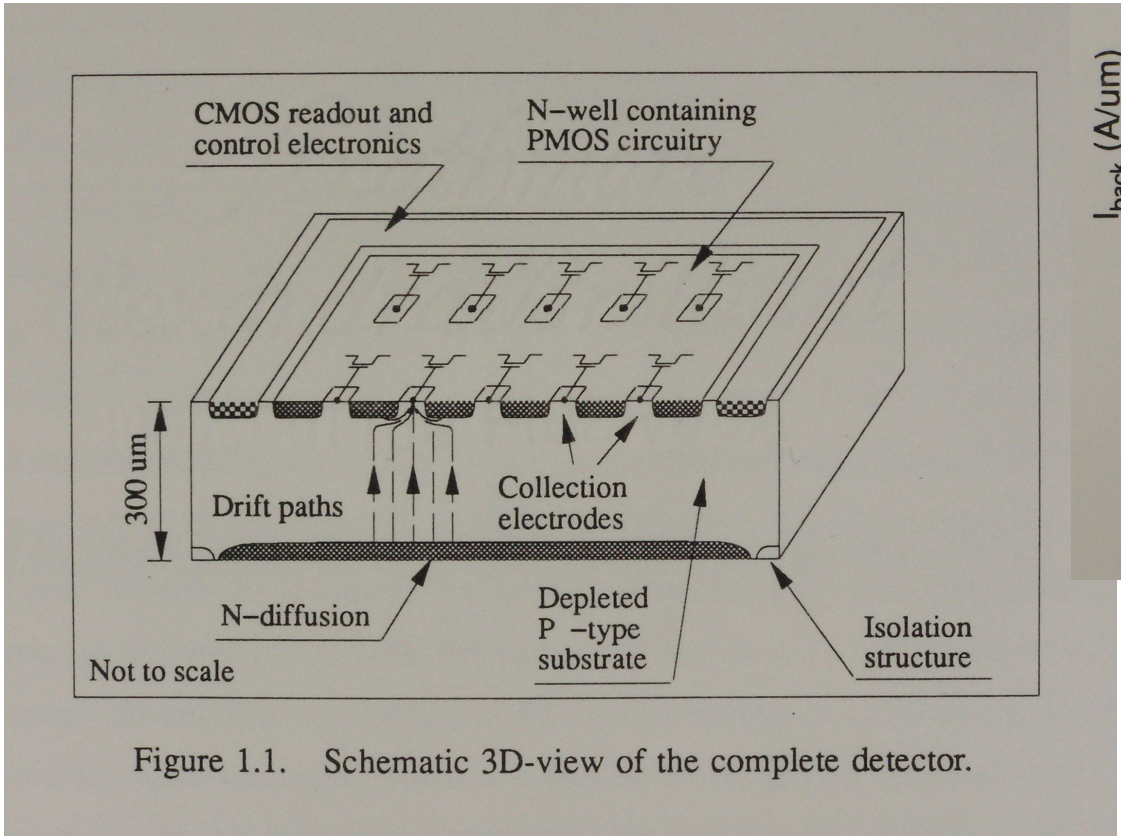
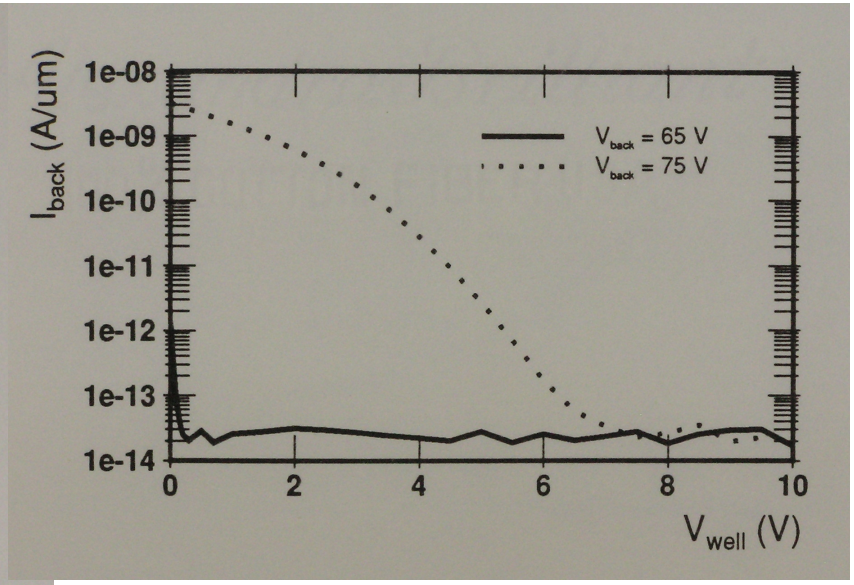


Figure 1.1. Schematic 3D-view of the complete detector.



Note 300 micron thick fully depleted substrate

$N=1E12cm^{-3}$

Ccoll=26fF

Same principle but junction at the bottom, high field region further removed from the well. Diversion of flow lines can be done with lower biases

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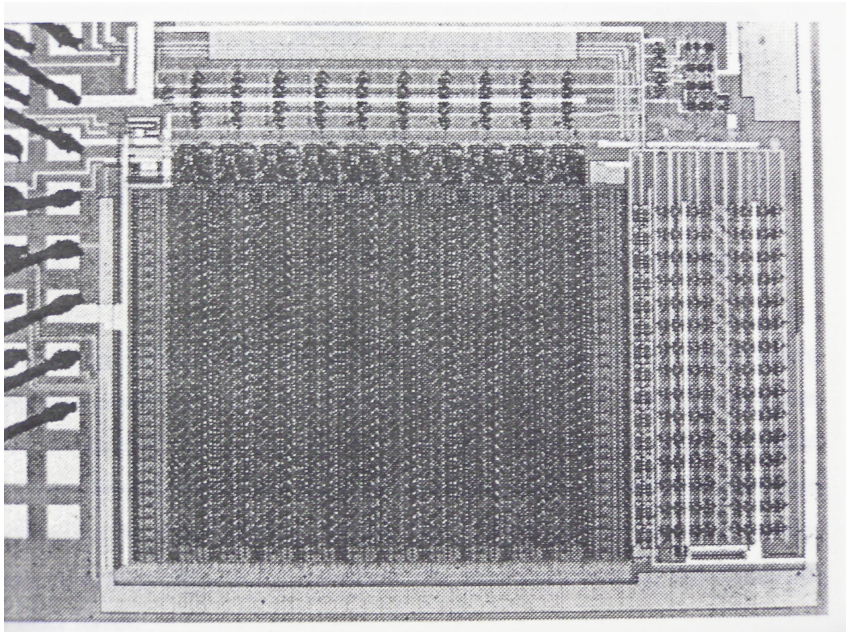
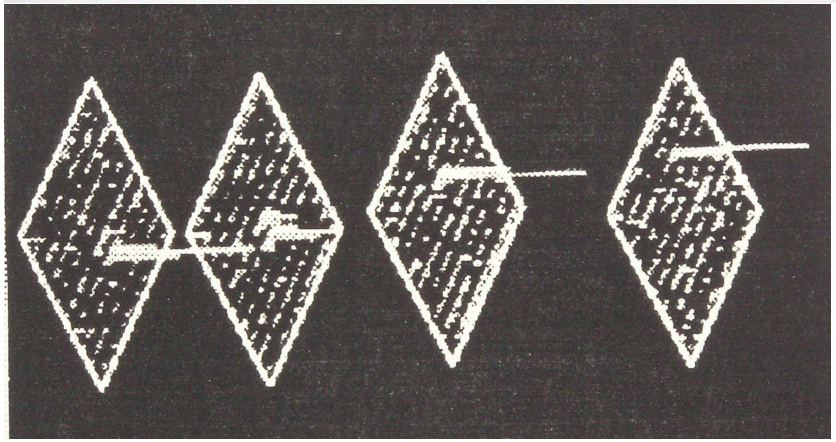
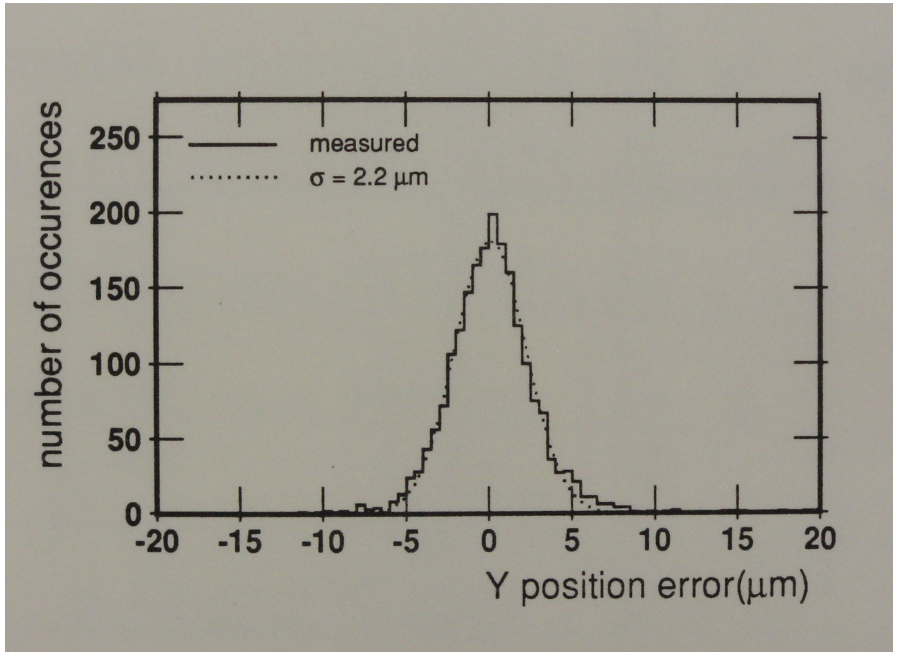






C. Kenney, S. Parker, W. Snoeys, J. Plummer et al.

1992

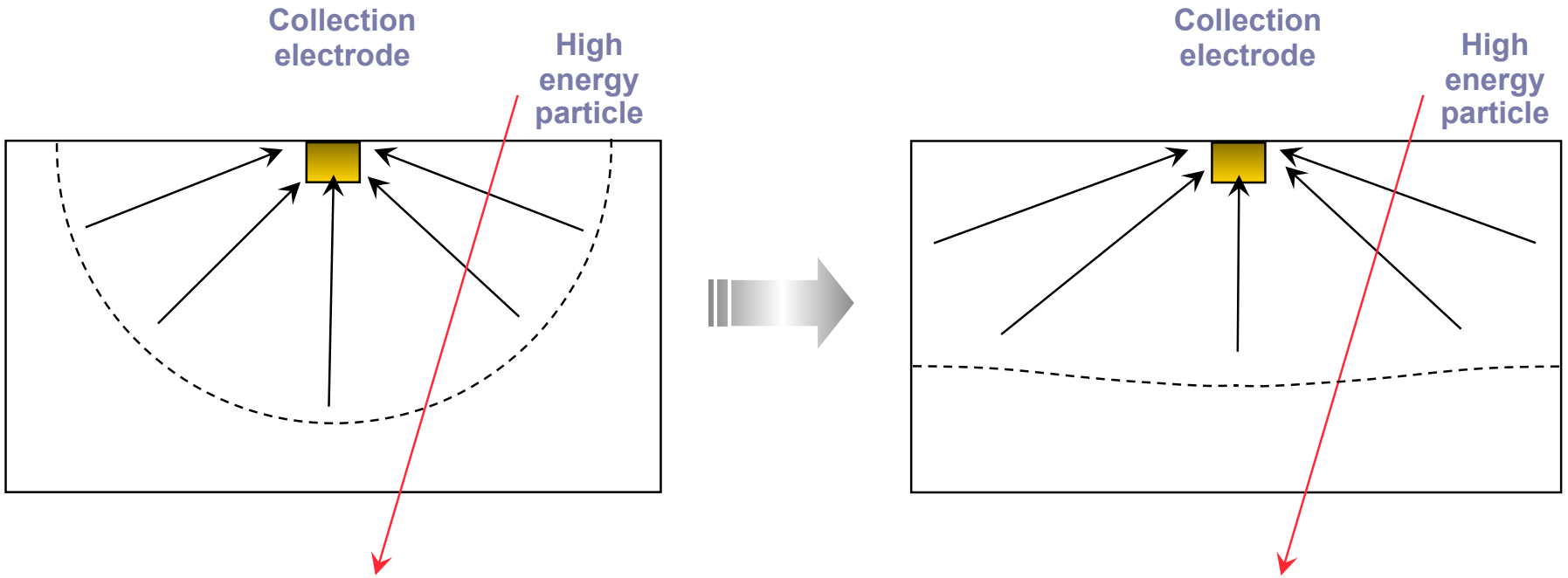
Device simulations

- Need to work on Q/C: 10 micron depletion layer established, means:

$$\frac{S}{N} = 25 \Rightarrow \frac{Q}{C} = 4mV = \frac{0.13\,fC}{33\,fF}$$

- 33 fF achievable (cfr CMOS imagers order of magnitude less, but smaller…)
- We are working with IN2P3 Strasbourg on device simulations for the detecting element:
  - Worked on convergence of simulations at high reverse bias
  - Now using 2D simulations to verify principles (less computation intensive)
  - First results (2D, verif in 3D to be done) indicate high biases 100 V should be possible, so ~ 30 micron depletion
  - Working to obtain uniform depletion layer even with small collection electrode
  - Need to verify charge collection, charge should be collected on designated collection electrode, not be 'lost' elsewhere

Device simulations: uniform depletion layer



Prototyping

- Foundry proposed alternative using MPW instead of engineering run for prototyping. Means significant cost savings. We are in contact with the MPW service and are finalizing the details.
- Would like to pursue this route, and submit a prototype as soon as possible. First possible submission date is October.
- Just received documentation and design kit from the foundry for this process
- First (preliminary) list of items to submit:
  - Test structures to characterize the substrate doping, structures allowing resistance measurements, some diodes, etc...
  - Transistor test structures for model verification, and for irradiation measurements. (First version almost finished, previously submitted to other foundry as well)
  - Test structures, probably small matrix in a few variants, related to the detecting diodes, where we can directly measure leakage current, breakdown voltage etc...
  - A matrix with simple (high power) readout compatible with test setup of Strasbourg (if possible). This would allow quick evaluation.
  - A matrix with the front end we would like to use for a real tracking environment. The front end is intimately linked with the matrix and we need to evaluate the two together. The peripheral readout of this matrix will probably be kept very simple. To detect problems or characterize something in the front end, at least one front end will be equipped with some extra buffers to study it in more detail. At least one of the pixels should be equipped with an electrical test input.

Conclusions

- Perspective for monolithic in standard deep submicron with several advantages
- Analog power can be reduced by segmentation, need work on digital, would like to exploit having all bits at the bottom of the matrix
- Possibility for prototyping with MPW in 90nm even on more lightly doped substrates
- Thinking about first submission
- CERN committed to at least ¼ of the material cost, already activity on front end, on test structures, and collaborating with IN2P3 Strasbourg on device simulations.
- Funding of engineering time from the Conseil General de la Haute Savoie
- Interest from Italian groups (CMS & Alice), from Imperial College, some discussions with ATLAS
- Very much work in progress