Flip-Chip and Wafer Level Packaging Technologies

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Gustav-Meyer-Allee 25

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Outline

- Introduction
- Module Assembly Process
  - Wafer Bumping
  - Flip Chip Bonding
  - New Requirements
- 3D Integration
  - Thin Chip Integration
  - Through Silicon Vias (TSVs)

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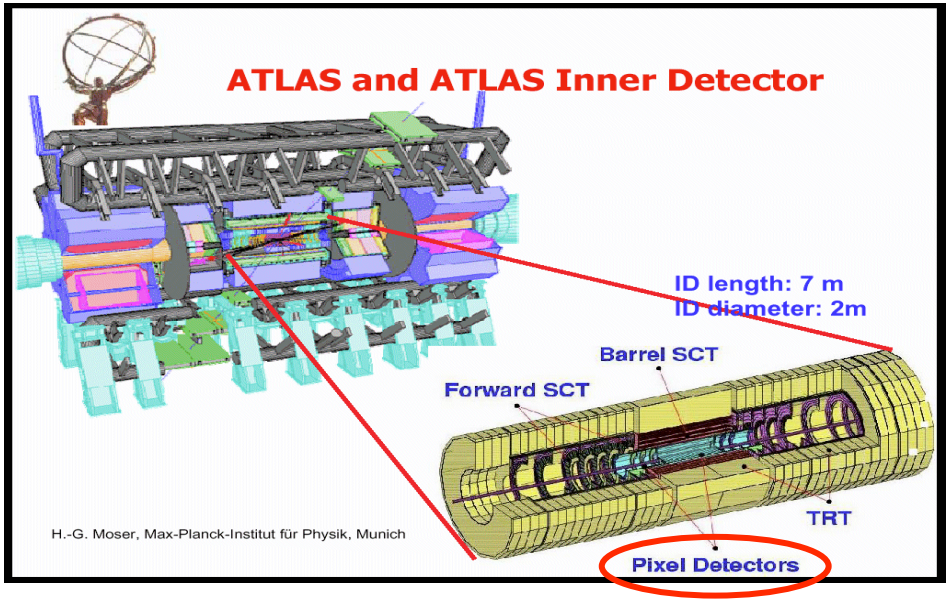
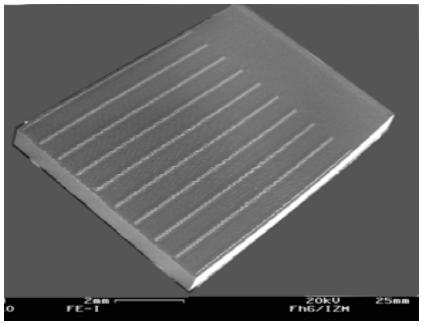
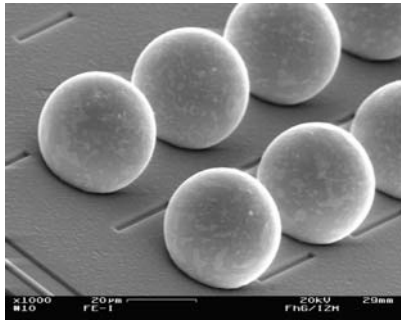
Assembly of Modules: ATLAS Detector at LHC at CERN

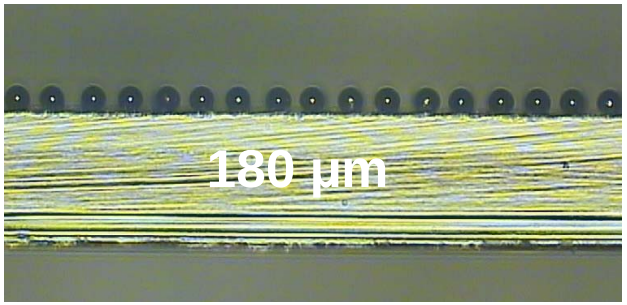


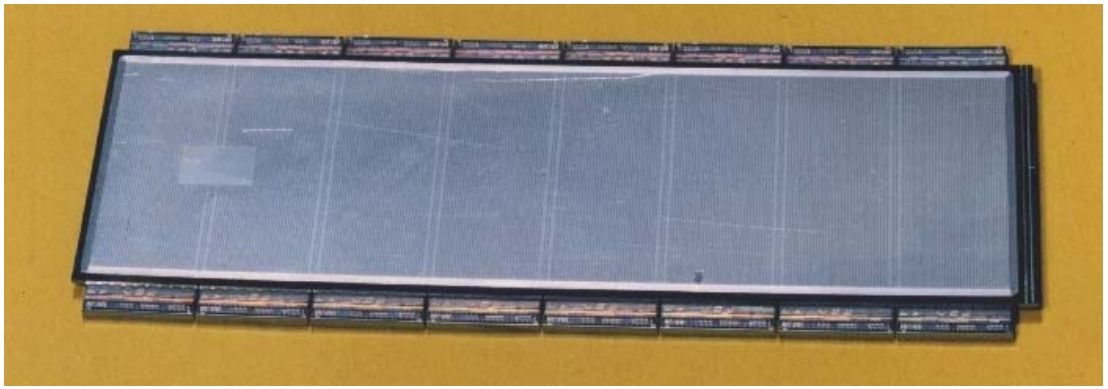


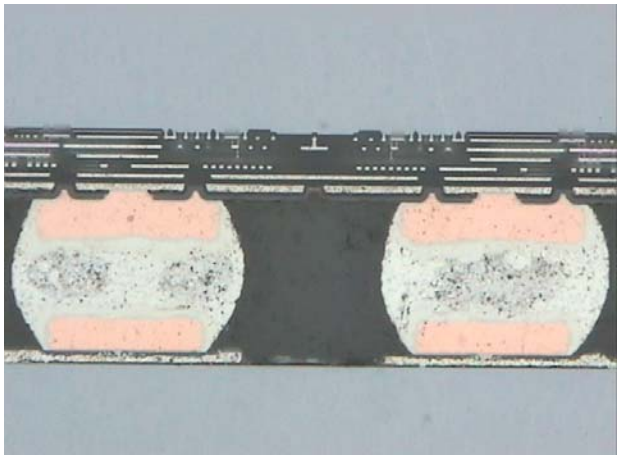


IBM 0.25 µm rad tolerant design
2800 Bumps/Chip 50µm Pitch

Thinning of bumped wafers:







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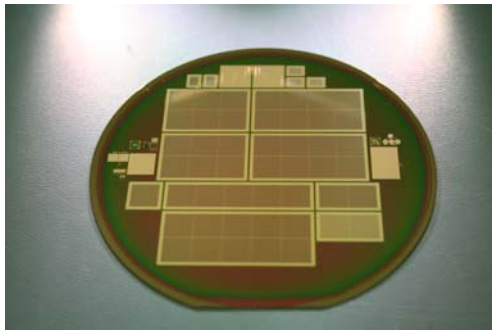
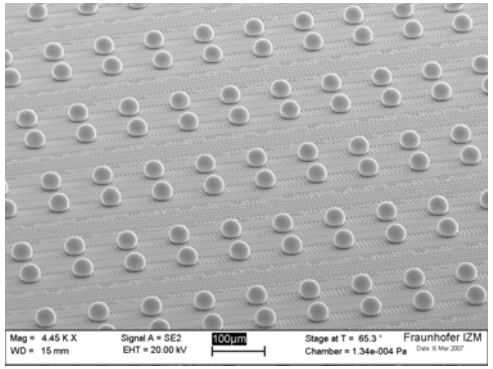
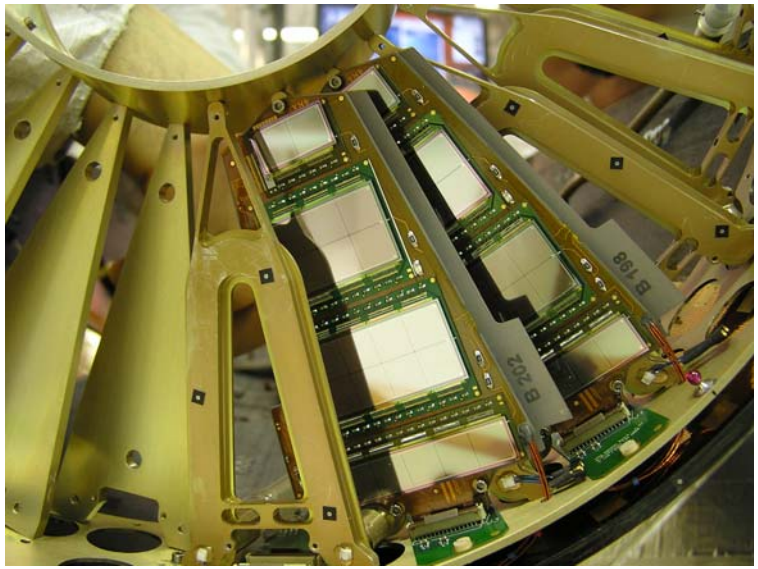
Assembly of Modules: CMS Detector at LHC at CERN



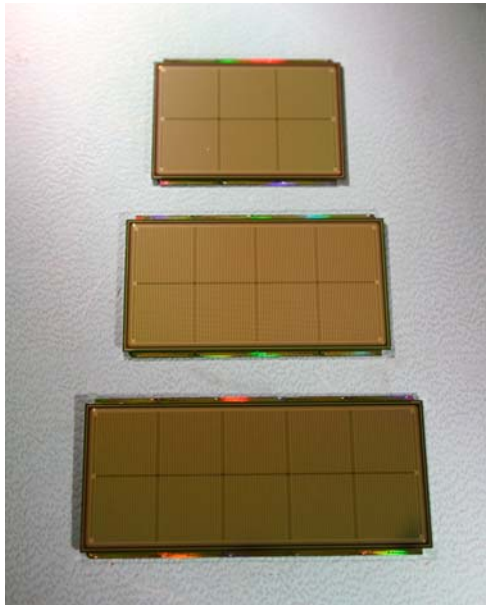
CMS pixel detector
4inch sensor wafer

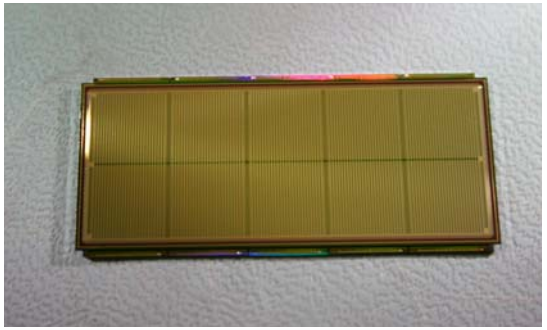


bumped CMS ROC



CMS silicon pixel detector
endcap segments





CMS pixel detector
endcap modules after
flip chip assembly

More than 530 modules have been manufactured during production phase from October 2006 to February 2008

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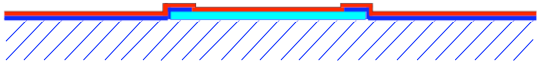
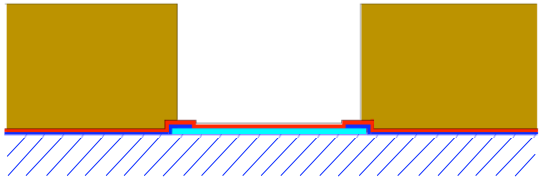
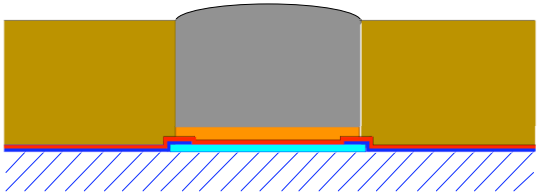
Processflow: Bumping using Electroplating



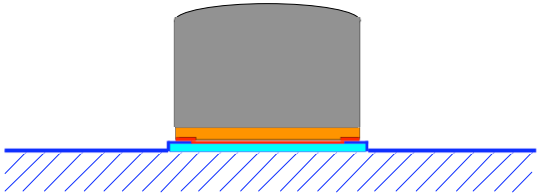
Sputter Etching and Sputtering
of the Plating Base / UBM



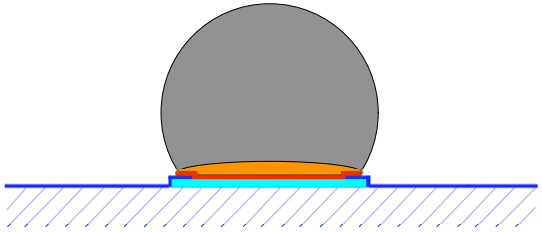
Spin Coating and Printi
of Photoresist



Electroplating of Cu and Solder



Resist Stripping and wet
of the Plating Base



Reflow

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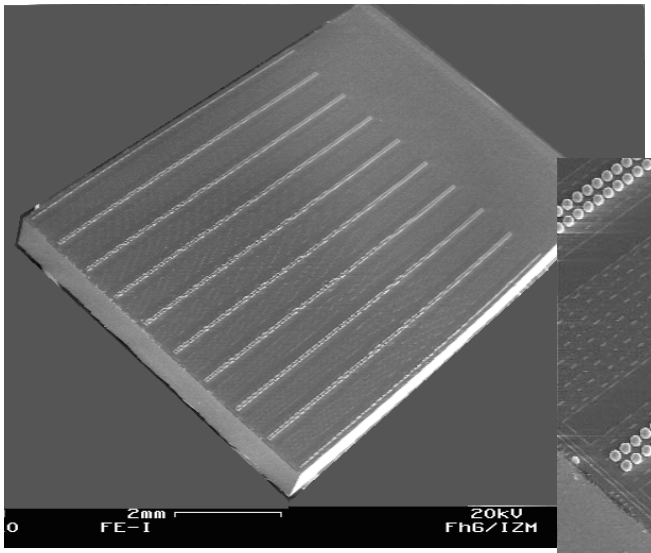
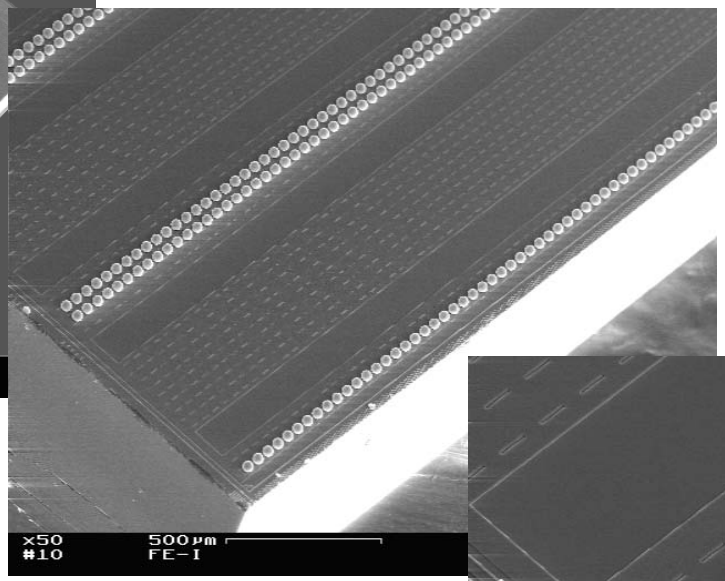
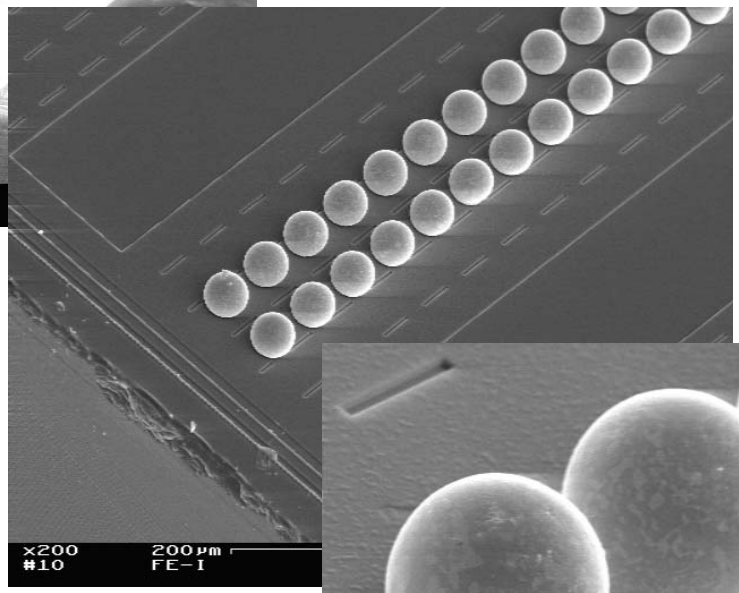
Bumped FE-I Chip

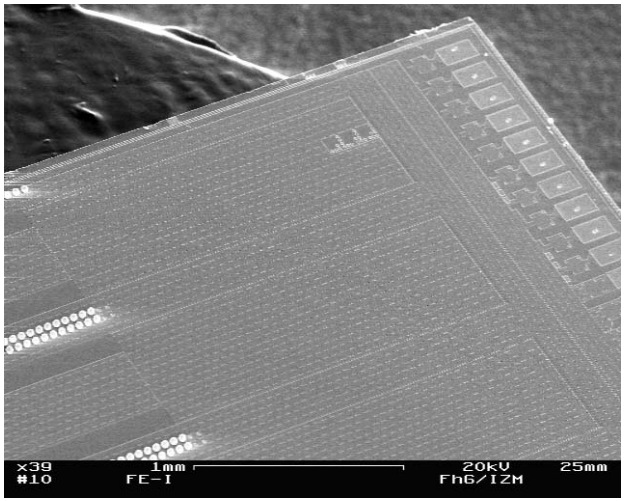
IBM 0.25 µm rad tolerant design

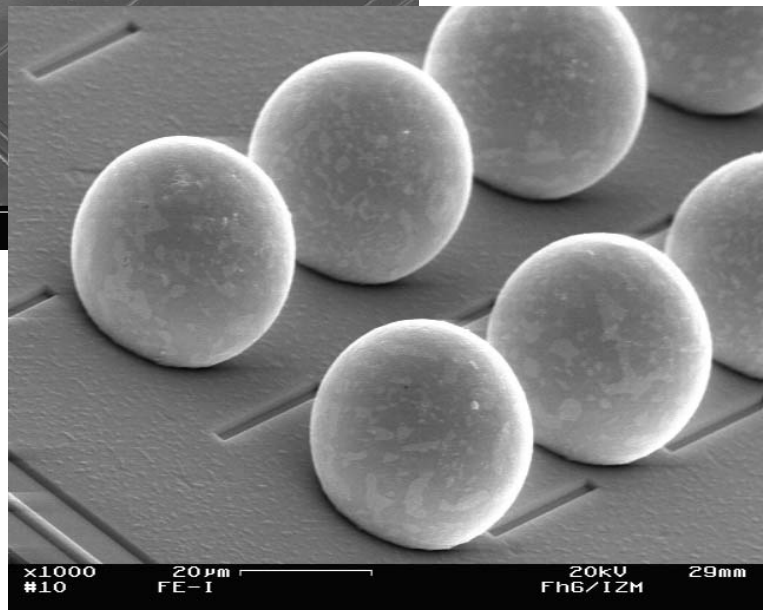


Chip with 9 column pairs









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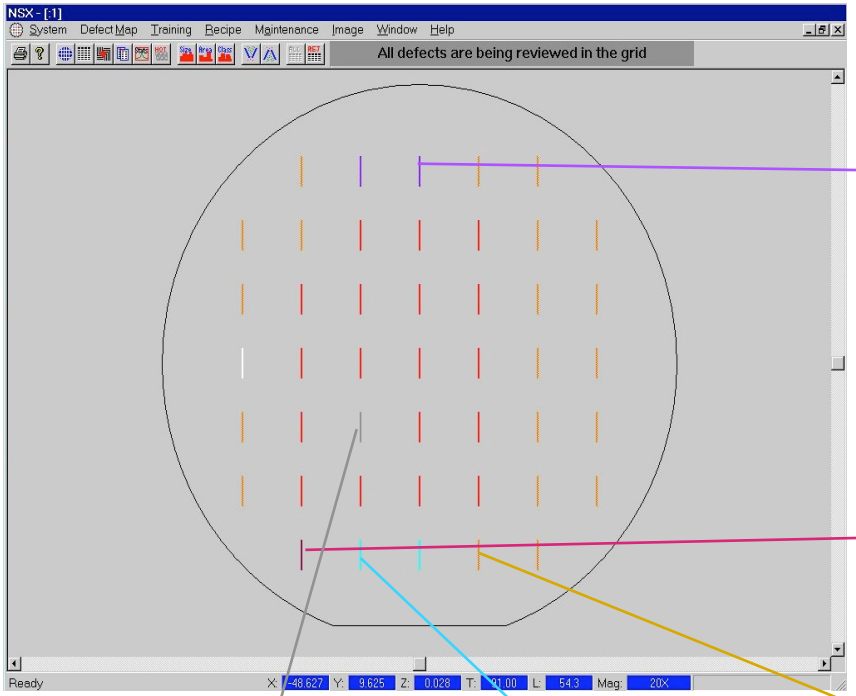
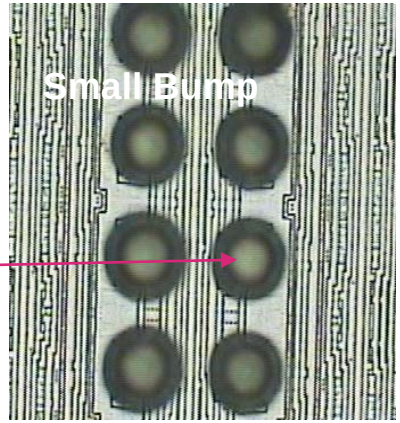
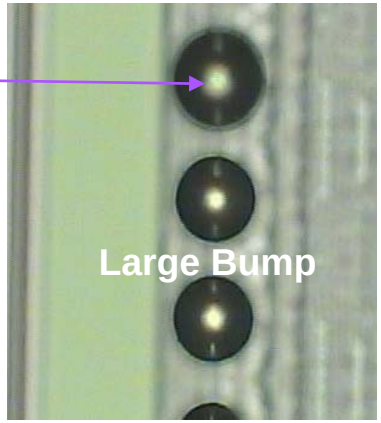
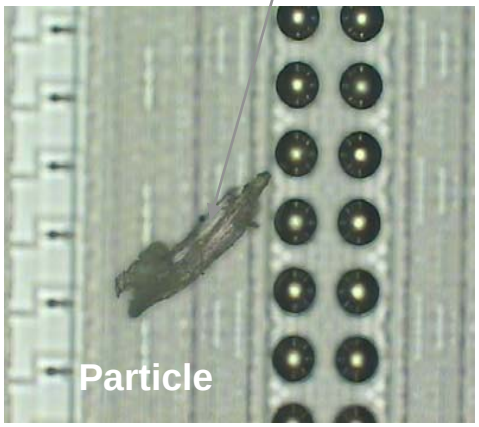
Inspection

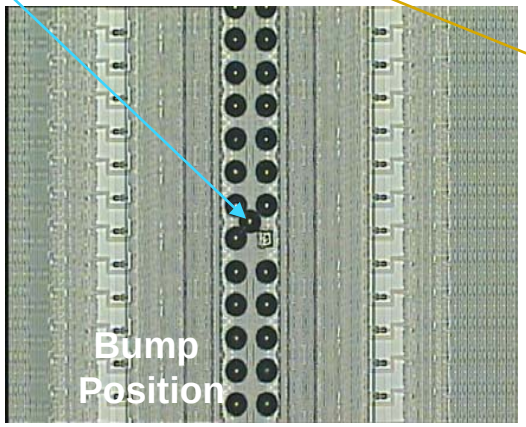


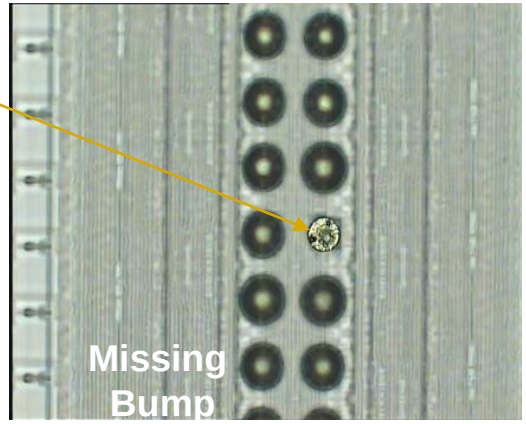




Defect Classes







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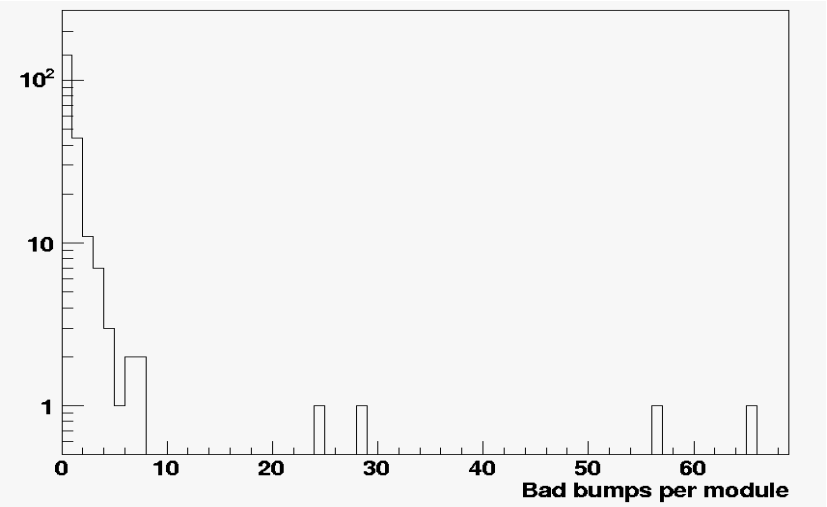
Assembly of ATLAS Pixel Detector Modules

- 16 ROC Flip-Chip Bonded to the Sensor
- 46 080 electroplated SnPb IO-Bumps, Ø 25 µm, pitch 50 µm

- Assembly of 1139 ATLAS Modules
- Assembled Chips: ~ 19000 chips
- Module Yield incl. rework: 97 %
- Chip Rework Rate: 0.7 %



98% der Module mit <10 Bumpdefekten

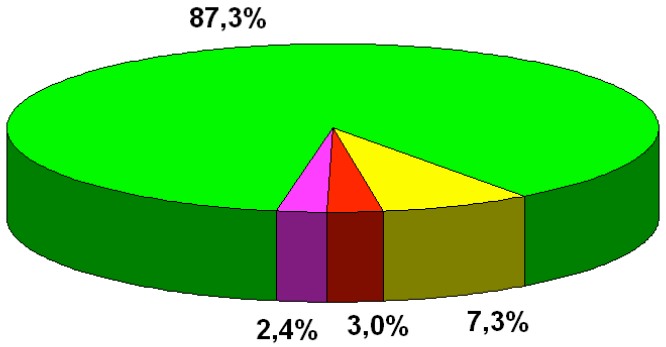
Chip Yield after Bumping:

20.720 processed Readout Chips

Class 1: perfect chips

Class 2: accepted defects
(< 4 defective bumps, small particle, ...)

Calss 3: rejected chips
(> 4 defective bumps,
scratches, residues, plating defects,...)



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Working Parts of the Module Assembly Process

-- Bumping of the FE wafer

-- Deposition of solderable pads on the sensor wafer

-- Dicing

-- Inspection

-- Sorting for FC bonding

-- Flip Chip Bonding

-- Inspection

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Processes for Waferbumping

-- Electroplating

-- electroless deposition of Nickel pads (UBM)

-- Stencil printing of solder paste

-- placement of preformed solder balls

-- C4NP

-- bonding by adhesives

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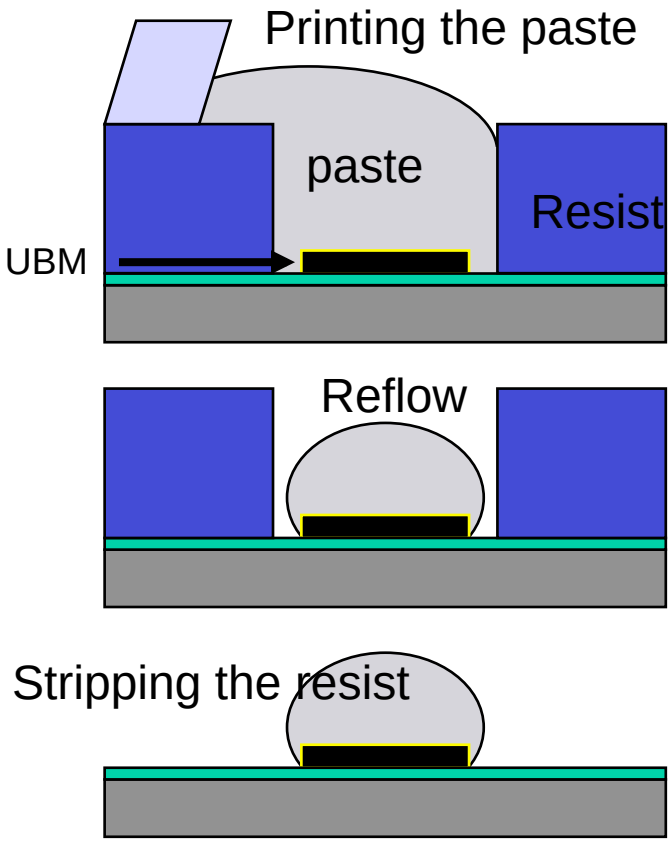
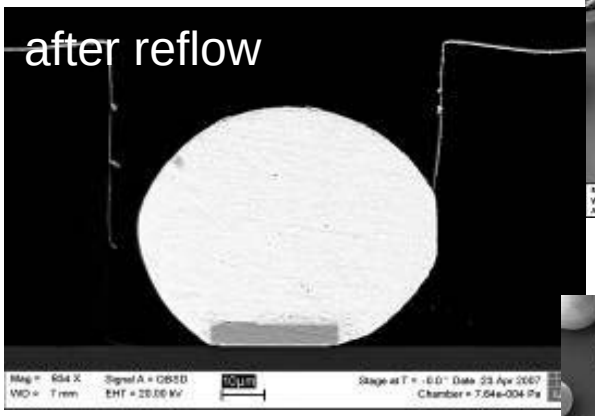
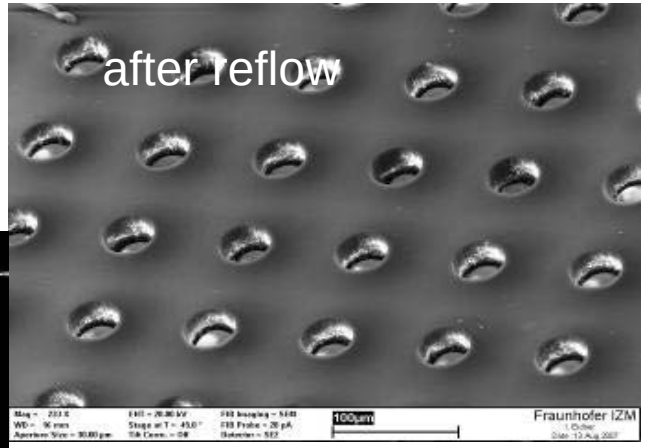
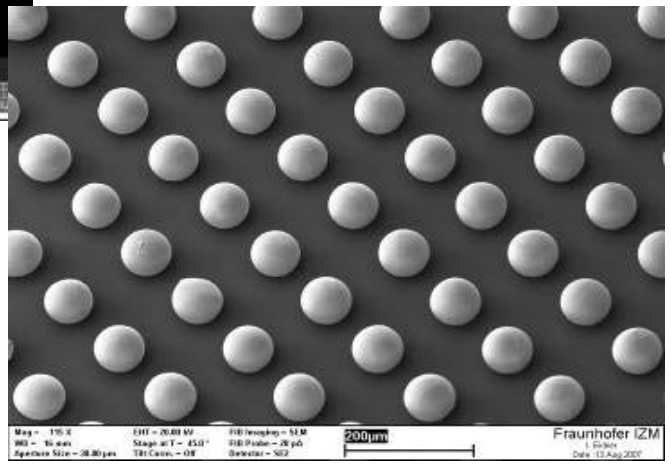
Waferbumping by Solderpaste Printing in Laminated Resist:









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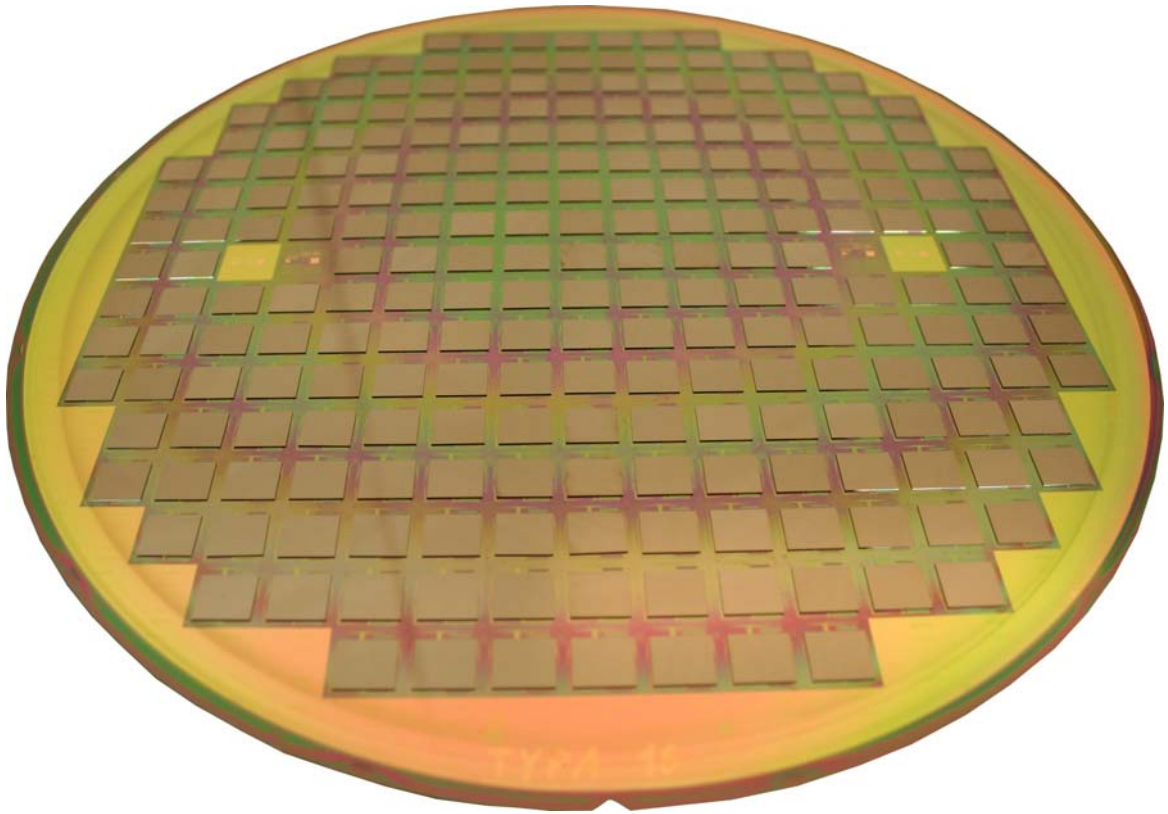
Reduce Handling: Chip to Wafer FC-Mounting

FC of thinned die on 8“ Wafer



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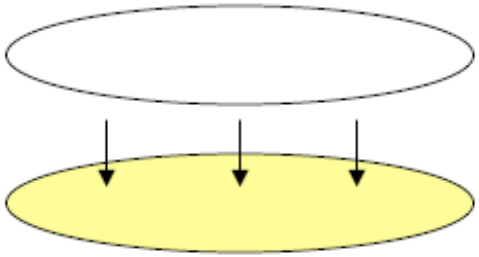
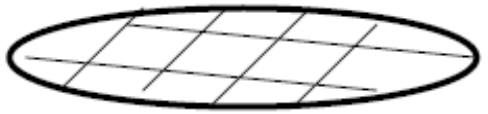
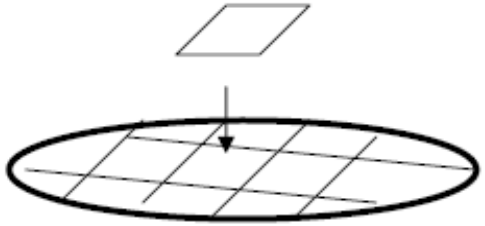


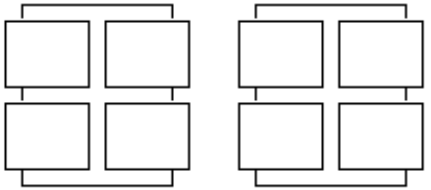
Mounting sensor wafer to support wafer



Dicing of sensor wafer without cutting the support wafer



Flip chip bonding of bumped FE dies to the sensor



Remove modules from support wafer

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Requirements:

-- Large FE chips (1,68 x 2.0 cm²)

-- Lager sensor wafers 150mm (still thin)

-- Small pitch (50µm - high bonding accuracy)

-- Reduce material budget (thinner FE-dies)

-- 3D Integration

-- Reduce cost

-- Low volume

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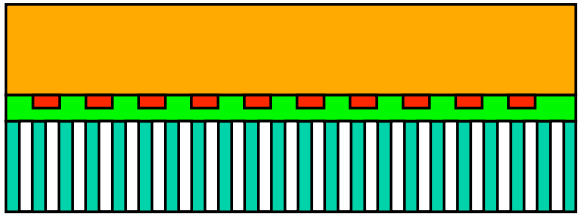
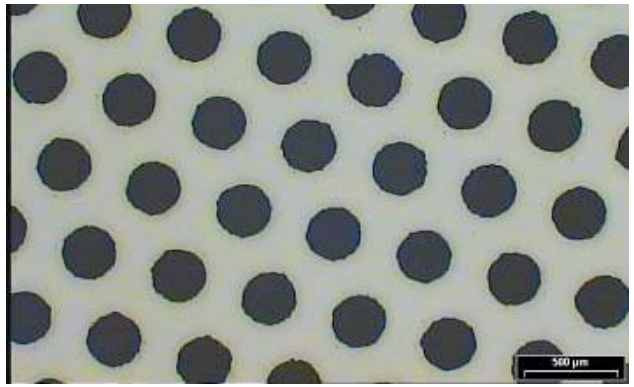
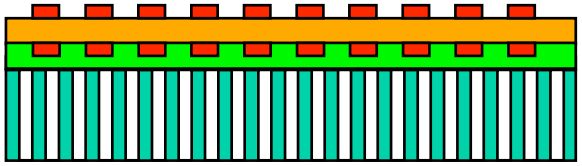
Temporary Support Bonding for Thin Wafer Processing



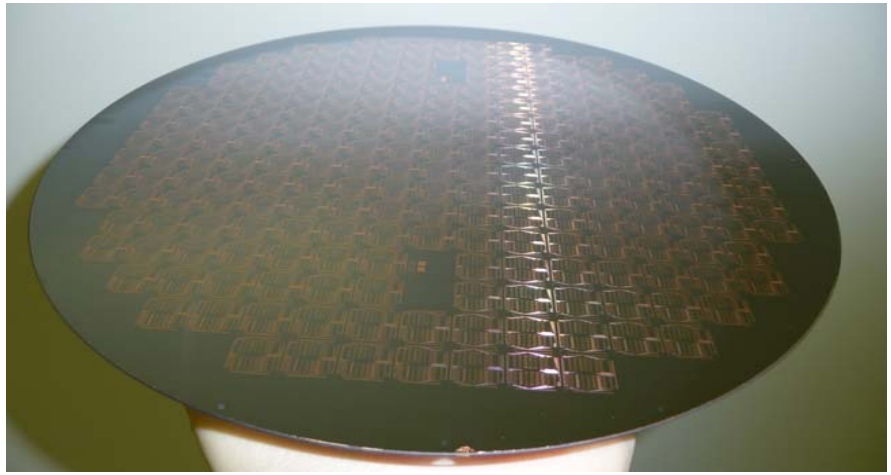
Temporary Support Bonding

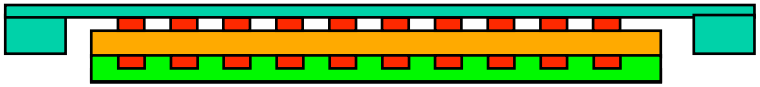


Support Wafer



Thinning and backside processing





Debonding

200mm wafer thinned down to 60µm and backside metallization

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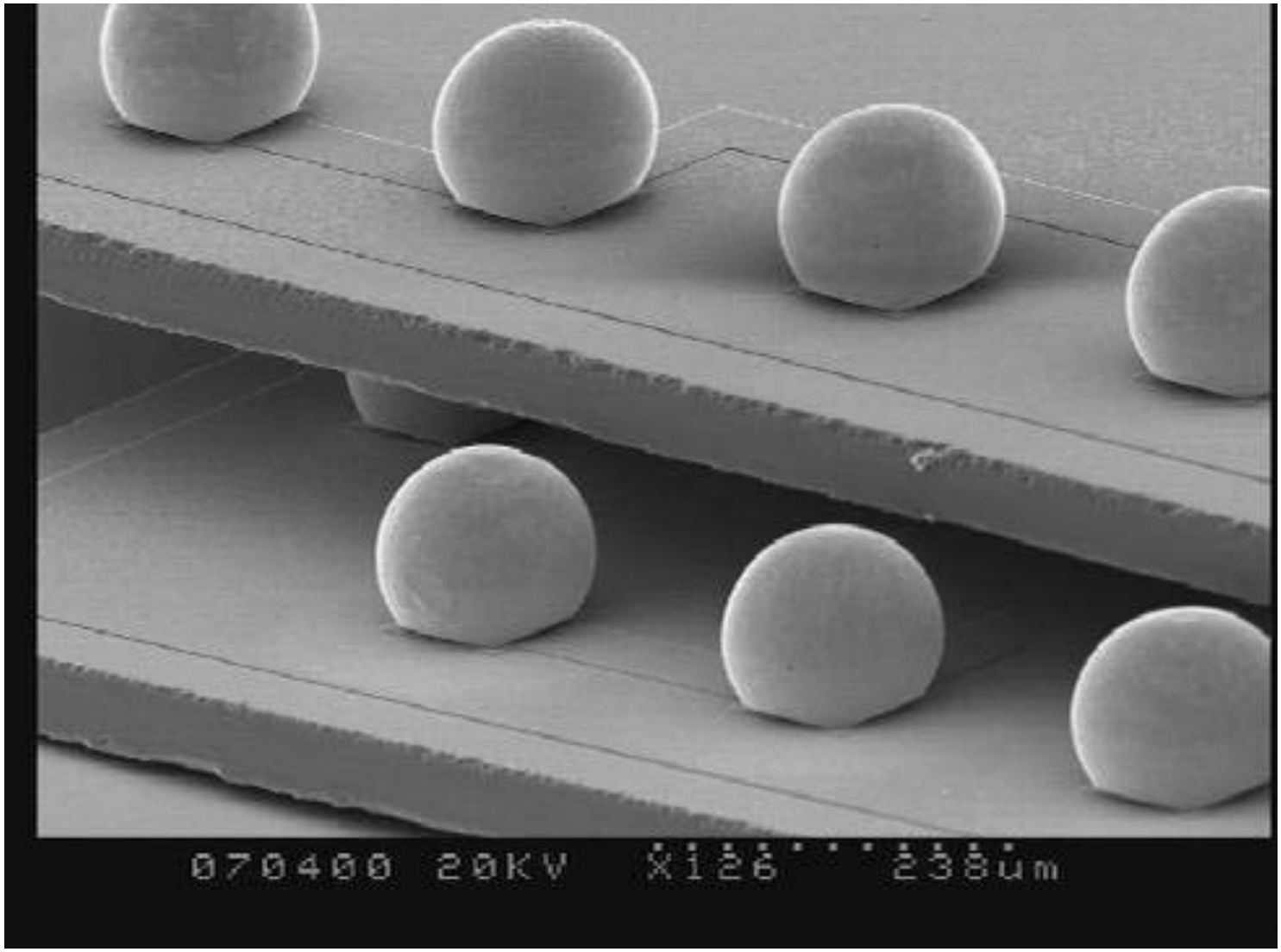

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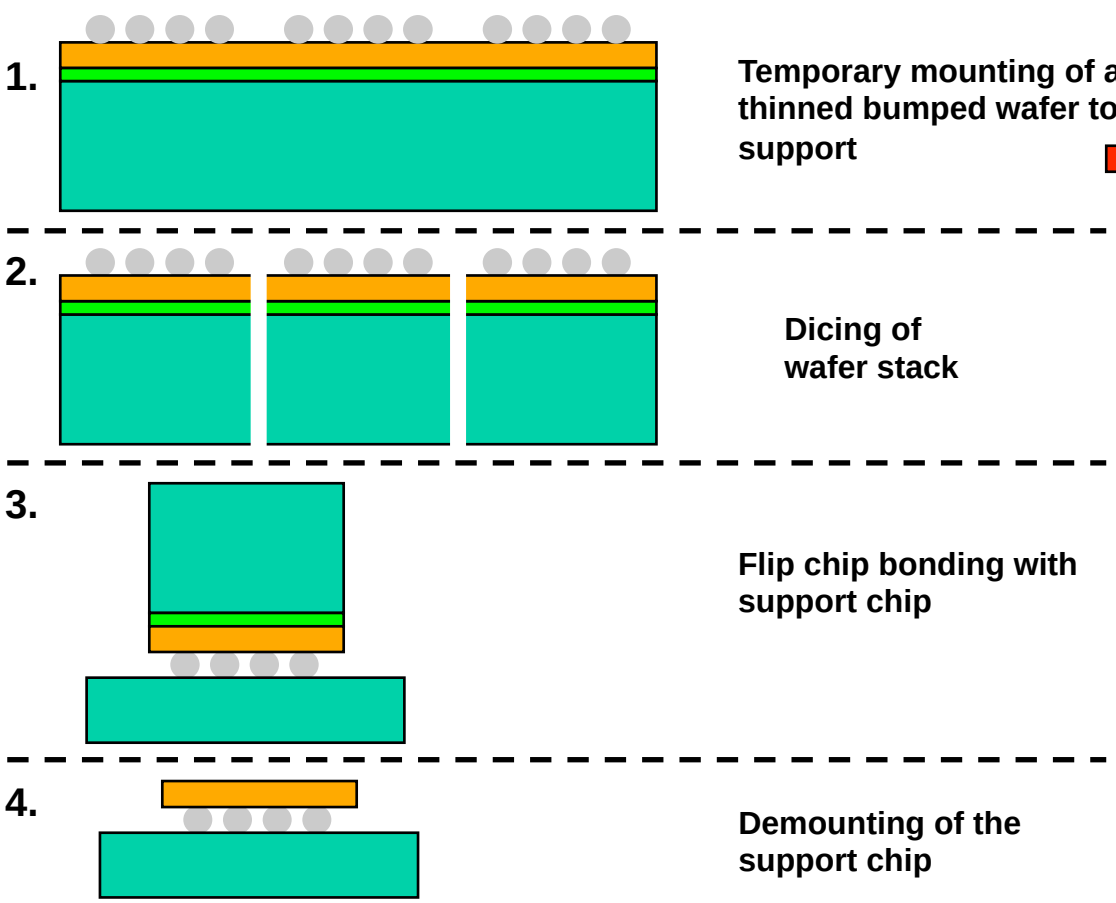
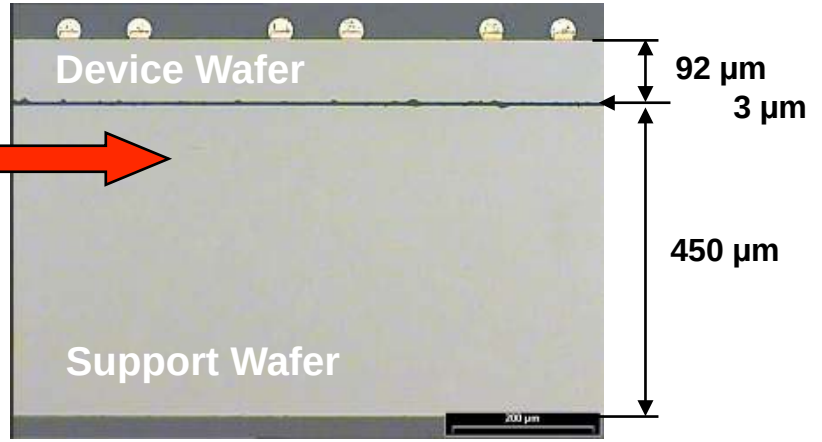
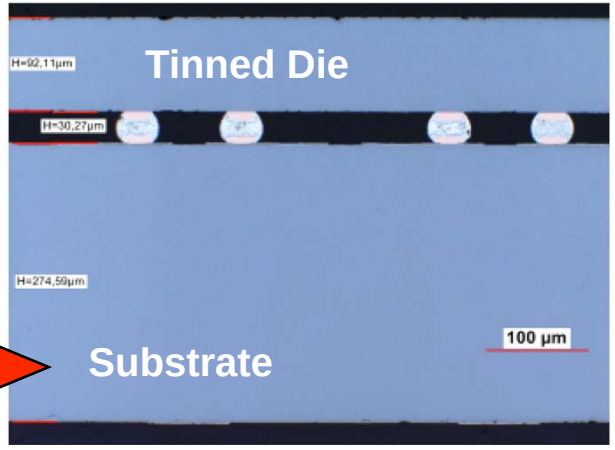
Temporary Support Bonding for Assembly of Thin Chips







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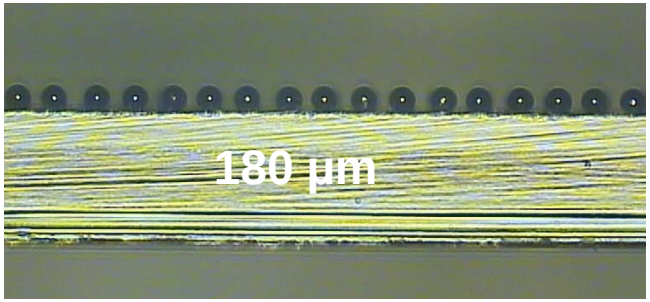
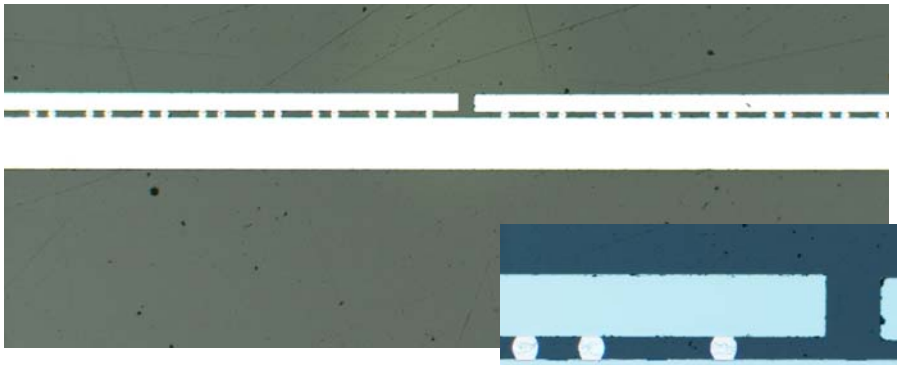
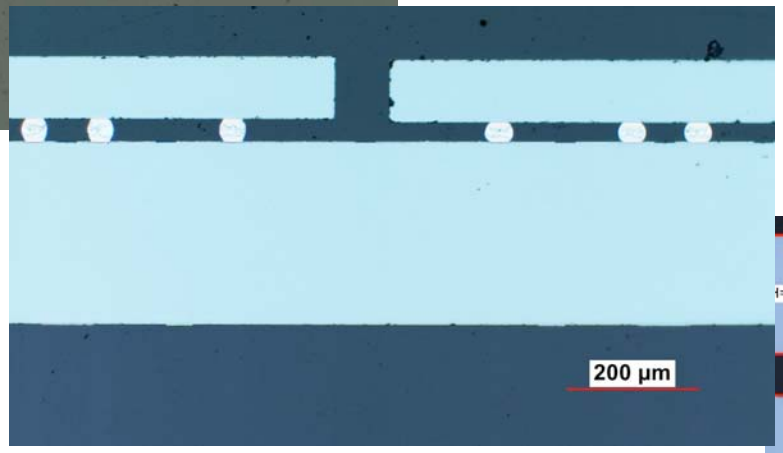
Future Requirements: Thin Silicon

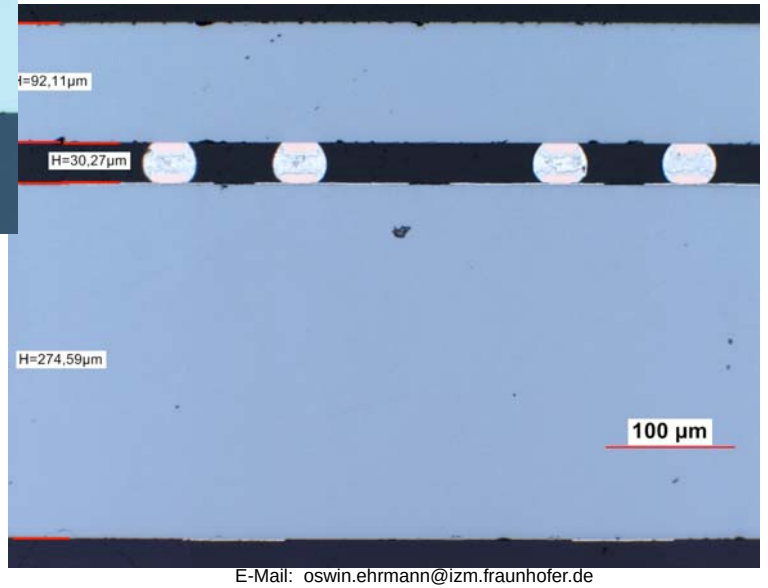
Thinning of bumped wafers:







90µm FE Chips assembled



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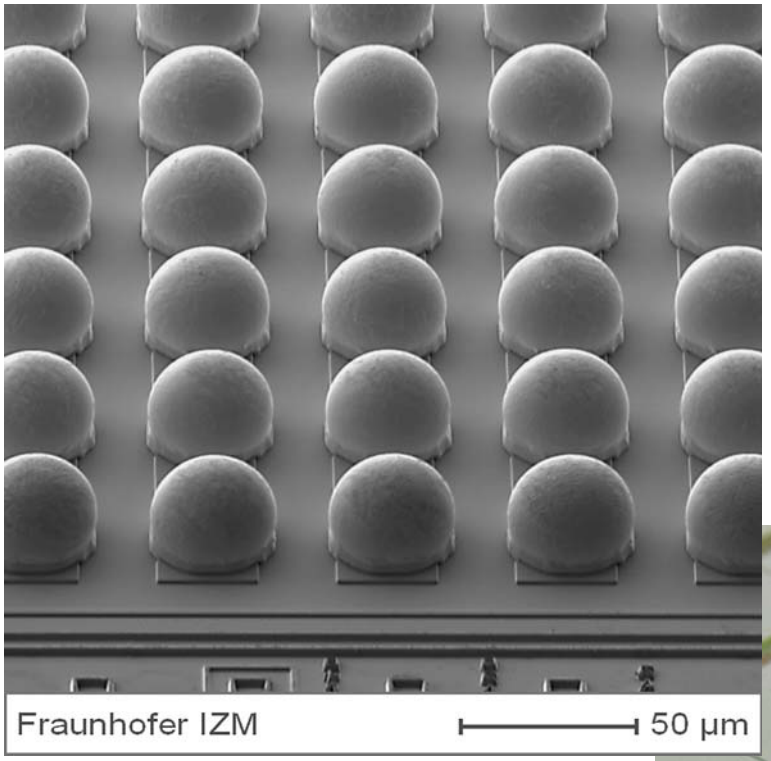

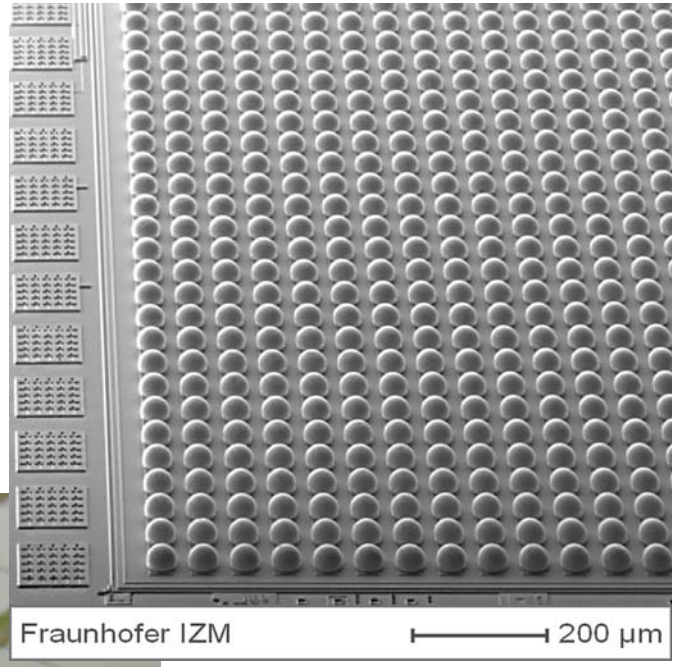

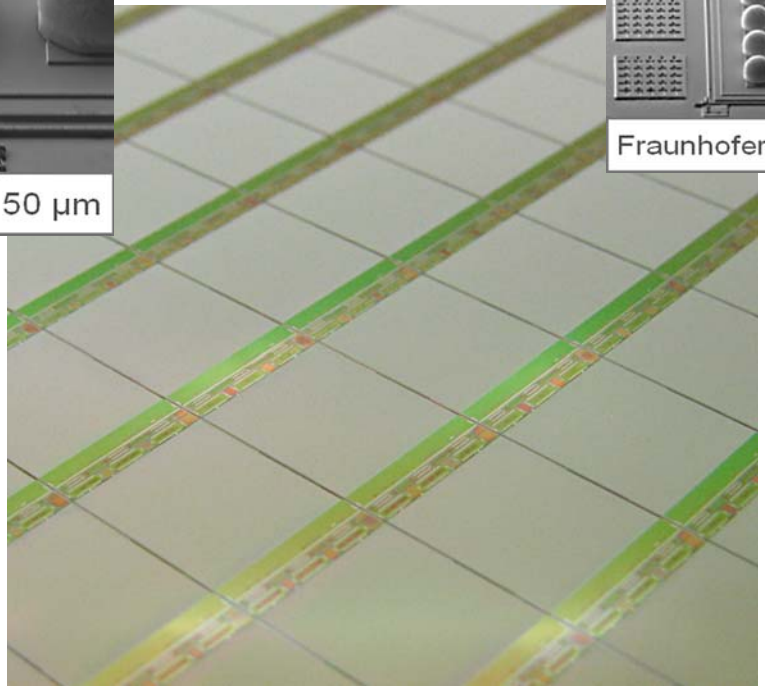

Lead Free Bumping
SnAg

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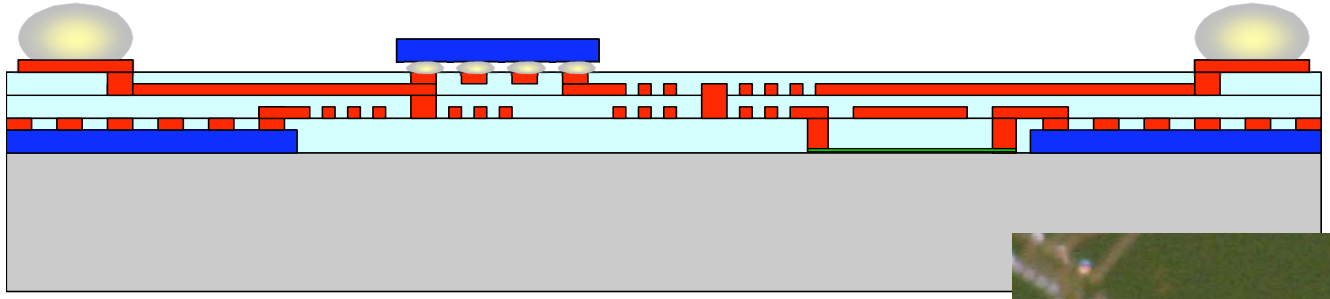
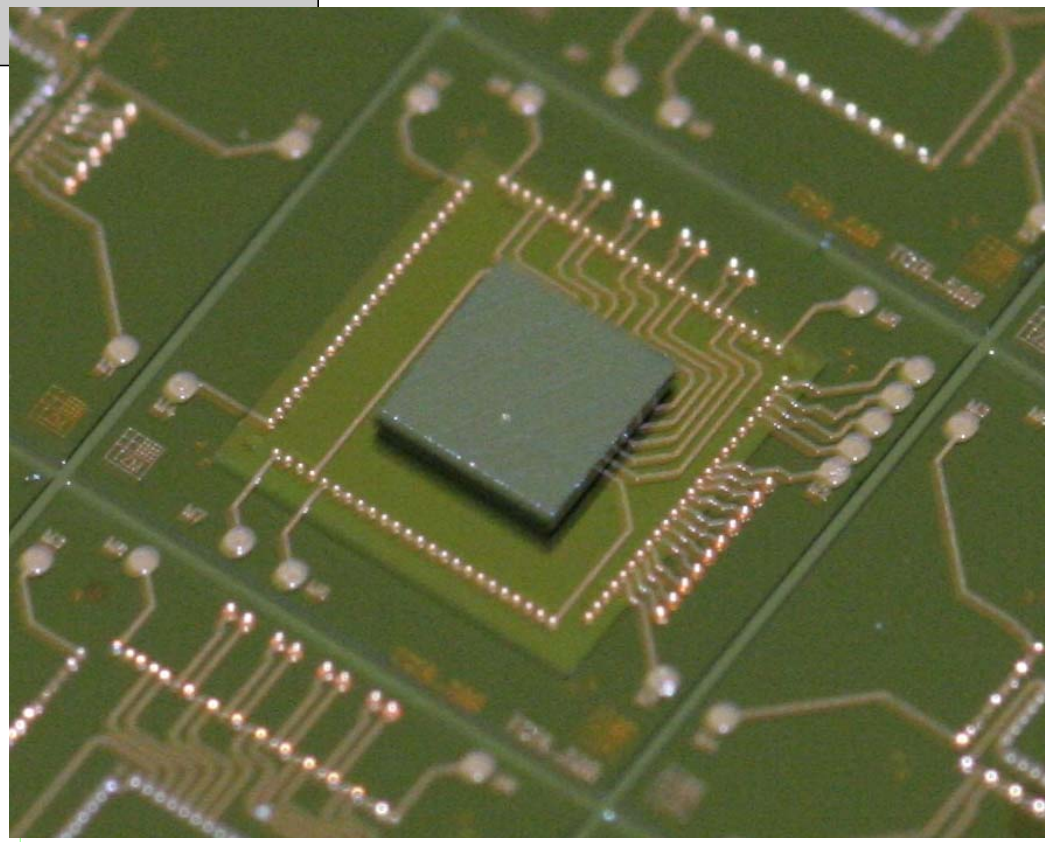
3D: Stacking by Thin Chip Integration





Combination of Flip Chip and embedding technology and integrated passive components

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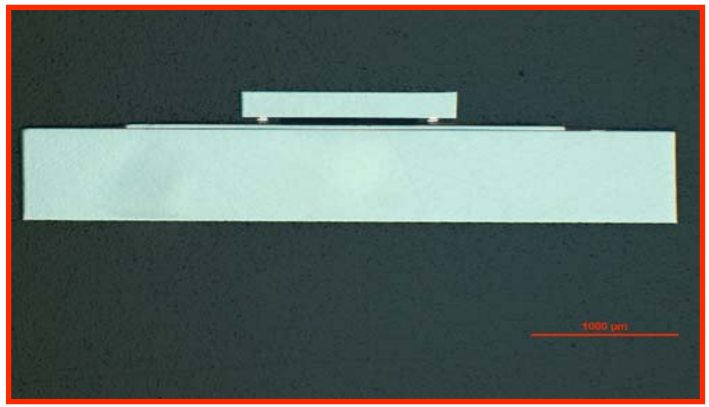
Stacking by Thin Chip Integration

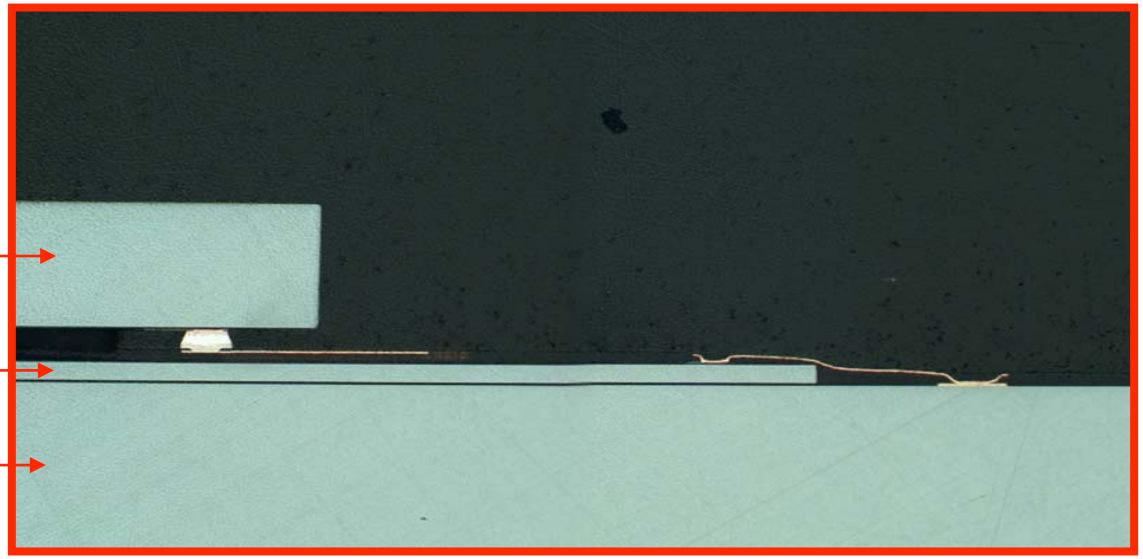


- Chip stacking of 3 Chips (Level 1 - 3)
- Thin Chip Assembly on Wafer Level – chip thickness 32µm
- BCB/Cu redistribution including thin chip embedding
- flip chip assembly of 190µm Chip on top of integrated thin chip

Level3: Daisy Chain Flip Chip

Level2: Thinned embedded Die

Level1: Substrate Chip



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Through Silicon Vias: Basic Questions

Pre Front End Process – Post Front End Process

New Front End Process

Restrictions in Process Parameters

Design Restrictions

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Through Silicon Vias

TSV – Formation and Metallization

- Deep Via High Aspect Ratio Etching (h >20 µm – 200 µm)
- Side Wall Insulation
- Deposit Seed- and Barrier Layers
- Via Filling
- Wafer Thinning
- Front and Backside Metallization

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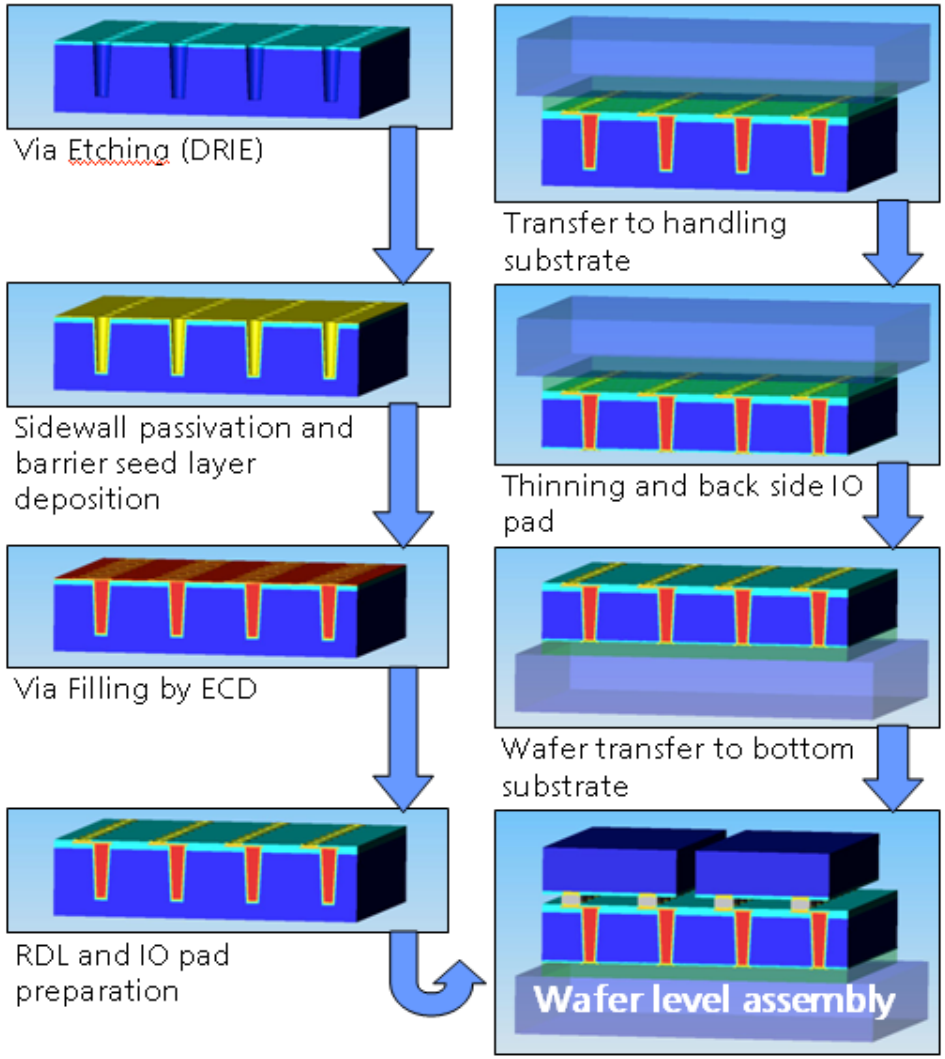
3D Integration using Through Silicon Vias (TSVs) for High Density Interconnects in Stacked Devices



Post Front-End TSV Process Flow

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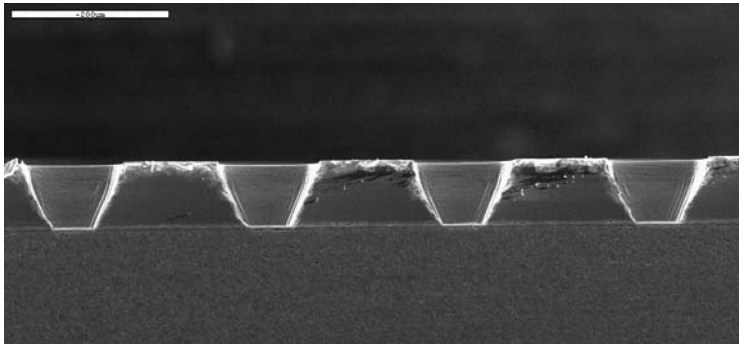
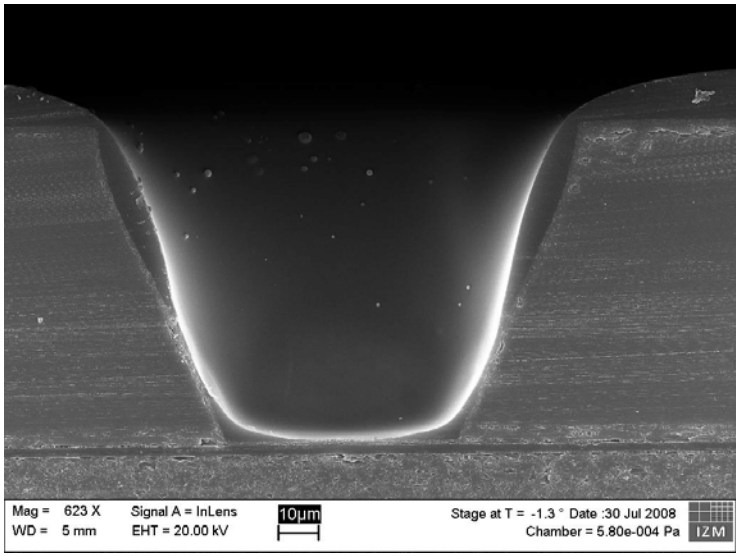
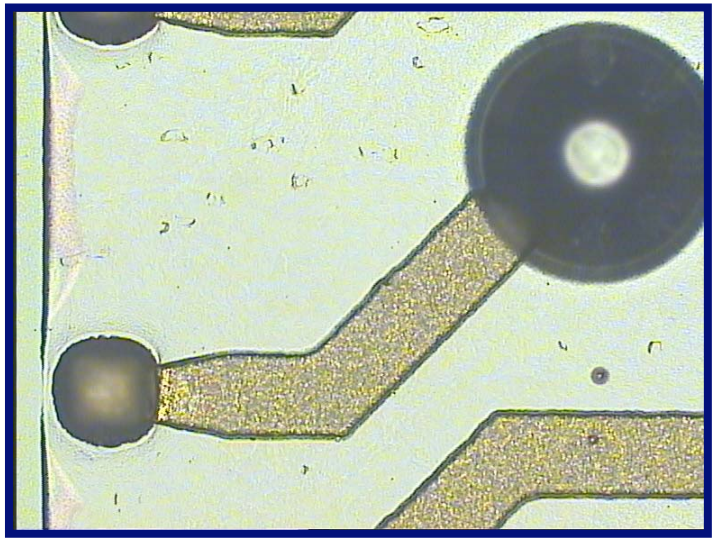
Tapered Silicon Vias

-- Low density backside contacts





Etched Vias



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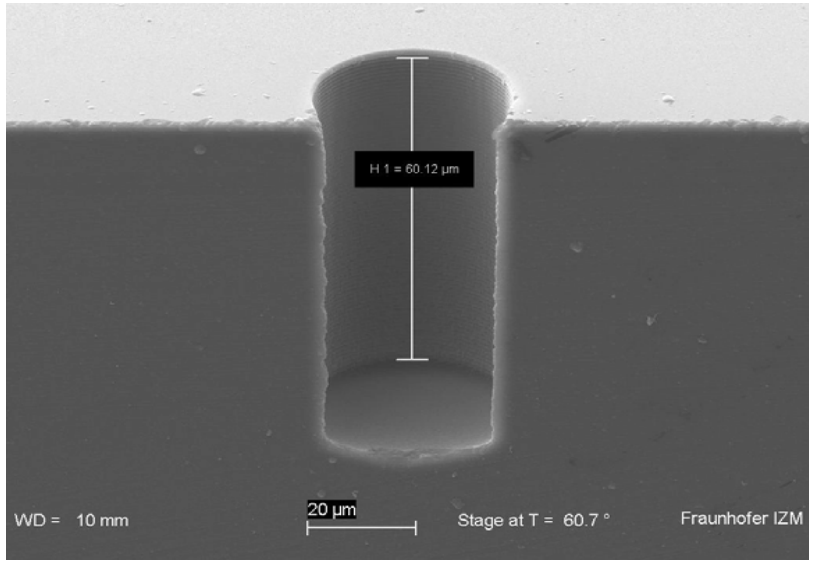
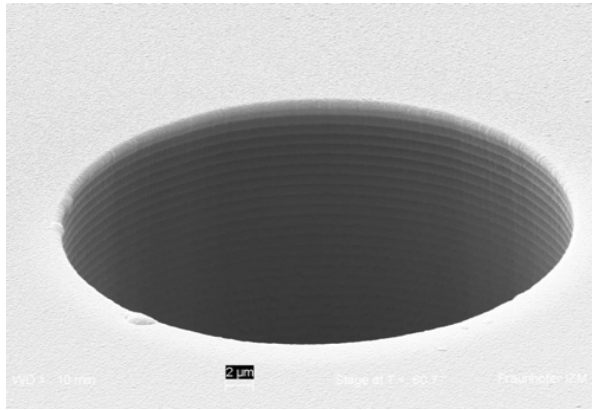
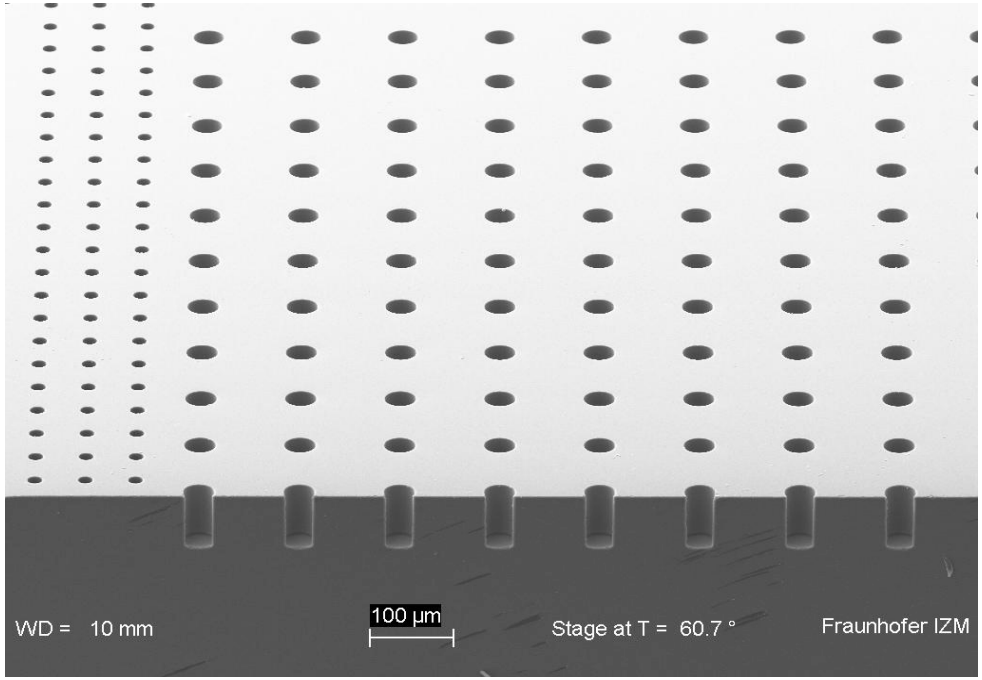
Deep Via Etching
TSV- Test Device – different Via Sizes



40 µm Vias
80 µm pitch
depth: 60 µm
CVD-Oxid: 120 nm





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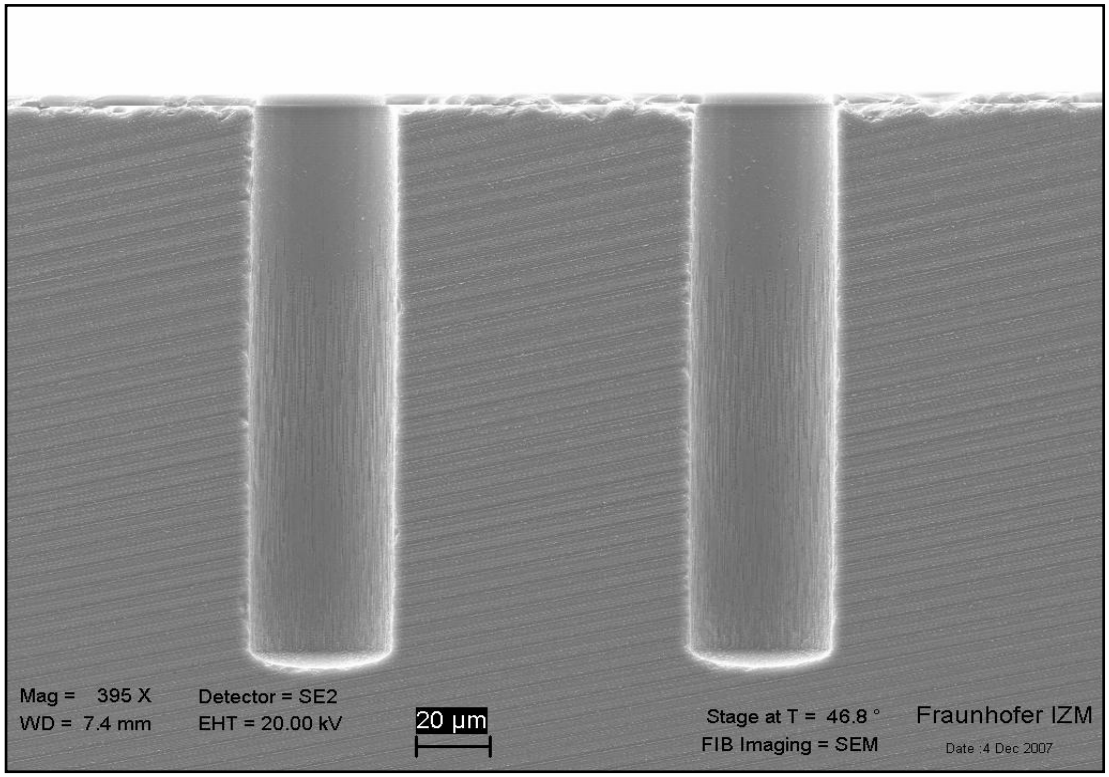
Via Formation by DRIE
(Bosch-Process)



Silicon via: Ø 40µm, depth: 160µm

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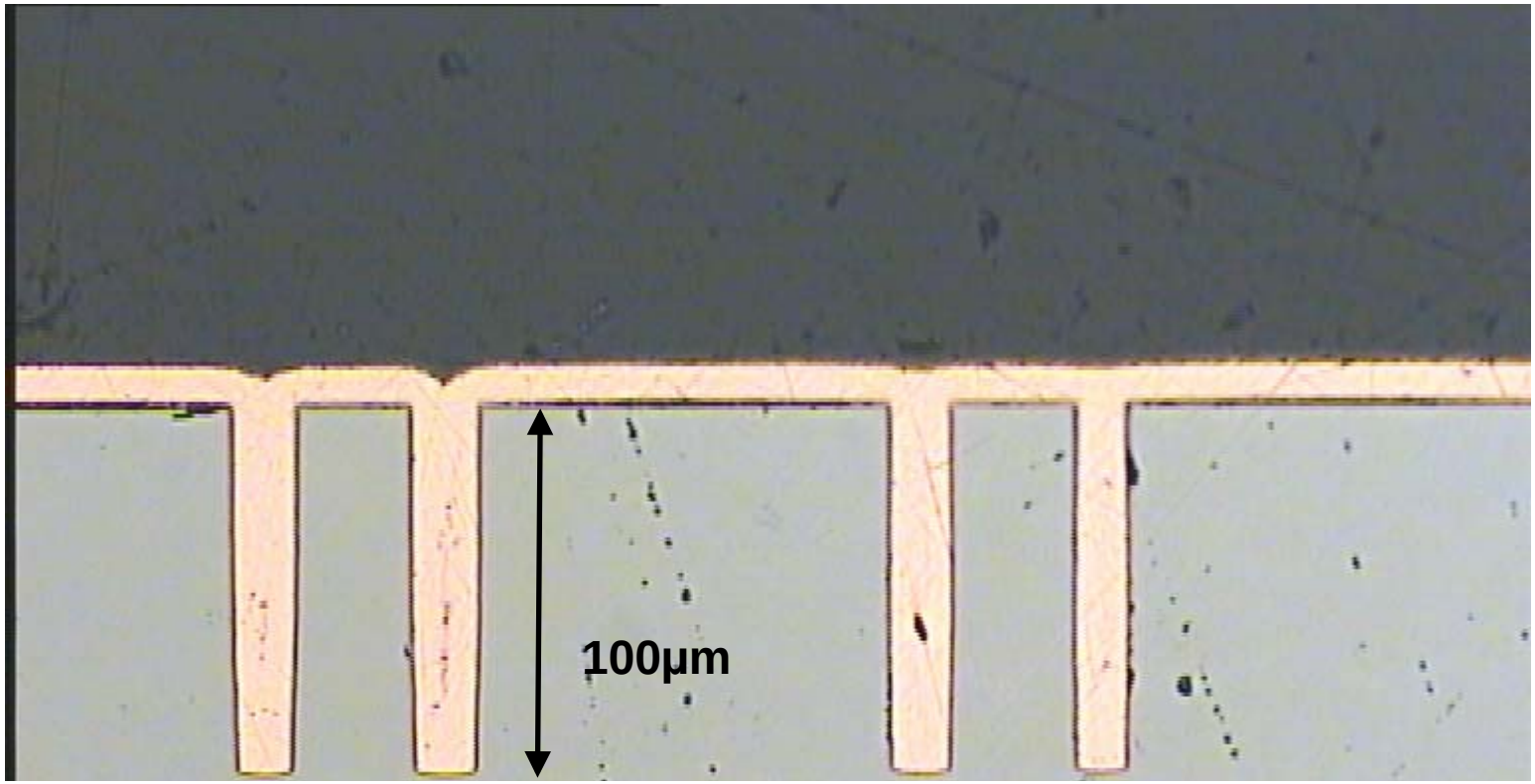
Through Silicon Via (TSV) Filling
Using Electrochemical Deposition of Copper (ECD)



Ø20µm
Depth: 100µm

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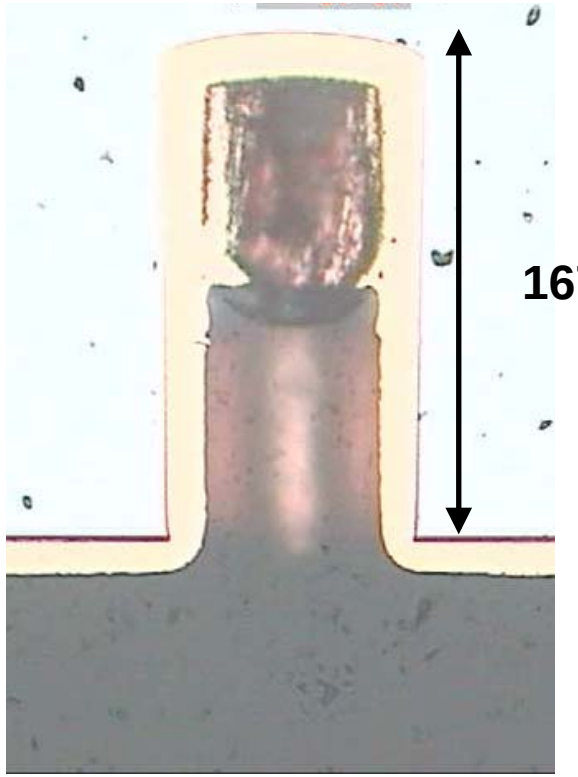
Testwafers for TSVs in FE dies



- Mounting to support wafer
- Thinning
- Etching the via from the backside
- Plating the sidewalls and backside
- Structuring the backside
- Supporting from the backside
- Opening the contact hole to the TSV from the frontside
- Metallization on the frontside

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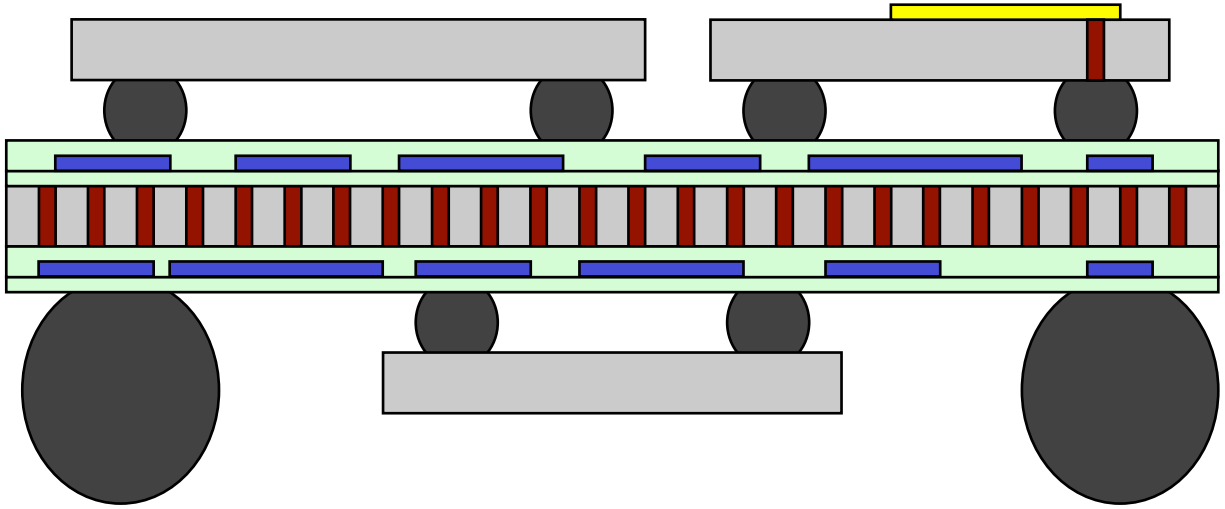
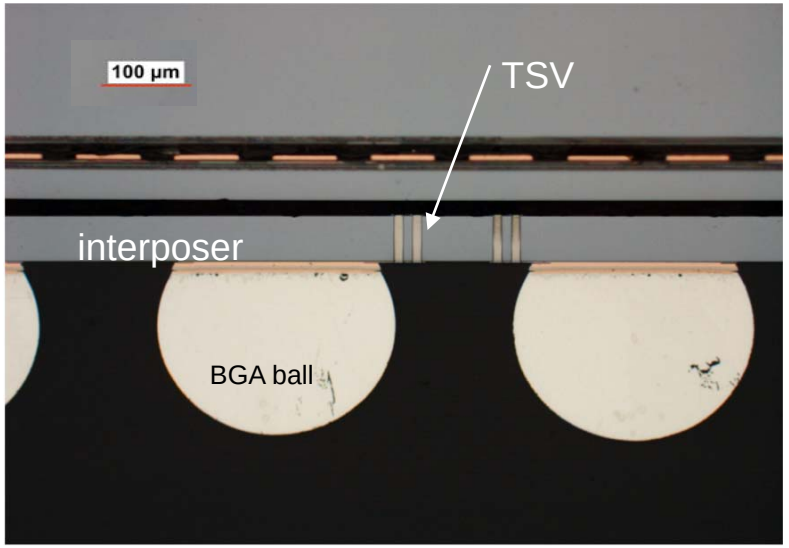
Silicon Interposers: Driving Force for TSVs



Interposer
with TSVs



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thank you for your attention

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