OVERVIEW OF THE PRE-FEI4 PROTOTYPE

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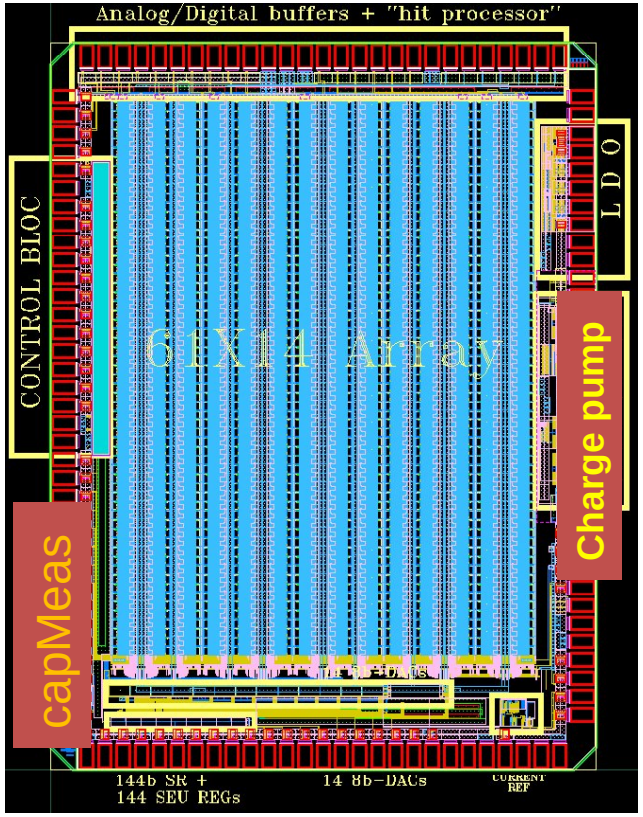
On behalf of the FEI4 collaboration (BONN, CPPM, GENOVA, LBNL, NIKHEF)

Introduction

- For the motivations, see Maurice's talk.
- The front-end is based on the FEI4_P1 design (some results will be shown).
- New distributed readout architecture with local memory to address new requirements. For physics simulation, and RO philosophy see Marlon's talk
- Configuration philosophy more a la FEI3: 1 shift register cell plus N SEU tolerant latches per pixel each with it own strobe.
- All the major analog blocs (FE, DACs, Bias and References, LDOs …) will be taken from FEI4_P1 without or with minor modifications
- We are trying to embed as much flexibility in the design as possible: one DAC for every bias, trim-able current reference, redundant config shift register, some programmable readout features etc …
- The large size of the chip presents some challenges : yield, power density and distribution, signal integrity, Xtalk, Power-up stability, etc …
- We are trying to address these challenges through collaborative efforts and due diligence and hopefully we can learn from current similar pixel projects (MEDIPIX, CMS pixels)

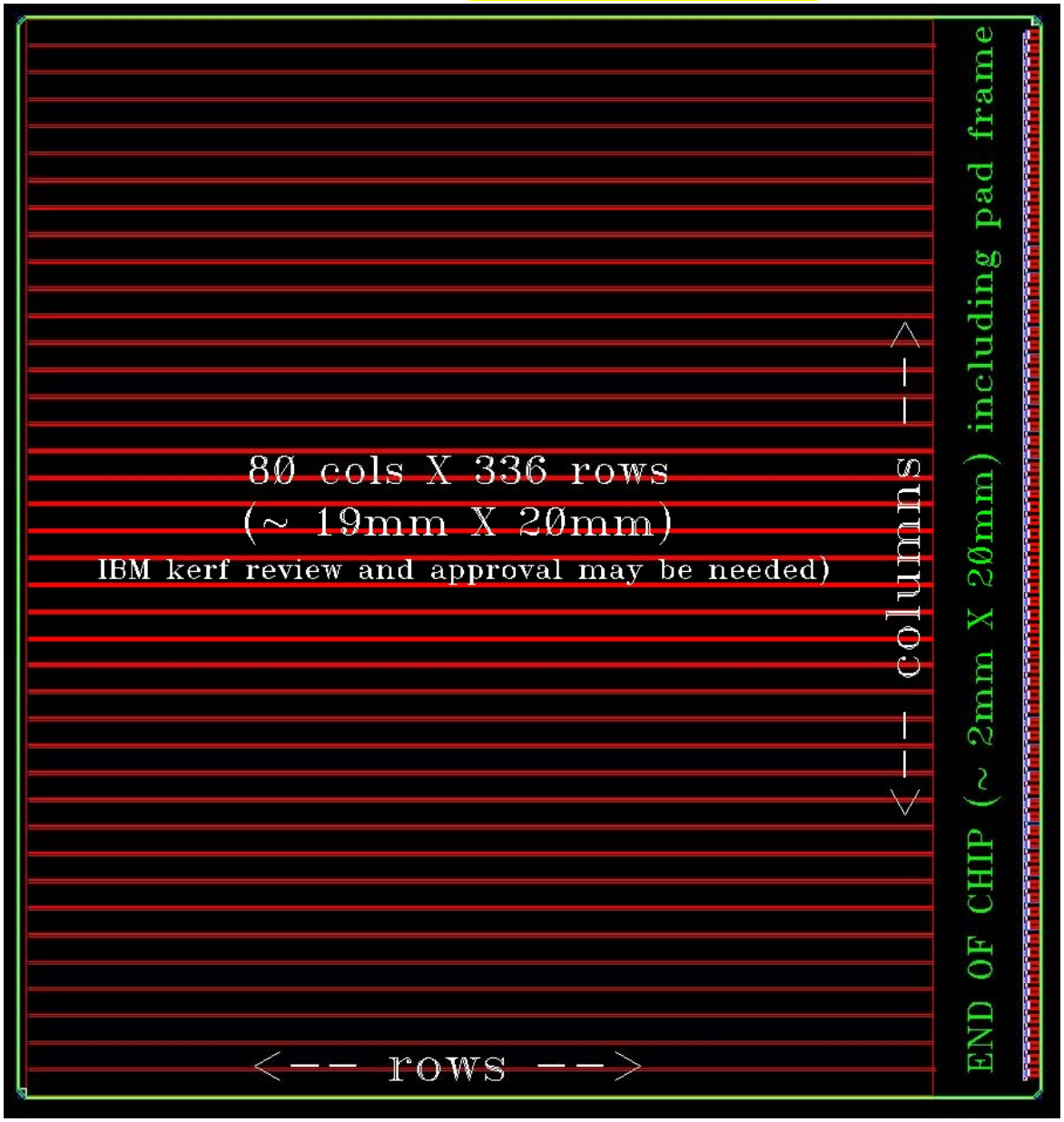
From FIE4_P1 to FEI4

FEI4_P1: 2008



3mm X 4mm
854 pixels

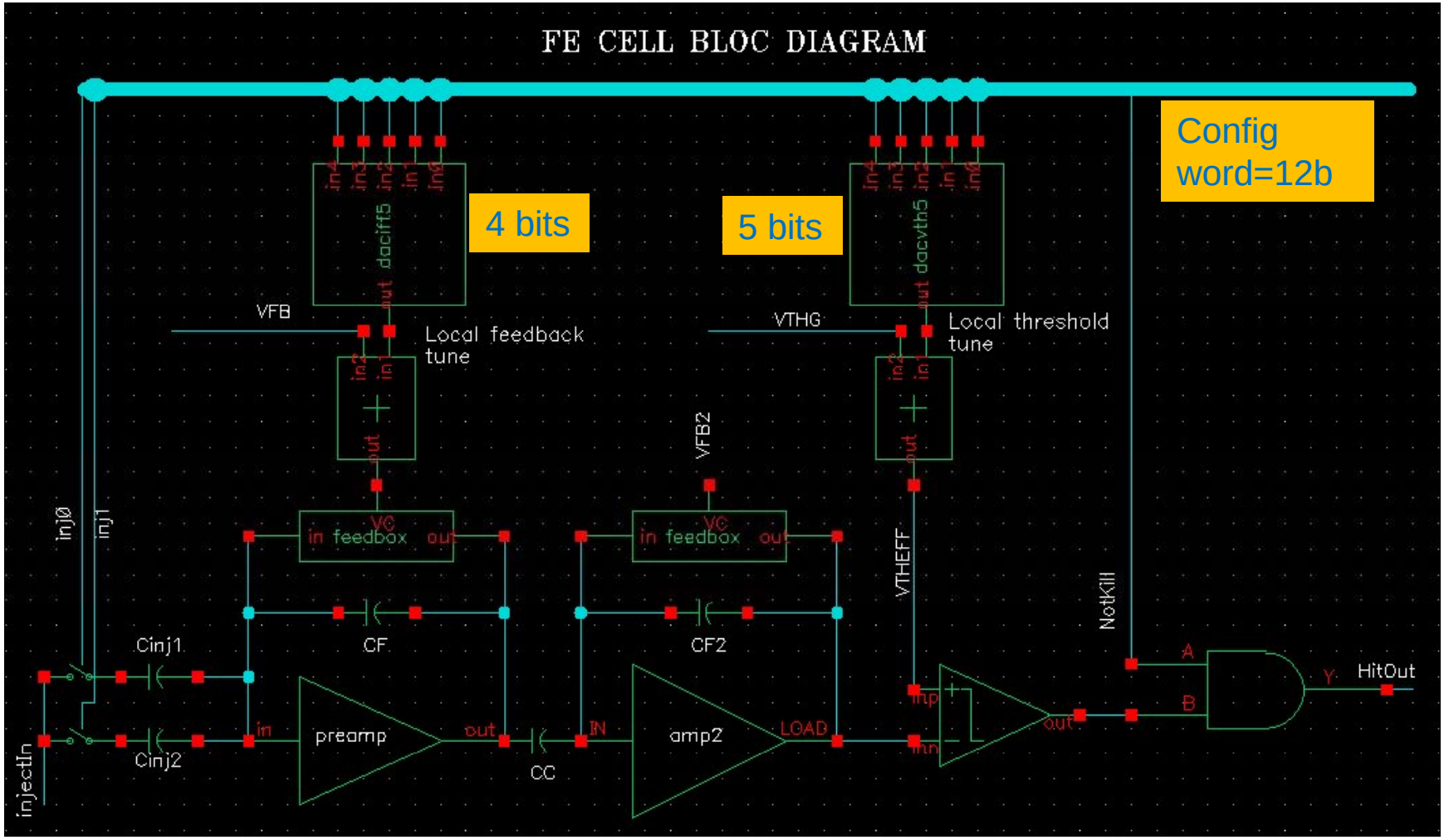
FEI4: 09/2009



19mm X 20mm
26880 pixels
(50μ X 250μ)

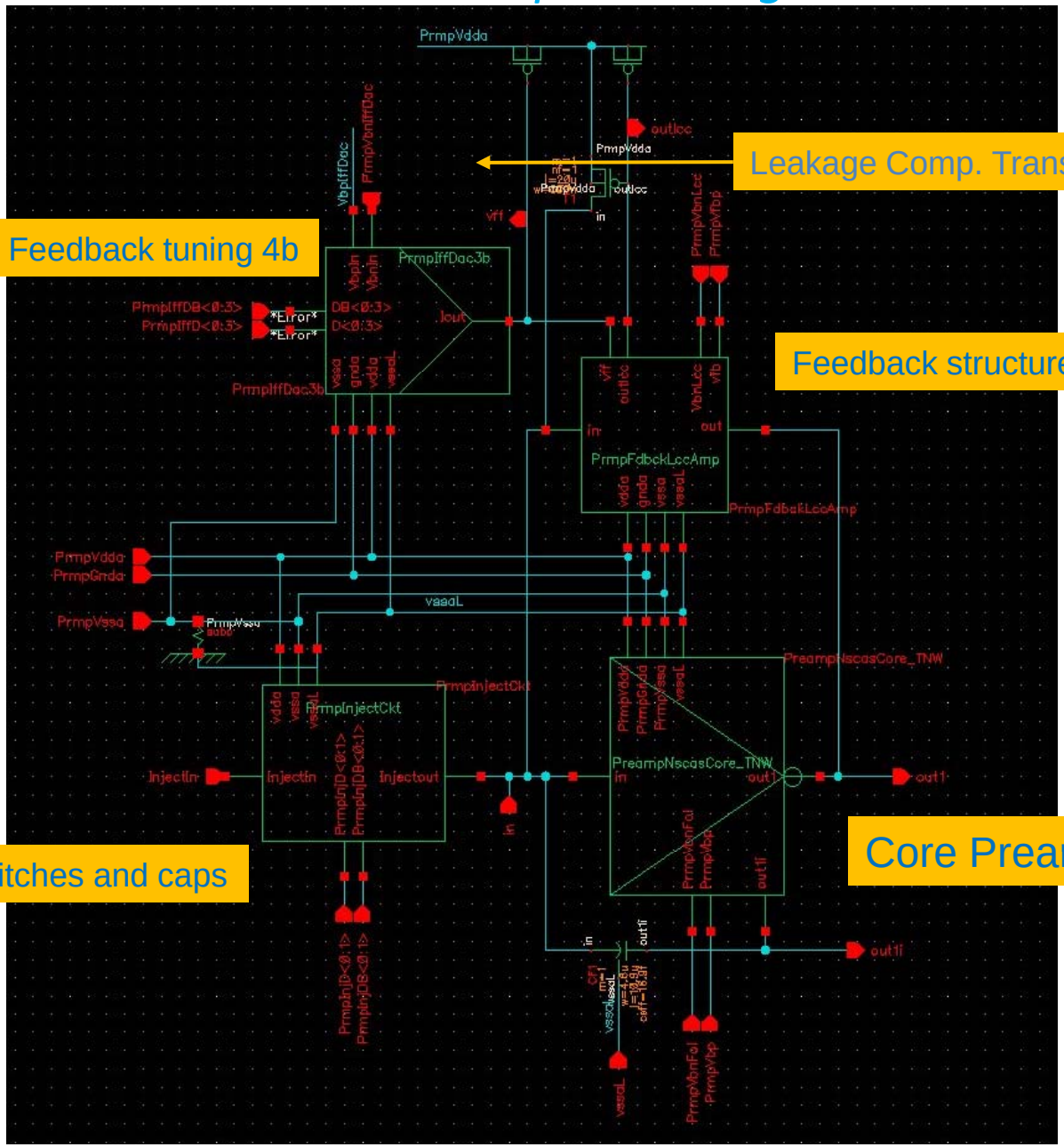
FEI3:
2880 pixels
(50μ X 400μ)

General cell architecture

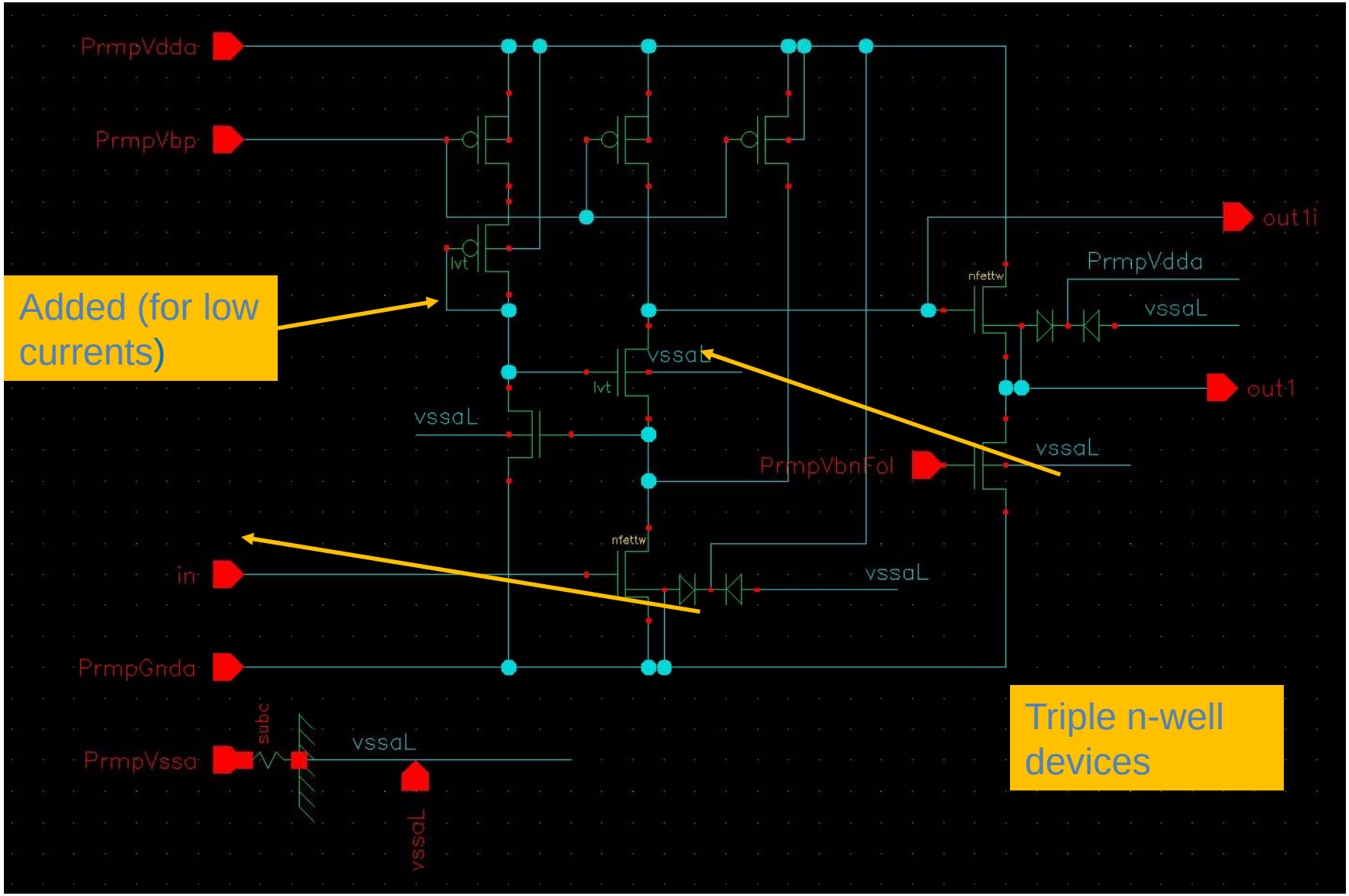


CF=17fF CC/CF2=5.8

Preamp Bloc diagram

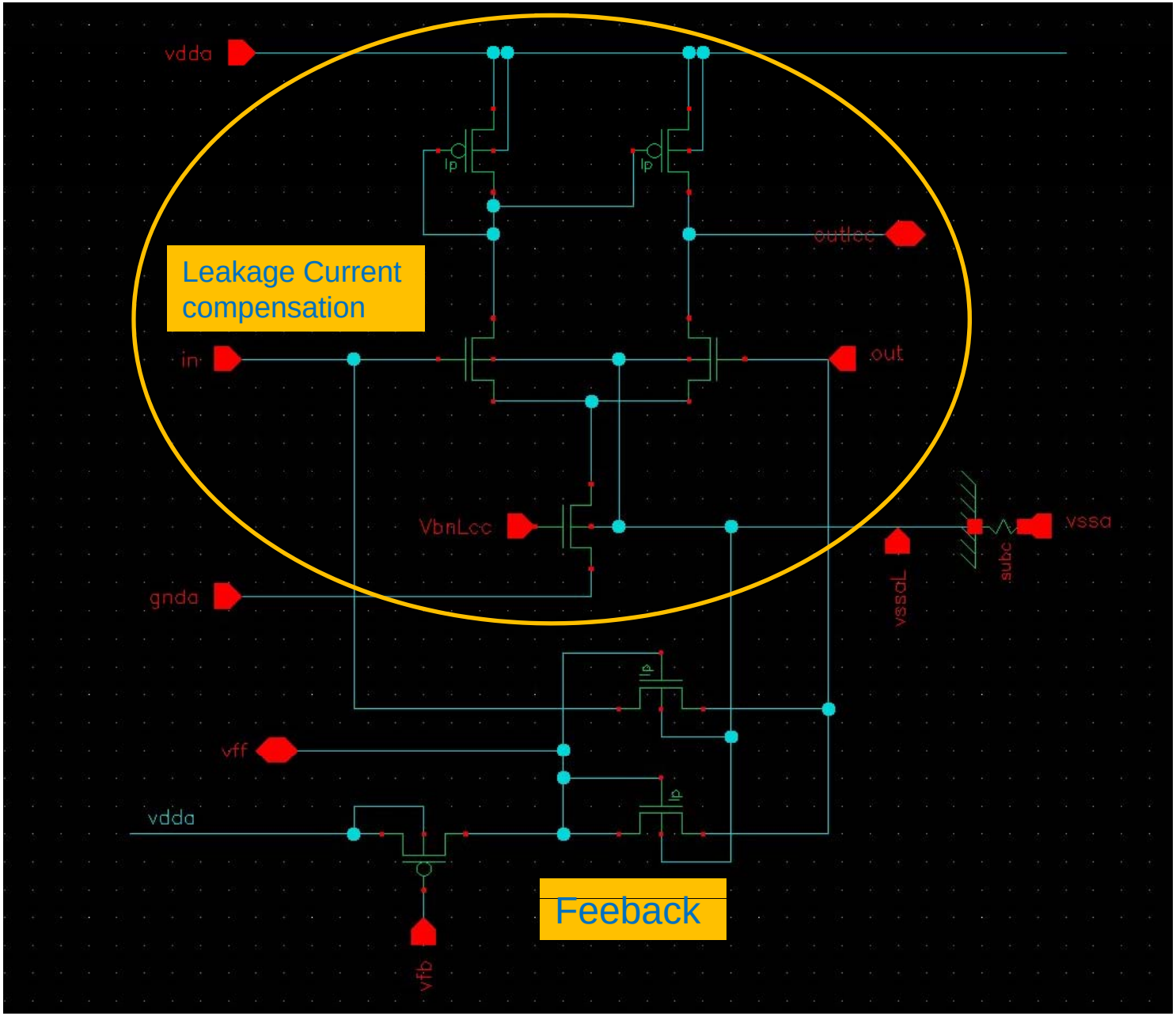


Preamp chosen variant

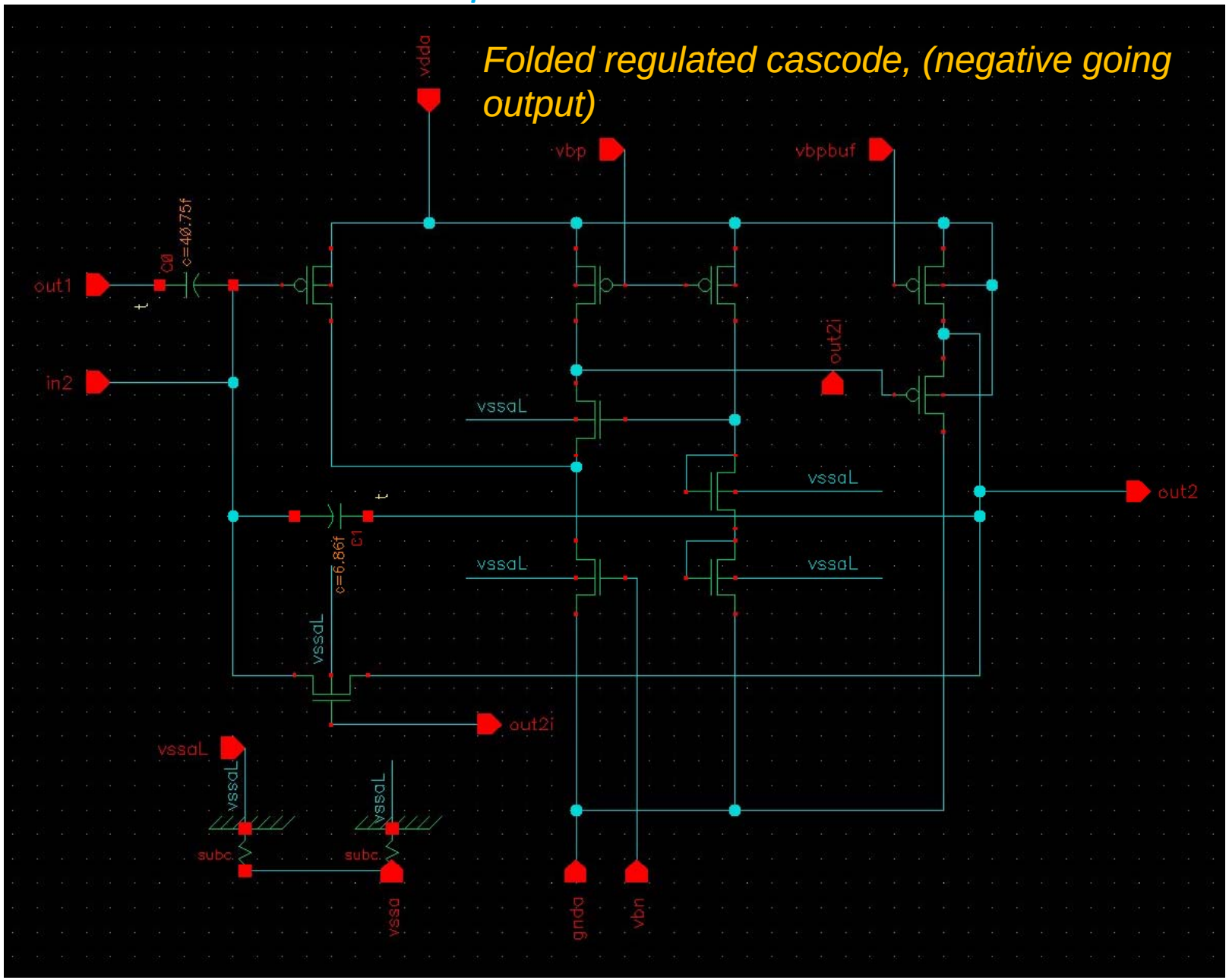


Straight regulated cascode, for electron collection (positive going output)

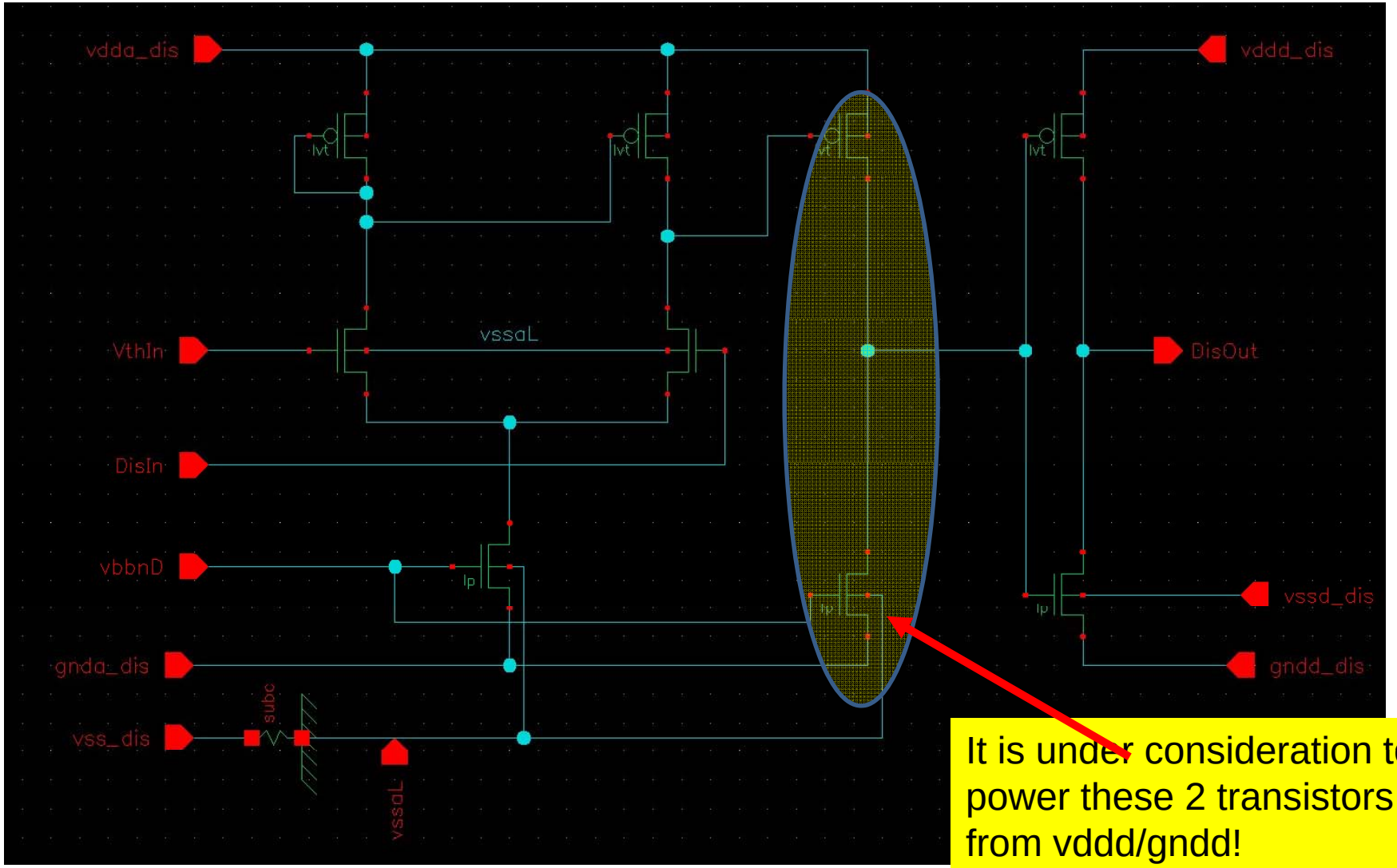
Feedback structure



Amp2 chosen Variant

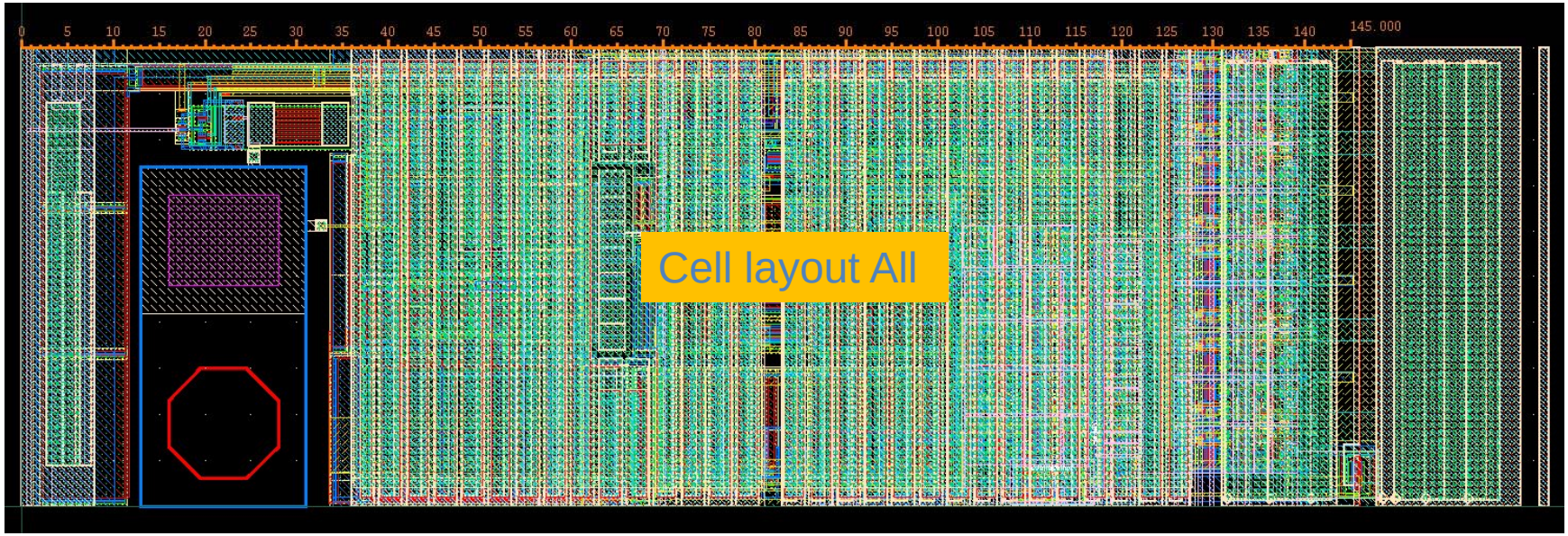


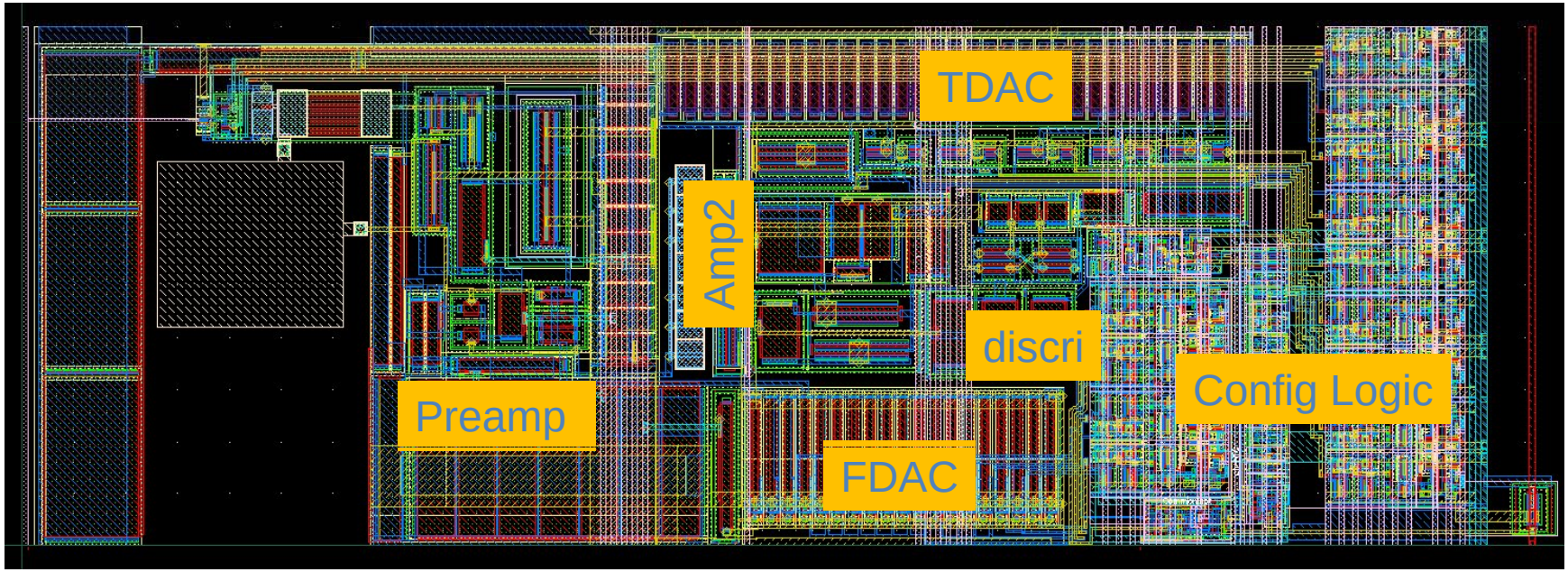
Discriminator schematics



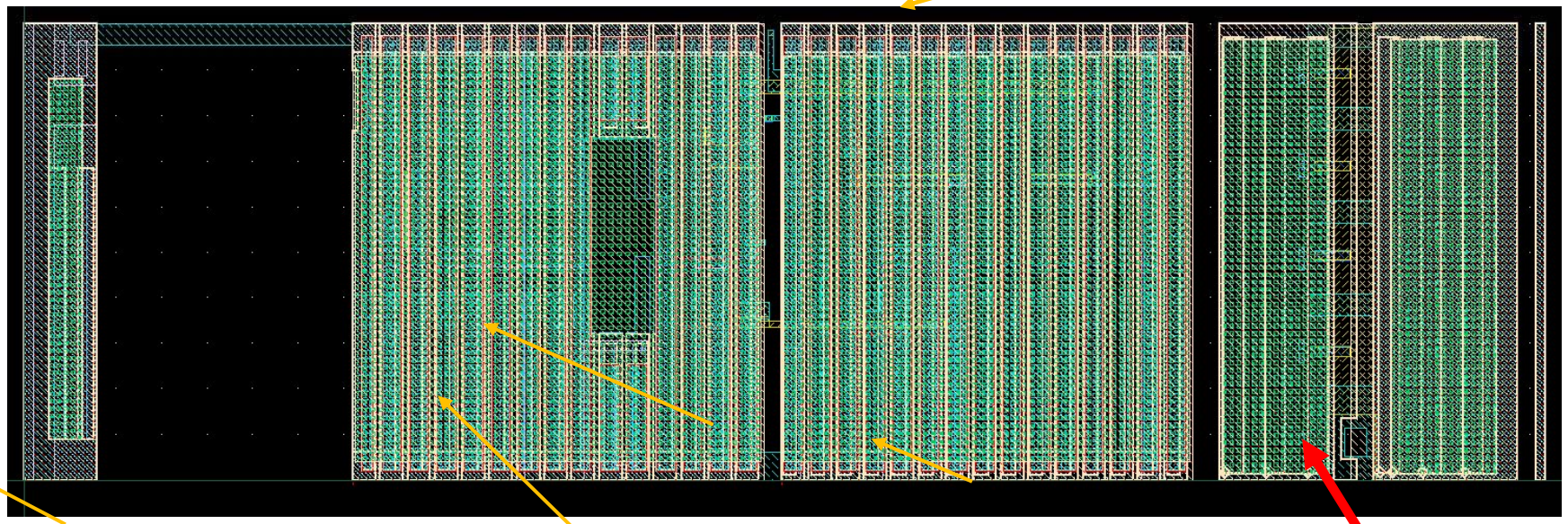
Classical 2 stage design. 3 ***different*** *transistor flavors!*

Cell layout:


0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145.000
Cell layout All


TDAC
Amp2
discri
Config Logic
Preamp
FDAC

Cell layout: Analog Power Scheme



Rdda < 13 mΩ (estimated maximum)

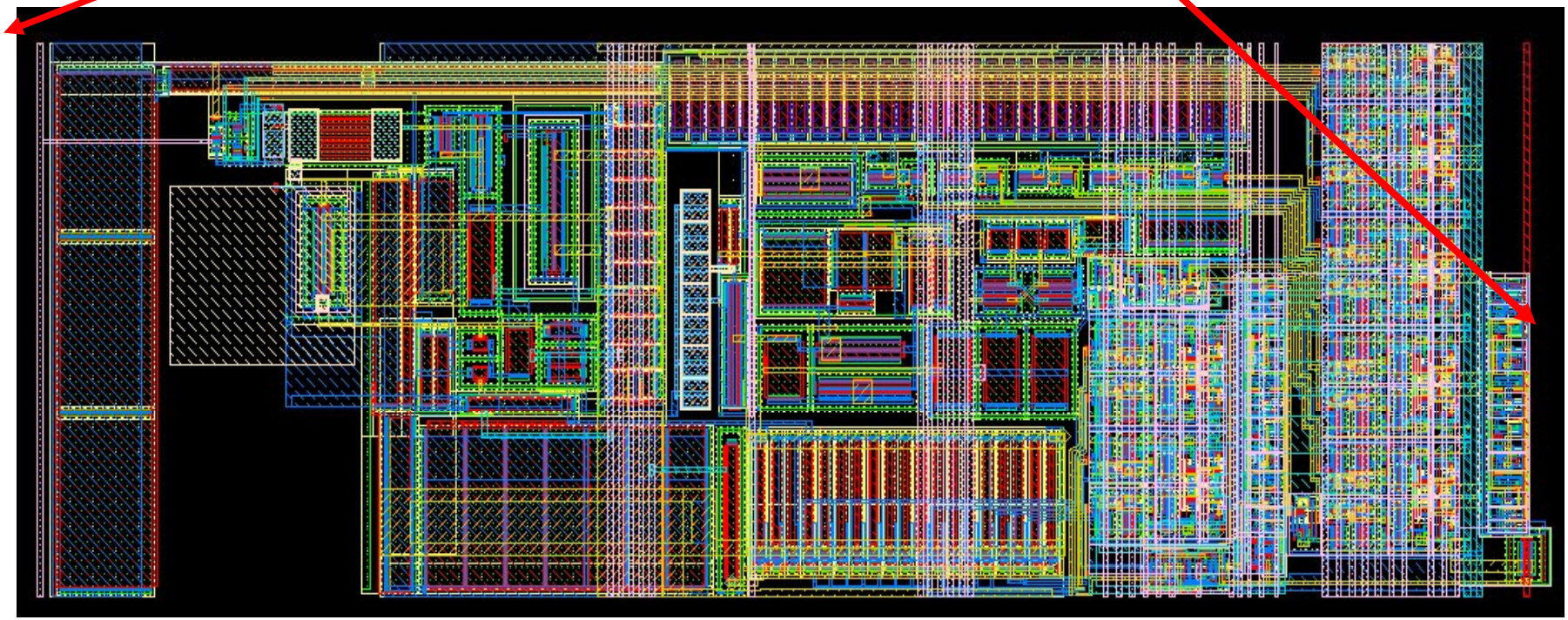
Δvdd < 20mV (assuming 25μa/cell, 350 cells/column)

LM is the main shield for the detector (MQ or Mx is used to fill the small gaps)

Measured Rdda: 11.2 mΩ/pixel pre-Irrad and 11.5 mΩ/pixel after 200Mrad
Δvdda < 10mV @ 336pixels and 15 μa/cell

New FE layout

- *Main FE layout will be the same (+/-)*
- *Redundant config SR added to the right*
- *A leakage current mirror will be also be added*

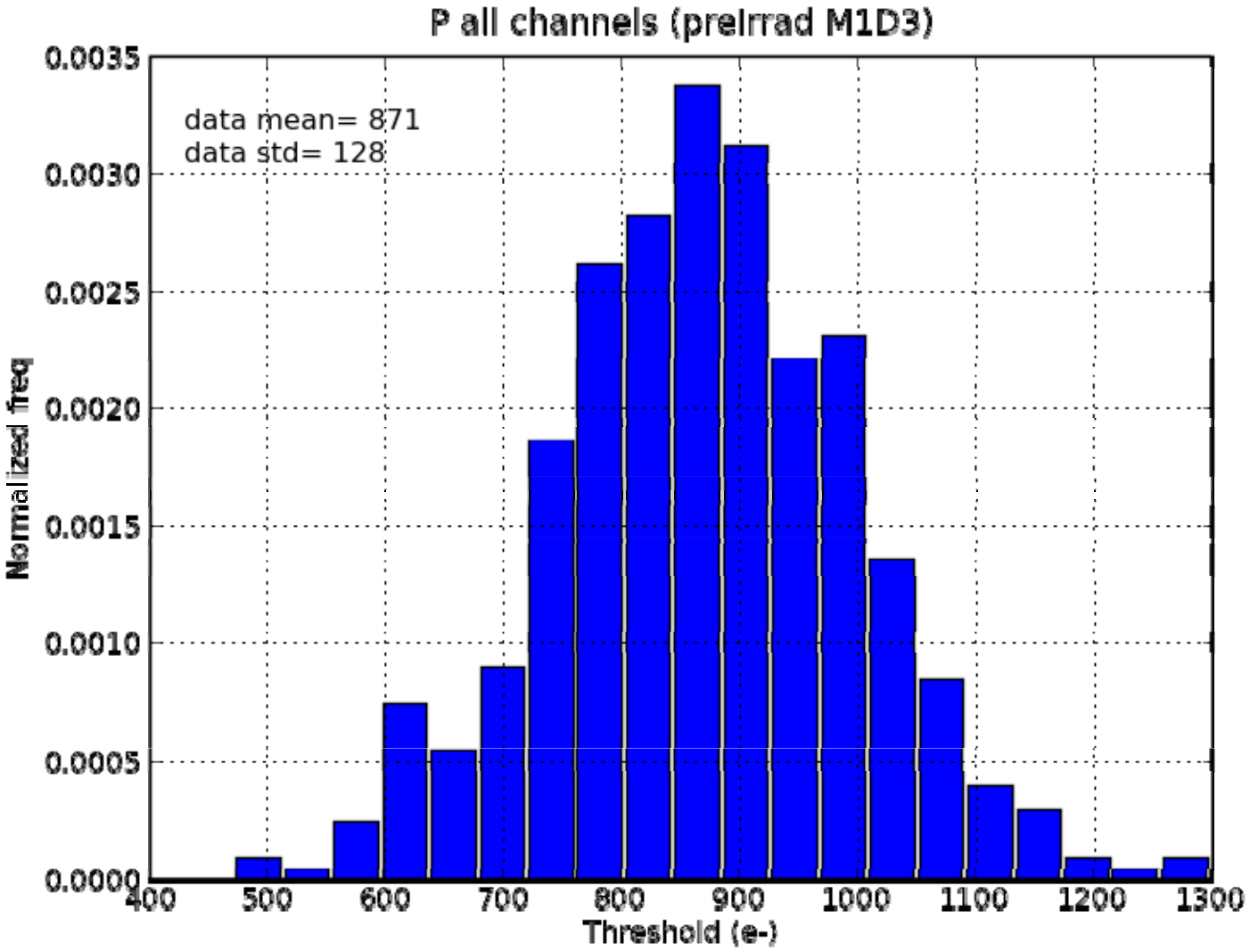



File Edit Vert Horz/Acq Trig Display Cursor Meas Mask Math App MyScope Utilities Help Button
Tek Run Average
25 Feb 09 17:59:36
ch 4/60 (with cap) @low current and high occupany setting (30ke)
TH~1800ke (>50%)
Curs1 Pos
55.6ns
Curs2 Pos
76.0ns
th; th+1ke; th+2ke and 45ke
1
C1 500mV Ω
R1 500mV 20.0ns
R2 500mV 20.0ns
R3 500mV 20.0ns
C1 t1 : 55 .6ns
t2 : 76 .0ns
Δt : 20 .4ns
1/Δt : 49 .02MHz
20.0ns/div
2.5GS/s 400ps/pt
A C2 280mV

Pixel per Pixel feedback tuning

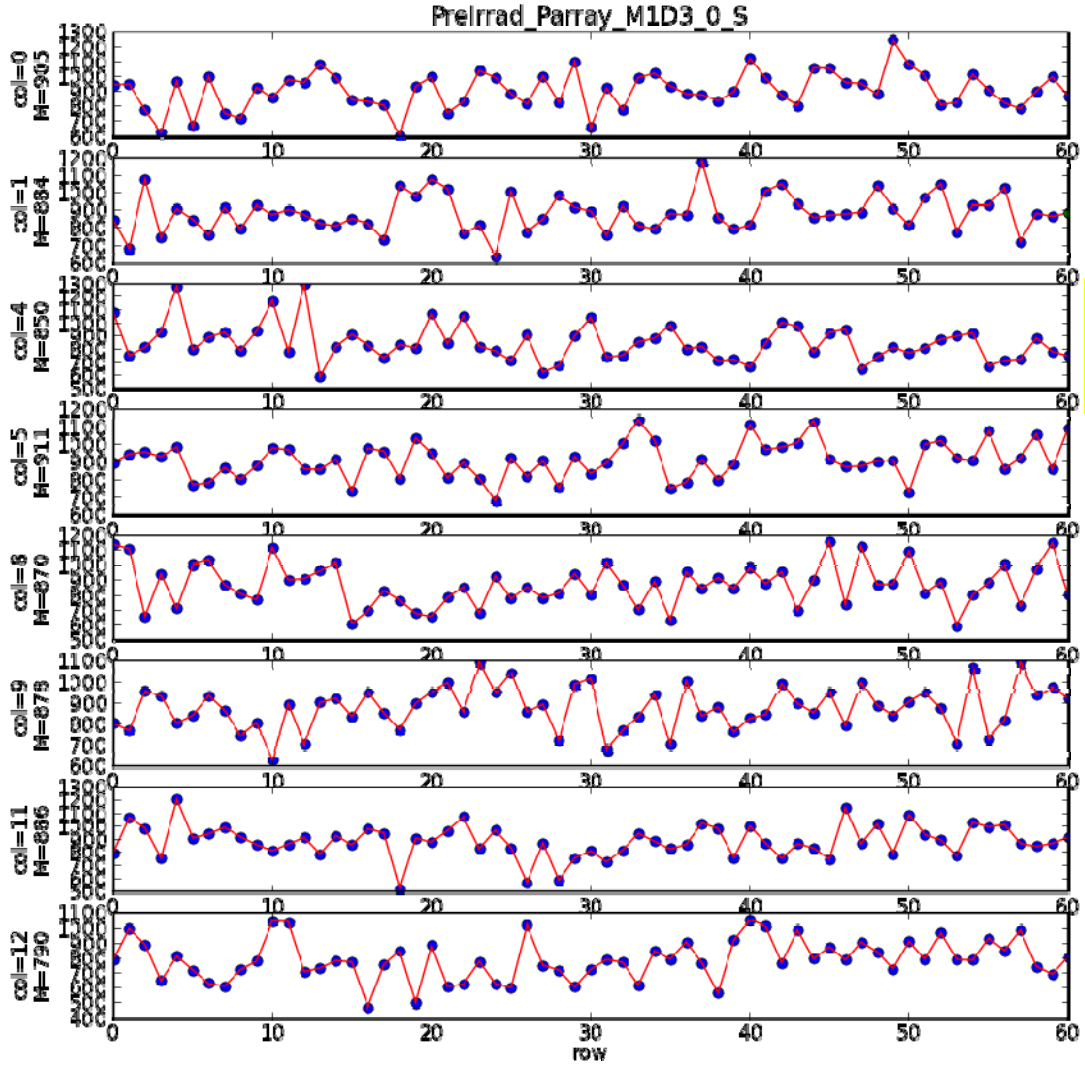
- Channel(12/60) with no input capacitance after 200Mrad.
- Step is programmable
- This on top of the global feedback current

P type pixels threshold distribution



NOMINAL SETUP @ 17μa/CELL

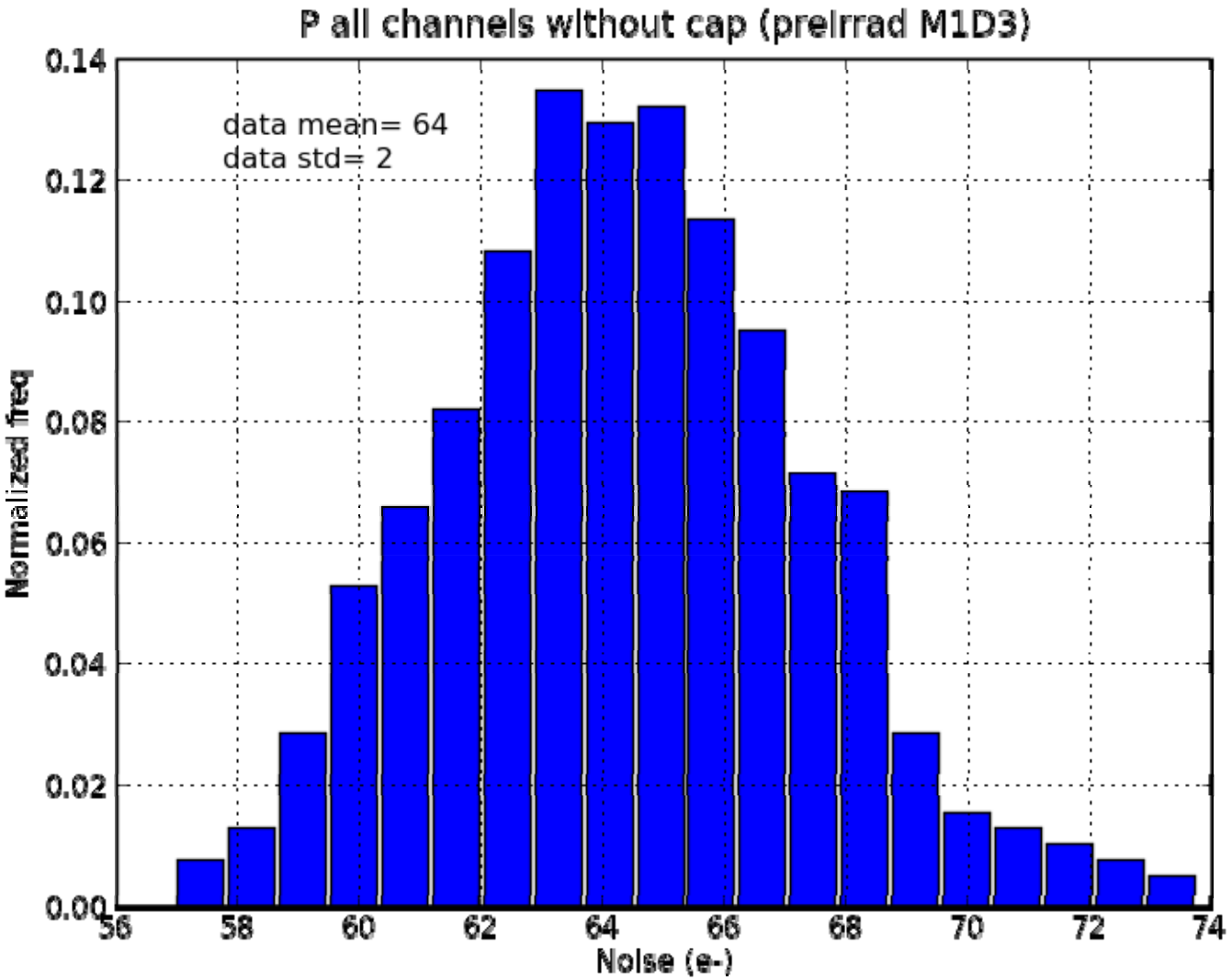
P type pixels threshold column by column



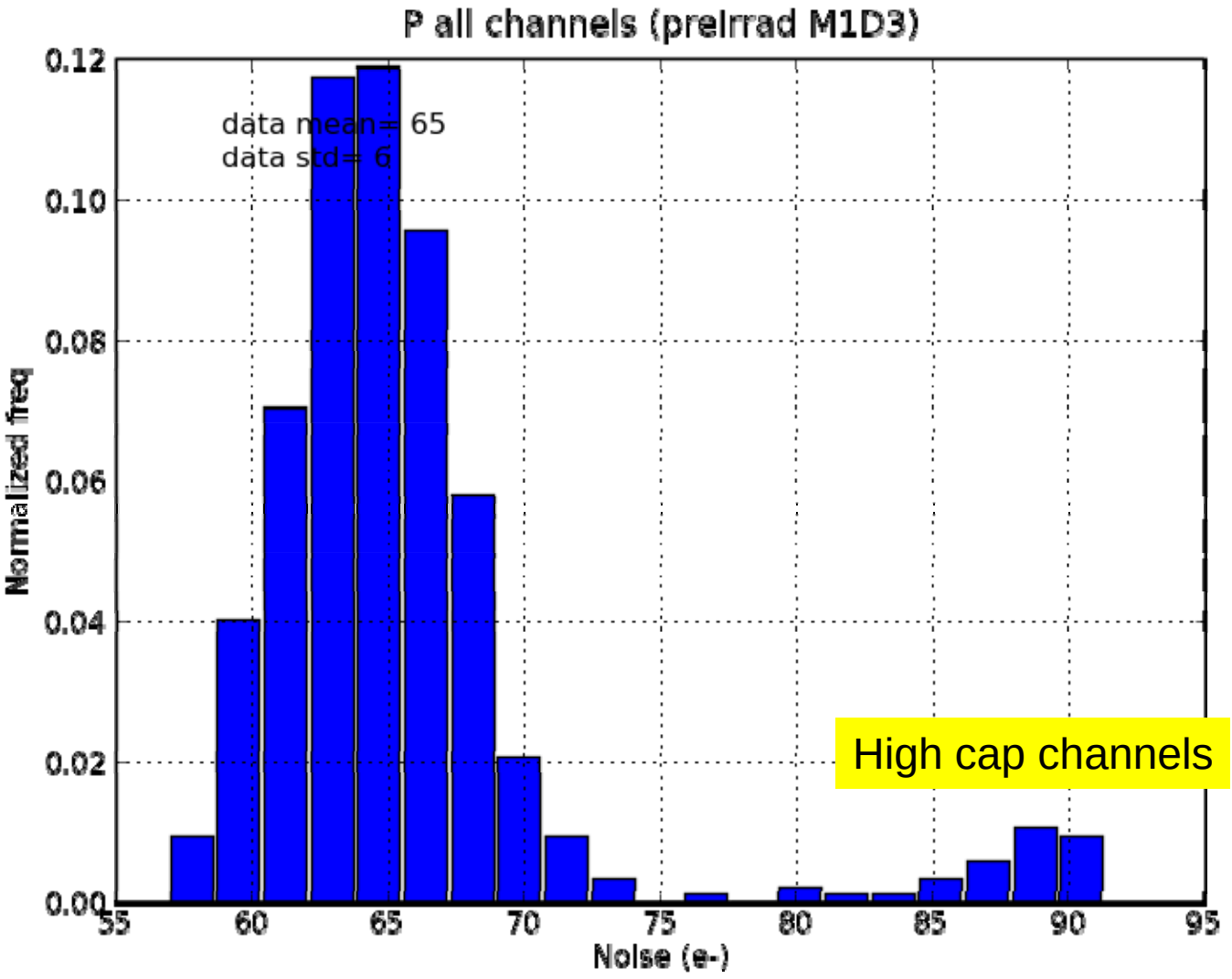
Row 31->60 have nwell diodes(caps) added

before irradiation measurements nominal setup @ 17μa/cell

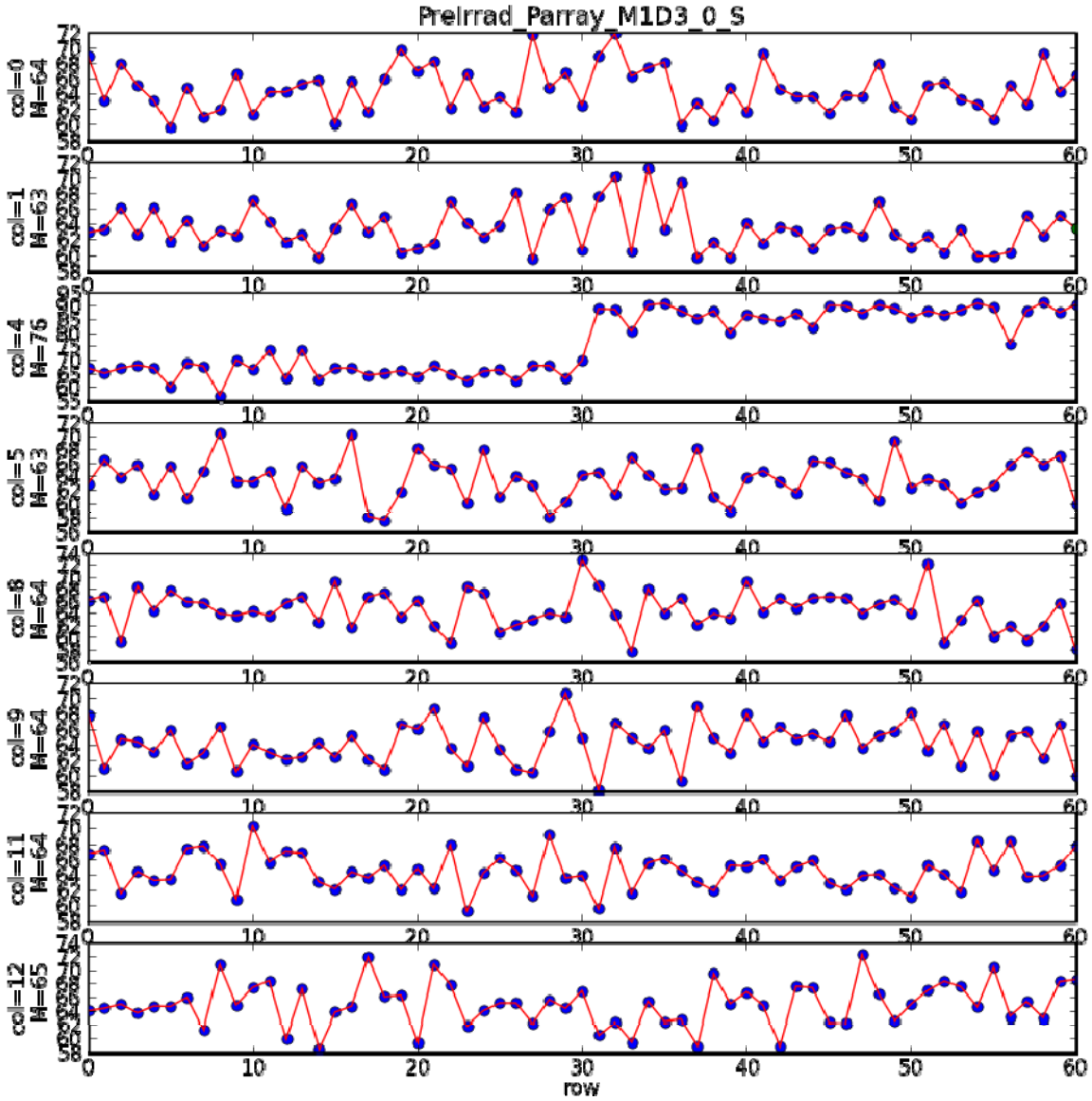
P type pixels ENC distribution (excludes cells with caps)



P type pixels ENC distribution all

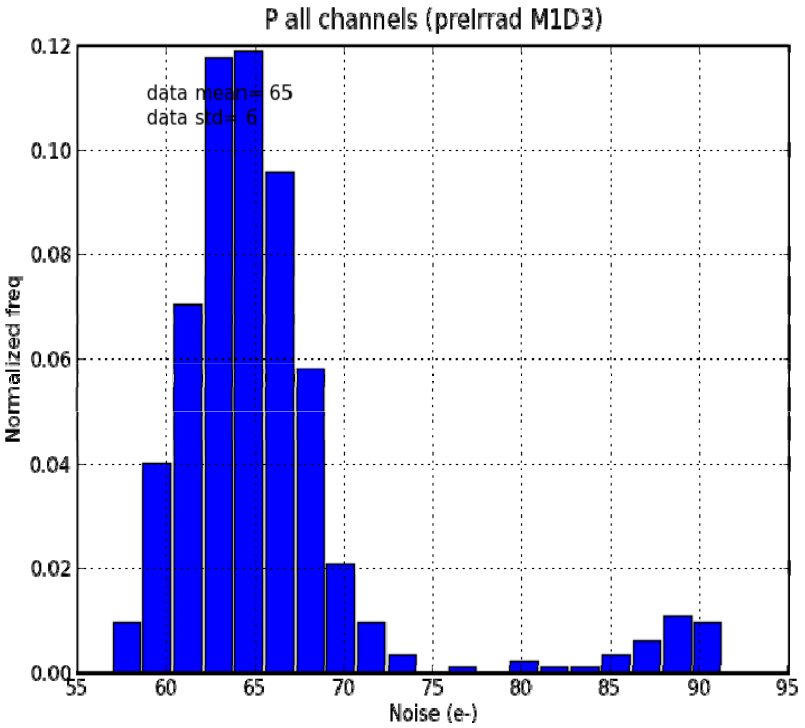


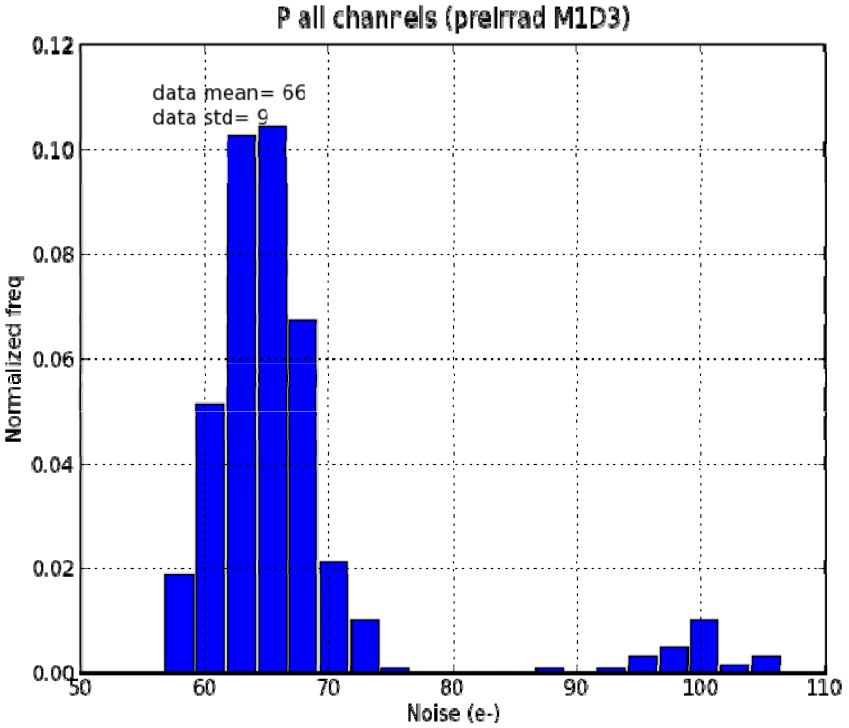
P type pixels ENC column by column



Row 31->60 have nwell diodes(caps) added

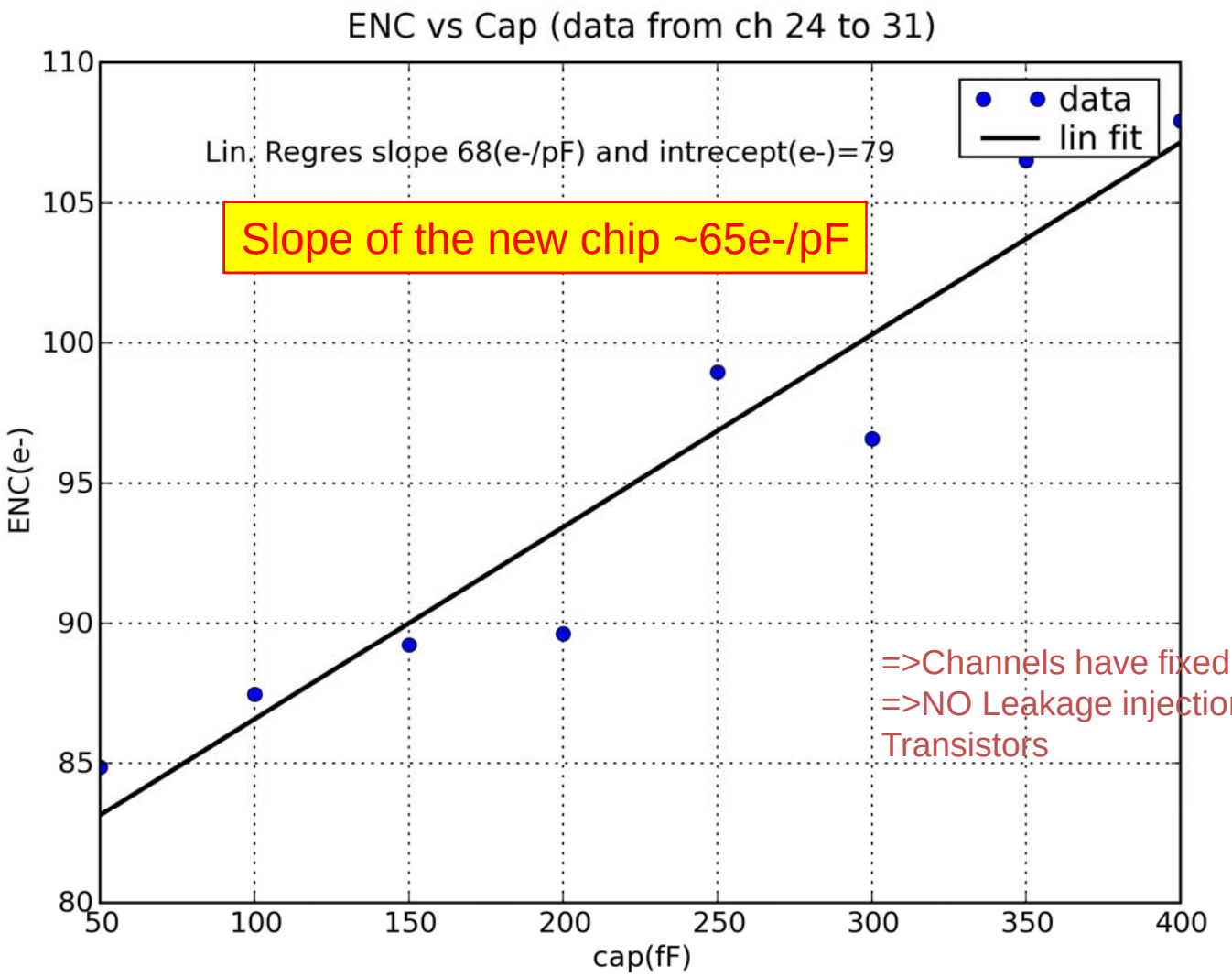
ENC @17uA/cell versus 12uA/cell





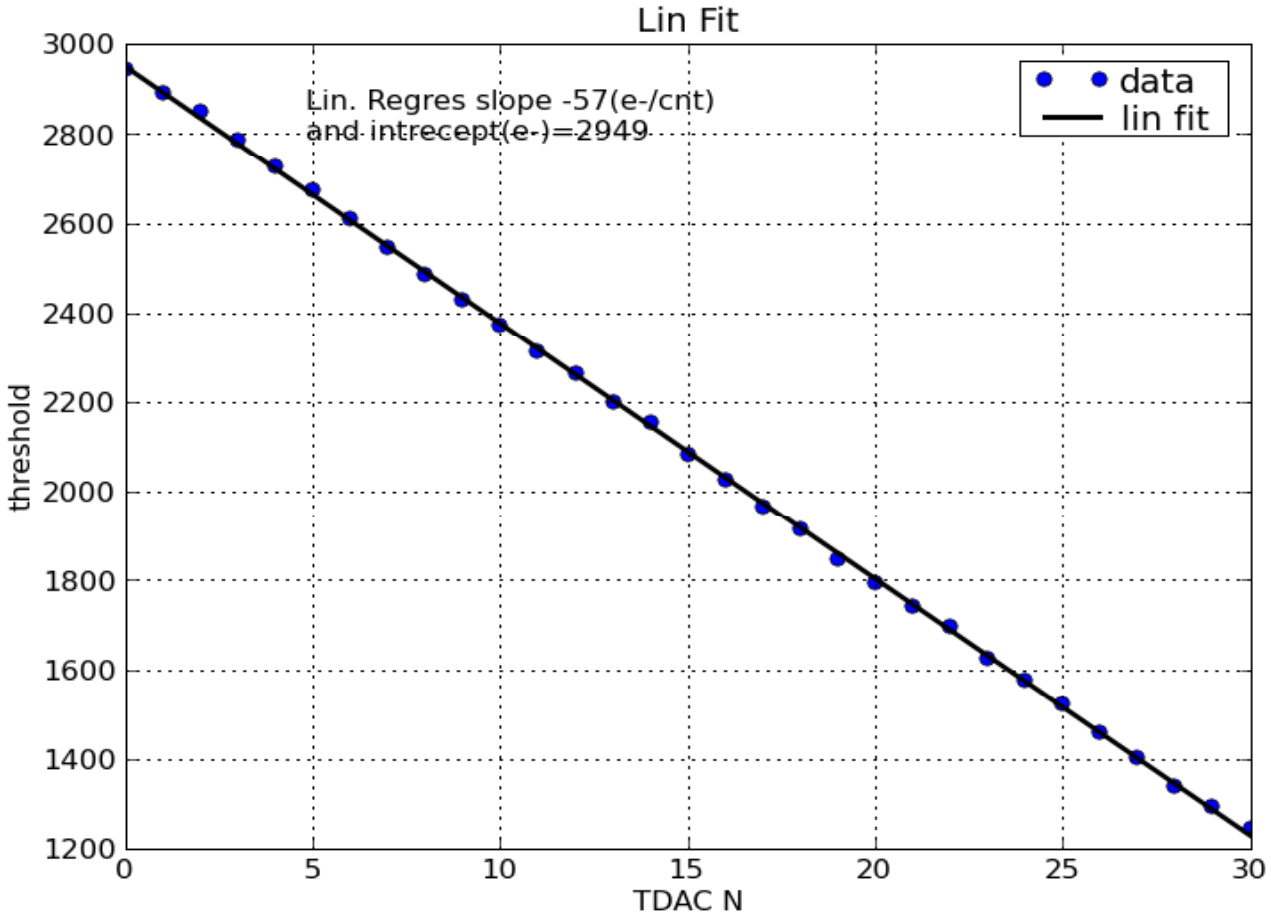
Only preamp current was reduced!
Preamp current nearly halved!

Old result for the APUP chip



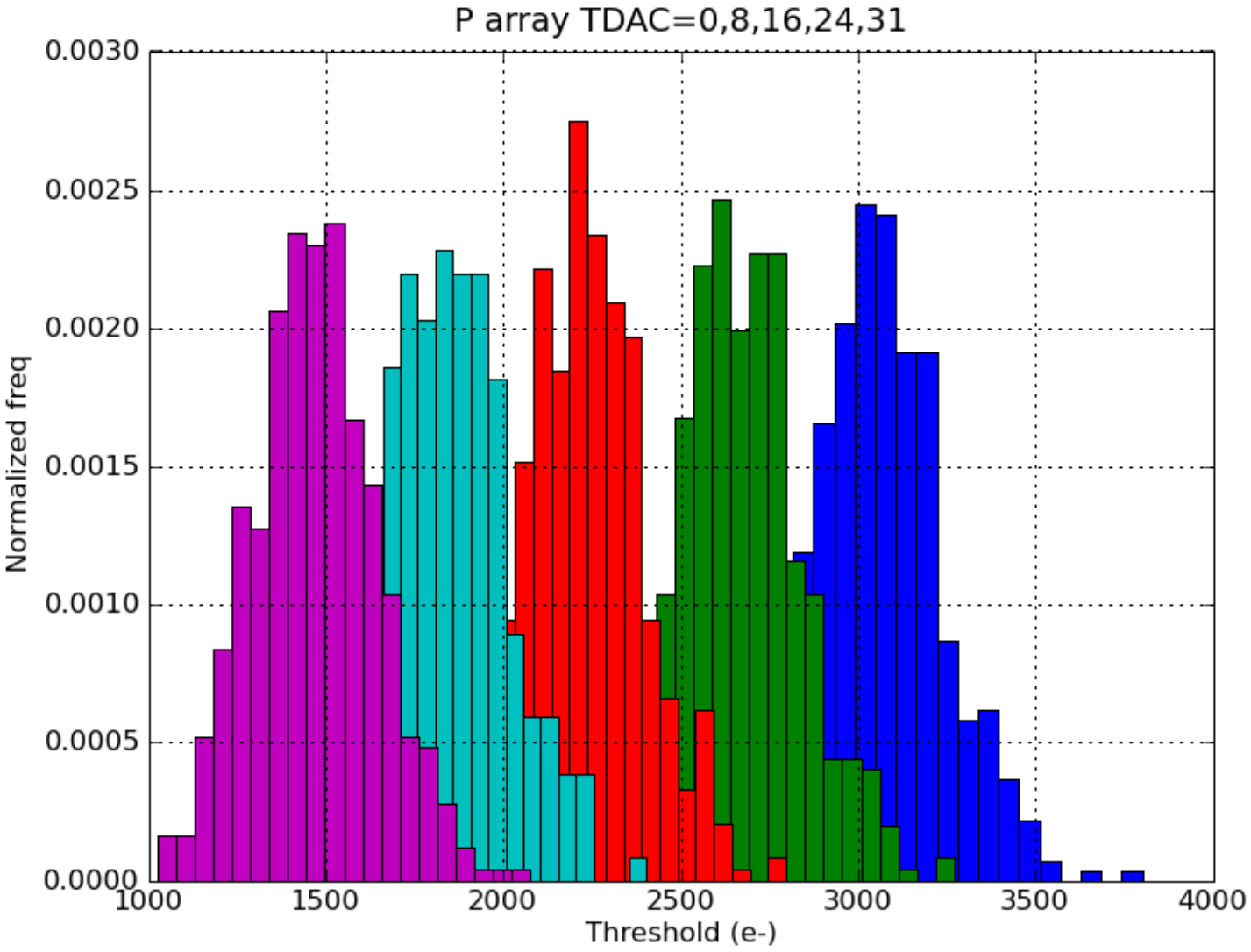
=>Channels have fixed cap
=>NO Leakage injection
Transistors

Threshold tuning: TDAC linearity



Slope set by a global DAC

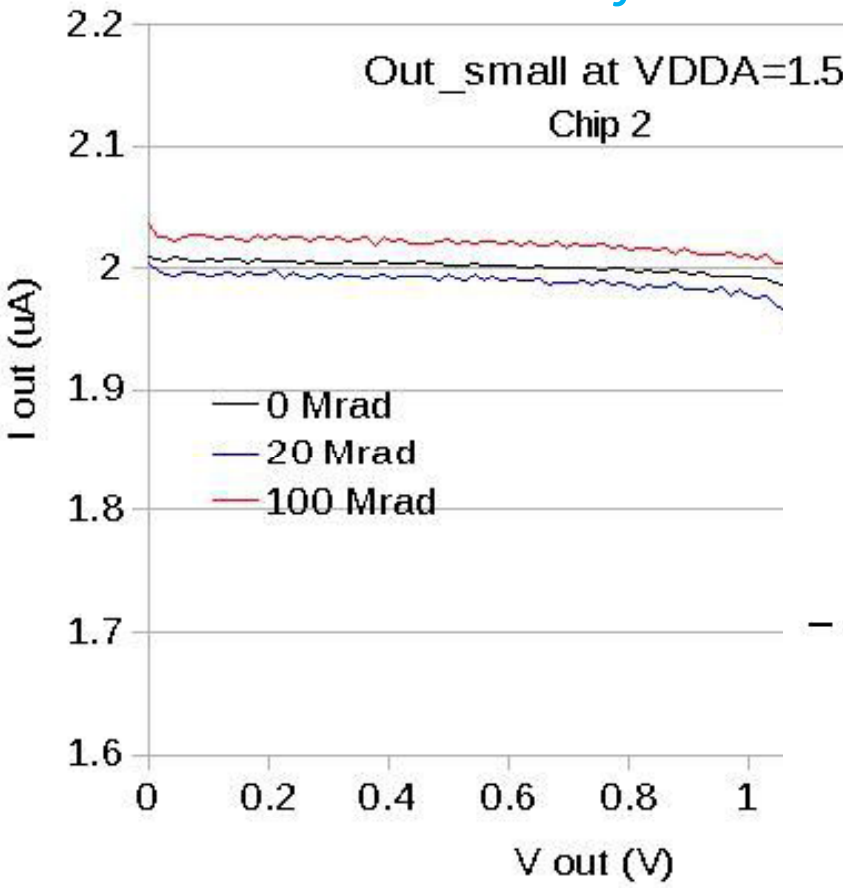
Threshold tuning: the whole P array (732 pixels)



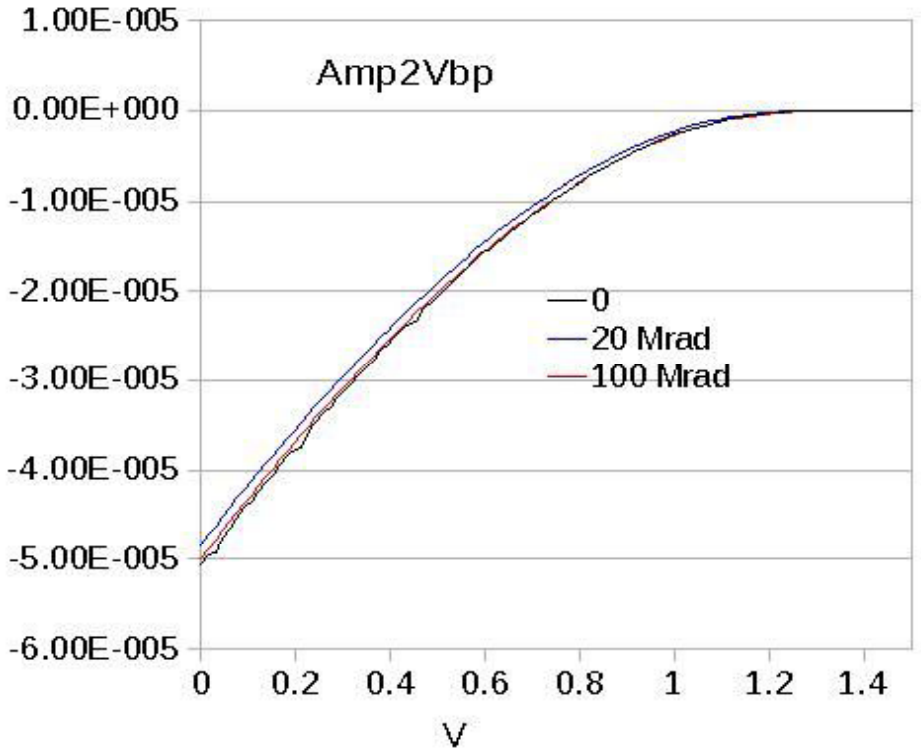
After 200 Mrad

Bias and Dacs: Radiation effects

Current reference

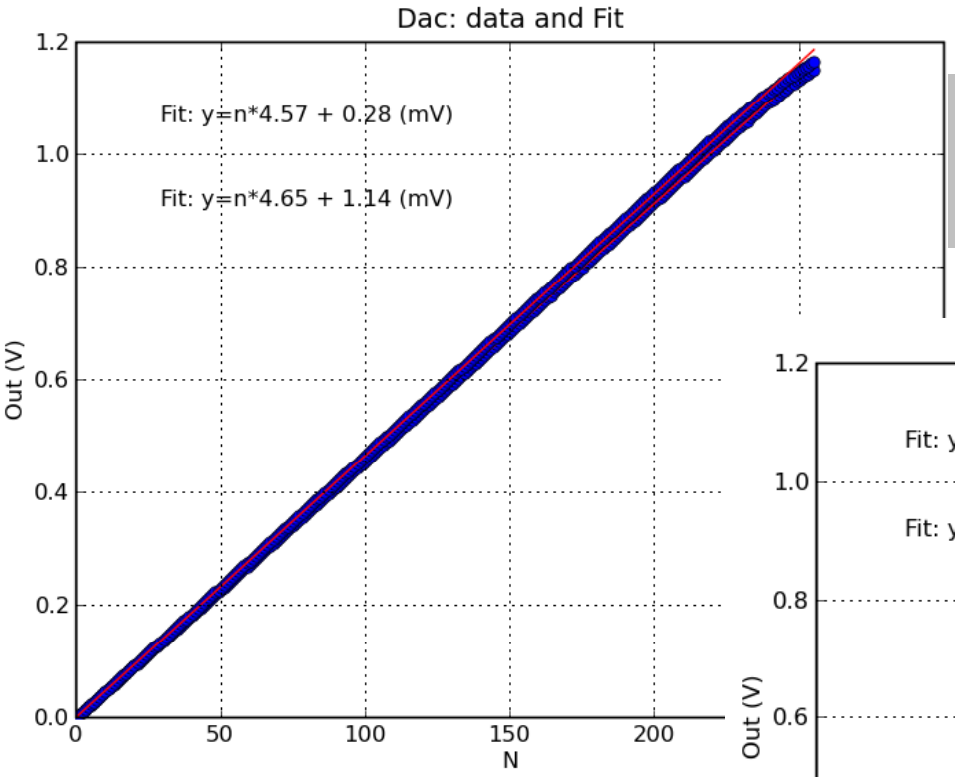


A bias DAC



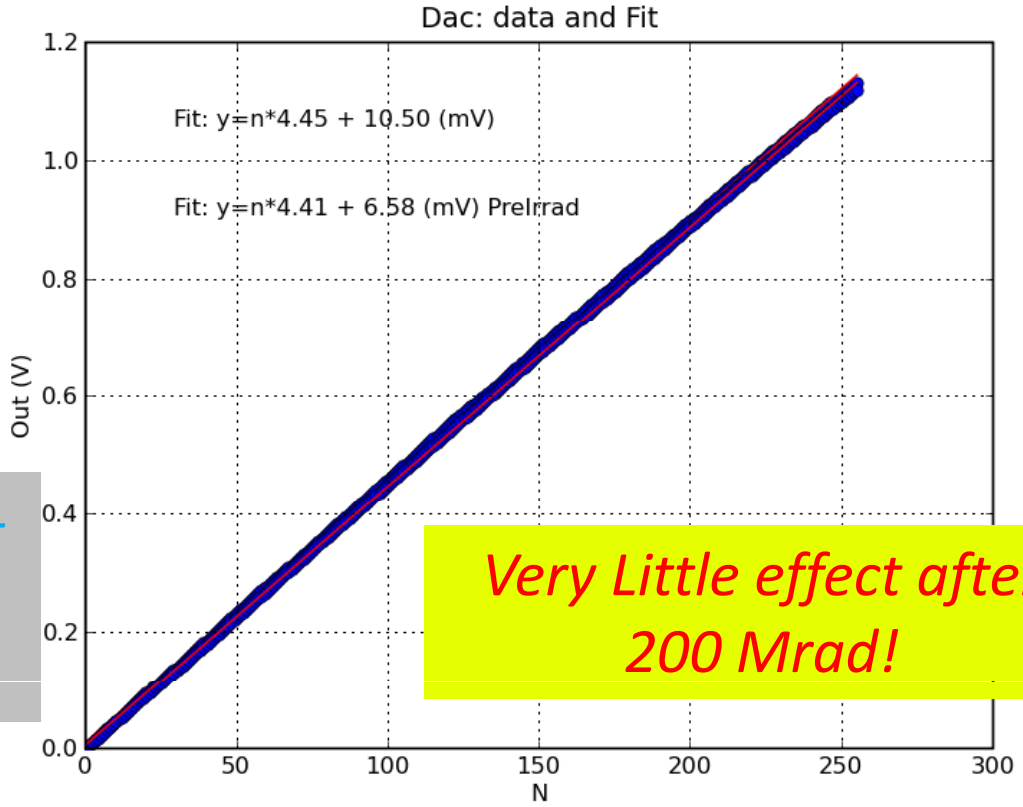
✓ ***Small effects!***

Bias and Dacs: Con'td



<= 8 bit DAC with < +/- 0.5 LSB Integral linearity (X3 area)

8 bit simple DAC with < +/- 1.5 LSB Integral linearity =>



Very Little effect after 200 Mrad!

Cell logic: template and design methodology

- *Based some initial idea(guess) on signal and power routing constraints propose a template that would be filled with circuit elements.*
- *Signal characteristics (delay and IR drop) are more predictable with an almost predefined structure to be imposed to the PR tool.*
- *Easier layout: Density rules could be almost satisfied beforehand.*
- *Power, ground, substrate and global signals are imposed. The rest preferably generated automatically by synthesis and PR tools.*
- *Based on that template, we have generated a realistic complete baseline design to study (and refine)*
  -Readout architecture
  -Xtalk and signal integrity
  -Power and shielding scheme
- *This design will be used to create a full chip impedance model power and shield lines (underway)*

Signal routing along the column

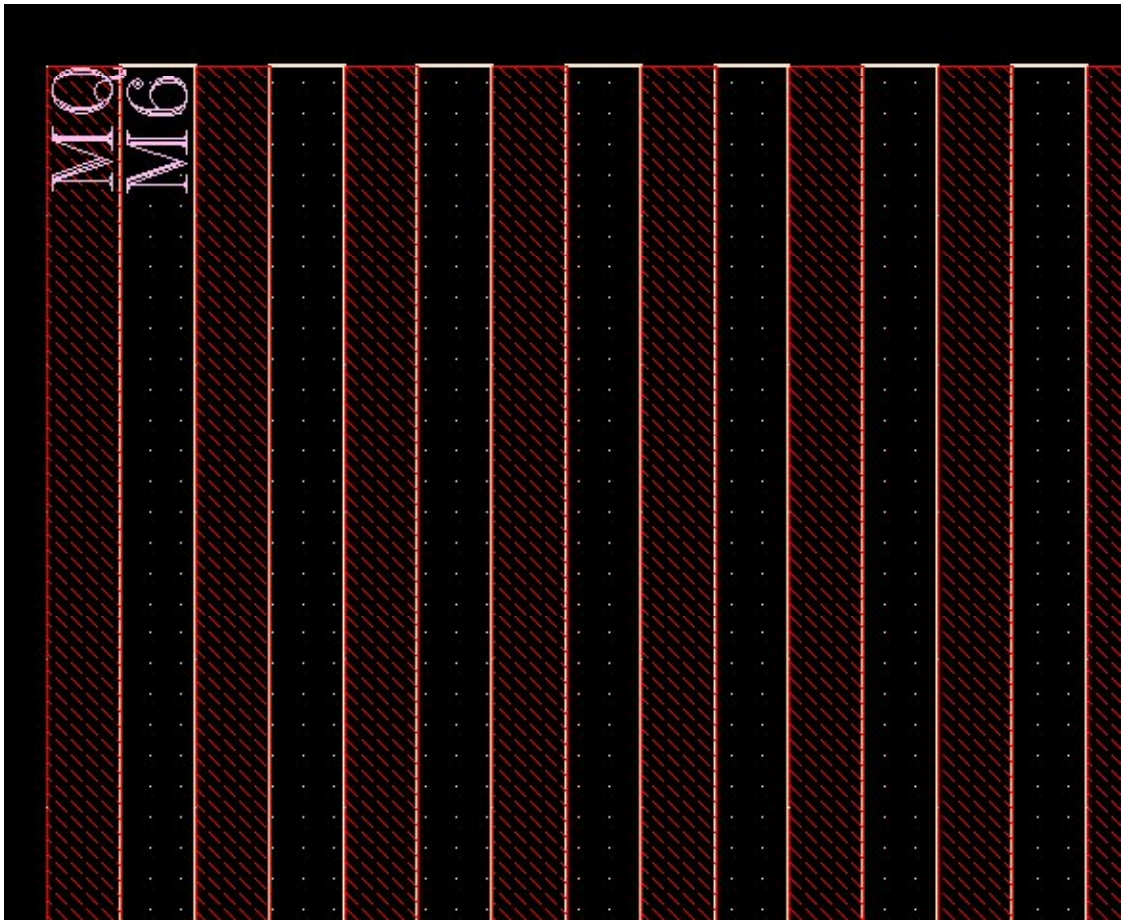
- Several metal utilization schemes have been considered. The following points have “imposed” the proposed choice:
- LM is reserved for shielding the detector. It can double as VDDD, GNDD or VSSA (depending on Xtalk studies)
- M1 cannot be used for global routing: too capacitive, too resistive, heavily used for local wiring.
- M2-M5 have higher up/down capacitances.
- M2-M6 have higher resistances than M7.
- Mx cannot be sandwiched between Mx+1 and Mx-1. Too much capacitance and Xtalk. (power!!)
- Mx and Mx cannot be used side by side at a minimum pitch.
- M2-M6 cannot be of a minimum width, unless capacitance is highly minimized (increase lateral separation and don’t use adjacent level).
- Unrealistic solutions were avoided (e.g. 4u line pitch).

Our Current choice M6-M7 routing

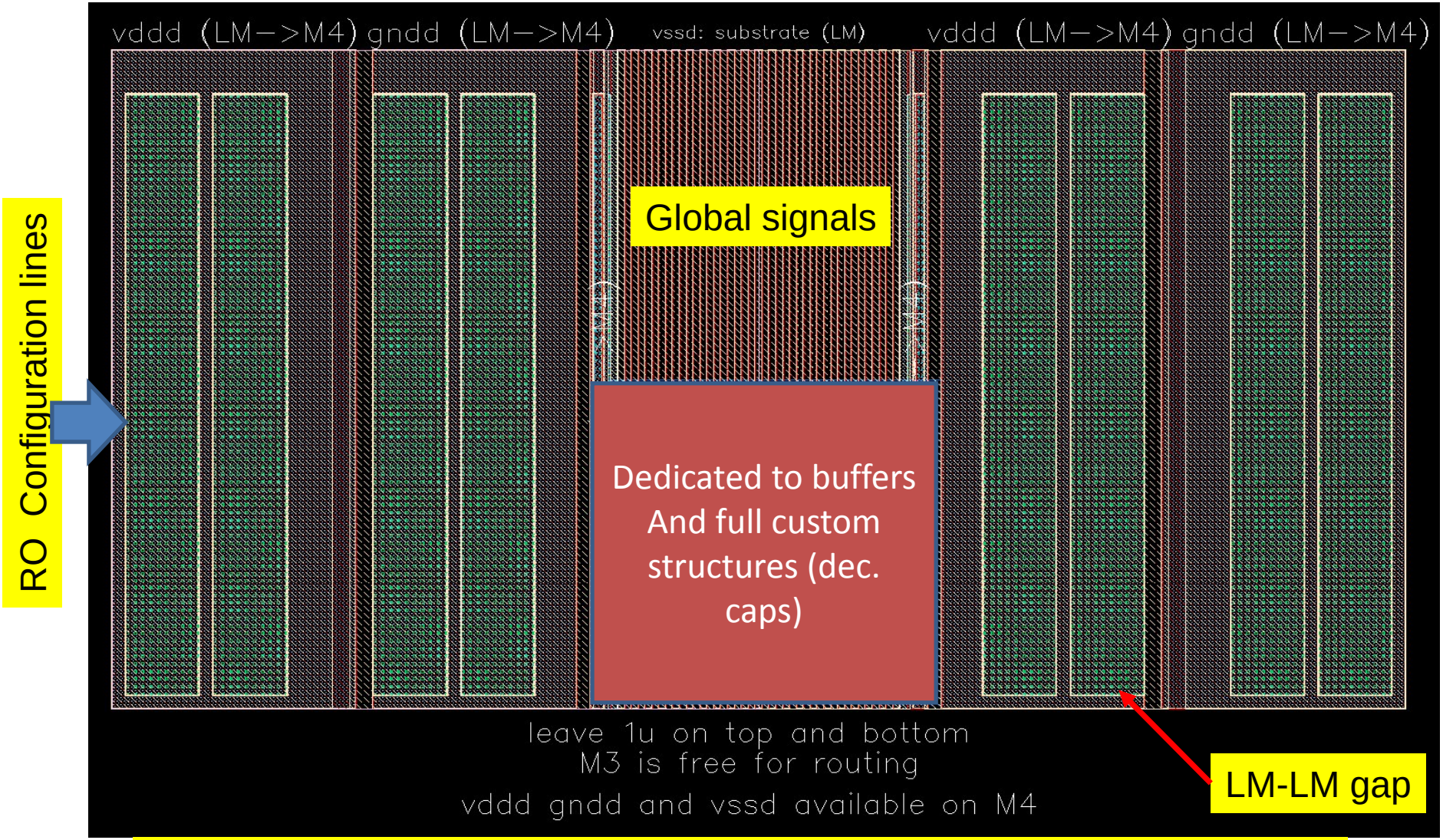
- M7 has the lowest resistance and the lowest capacitance to its up/down neighbor metals.
- Among M2-M6, M6 has the lowest capacitance to its up neighbor metal.
- Using M7 or M6 alone would result in excessive pitch.
- Using M7 and M6 on top of each other would result in excessive capacitance
- Compromise: use M7 and M6 so that there is no overlap between them.

M7-M6 routing: baseline choice

Based on the width of either metals
Different fringe and parallel cap would result.
5 possibilities were studied. The maximum average pitch was kept <=1u.
Best compromise
Base on some assumptions, seemed to be MQ=1u and M6=1u.
Signal pitch=1u.
Takes into account
Some contingency!

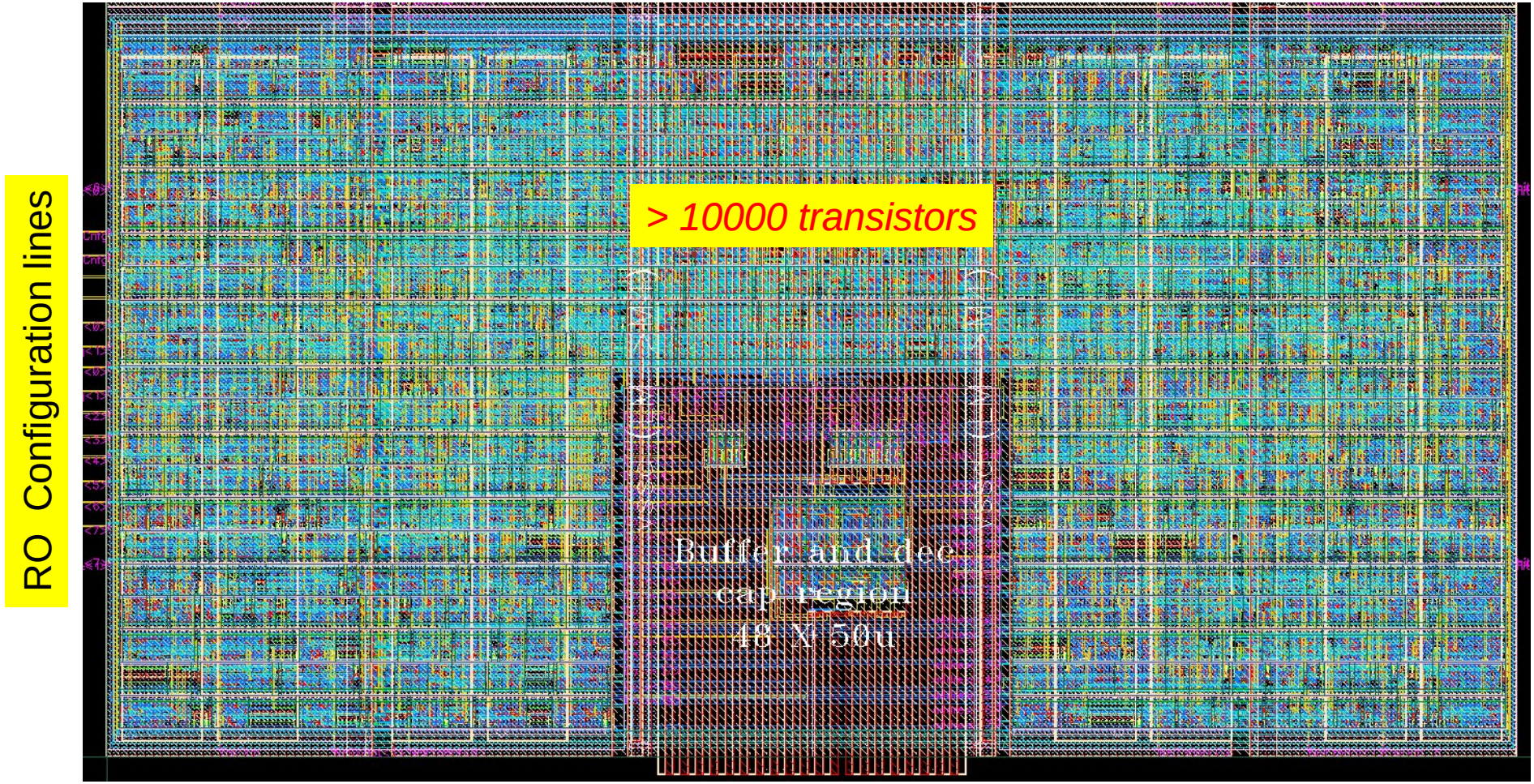


Cell logic current power and routing scheme:



- Detector exposed mostly to LM. (MQ in the small gaps)
- Based on Xtalk studies the LM can be freed to be used as a shield only
- The MQ in the gaps can also be freed if warranted

Digital pixel region (2X2 pixels) layout



Under evaluation

Region simulation: A work in progress

We would quantify:

- Average and peak currents and their paths
- bounce on the power/substrate lines
- Amount of Xtalk

From this we would determine:

- whether differentiel structures are needed and for what signals
- If a dedicated shield layer is needed
- Should new or special circuits used

Every fancy scheme that is not motivated can very costly

Conclusions

- *The proverbial "Encouraging results" holds*
- *More testing and characterization are underway*
- *Some problems cannot be revealed by small size prototypes*
- *The cost of prototyping of large chips is very high: increased due diligence is needed.*
  =>Learning from others is very valuable.
- *A huge amount of work is still to be done.*