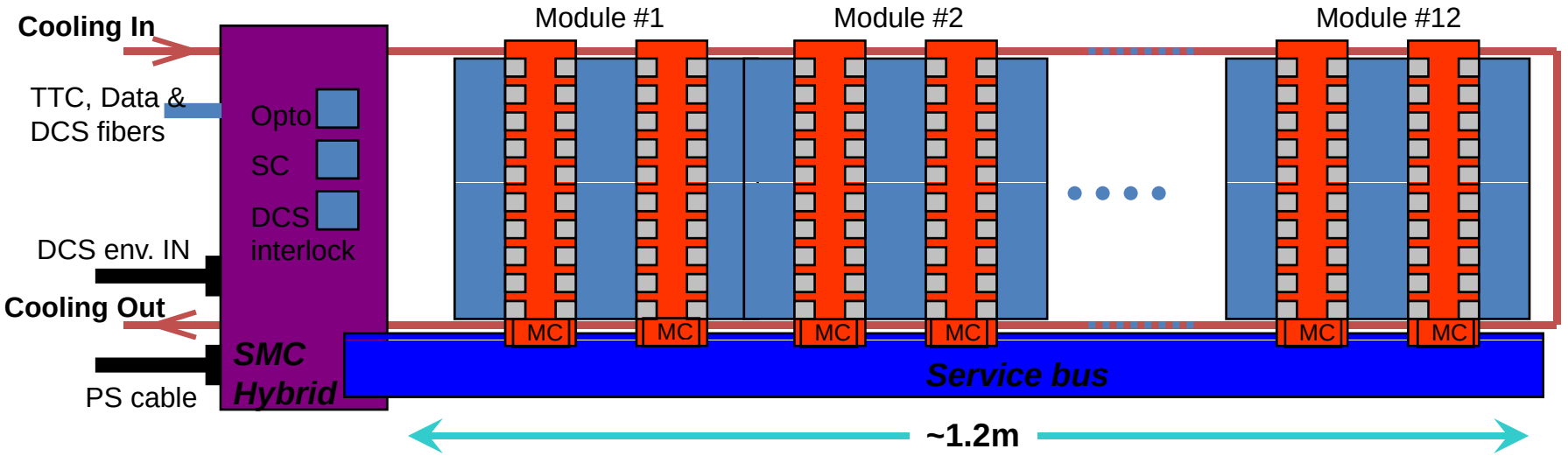
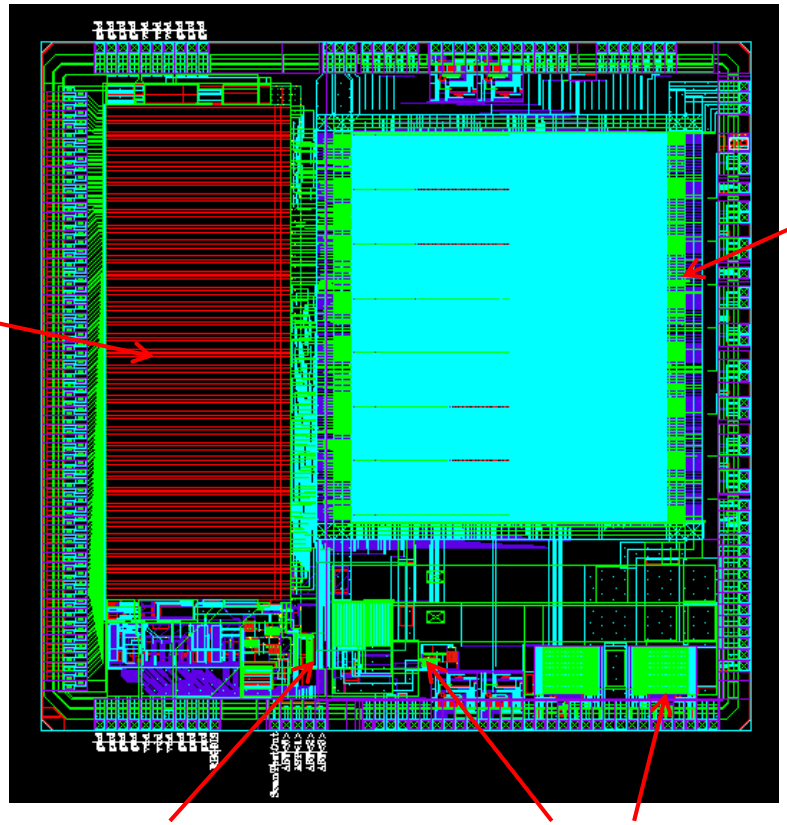
Front-End Design for the ATLAS Strips Detector at SLHC



ABCN in 250nm technology (ABCN25)

128
Channels
Front-End opt.
for Short Strips
0.7mW/channel



Digital part : reuse of existing SCT protocols, SEU protections, 80Mbits/sec output rate, power control , 2.3 mW/channel @2.5V

ABCN 250nm is an intermediate version of the FE chip for stave/modules prototypes

Serial regulator to provide analogue voltage from a unique digital+ analogue power source

Shunt regulators (2 options) to exercise 2 different serial powering systems

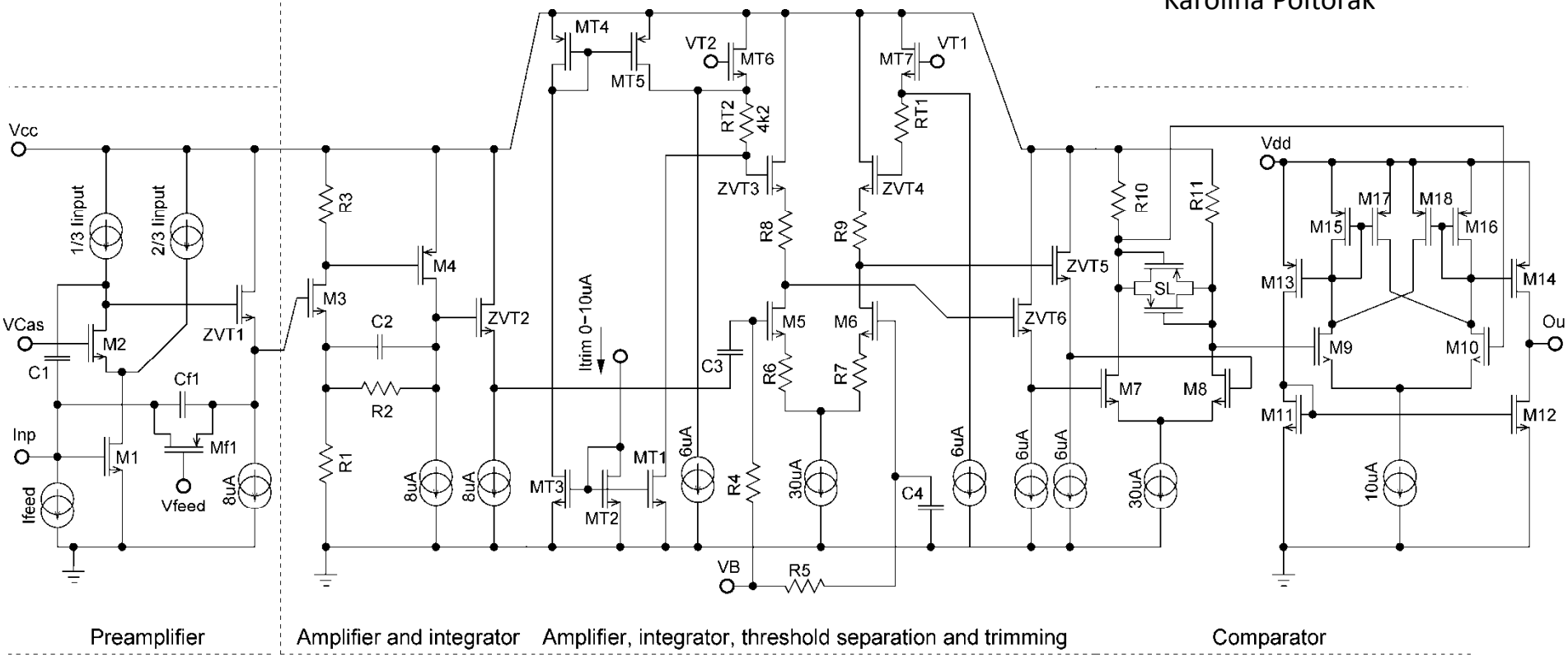
Design from Uni GE, Krakow, Penn University & CERN, reuse of cells of the ToTem VFAT2 chip

ABCN in 250nm technology (ABCN25)

Main Analogue FE Specs	
Gain at the discriminator input:	100 mV/fC for the nominal bias currents and the nominal process parameters
Effective gain extracted from the response curve:	90 mV/fC for the nominal bias currents and the nominal process parameters
LINEARITY:	BETTER THAN 3% IN THE RANGE 0 – ±6 FC
Time walk	<15ns 1.25-10fC @ 1fC Threshold
Noise:	<= 750 electrons rms for unirradiated module
Max Parasitic Leakage Current:	200 nA DC per channel with <10% change in gain at 1 fC
Power	700uW (optimized@ short strips)

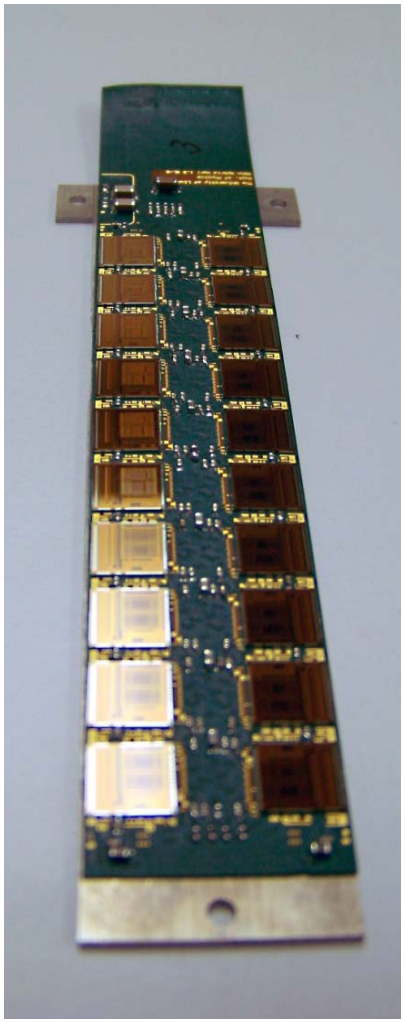
ABCN25 : Front End Circuit

TWEPP 08
Jan Kaplon, Wladek Dabrowski,
Karolina Poltorak



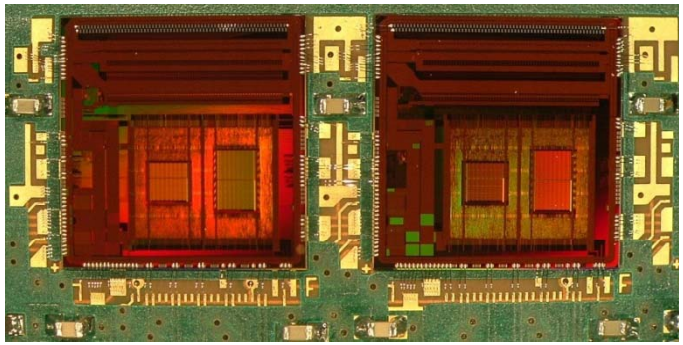
- Input transistor; NMOS 320um/0.5um, nominal bias **140uA**
- Nominal consumption **280uA** @ 2.5V (2.2V after regulator) (**0.7mW / channel@2.5v**)
- Peaking time **25ns (22ns intrinsic)**
- Time walk 1.25 – 10fC @ 1fC threshold ~**15ns**

ABCN25 Status



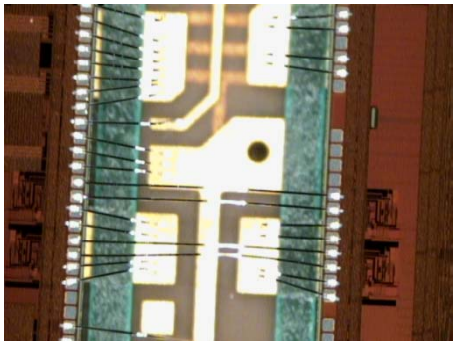
Fully Populated Liverpool Hybrid

Neighbouring ABCns wire bonded



7.5mm 2.1mm 7.5mm

Inter-chip bonding



Photos : courtesy Ashley Greenhall

Full functionality at 40 MHz BCO and 80MHz RO

Analogue performance according to specs @ no detector

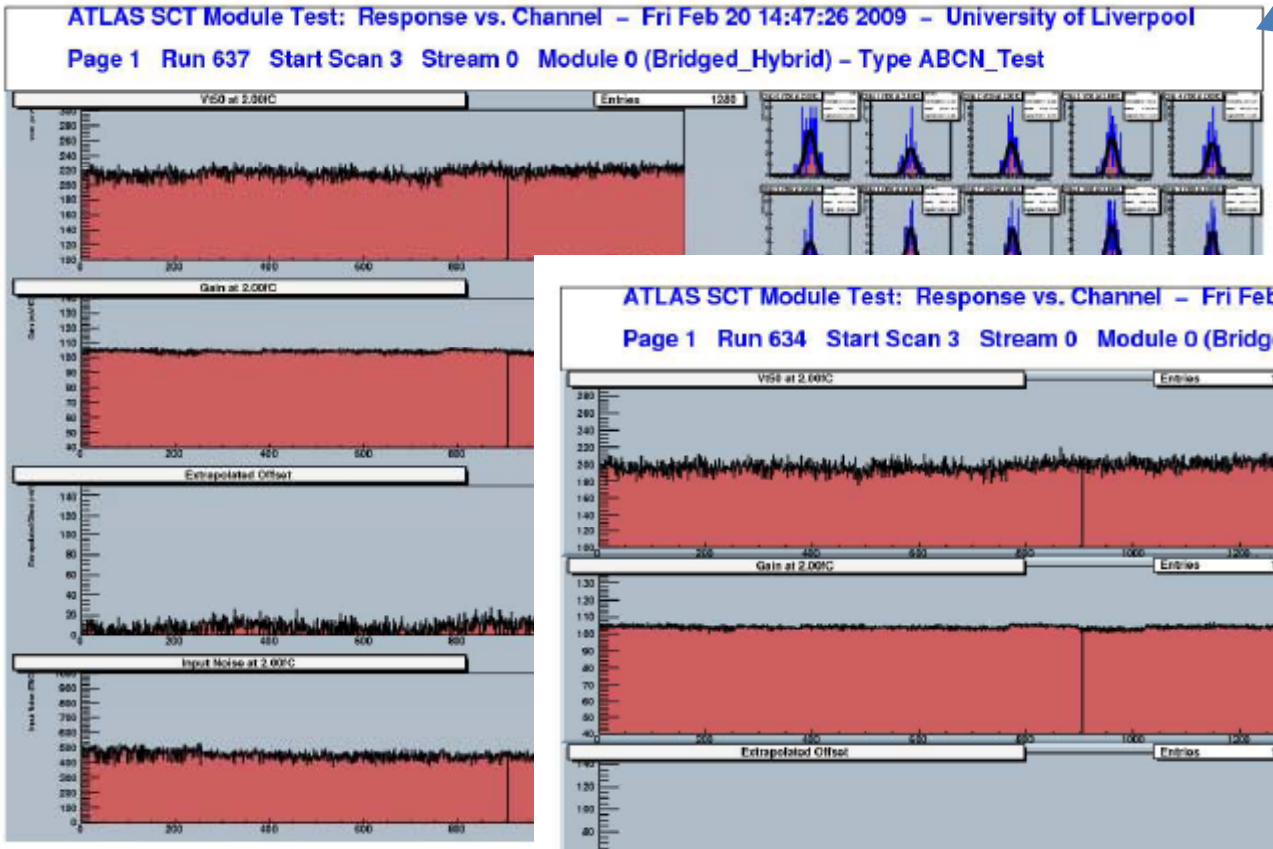
Preliminary results with 2.5cm strips detector

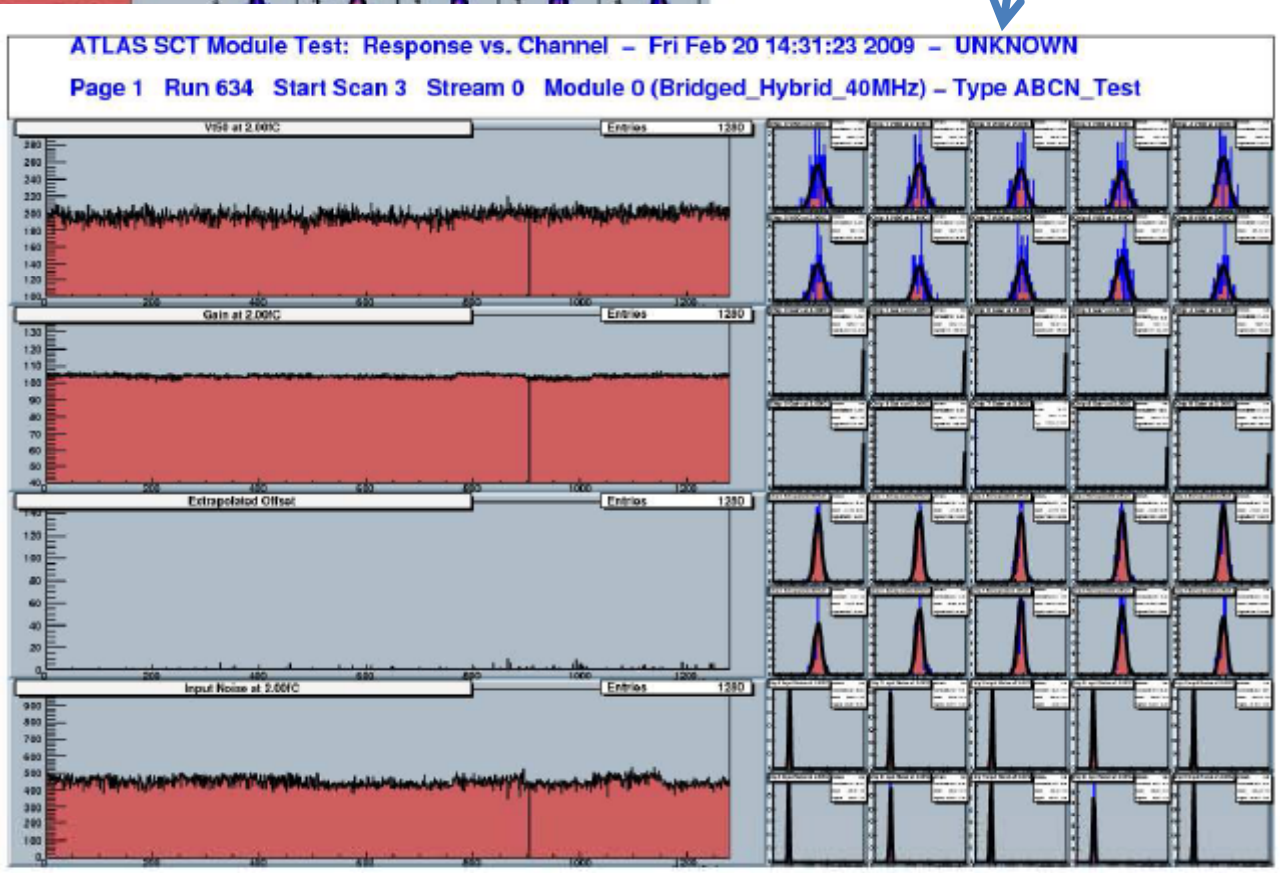
ABCN25 Status

A. Greenhall courtesy

Hybrid readout 40/40MHz

Hybrid readout 40/80MHz

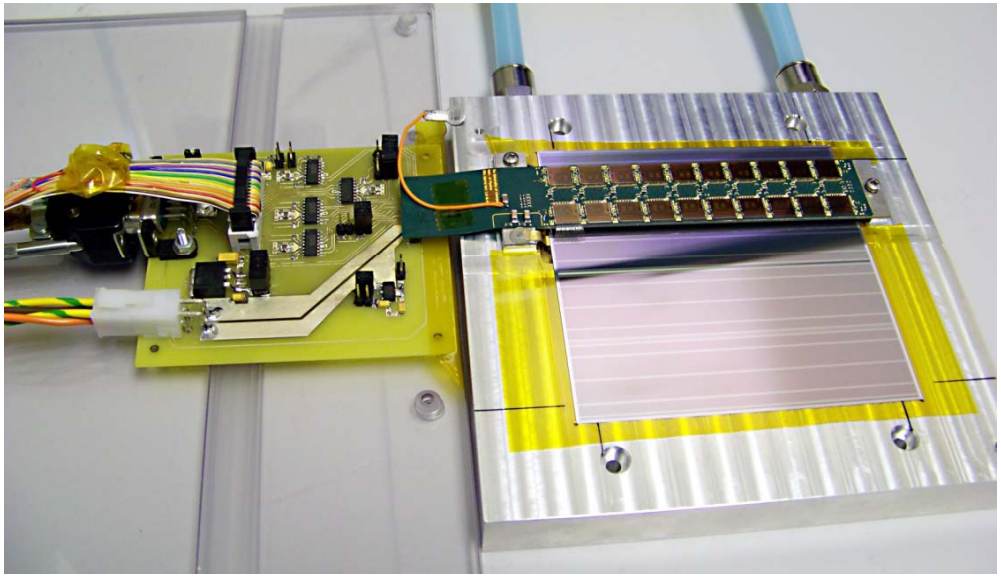




- 105mV/fC gain at discri. input
- 450el noise @ no detector
- Threshold uniformity < 0.03fC (after trimming)

ABCN25 Status

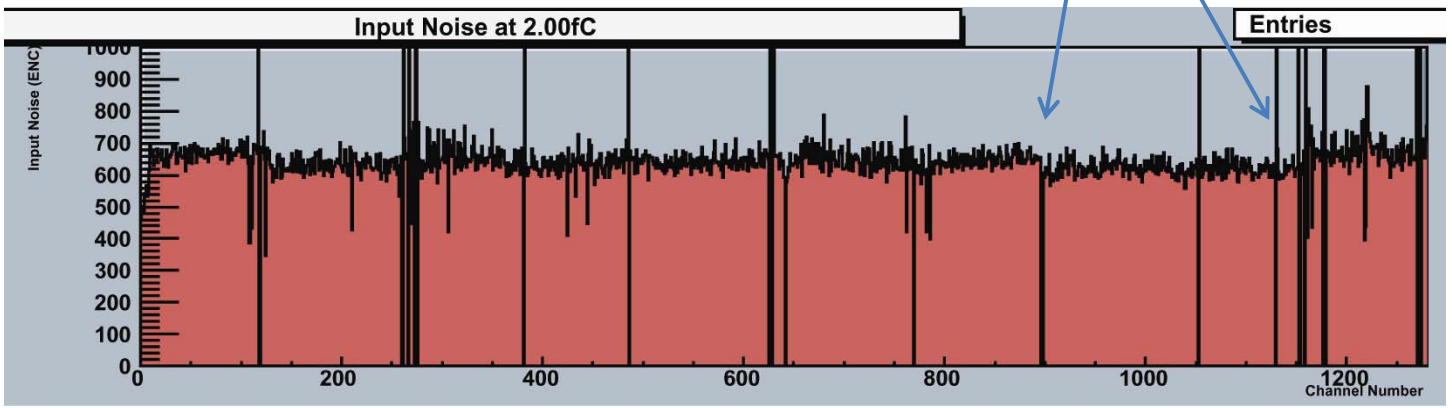
Courtesy : Tony Affolder



Hybrid on detector, SCTDAQ

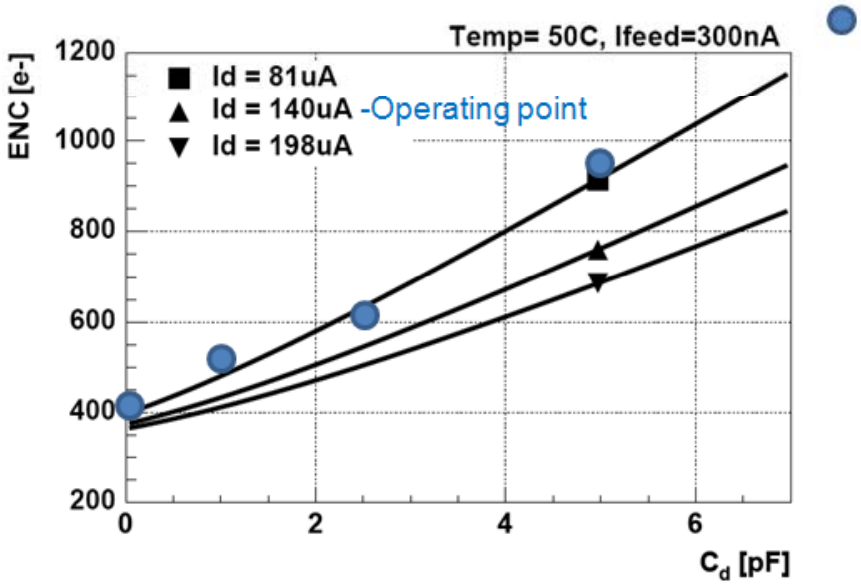
650el noise with 2.5cm n-on-p detector

Issues with bondings near chip edges



Preliminary Noise Slope Results

	With separate analogue/ digital power	With analogue regulator
Bare Hybrid	400-450 e^-	400-450 e^-
1 pF		525 e^-
2.5 pF	605 e^-	575 e^-
5 pF	986 e^-	952 e^-
7.5 pF	1364 e^-	1313 e^-



Noise prediction from Jan Kaplon with no detector leakage

- Input transistor; NMOS 320um/0.5um, nominal bias **140uA**
- Nominal consumption **280uA** @ 2.5V (2.2V after regulator) (**0.7mW / channel)**

ABCN13 : NEXT STEPS (130nm technology)

For the next technology version we are considering :

To keep the same generic architecture as ABCD, ABCN25 :

- Binary readout with L1 latency pipeline, L1 buffer, DCL and serialiser

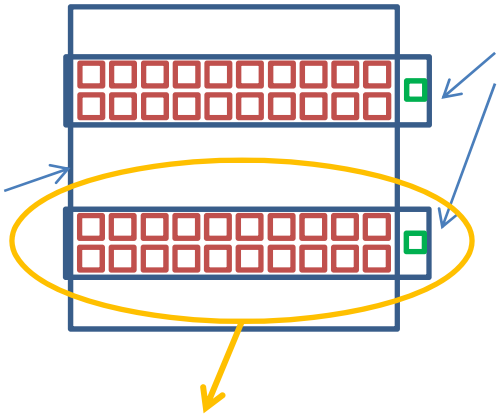
But to modify/add the following :

- Readout protocol
- SEU detection/correction in chip
- Number of channels per chip
- Data coding (ECC, DC balancing, clock recovery)
- On-chip power devices to adapt the DC-DC or SP powering schema
- DCS functions

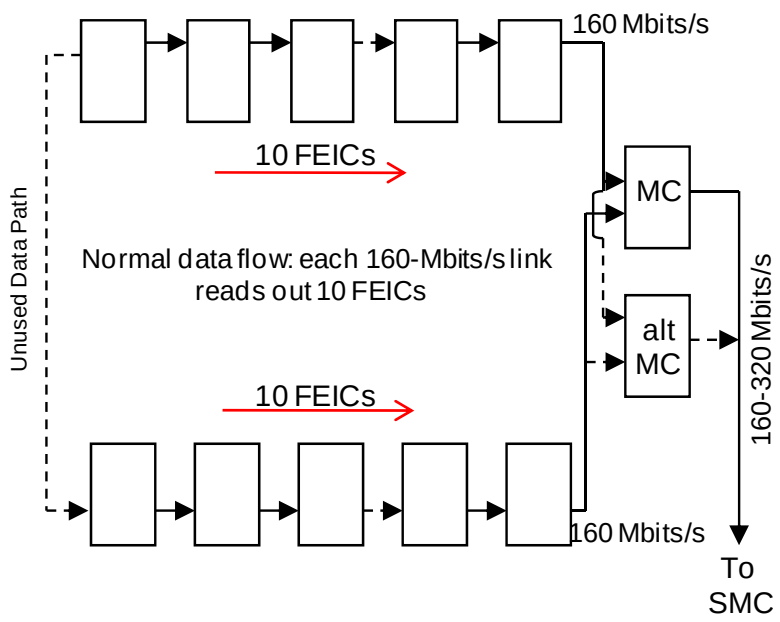
ABCN13 : NEXT STEPS (130nm technology)

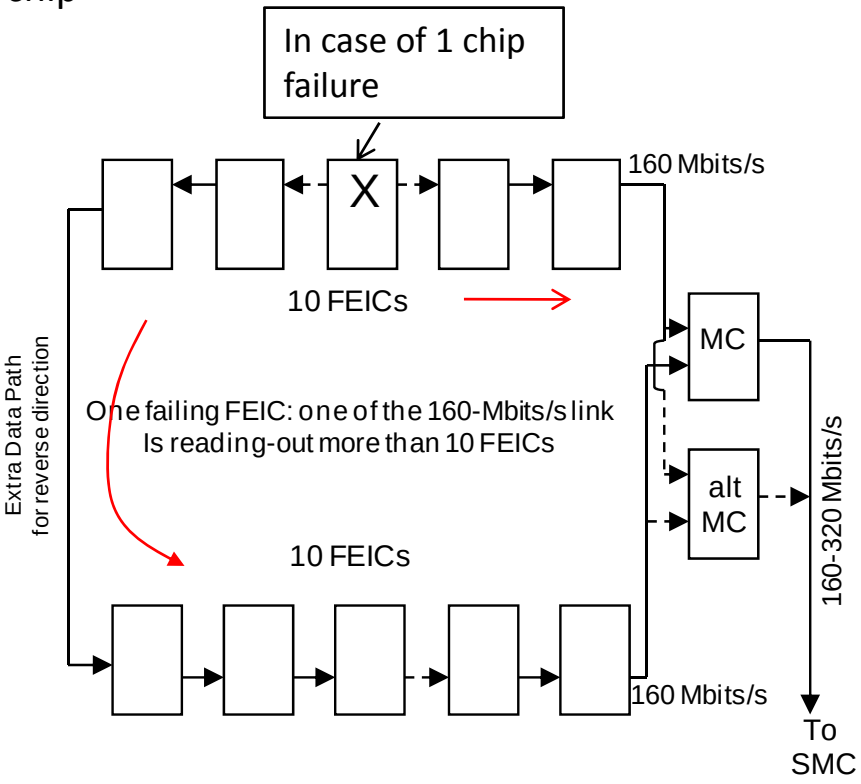
Short strips module concept : 2 hybrids, each one reads 2 rows with 20 FE chips of 128 channels

Detector has 4 rows of 1280 strips

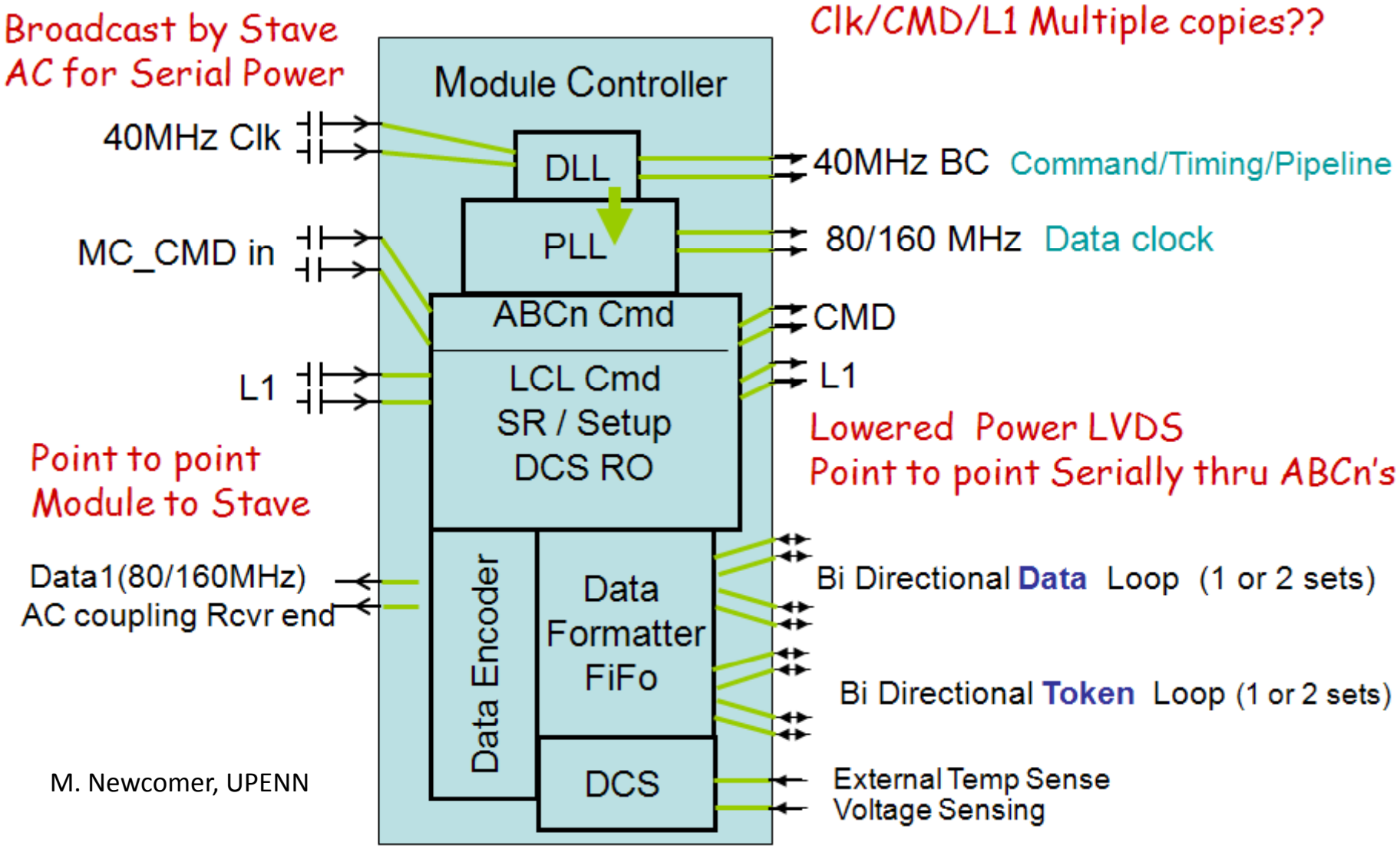


Per hybrid, data are daisy-chained from chip to chip up to the MC chip



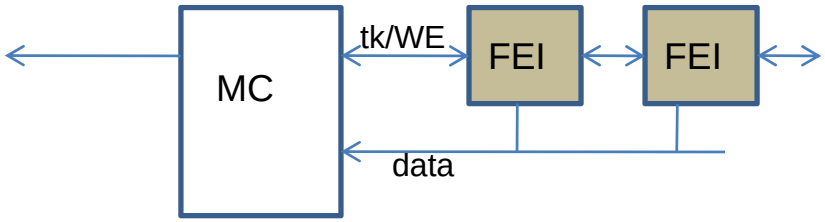


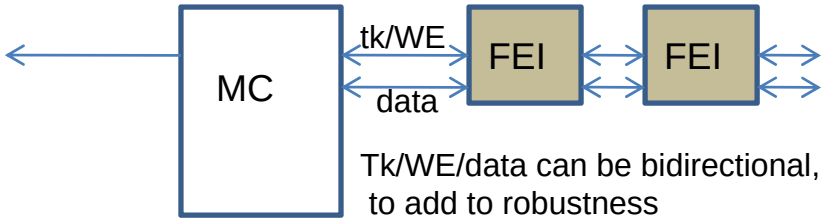
MC chip draft (communication btw. ABCN and End-of-Stave Electronics)

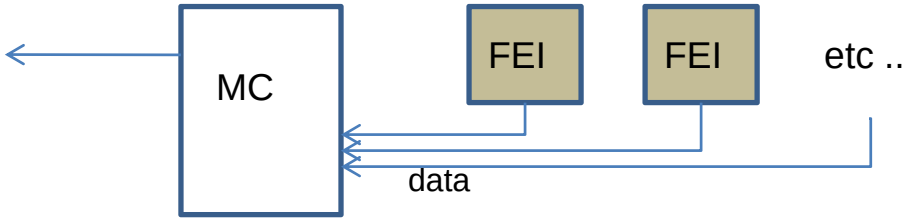


SERIAL DATA COLLECTION

HARDWARE CONFIG





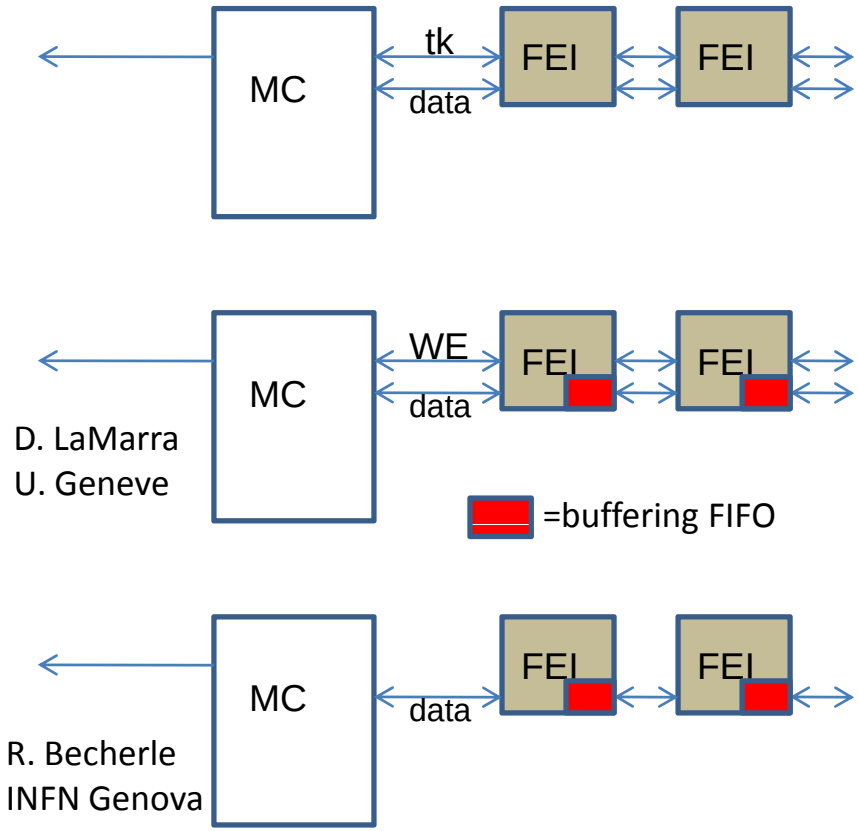


	Pro	Con
Common bus		Sensitive to bus default Data concatenation in FEI
Daisy Chain As present ABCN 3 possible variants (next slide)	Large number of FEI	Data concatenation in FEI
Star	Data concatenation in MCC Robustness	Limited number of FEI per hybrid

SERIAL DATA COLLECTION

HARDWARE CONFIG

Variants of daisy-chains



Tk/WE/data can be bidirectional, to add to robustness

	Name	Comment
Token (as present ABCN)	token	Timing critical
Write Enable	WE	Additional FIFO buffer in FEI. RO order from 1st to last chip
Trailer Detecti on	No WE	Additional FIFO buffer in FEI. RO order from last to 1st chip

SERIAL DATA FRAME (OPTIONS)

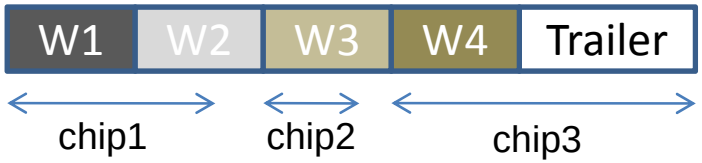
SHOWN BELOW IS THE SERIALIZED DATA FROM MULTI FE CHIPS AT THE MC INPUT
THE MC MAY ADD HEADER AND DATA CODING

Data packet :
DATAID {+ CHIPID}{ + CHANNELID + DATA}
DATAID {+ CHIPID}{ + REGID + DATA}
DATAID {+ CHIPID}{ + ERROR CODE}

1

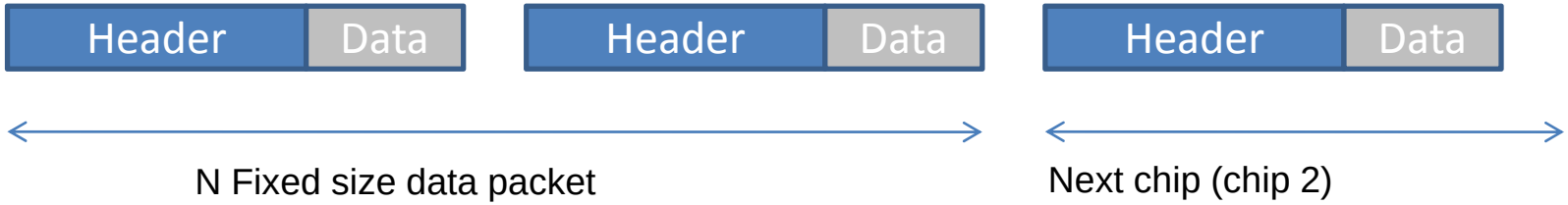
Adjacent Variable size data packets (present schema)

2



Adjacent data packets in fixed size words

3



Independant data packets in fixed size words

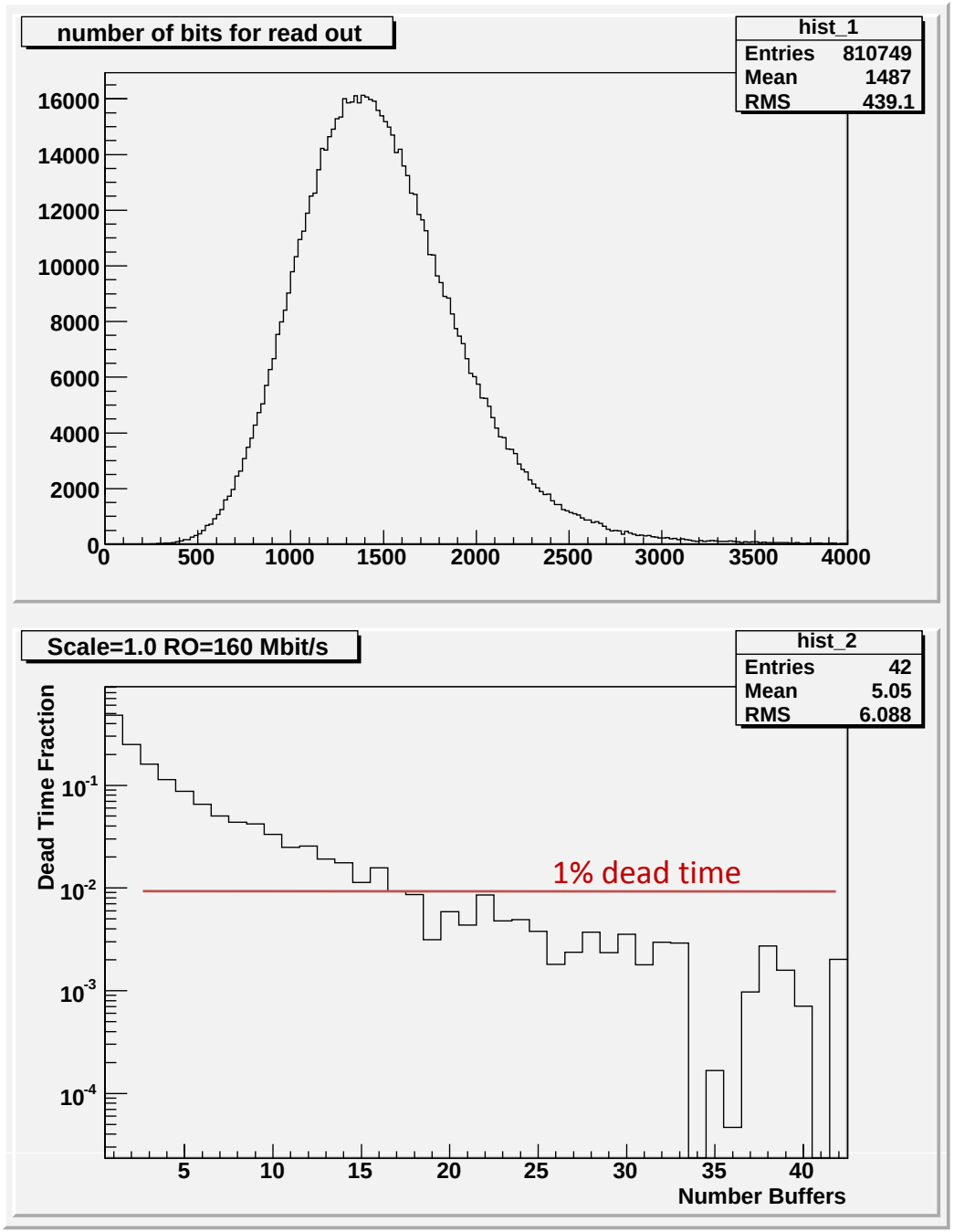
Physics simulation support for evaluation of the different readout protocol schemas
T. Weidberg, Oxford

- **Trigger Rate <L1> = 100 kHz**
- **Assume 20 MHz BC ➔ <pile up> = 400**
- **20 ABC-Ns read out through one MCC at 160 Mbits/s.**
- **Look at inner layer of short strip detector only (worst case).**
- **Strip length = 2.5 cm.**

Option 1, “Daniel’s” variant

Scale factor = 1.9

Dead time remain below 1% ➔ reasonably large safety factor.



ABCN13 : NEXT STEPS

ABCN in CMOS 130nm or less

SEU issues:

•Assess that we can use the standard transistor layout and standard cells libraries. We need to verify the total dose effect on transistors at the projected temperature of the chips in the staves (-20 deg. C)

• SEU immunity will require specific actions. The TMR technique would work but at cost x3 in power.

• SEU safe sequencers, autorecovery mechanisms, at cost of additional circuitry (= power)

ABCN13 : NEXT STEPS

ABCN in CMOS 130nm or less

Power gains versus 250nm:

- In 130nm technology the nominal voltage is 1.2 V. The analogue should be at this voltage, however the digital may be as low as 0.9V for 40/80/160MHz operation.

- The net gain on digital power can be as high as /6

Preliminary Look at **relative** **Digital Power** Requirements for 130nm / 250nm Rad Tolerant CMOS Technology

Digital Design Studies → Brandon Bloch and Jake Hindenburg (Penn undergrads)

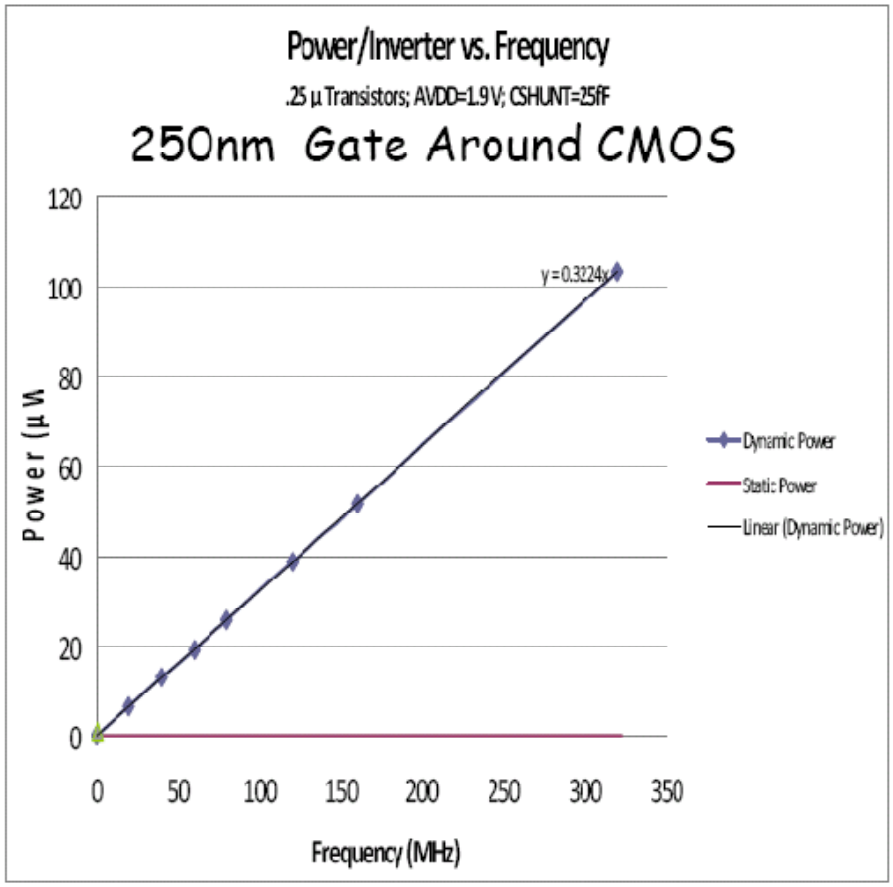
¼ um Reference
SPICE Simulation Results

To begin we implemented a CMOS8RF (250nm) (RAL Digital Library parts) inverter chain with 2X drive six levels deep. Our previous work with this process showed that 25fF was a reasonable wiring load.

PMOS W= 14um

NMOS W= 8um

We found Acceptable response (Full rail to rail logic swings) out to 320MHz at 1.9V.



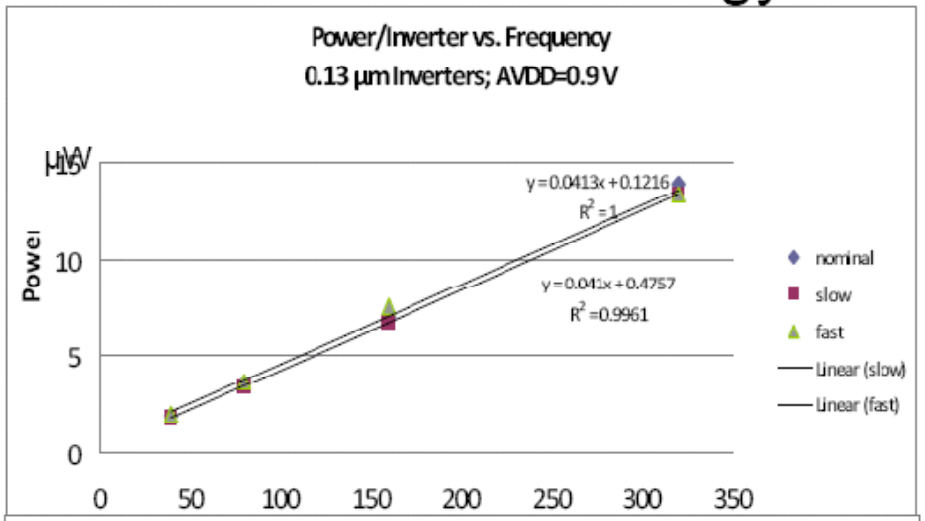
Preliminary Look at **relative** Digital Power Requirements for 130nm / 250nm Rad Tolerant ASIC Technology

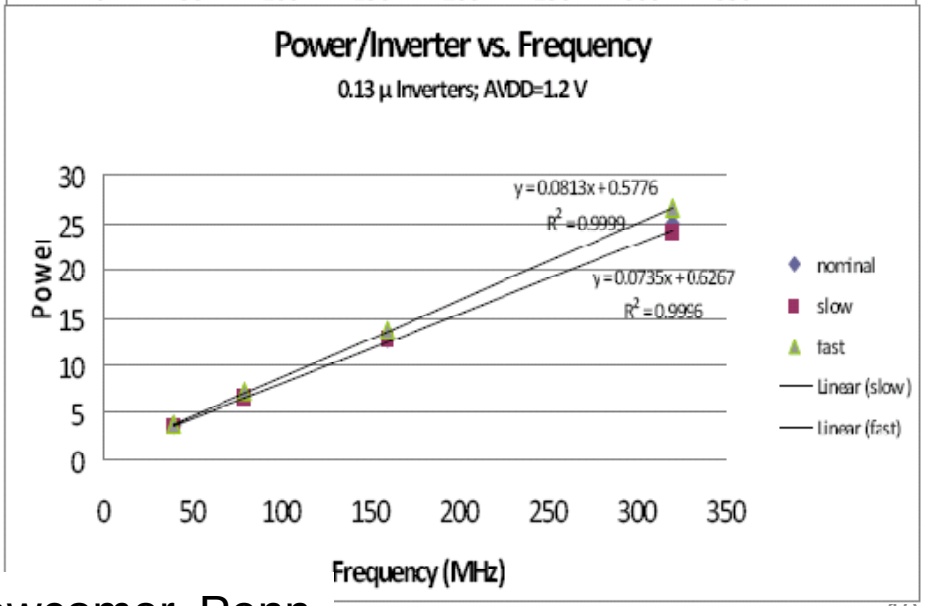
130nm candidate Technology SPICE Simulation Results including layout extracted parasitics for 6 level clock tree. A 15fF load was added.

CERN Digital library parts for their 130nm designs. We chose the 2X and imposed the same conditions as for the 250nm parts, scaling the inverter load from 25fF to 15fF.

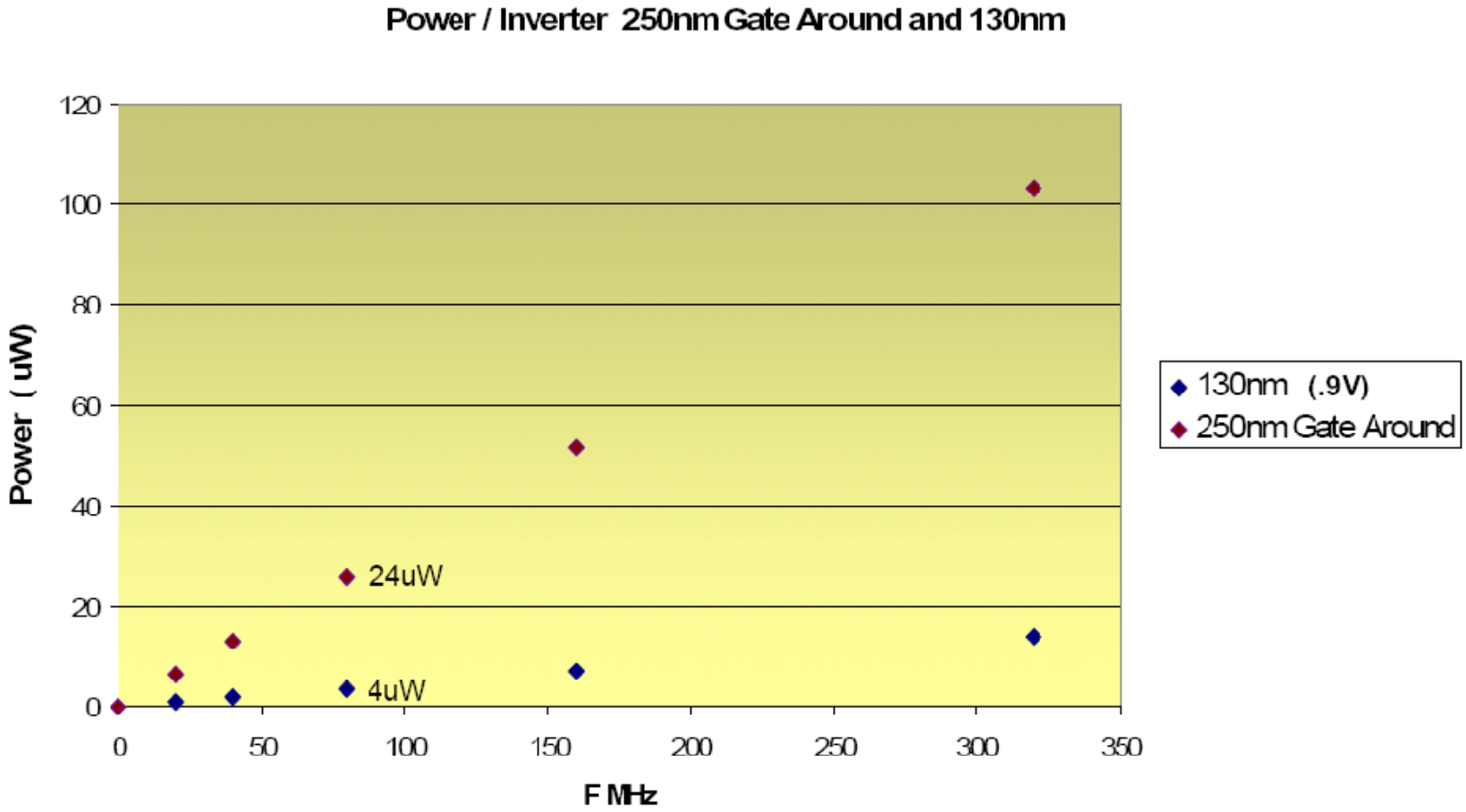
PMOS W=1280nm
NMOS W=920nm
Full Logic swings @.9V w15fF load to 320MHz

Note that we looked for and found the static leakage current but it was less than 1% of the total power consumption.





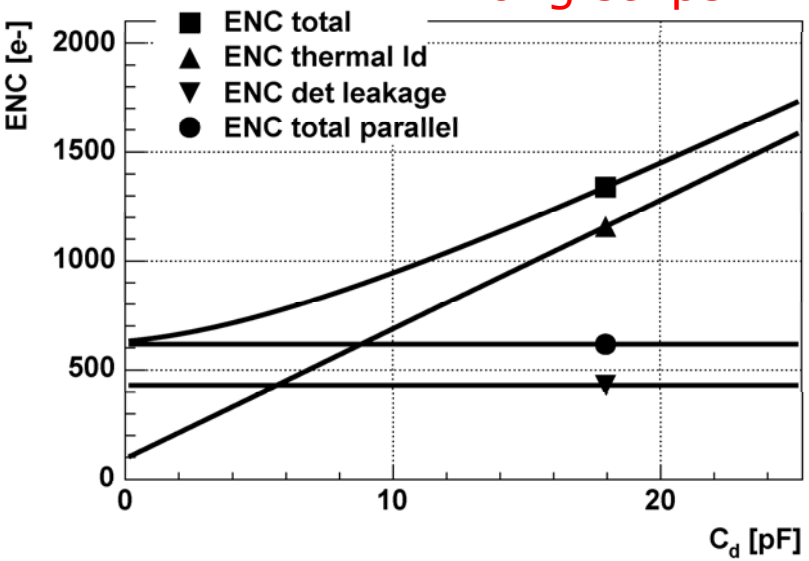
250 / 130nm Direct Comparison



This study, based on layouts with parasitics suggests a **6X** reduction in Power for the native CMOS Digital parts compared with the "gate around" 250nm process.

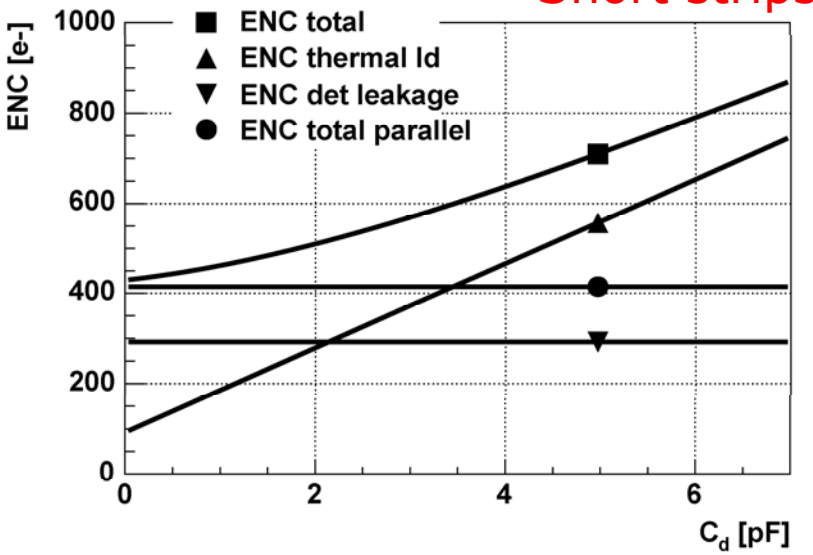
POWER ESTIMATES FOR THE FRONT END IBM CMOS8 130nm

Long strips



Id=200uA, NMOS 500/0.3
Ifeed=700nA, Ileak=1.3uA

Short strips



Id=80uA, NMOS 200/0.3
Ifeed=300nA, Ileak=600nA

Improvement for 130nm process due to:

- ❑ lower slope factor n; 1.45 → 1.25 (so gm is only 25% lower wrt BJT)
- ❑ no excess noise for L>250nm (Γ=1.3 for IBM250nm)
- ❑ higher transconductance; K_{pNMOS} 300 → 750 uA/V

Calculations and slide content by Jan Kaplon, CERN

POWER ESTIMATES FOR THE FRONT END

- IBM 250nm; Bias currents in shaper and discriminator stages in the range of 6 to 8uA due to the lack of high value resistors (we use polysilicon resistors 250 Ω/square)

Current consumption in present shaper/discriminator ; **140uA**

- IBM 130nm;
  - 1.7k Ω /square polysilicon resistors available;
  - Higher transconductance and better matching → smaller devices

Evaluation of current in shaper/discriminator for 130nm (number from design for GTK; 5ns peaking time); **50uA**

Total power consumption for front end in 130nm optimized for:

- **Short strips; 130uA @ 1.2V (160uW/channel) 20mW / chip**
- **Long strips; 250uA @ 1.2V (300uW/channel) 38mW / chip**

Jan Kaplon, Topical Workshop on Electronics for Particle Physics Naxos, September 15-19, 2008

SiGe Design* Long Strips 175uA @1.2V (210uW / channel) 26mW / chip

* Completed Design, Ned Spencer, UCSC Ready for submission 11/08

Compare with ABCN 280uA @ 2.2V = 616uW / channel 80mW/chip

POWER ESTIMATES FOR ABCN13

130nm predictions

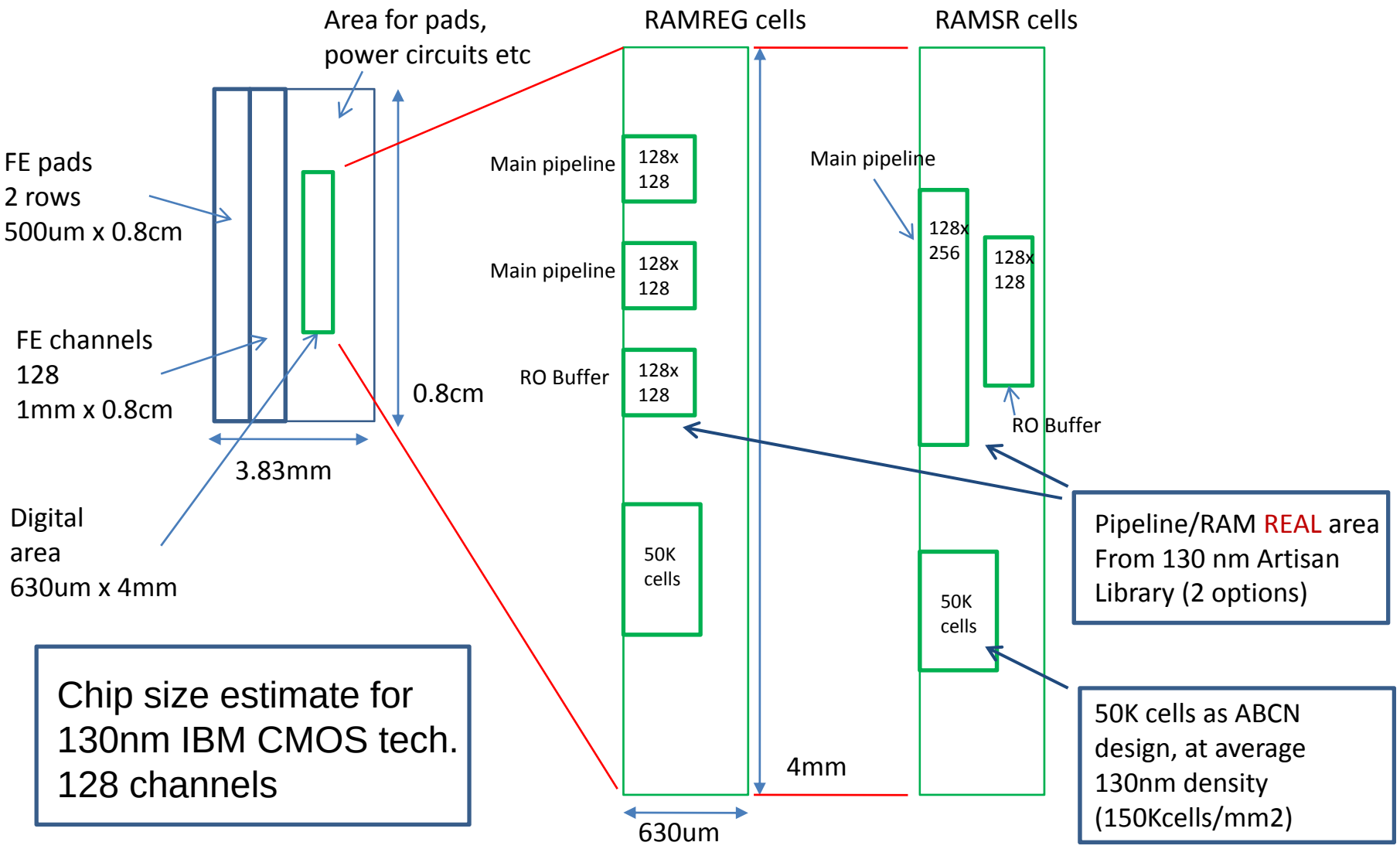
130 nm Estimate 128 Channels / chip	Supply	Short Strip Power, Current	Long Strip Power, current
Analog	VDDA @ 1.2V	20 mW, 16mA	39 mW, 32mA
Digital Supply	VDD @ 0.9V	46 mW, 51mA	46 mW, 51mA
Total Power* / Chip		66 mW	85 mW
Total Power * / 20 Chip Module		1.3 W	1.7 W

*This Power estimate does not include overhead for Regulators or single line supply. Eg. Digital power @.9V derived from Analog voltage @1.2V would be larger by a factor of 1.2/.9 (33%) if a linear regulator was employed.

We propose an upper limit for system design at 1mW/channel

ABCN13 : CHIP SIZE

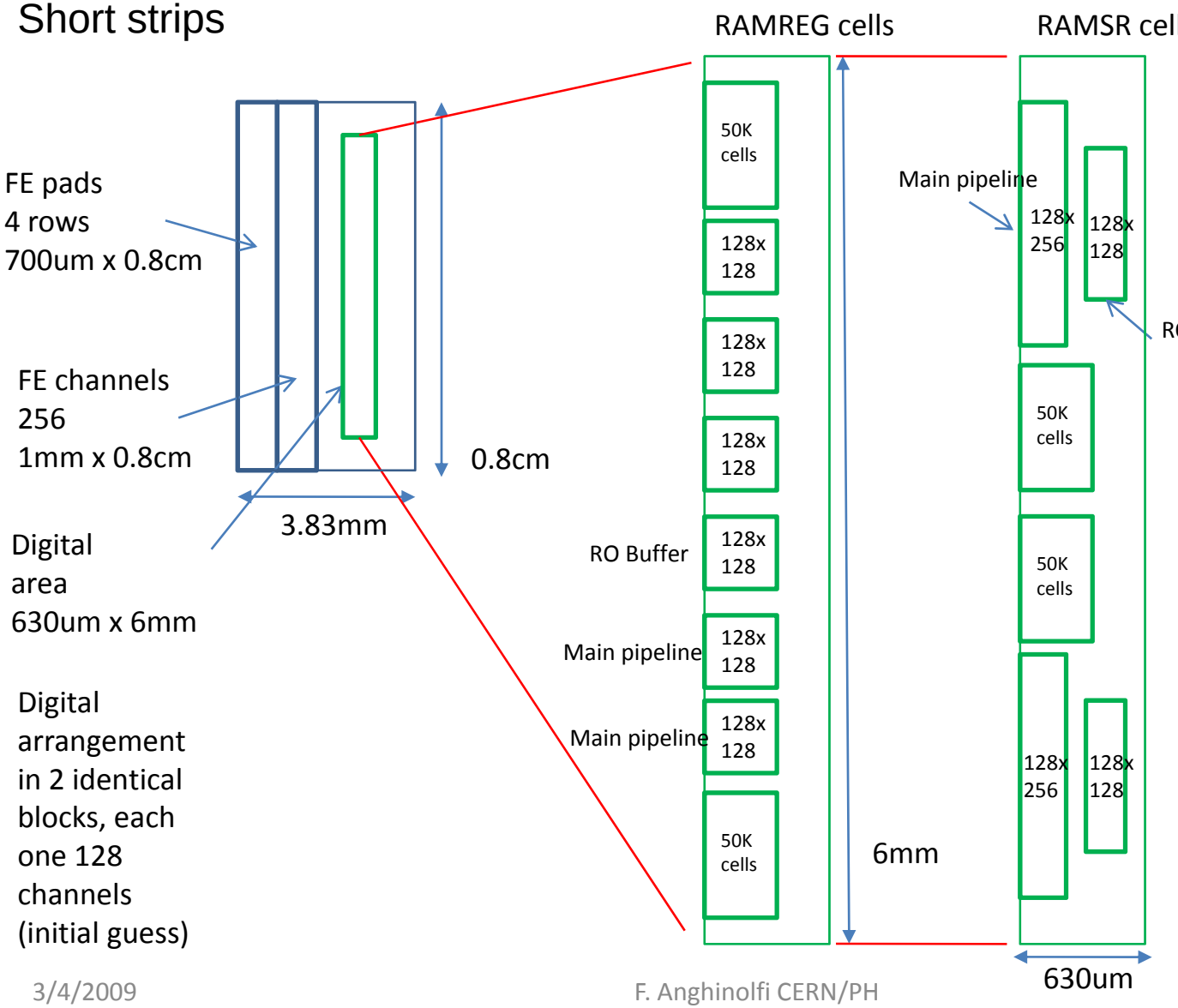
128 channels



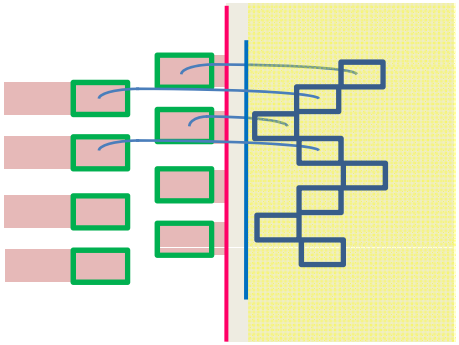
Chip size estimate for
130nm IBM CMOS tech.
128 channels

256 channels
chip options
Short strips

ABCN13 : CHIP SIZE

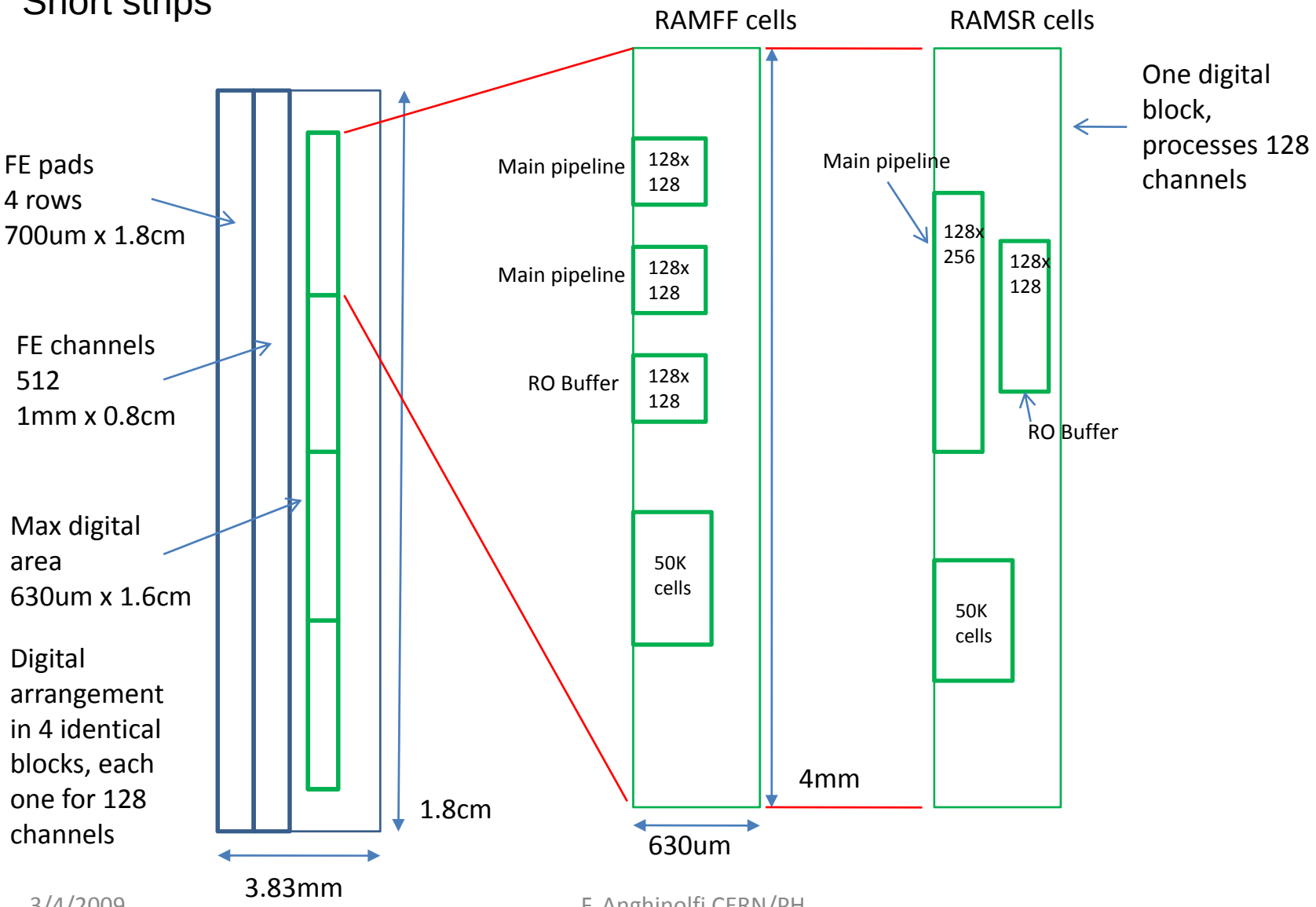


2 strip rows Bonds arrangement



512 channels chip option, Short strips

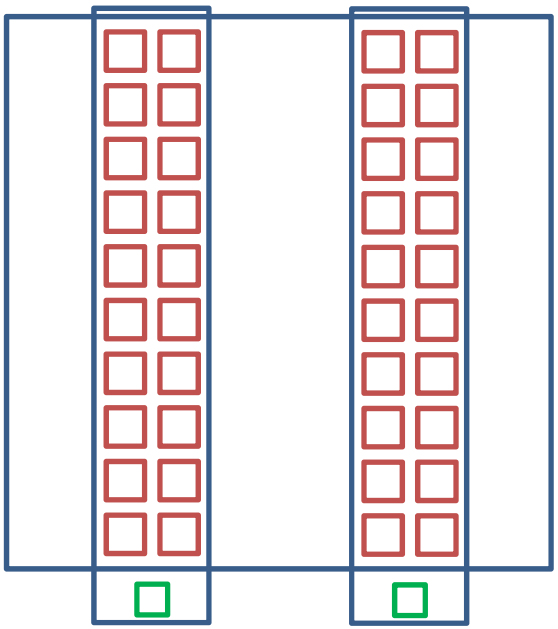
ABCN13 : CHIP SIZE



ABCN13 : NEXT STEPS

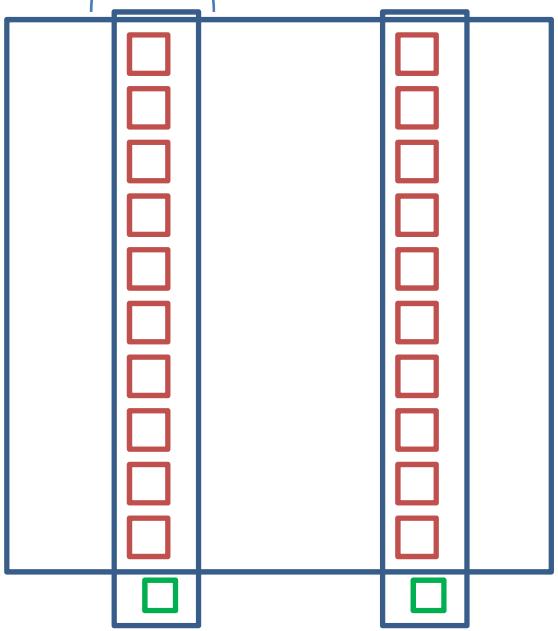
SHORT STRIPS

2 x 10
128
channels



Module arrangement, Short strips,
128 channels ABCN

10 x
256
channels



Module arrangement, Short strips,
256 channels ABCN

ABCN13 : TODAY'S CONCLUSIONS

There are many open options. However the present ABCN25 is helping to test some options (like the powering schema) and to tune the future chips specifications.

The power estimation/optimization is first priority for the ABCN13 design (critical in the digital part)

We may consider fixing the ABCN13 chip design in the 2010-2011 period

We should fix at the end of 2009 the following items :

- Readout architecture and protocol
- Number of channels per chip
- First sketch of powering schema, SEU correction in chip, data coding, integrated DCS