Progress on the CMS Pixel front-end system

ACES Workshop
CERN

4. March 2009

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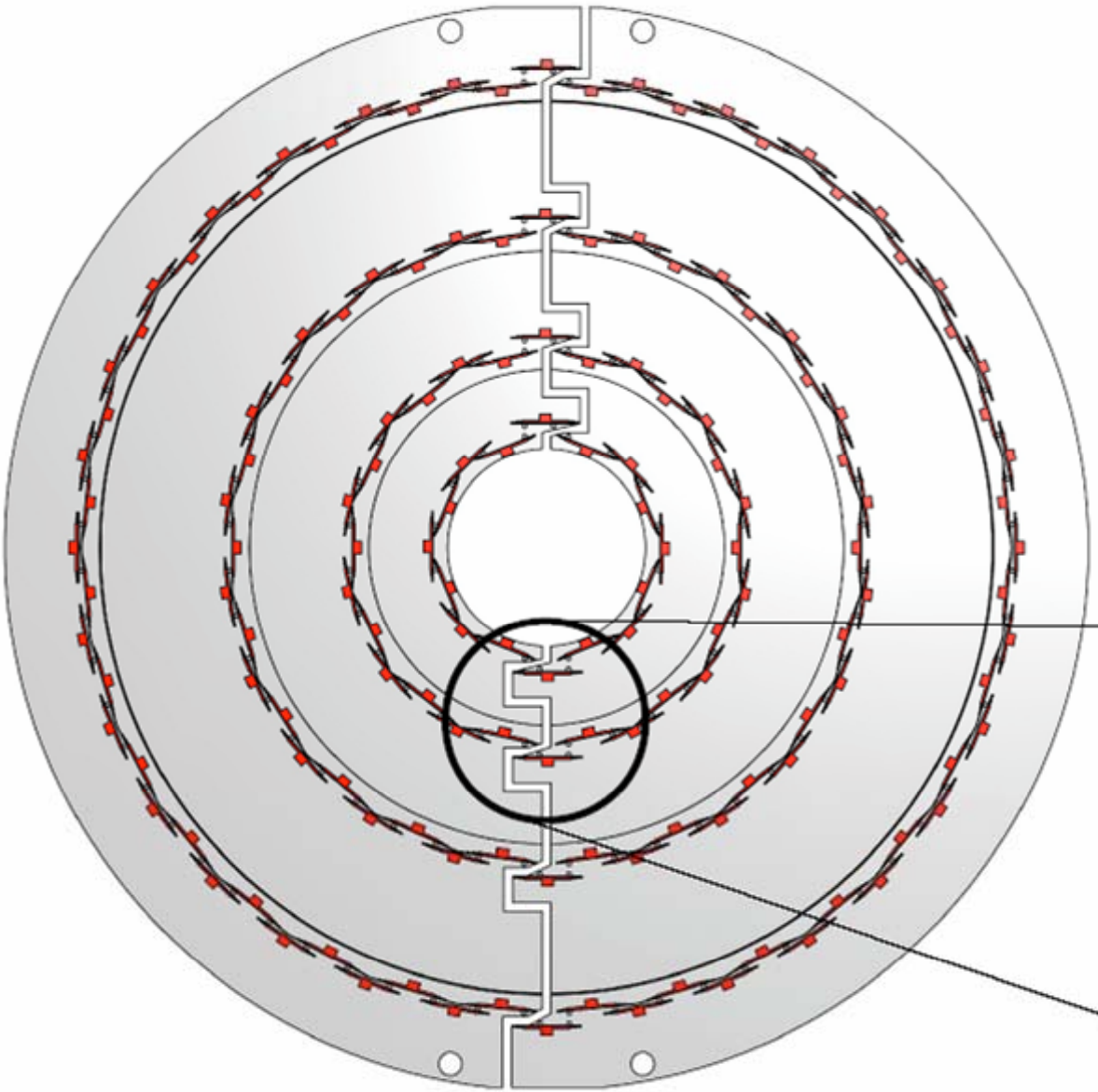
Paul Scherrer Institut

BPIX Upgrade Phase 1 (2013)

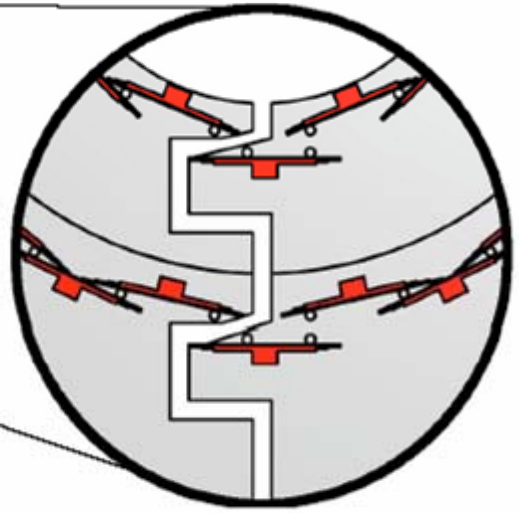
- 4 layer pixel system 4, 7, 11, 16 cm → 1216 full modules
- CO2 cooling based
- Ultra Light Mechanics
- BPIX modules with long 1.2m long microtwisted pair cables
- Shift material budget from PCB & plugs out of tracking eta - region
- **Modify PSI46 ROC for 160MHz digital readout & Increase depth of ROC buffers**
- **Serialized binary optical readout at 320 MHz to old, modified px-FED**
- Recycle & use current AOH lasers → 320MHz binary transmission
- Same FEC's , identical TTC & ROC programming
- Keep LV-power supply & push more current through cables

BPIX Upgrade Phase 1 (2013)

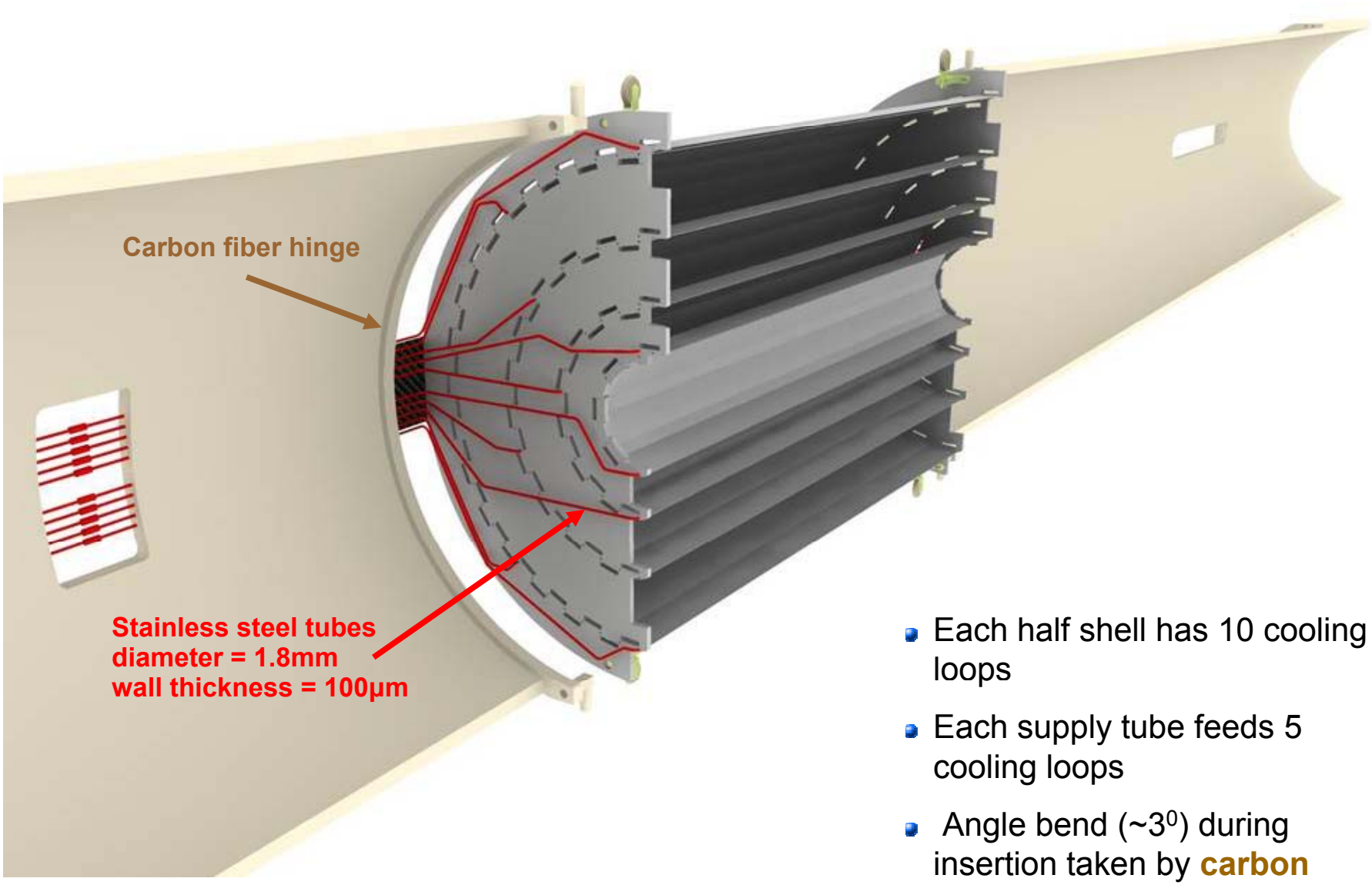
→ **1216 modules**
(1.6 x present BPIX)



- Two identical half shells
- 1 type of fullmodule only
- Layer 1: R 39mm; 16 faces
- Layer 2: R 68mm; 28 faces
- Layer 3: R 109mm: 44 faces
- Layer 4: R 160mm: 64 faces
- Clearance to beampipe 4mm

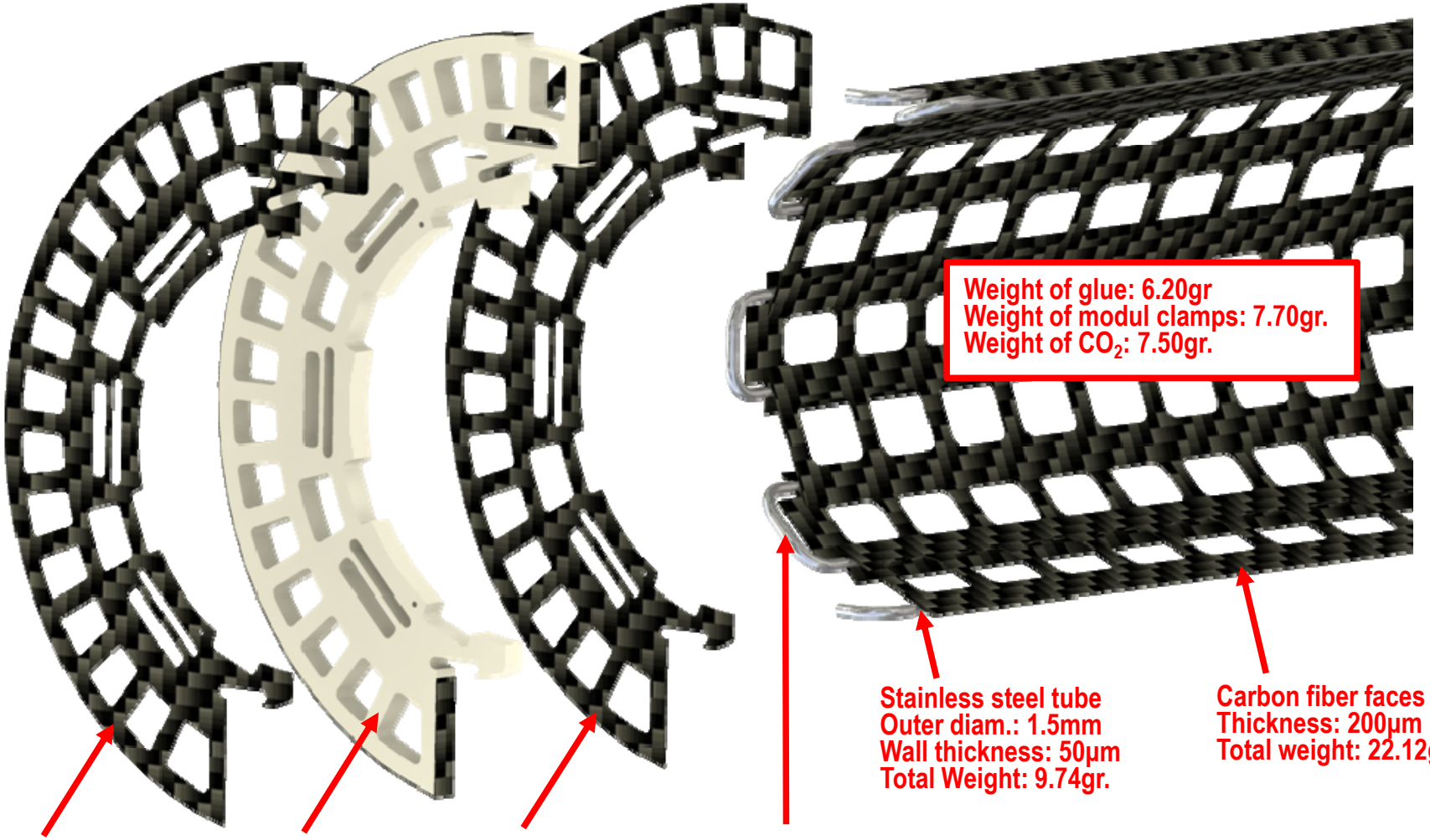


CO_2 Cooling Loops and Connection to Supplytubes



- Each half shell has 10 cooling loops
- Each supply tube feeds 5 cooling loops
- Angle bend (~3^0) during insertion taken by **carbon fibre hinge**

PBIX mechanics 2013 in detail



Weight of glue: 6.20gr
Weight of modul clamps: 7.70gr.
Weight of CO_2: 7.50gr.

Stainless steel tube
Outer diam.: 1.5mm
Wall thickness: 50µm
Total Weight: 9.74gr.

Carbon fiber faces
Thickness: 200µm
Total weight: 22.12gr.

Carbon fiber flange
Thickness: 200µm
Weight: 0.86gr.

Airex flange filler
Thickness: 4mm
Weight: 0.55gr.

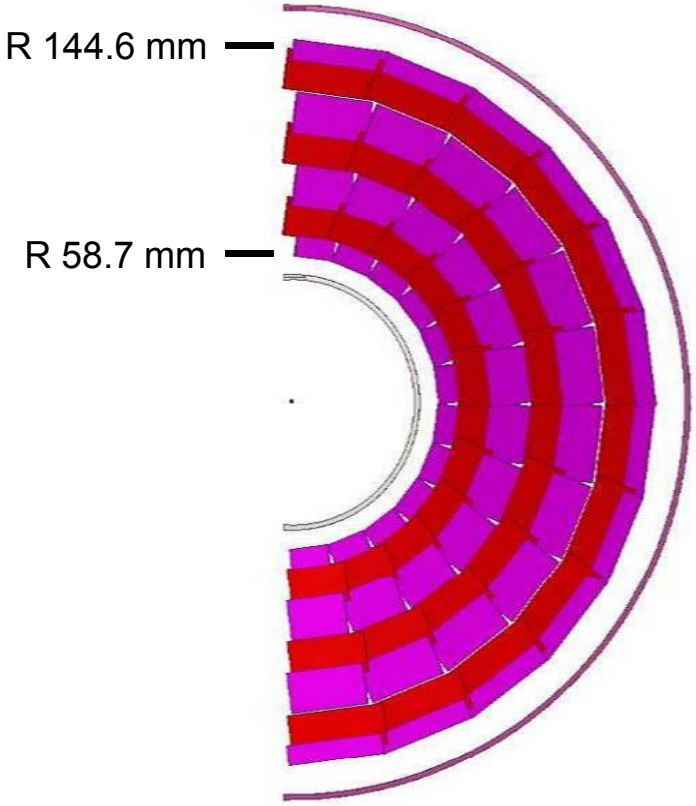
Carbon fiber flange
Thickness: 200µm
Weight: 0.86gr.

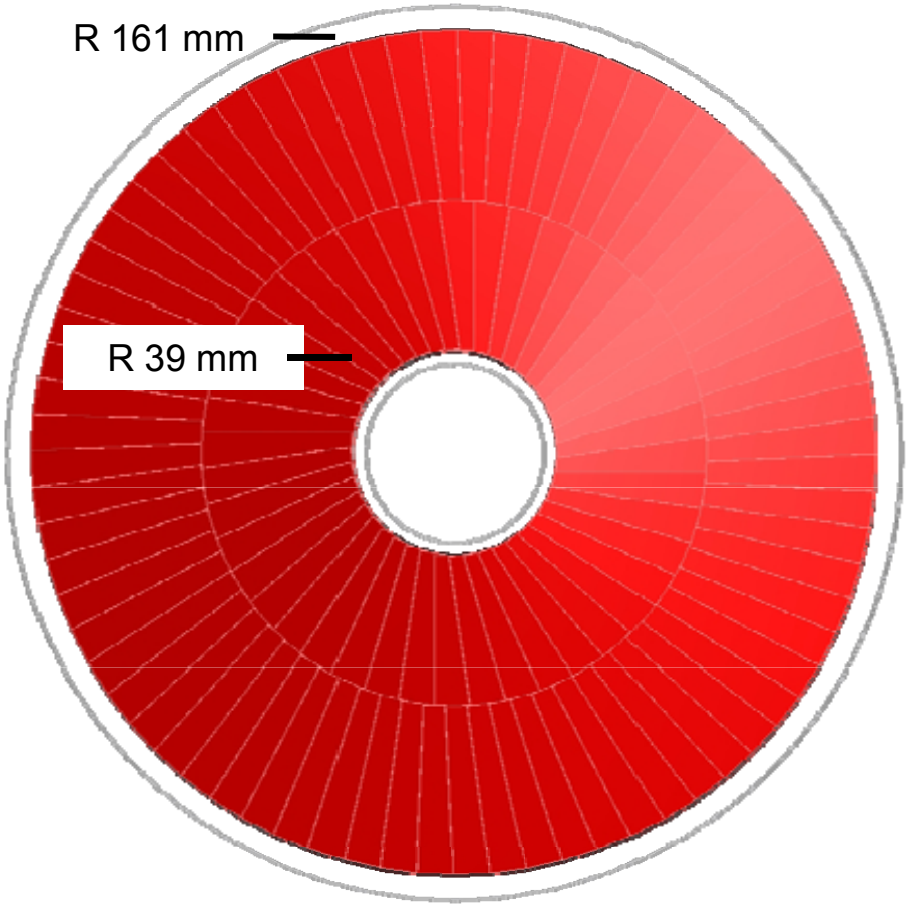
Stainless steel bends
Outer diam.: 1.8mm
Wall thickness: 100µm
Total weight: 1.09gr.

Total weight: 59.11 gr.

Conceptual Disk Module Layout

radial and ϕ overlaps (with 20° tilt of sensors) to cover Phase 1 FPIX region

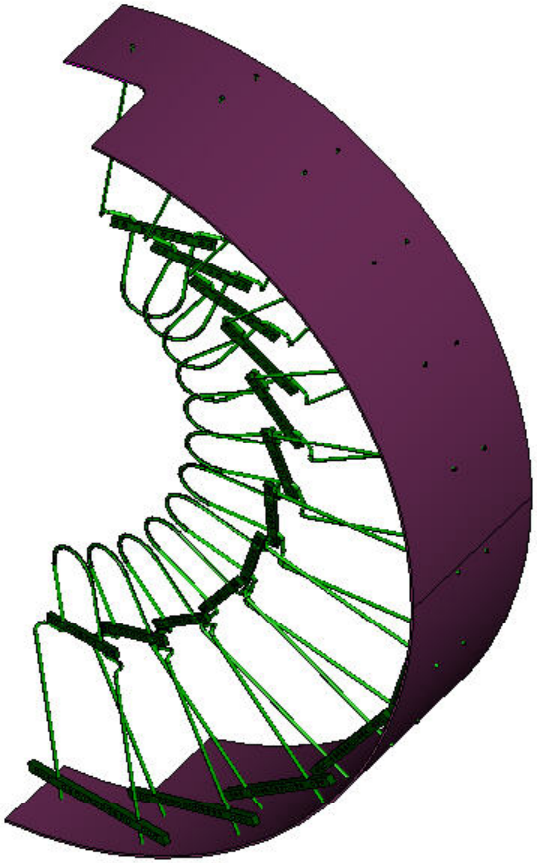




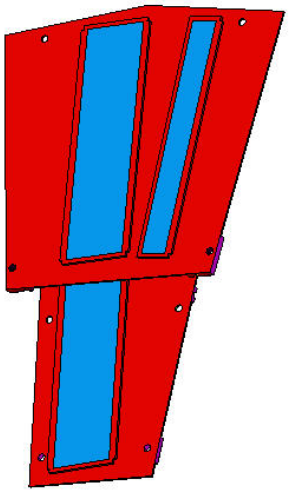
- Current Fpix module layout
- 7 module geometries
- 168 modules per disk →1080 ROCs

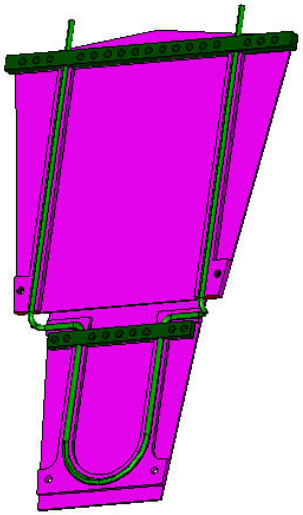
- Radial layout of (72) 2x8 outer and (44) 2x8 inner radius modules
- 1 module geometry
- 116 modules per disk → 1856 ROCs

The Complete FPIX Assembly

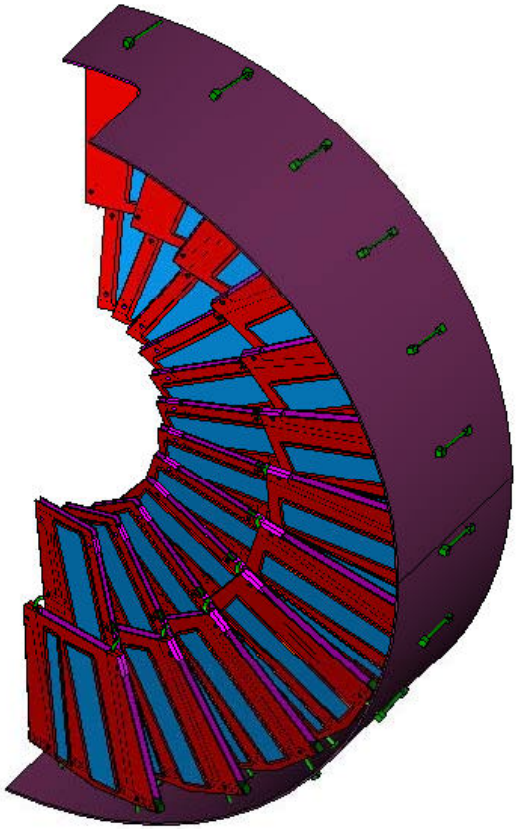


CO_2 cooling structure





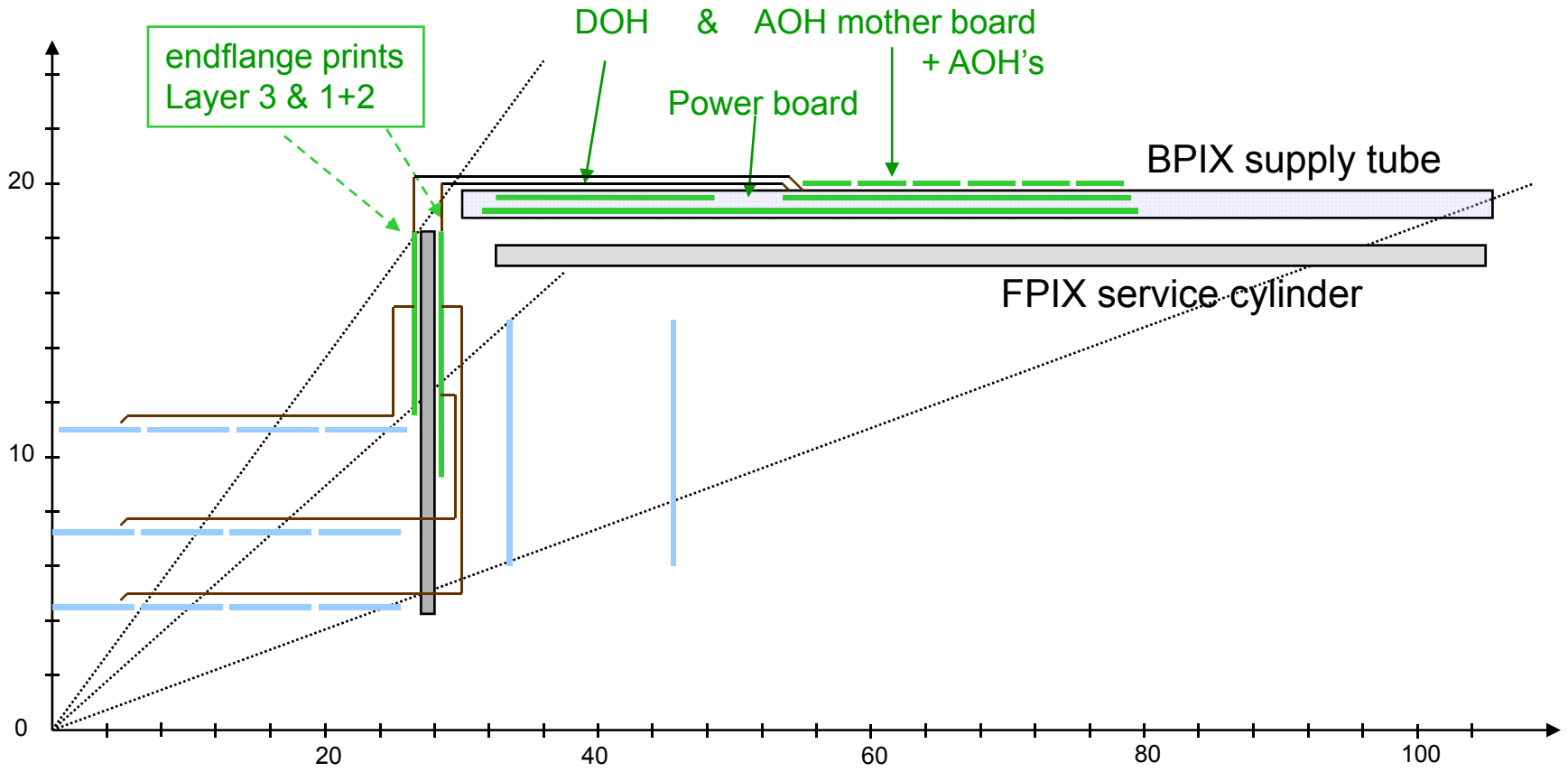
Conceptual design of new blade with TPG substrate and cooling pipe



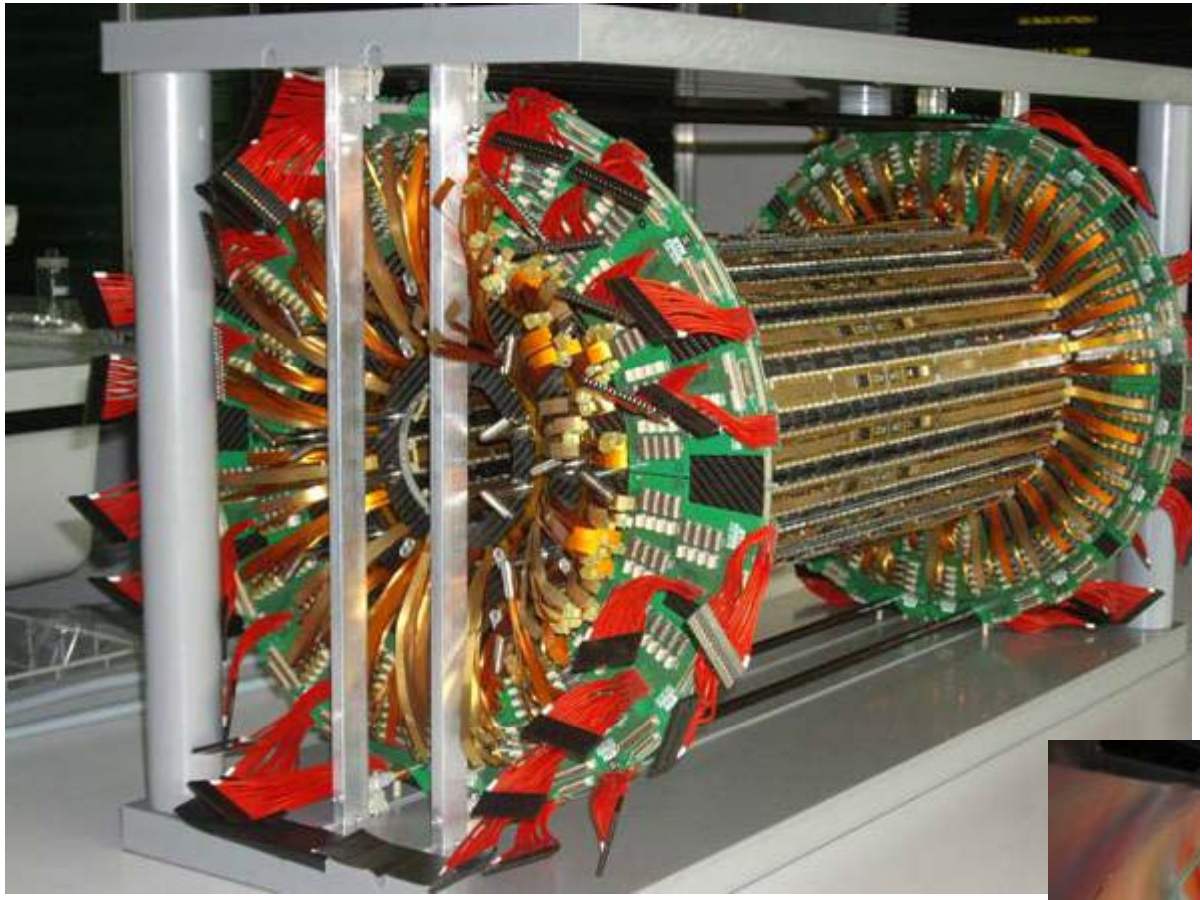
Total Quantity per half disk:

Outer: 2X8 : 24 modules, 384 ROCs
1X8 : 24 modules, 192 ROCs
Inner: 2X8: 24 modules, 384 ROCs

Current Pixel System with Supply Tubes / Cylinders

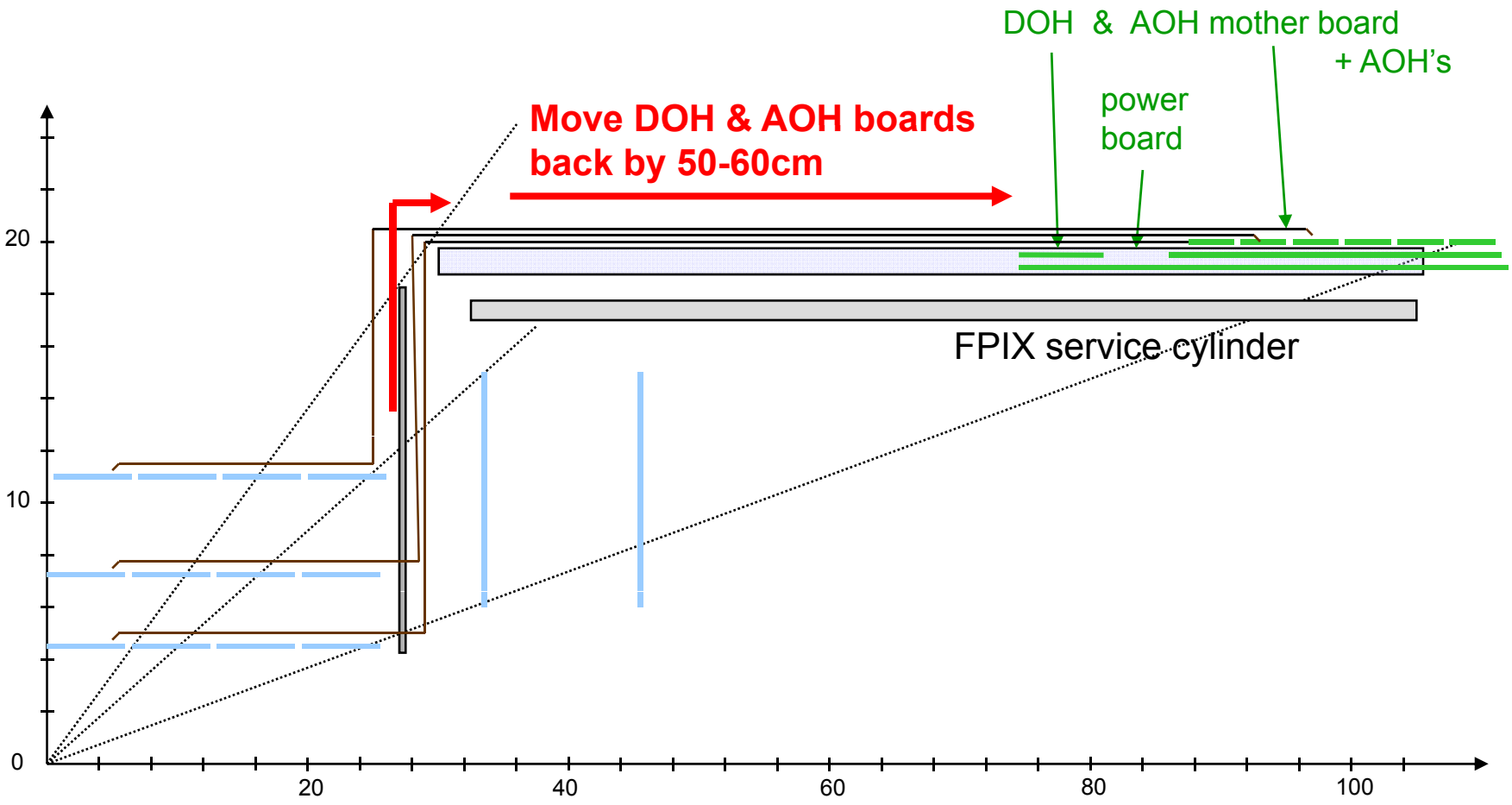


BPIX Cabling & flexible cooling pipes

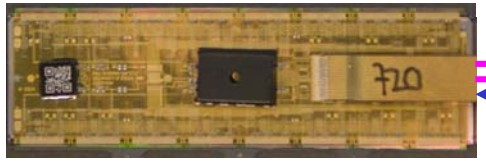


Shift PCB/Plug Material out of tracking Volume

- Modules with long pigtails (1.2m) CCA wires 16x(2x125μ)



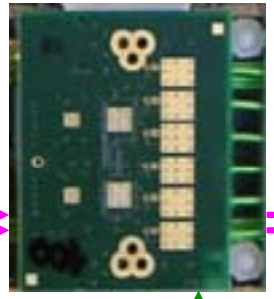
CMS Pixel System



320 MHz binary

40 MHz analog out

px-AOH



320 MHz binary optical

40MHz analog optical

px-FED

A

B

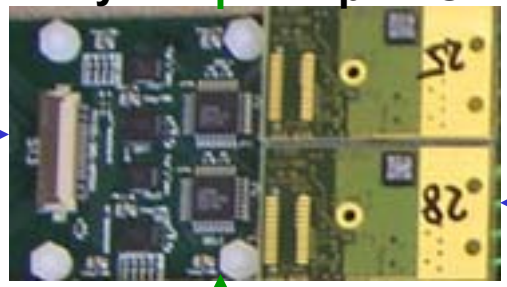
crt, 40MHz

fast I²C

I²C

PLL Delay25

px-DOH



px-FEC

I²C

CCU

trk-FEC

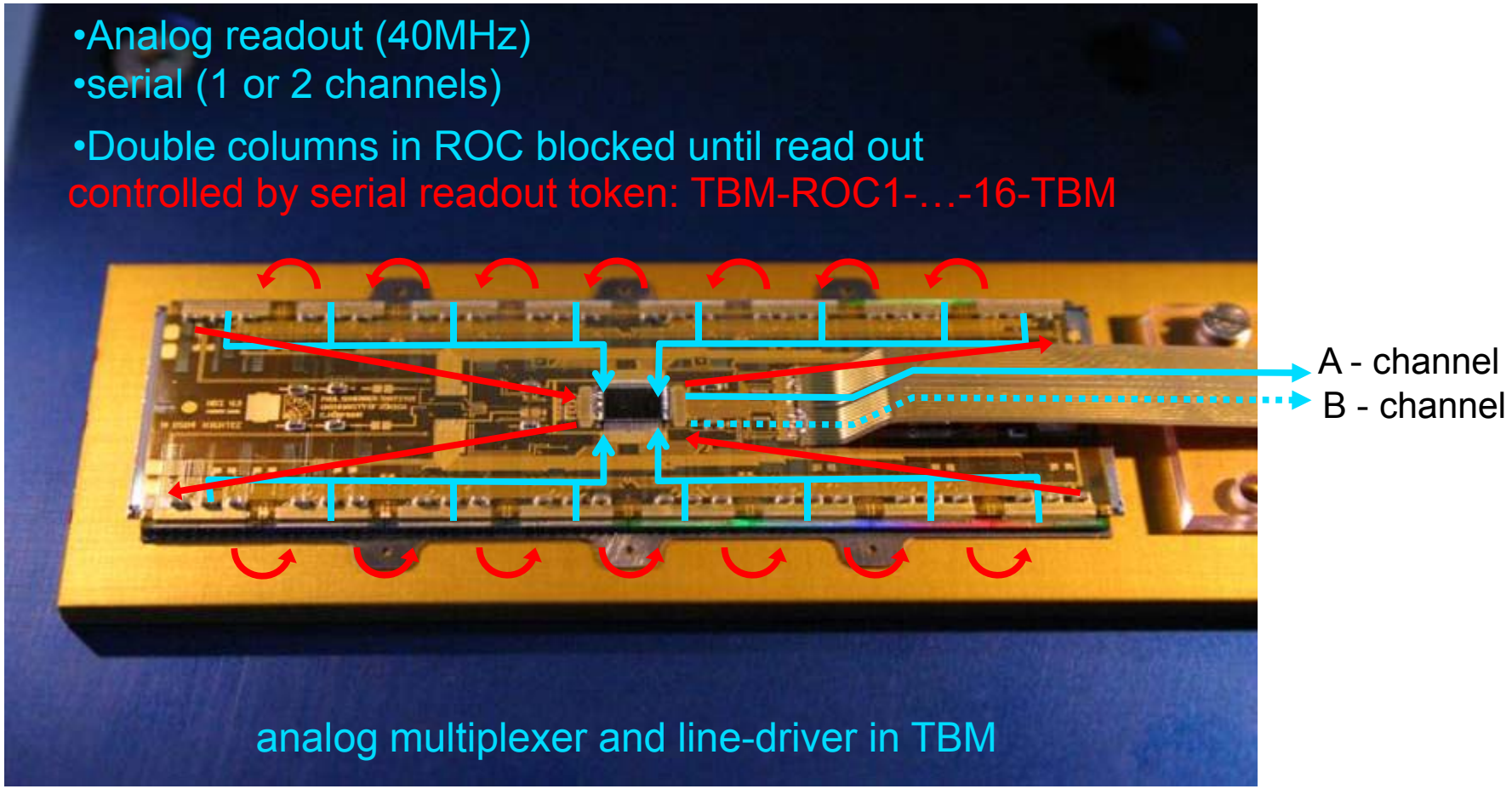
New Phase 1 System: 0-suppressed serial binary data readout at 320MHz, same data structure

Current System: 0-suppressed analog coded data readout at 40MHz

skip

BPIX module

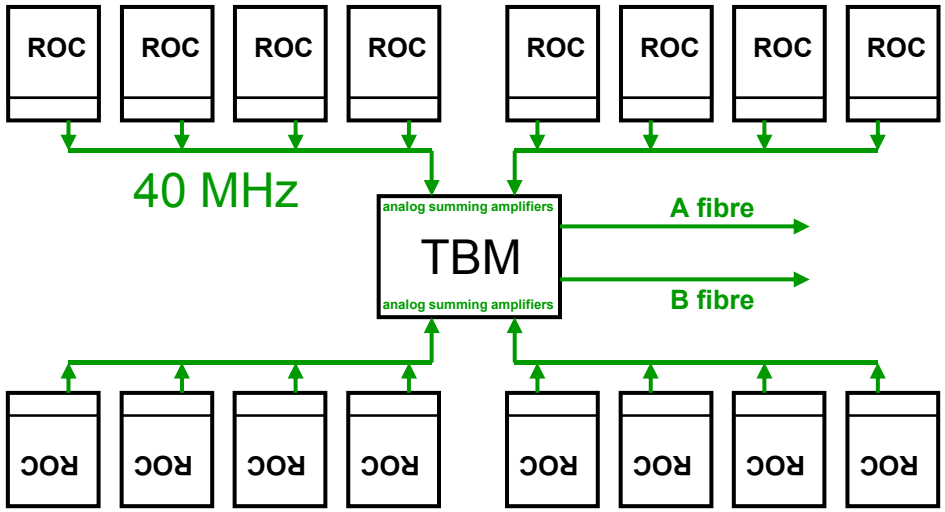
4 x 4 ROC → TBM → AOH → pxFED



Current Pixel Module Readout

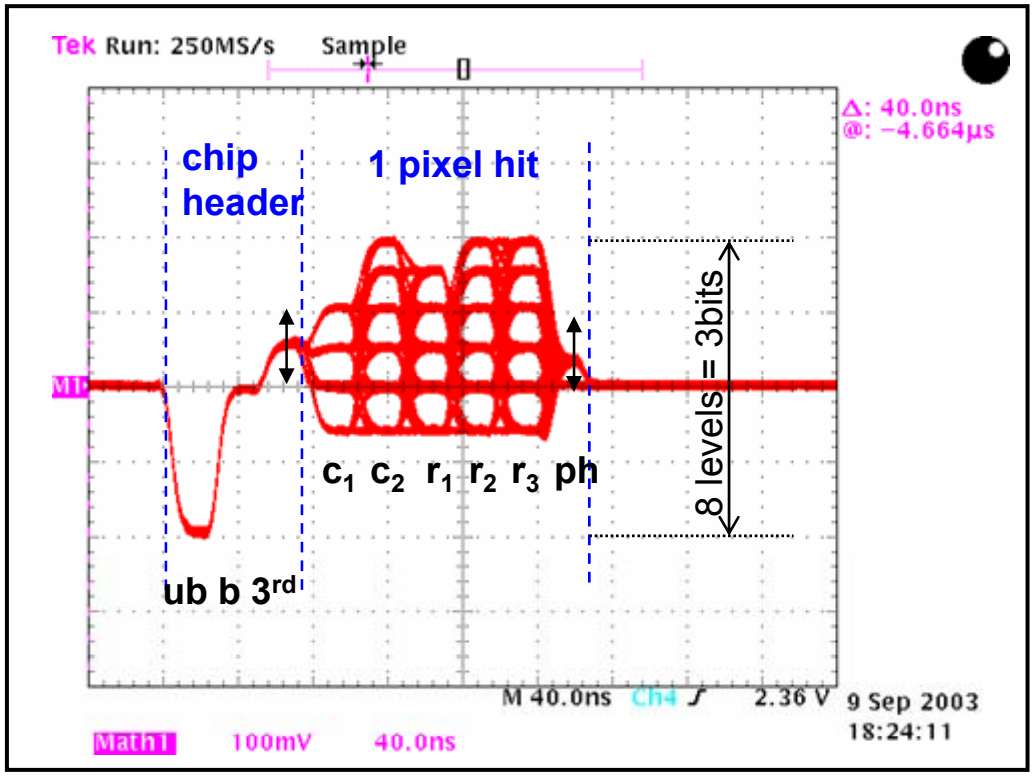
ROC → TBM : 40 MHz analog readout

TBM → pxFED : 40 MHz analog readout



Layer 1& 2 → 2 Fibre A & B
Layer 3 → 1 Fibre A

Present analog coded data transfer of pixel system



Pixel uses analog coded digital pixel readout

Pixel address 5 x 3 bit

Pulse height 1 x 8 bit

→ **total 23 bits/ pixel hit**
in 6 clock cycles

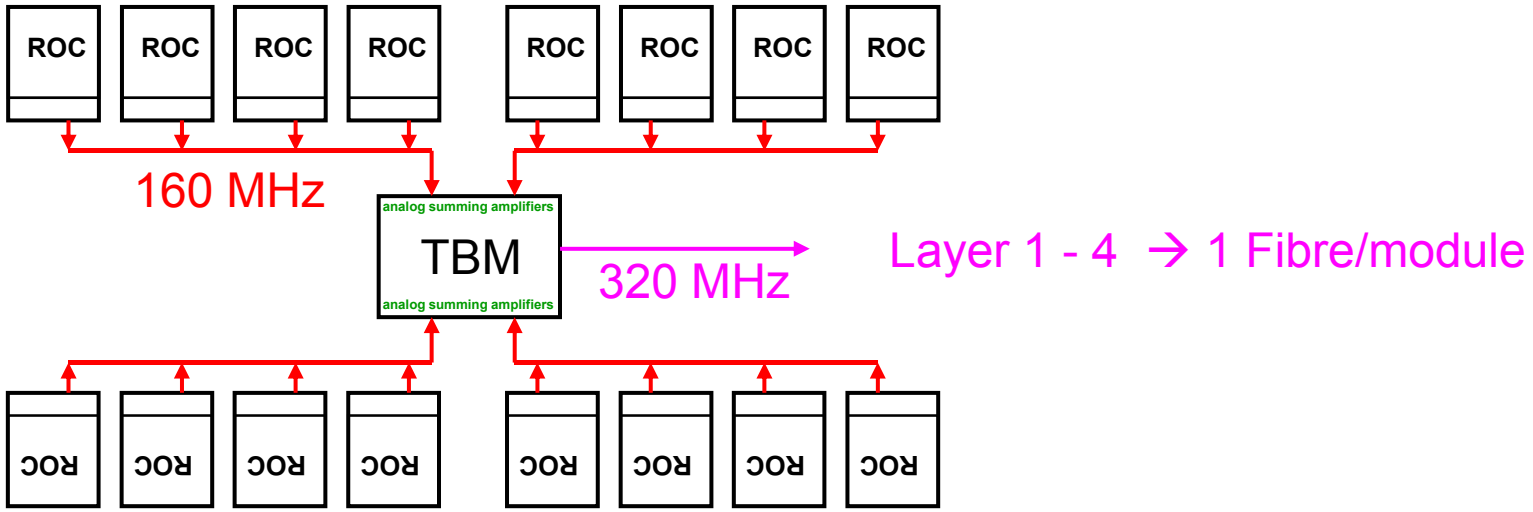
→ 160 Mbits/sec link speed

resp. 1300 pJ/bit

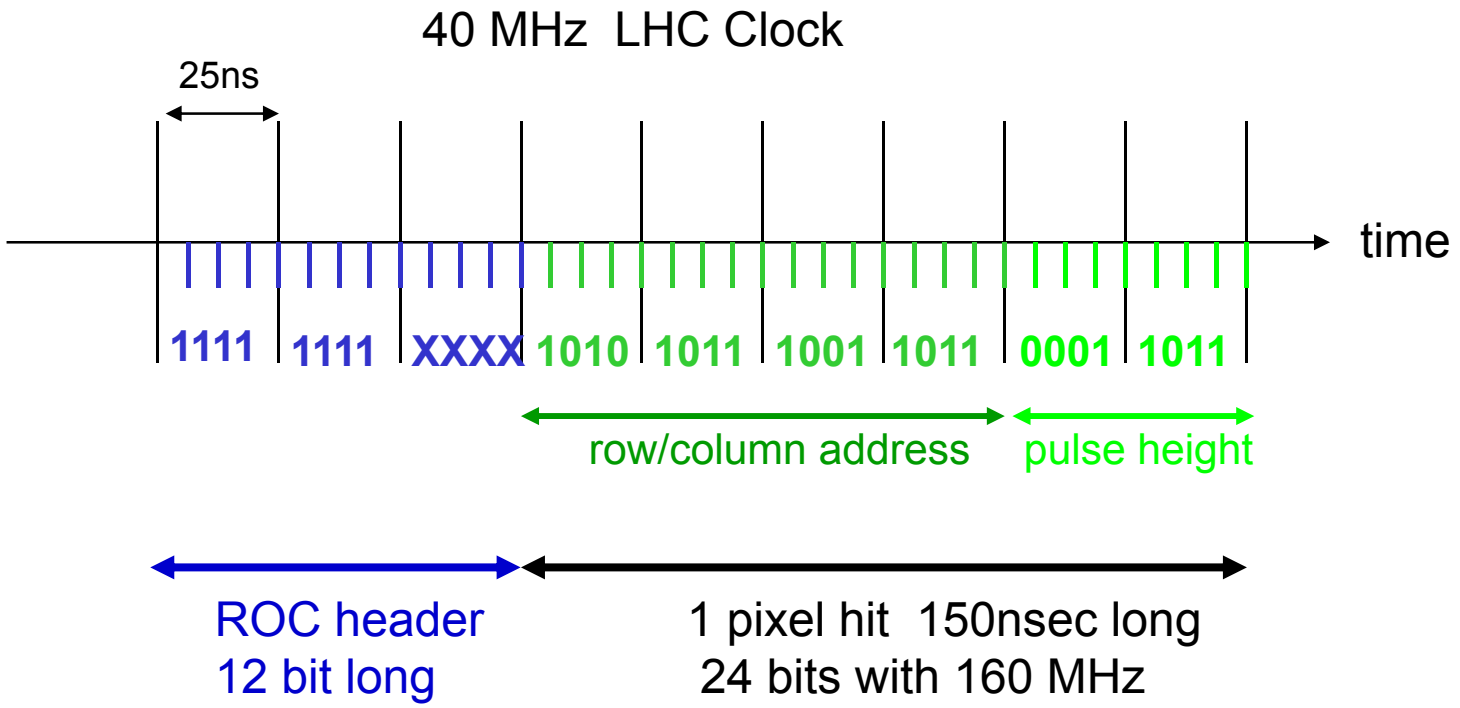
New Serialized Binary Pixel Module Readout

ROC → TBM : 160 MHz digital readout

TBM → pxFED : 320 MHz digital readout



New serial binary data transfer of pixel system

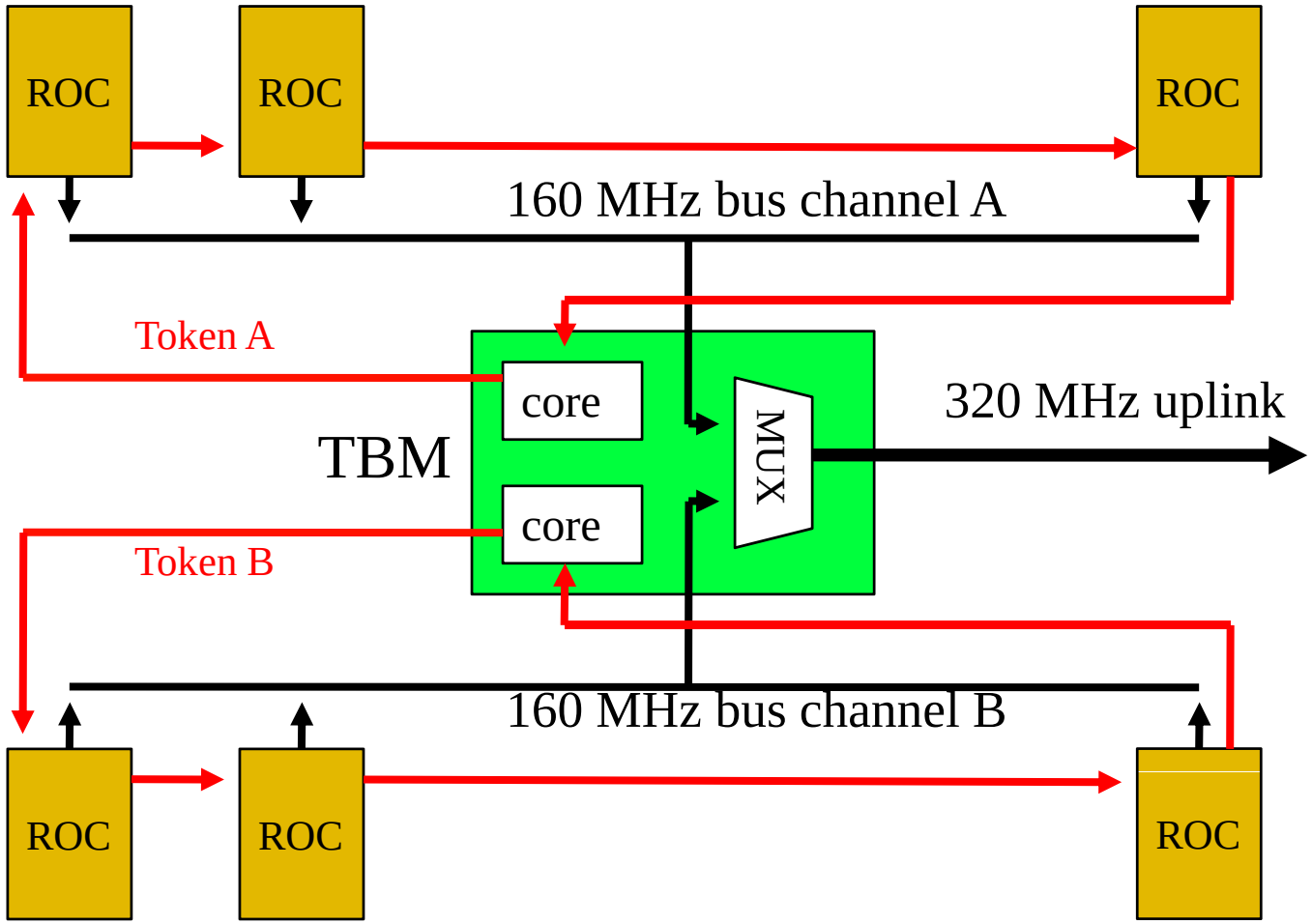


New ROC serial bit clock is 160MHz → 4 bits / LHC clock cycle

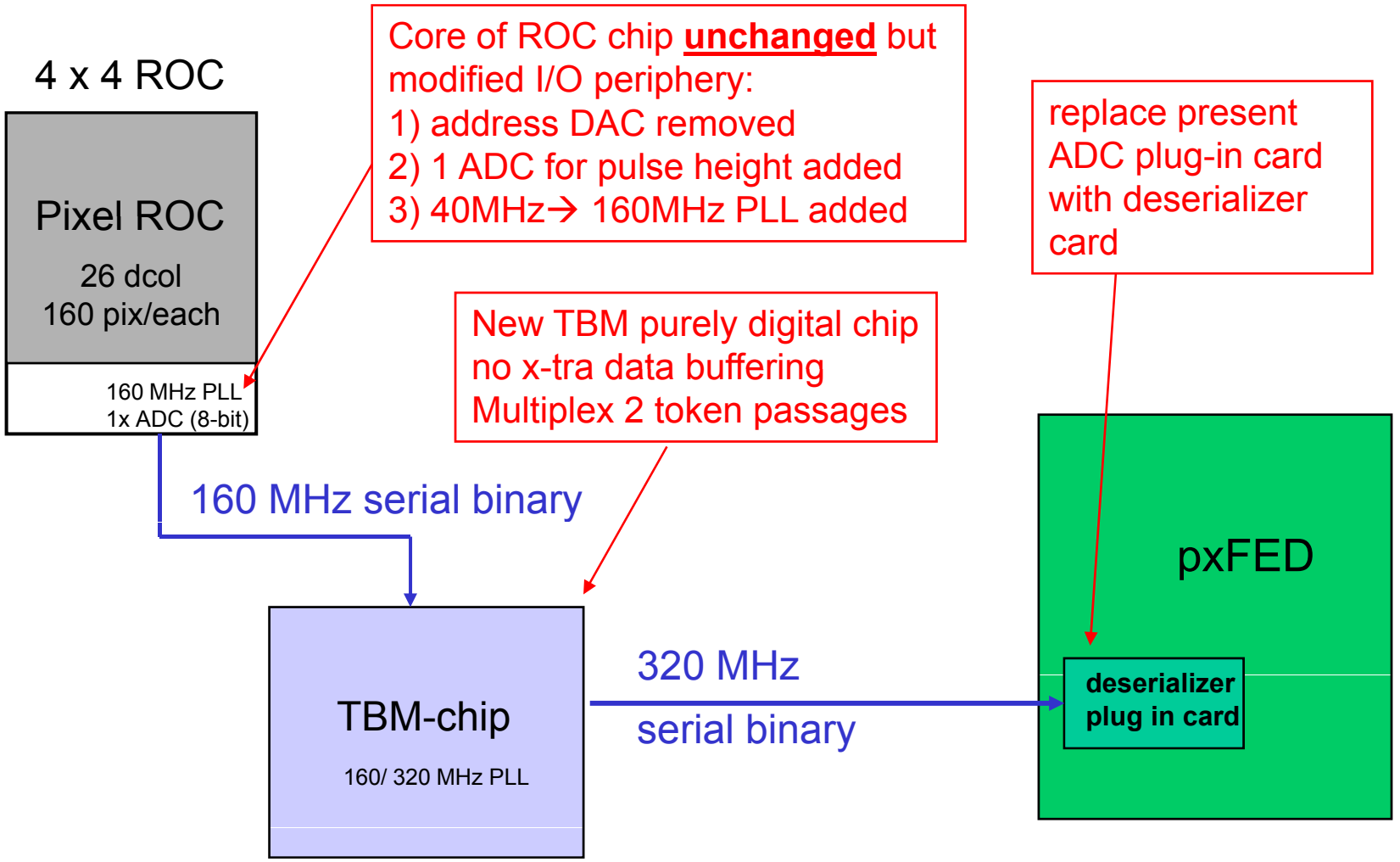
160 MHz clock to be generated in each ROC by 40 MHz → 160 MHz PLL circuit

→ See talk H-C. Kästli

Basic Idea of digital module



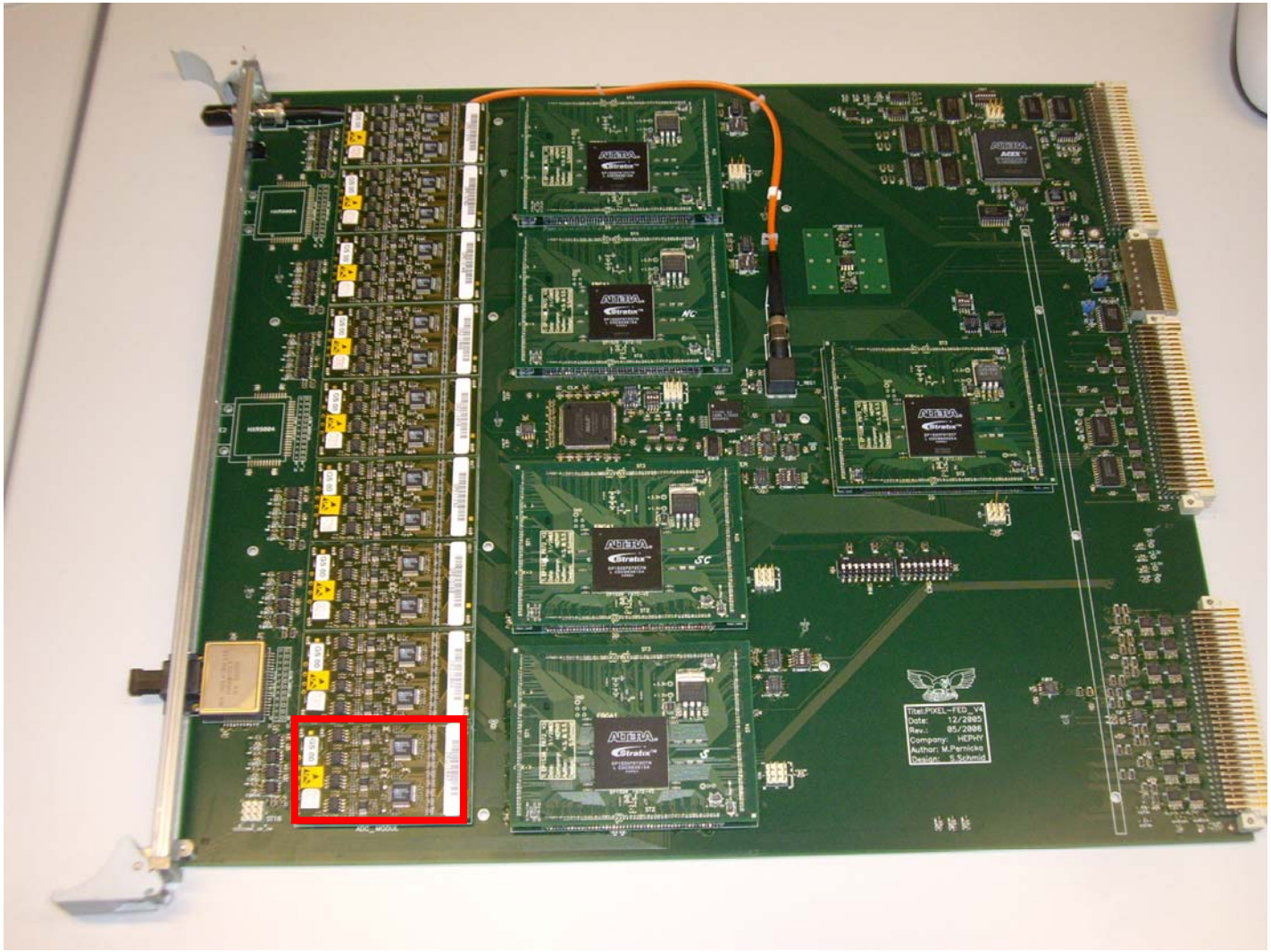
Changes for 160/320 MHz serial binary readout



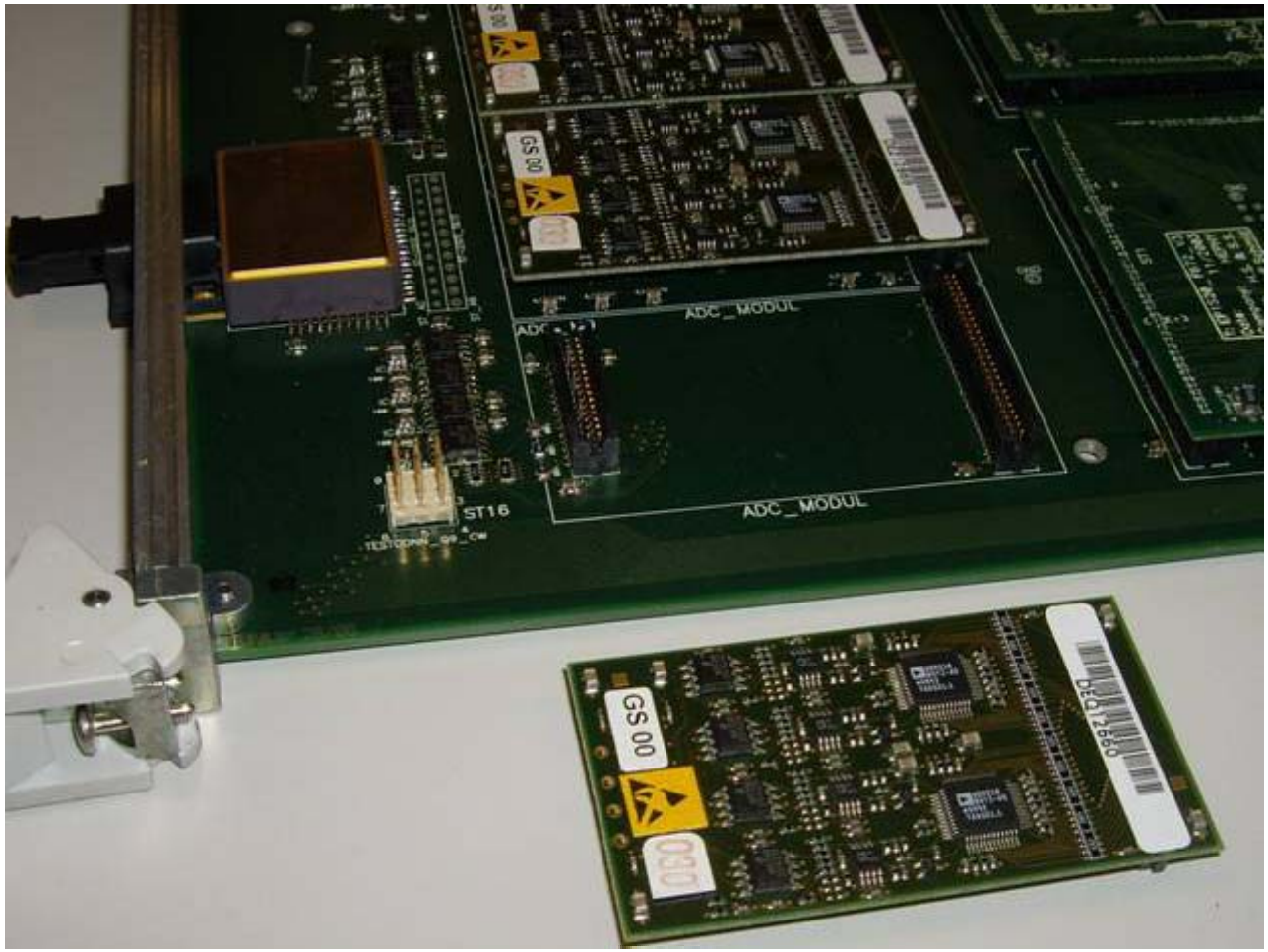
Pixel FED

HEPHY, Vienna
M.Pernicka
H. Steininger

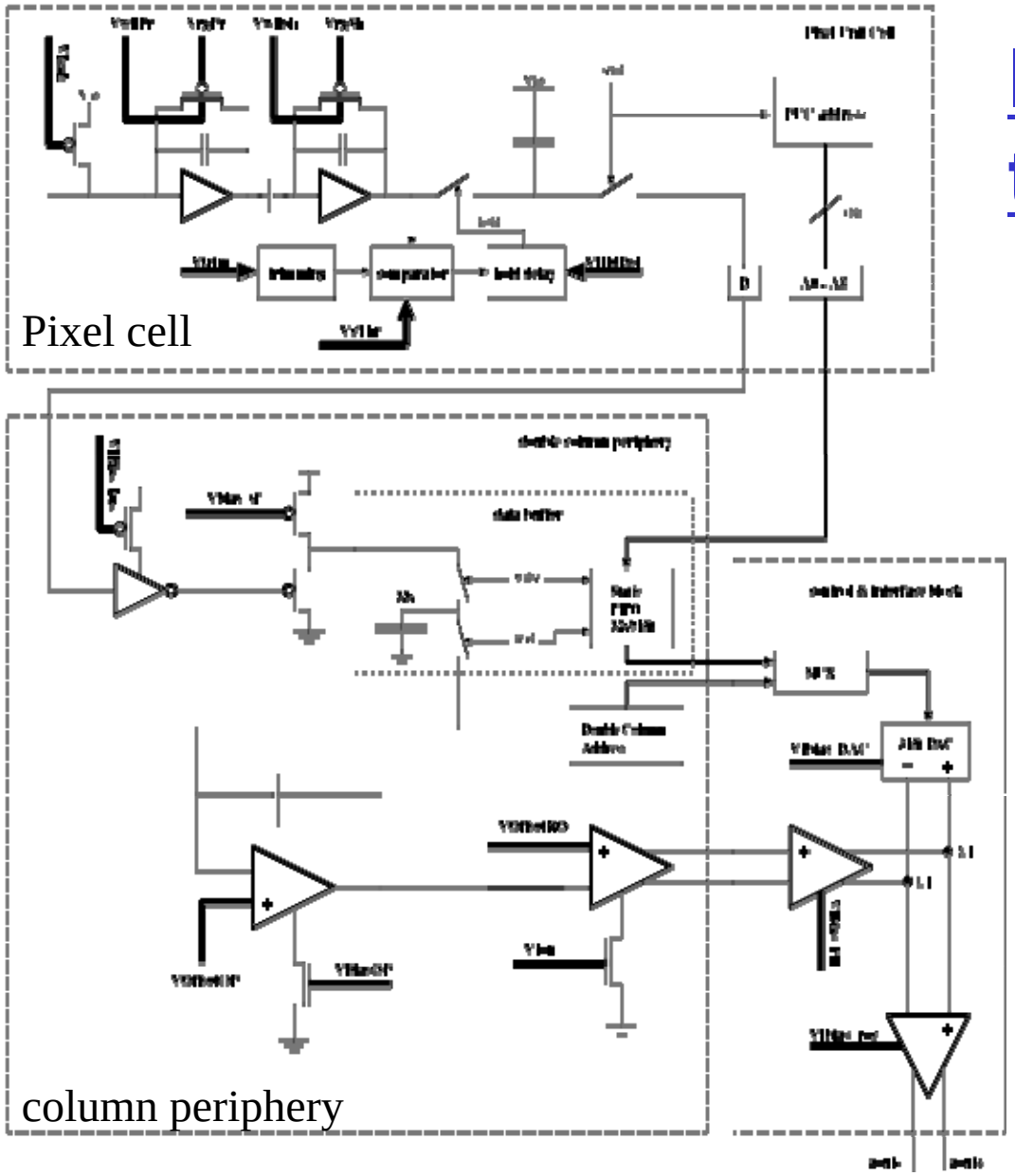
3x 12 channels with 9 piggy-back ADC cards



Discussions with M. Pernika, M. Friedl, H. Steininger from HEPHY about replacement of ADC card with deserializer card look technically promissing.



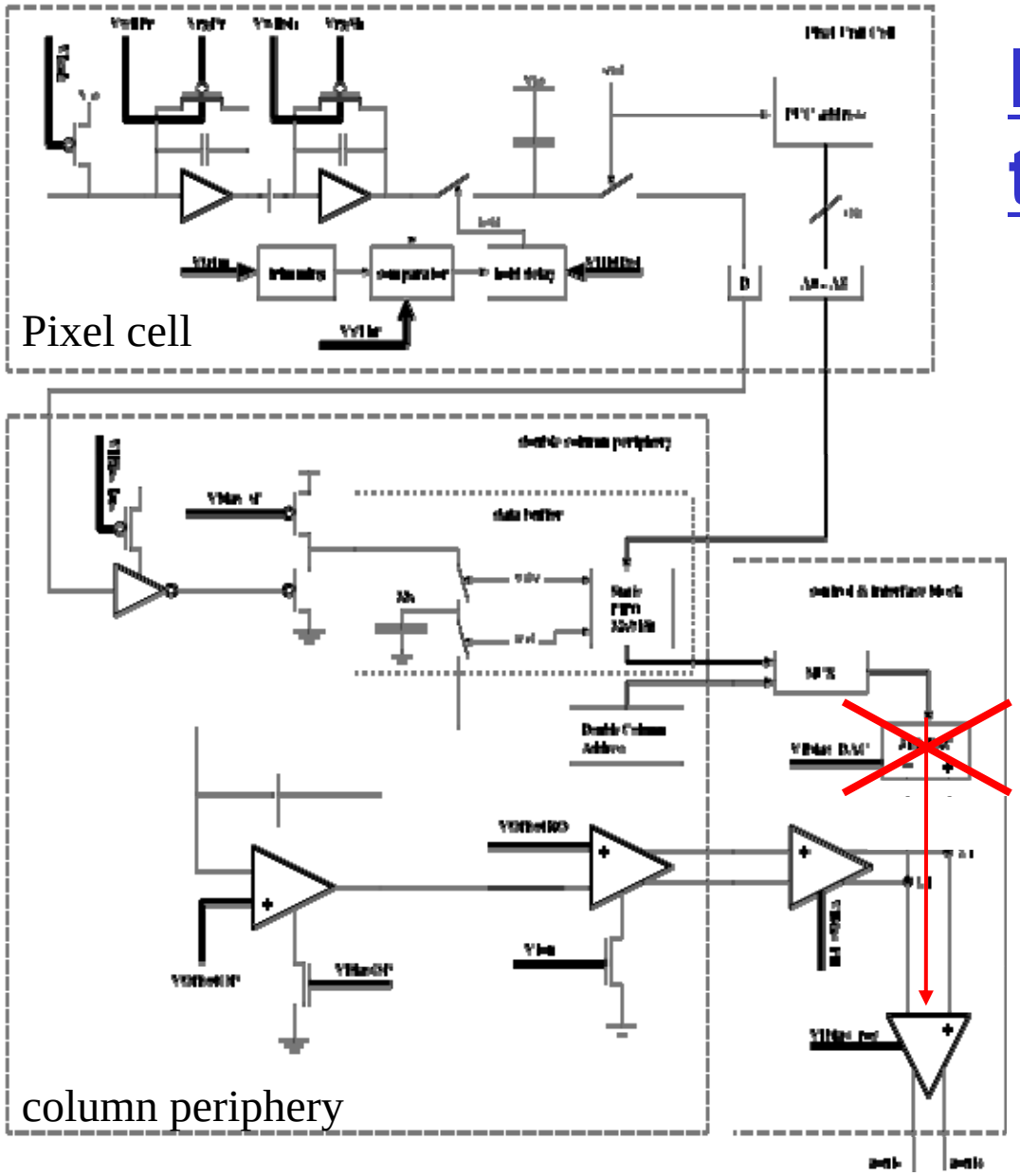
Implications for the ROC



Signal chain in present ROC psi46V2

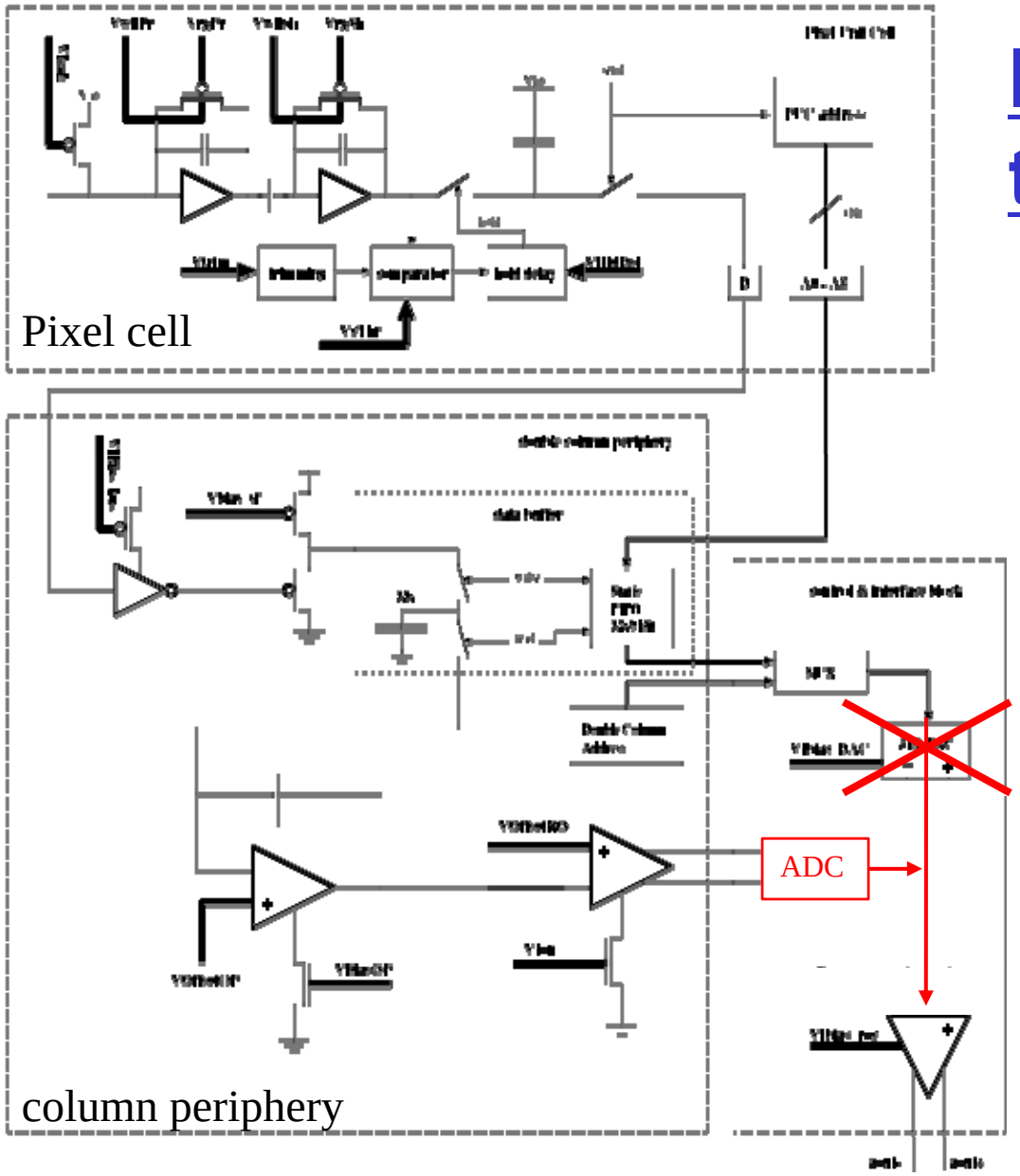
Chip periphery

Implications for the ROC



Address internally already digital
→Remove DAC
→trivial

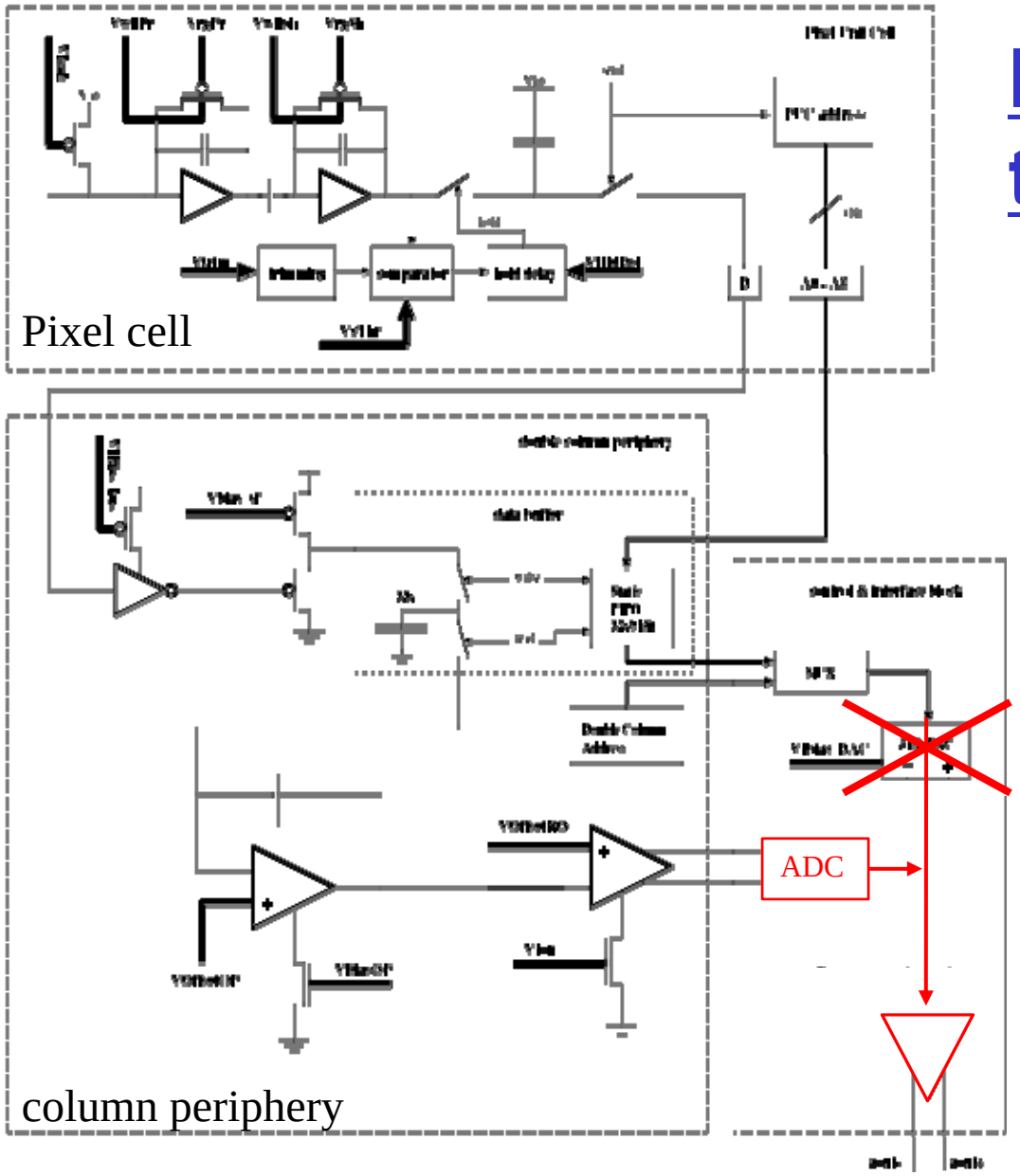
Implications for the ROC



Need to digitize pulse height information

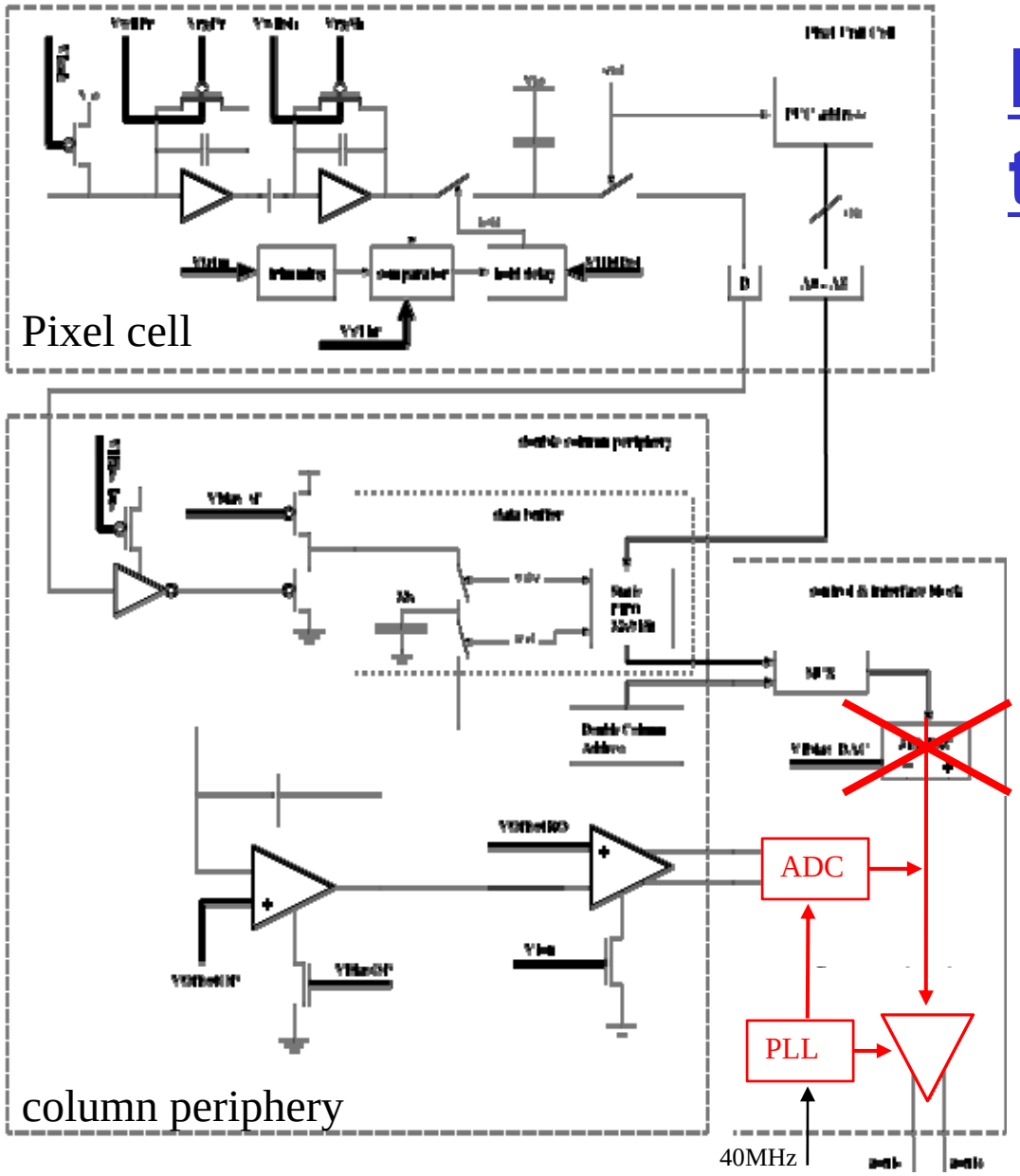
→Need fast 8 bit ADC

Implications for the ROC

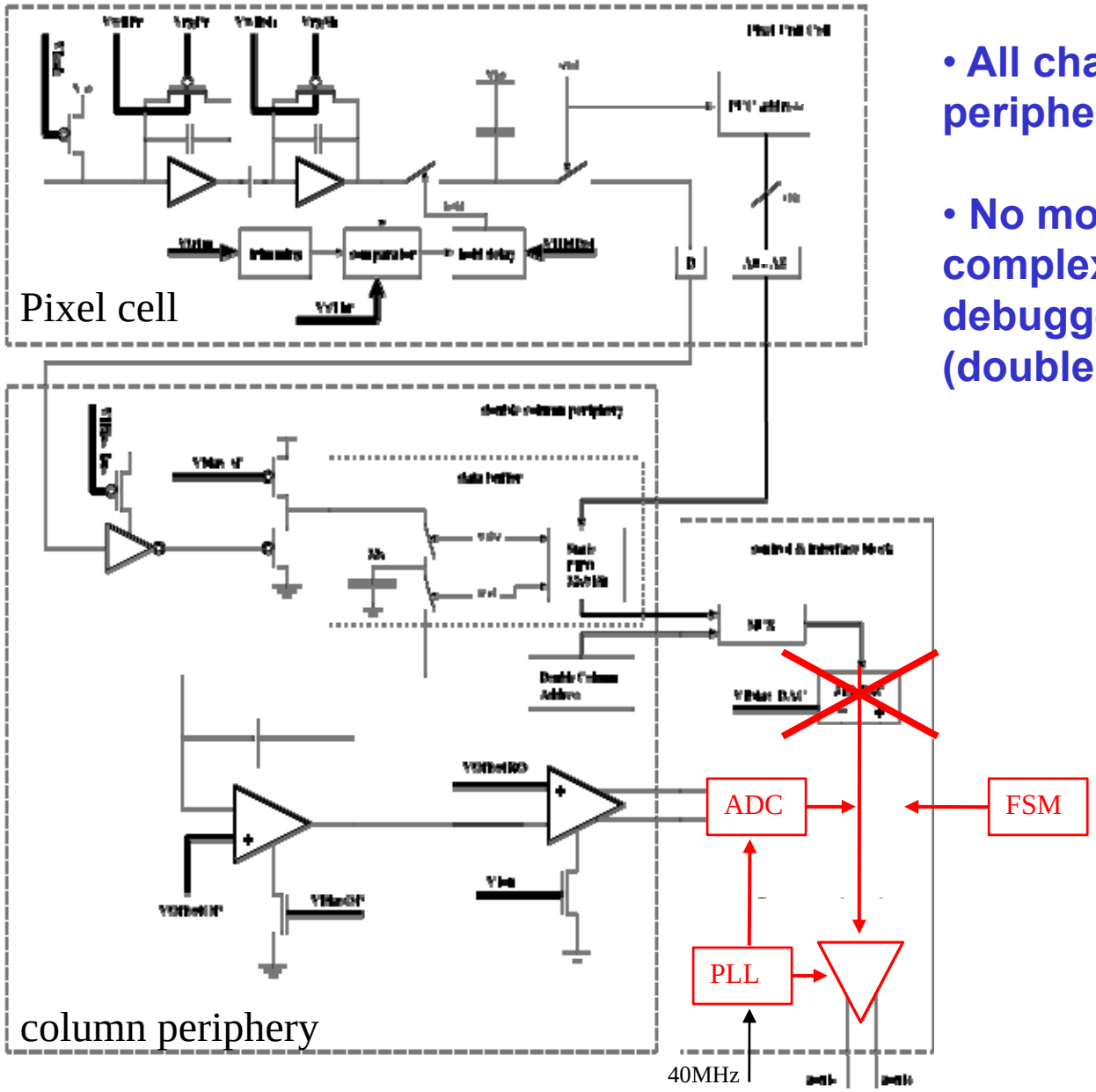


New fast and low power output driver

Implications for the ROC



Output at 160MHz
→Clock multiplier with PLL



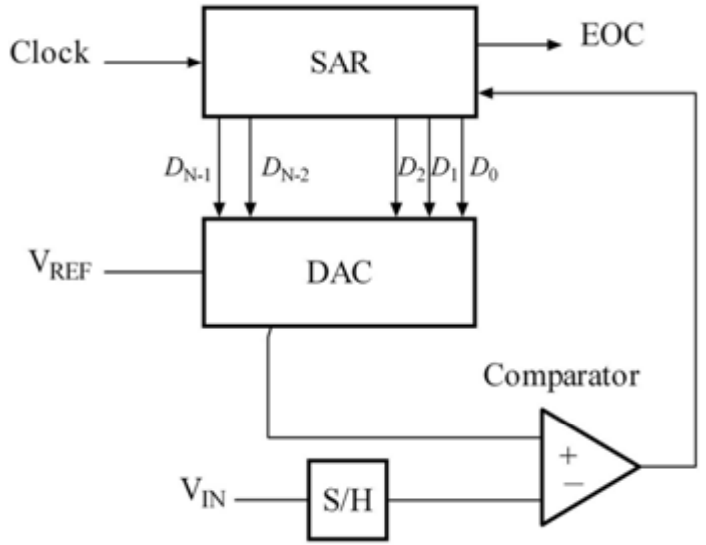
- **All changes in the ROC periphery**
- **No modification of the complex and well debugged chip core (double columns)!**

Modified logic

Pulse Height ADC

- 8 Bit successive approximation current ADC
- Not pipelined → need 8 clock cycles conversion time
- Last year first 4 Bit prototype in 0.25µm produced and tested @ PSI
- Works well up to 80MHz
- Noise problems and non-linearity discovered
- Improved version resubmitted

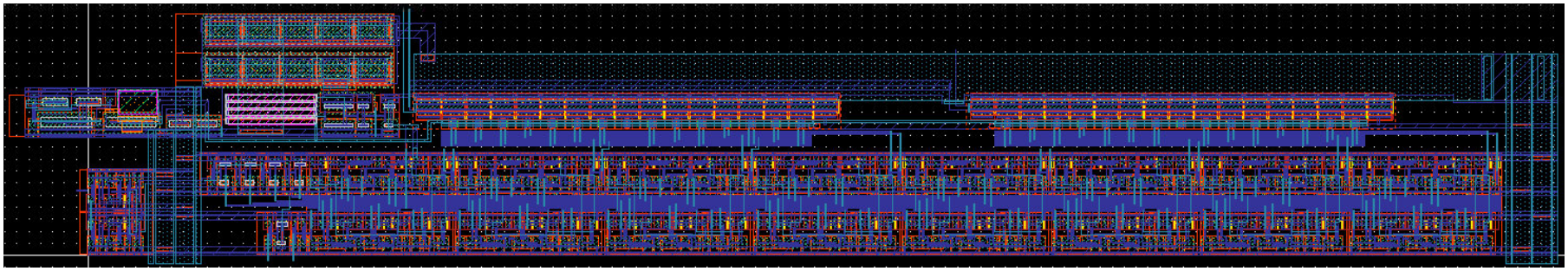
  (B. Meier)



Pulse Height ADC

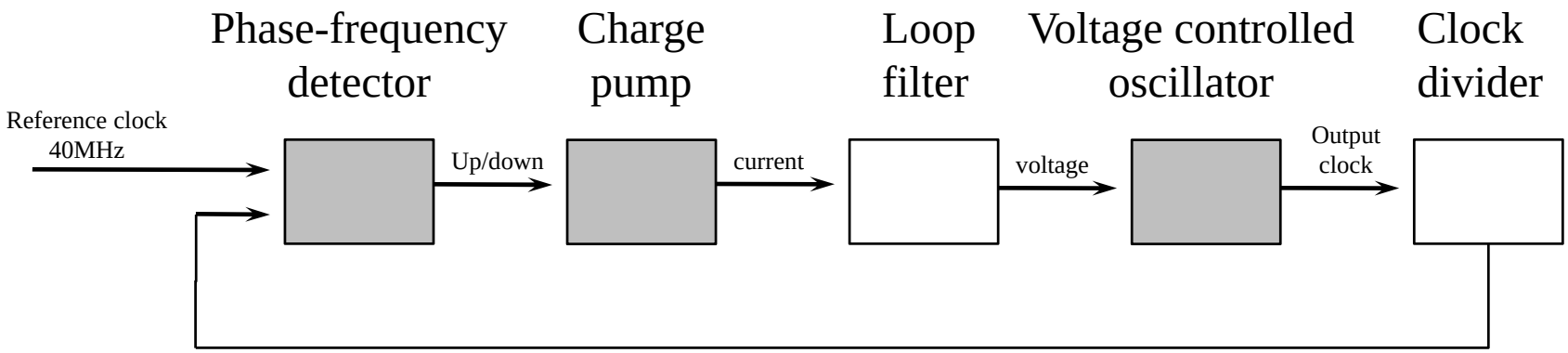
→ one per ROC

B. Meier PSI



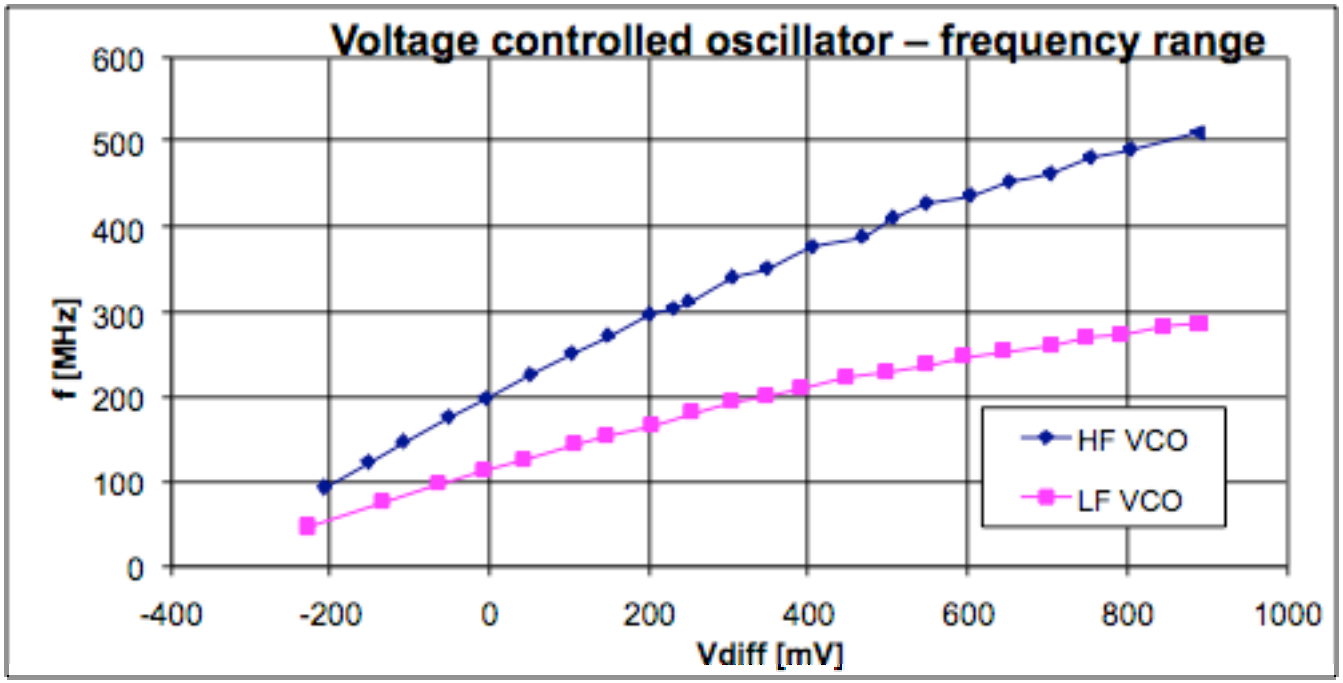
- Improved 8 Bit version submitted in February 09
  - Added sample/hold circuit at input
  - 8 bit DAC
  - Added capacitance to power rails
  - Size: 640µ x 90µ
  - 80 MHz conversion clock → 100nsec/conversion

Clock multiplier / PLL



- Some building blocks (grey) submitted in IBM 0.25µm in 4/08
- Tested individual components and complete PLL with external filter / divider
- Works as expected from simulation, appeared very robust
- Locks immediately for 80/160/320 MHz output

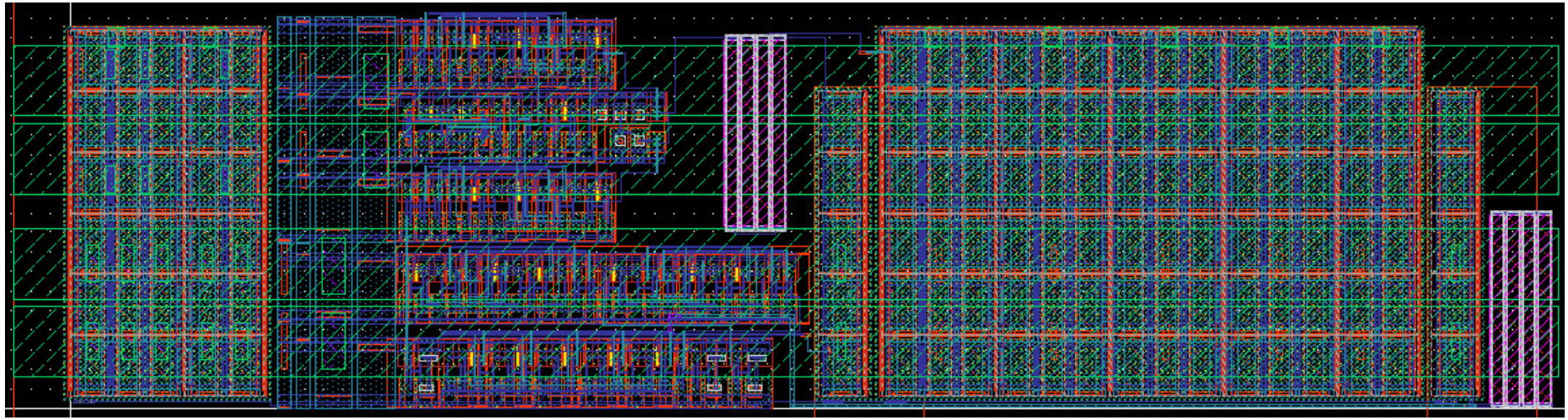
PLL – Voltage Controlled Oscillator



- Measured frequency range of 2 VCOs in 0.25µm
  ≈ possible target output frequencies

- Doesn't fit well with simulations (not a surprise)
  → large margin

Clock multiplier / PLL



- Complete clock multiplier cell Size: **380µm x 100µm**
- No external components, but added pads to change filter characteristics with external R/C (diagnostics)
- Improved design ready (Beat Meier)
- To be submitted in February 09

Conclusion & Outlook

- 4 layer system needs higher uplink bandwidth
- Only feasible with digital links
- Implementation with minimal impact on overall system
- Changes in present 0.25mm ROC limited to small regions in interface block
- No change in down link chain
- All new functional blocks were submitted mid February on MPW.
- ROC modifications planned until November 09
- Changes in TBM restricted to uplink signal path. Target speed: 320 MHz

Schedule & Crucial Dates

1st R&D Sumission of PLL, ADC & LCDS blocks on 0.25um	March 2008 done
Design of UL Barrel Mechanics	Fall 2008 done
2nd Submission of final 160 MHz PLL & 8bit ADC	Feb. 2009 done
→ Fabrication of 1 Layer prototype barrel mechanics	March 2009 now
Phase 1 TDR	Summer 2009
Submission of digital pixel ROC (PSI46dig)	Nov. 2009
Submission of new digital TBM	Nov. 2010
Start of module production (18 month)	Spring 2011
Start of module integration onto mechanics	Summer 2012
Install new 4 layer pixel detector	Feb. 2013