



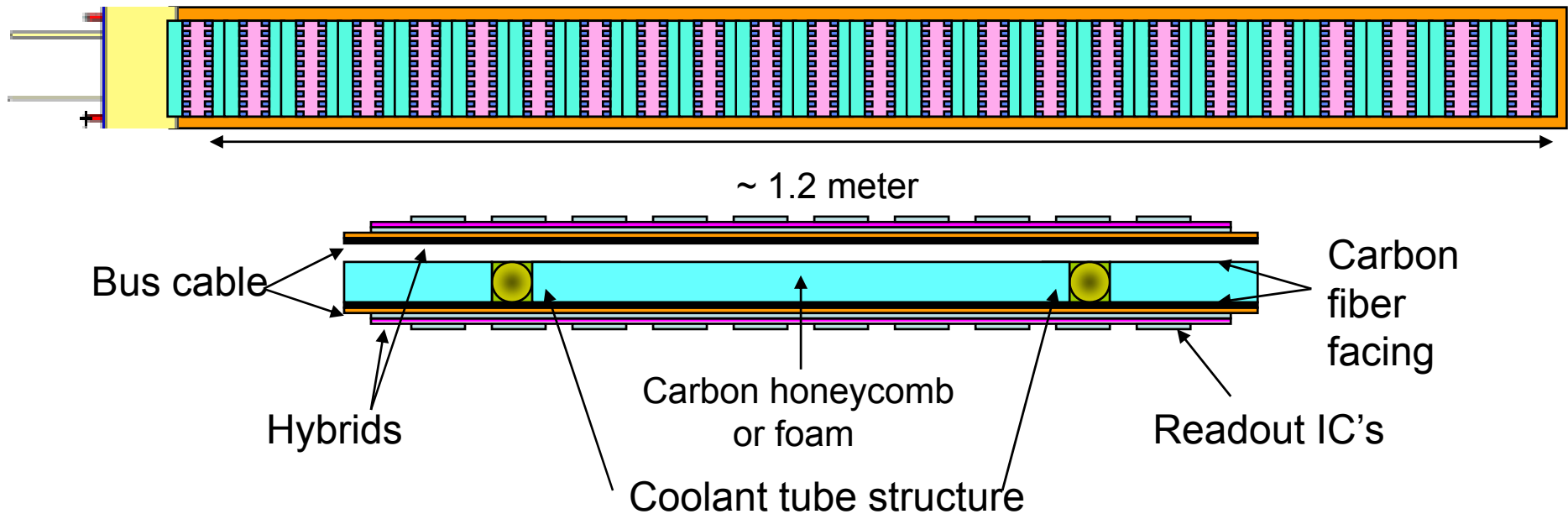
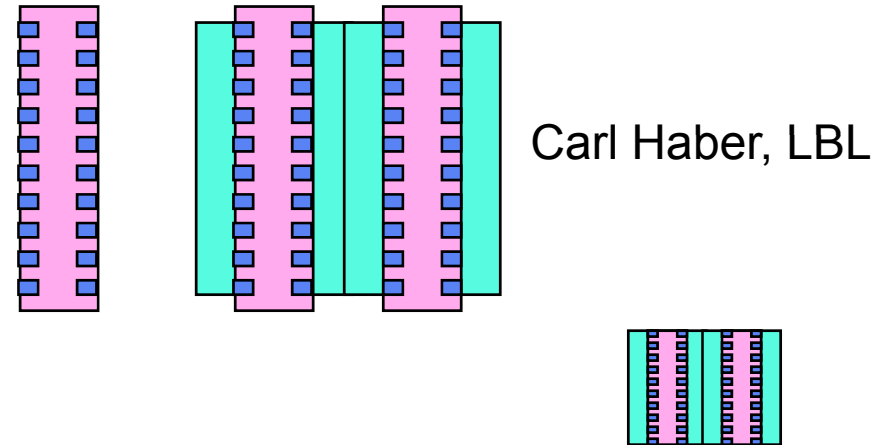
UK Hybrid Development for ATLAS SLHC Short Strips

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Stave-2009 Components

- P-type 4 segment crystals
- ABC-next
- Kapton hybrid with BCC chip
- Embedded bus cable
- End of stave card
- FPGA based DAQ system
- Stave mechanical core
- Assembly and measurement fixtures



Stave Hybrid

Hybrid build and what has to be considered

- Hybrid layout is driven by minimising material
 - Keep the area small
 - Need to communicate early with ASIC and sensor designers, lab staff, foundries, etc.
- Use of low impedance power and ground planes to ensure reduction of high frequency parasitics
 - Otherwise, potential for capacitive coupling, crosstalk, voltage drops, etc.
 - Implies more material! But put where needed!!
- Remember that we will ultimately want to source a large number of these circuits
 - Yield and reliability has also to be considered from the outset
 - Don't push the limits on the design rules (especially feature size)
 - Repeatability becomes problematic for non-standard capability
 - Limits vendor choice
- Feedback from UK (flex) manufacturers:
 - 100 μ m track and gap routing is best for large volume/yields
 - Vias lands need to be >300 μ m Via lands
 - Ref: CMS had many problems with micro-vias (had to increase to 320 μ m to recover yield/stability)
 - Settled on 375 μ m via lands, with 150 μ m laser drilled holes
 - For large volumes, thinnest dielectrics of 50 μ m

Staged Design/Production

- First Stage
 - Cautious
 - Determine performance of ASIC/sensors with maximal power planes, filtering, decoupling, etc.
 - Evaluate powering and decoupling choices, fast signal quality, ...
 - Test plans for mass reduction
 - Populate/bond in house
- Second Stage
 - More aggressive
 - Reduction in hybrid mass by removing surface mounts, reducing power planes, etc.
 - Focus more on layout for mass production compatible with staves

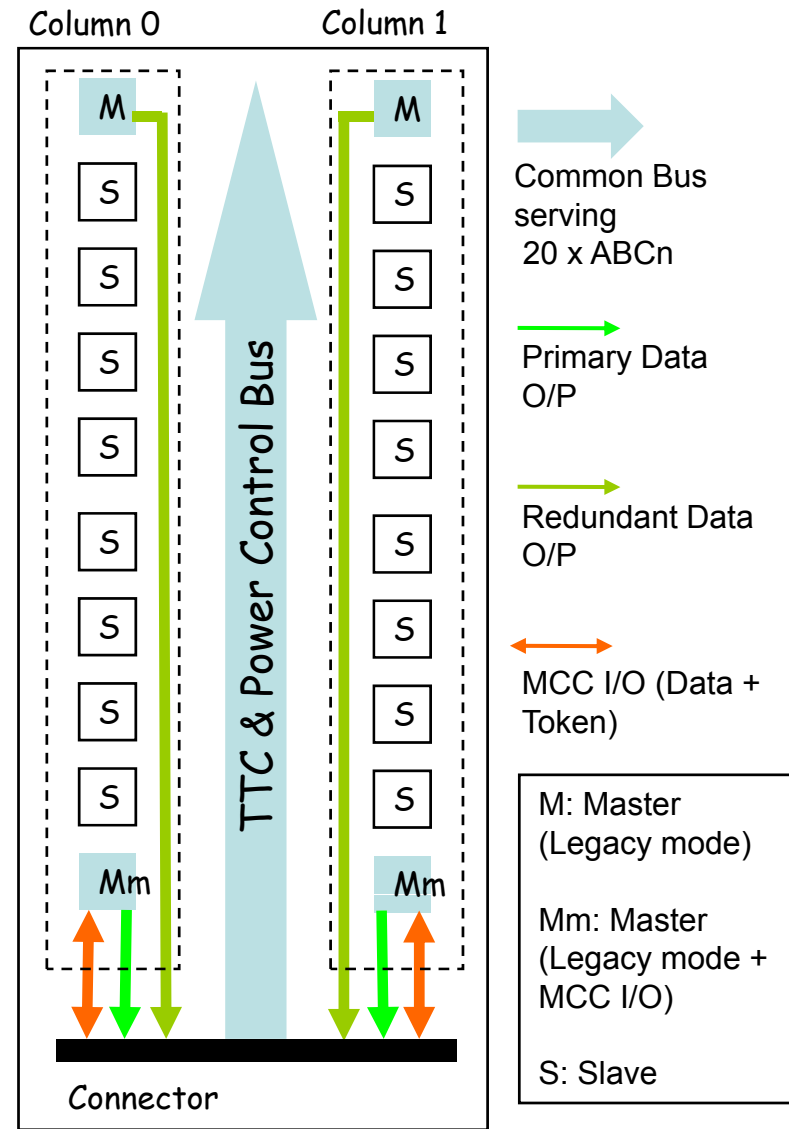
Basic Hybrid Topology

Consists of 2 columns of 10 x ABCn ASICs with a single services connector.

Readout Architecture made up of

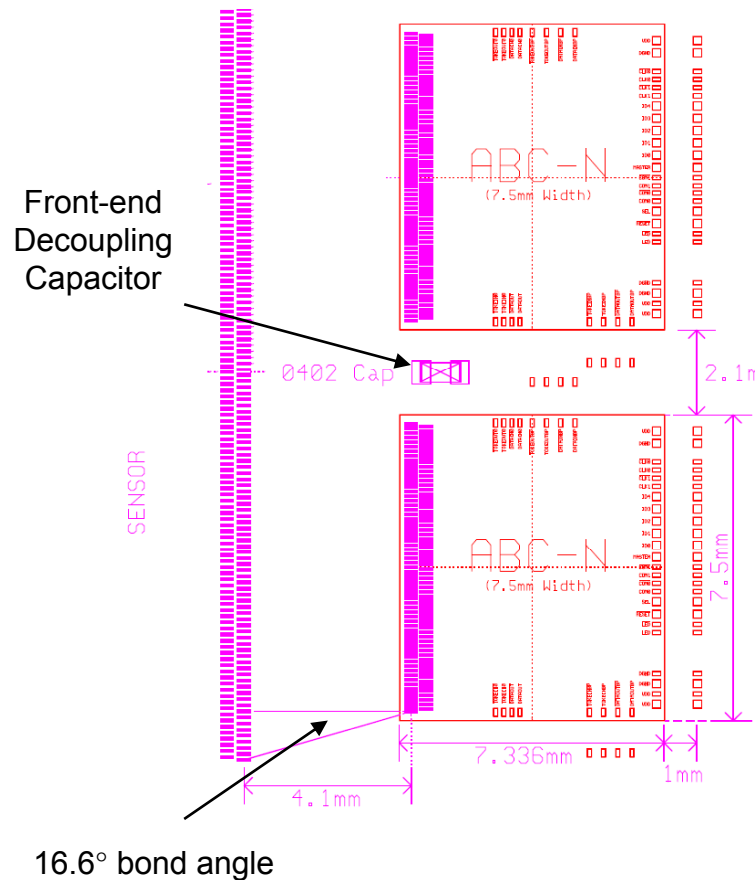
- Single TTC Bus (Clk, Com, L1, DataClk)
- Single Power Control Bus for controlling serial powering circuitry
- Auxiliary Analogue Supply routed to front-end of ABCNs
- Common Digital Supply for ALL ABCNs
- Legacy data paths at top/bottom of each column for use with current DAQ available
 - Allows for testing of bi-directional data paths within columns
- Data & Token I/O for 2 leading ABCNs for use with upgrade DAQ

The connection detail depends on hybrid version



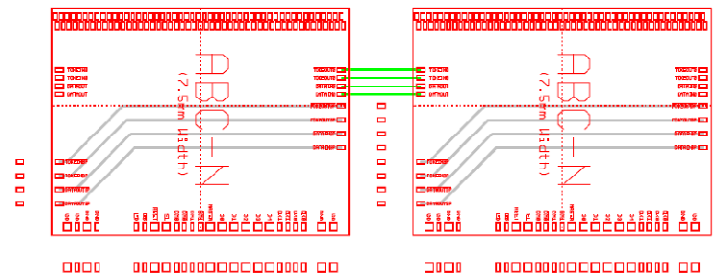
Discussions with Designers

ASIC – Sensor Detail

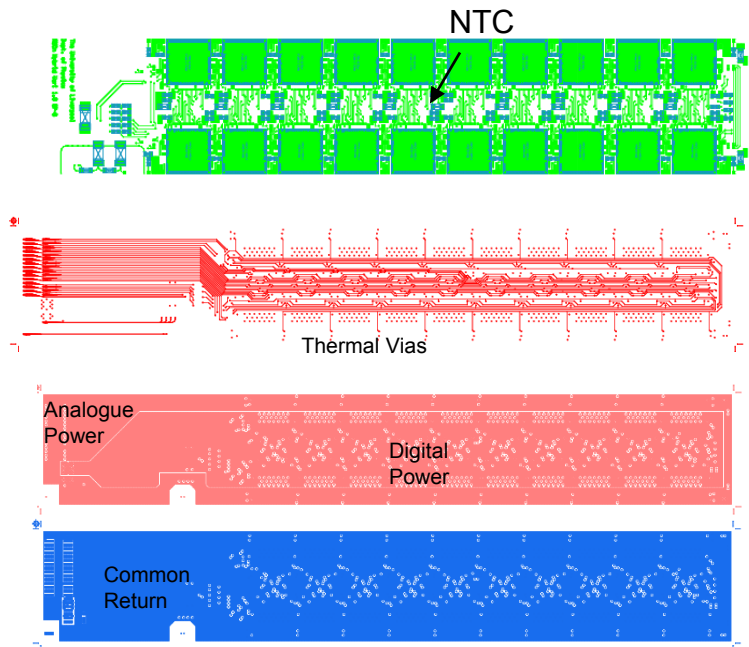


Early dialogue with ASIC and sensor designers lead to modifications to increase manufacturability, reduce mass,....

- Wire bond pad locations and chip size/placement set to allow for direct ASIC/sensor wire bonding
 - No pitch adaptors (less mass/bonds)
- Bond pads on ASICs moved to enable ASIC-to-ASIC bonds for communication without added complications to hybrid layout



1st Flex Build Layup



4 layer-build designed to qualify components (ASICs/sensors) and to prove signal quality as fast as possible

- Layers 1 & 2: Signal
- Layer 3: Power
- Layer 4: Ground

- Built with Stevenage Electronics, LTD UK
- 100 μm track/gap
- 375 μm via lands
- 150 μm laser drilled via holes
- 50 μm dielectrics

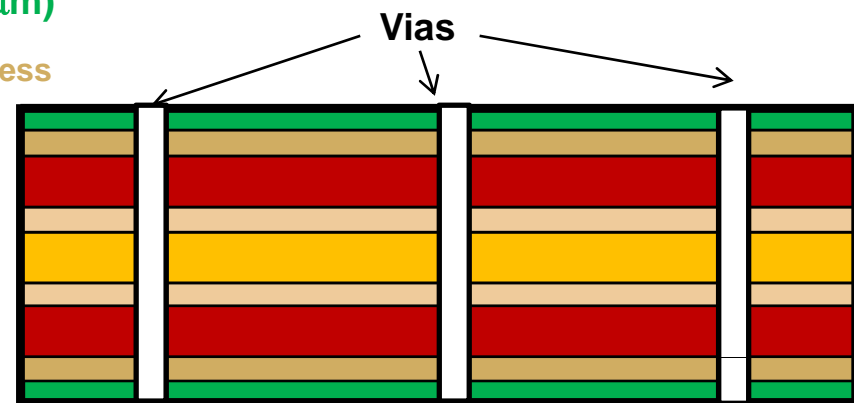
Solder Resist (25 μm)

5 μm Cu foil + electroless Ni/Au plating(3-5 μm)

Bond Ply (50 μm)

Copper (18 μm)

Polyimide-Espanex (50 μm)

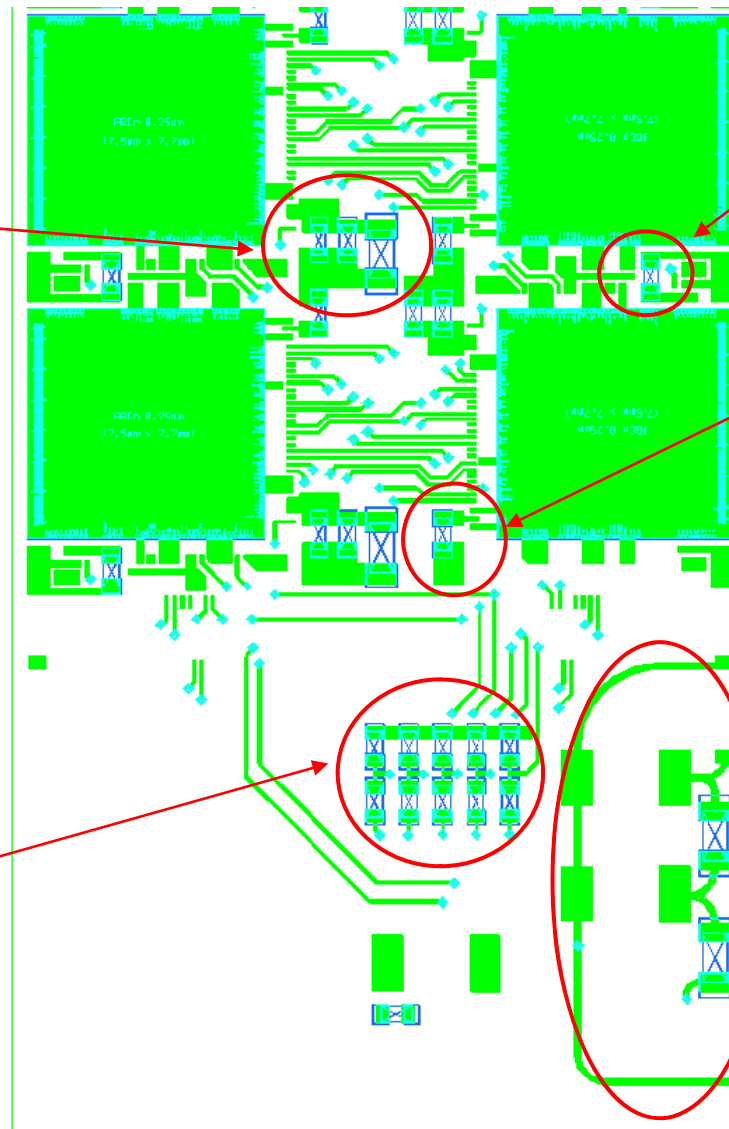


Hybrid Realisation, a bit of detail...

ABCn Digital decoupling:

- 1nF placed closest to ASIC followed by 100nF in parallel
- 2.2 μ F Capacitor per bank of 2 x ABCNs

RC filter bank for ALL single-ended signals

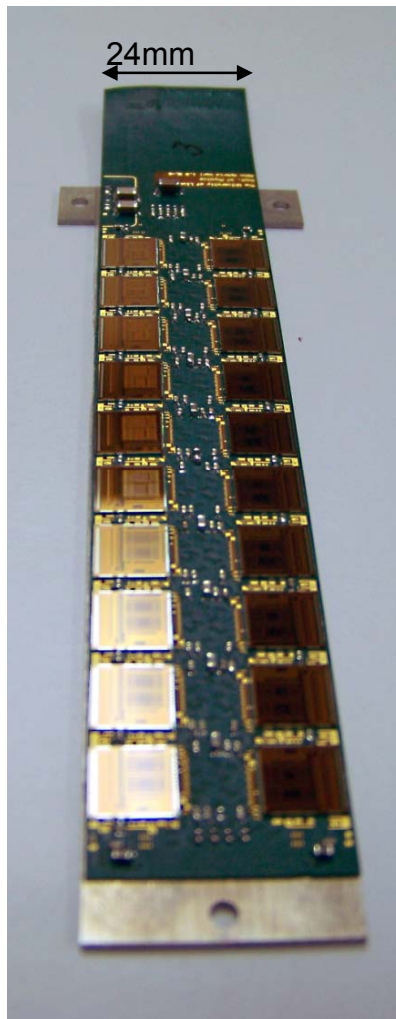


220 nF Front-end Decoupling Capacitor

Additional 100nF digital decoupling capacitor (1 per ABCn)

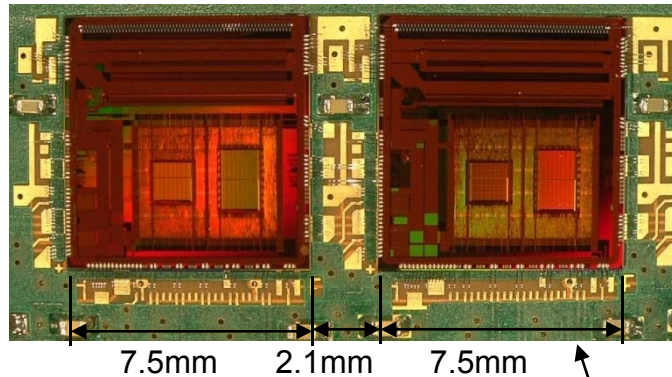
HV filter circuit with Guard ring (to protect against HV tracking to adjacent exposed signal paths)

UK Hybrid: Delivered 24/10/08

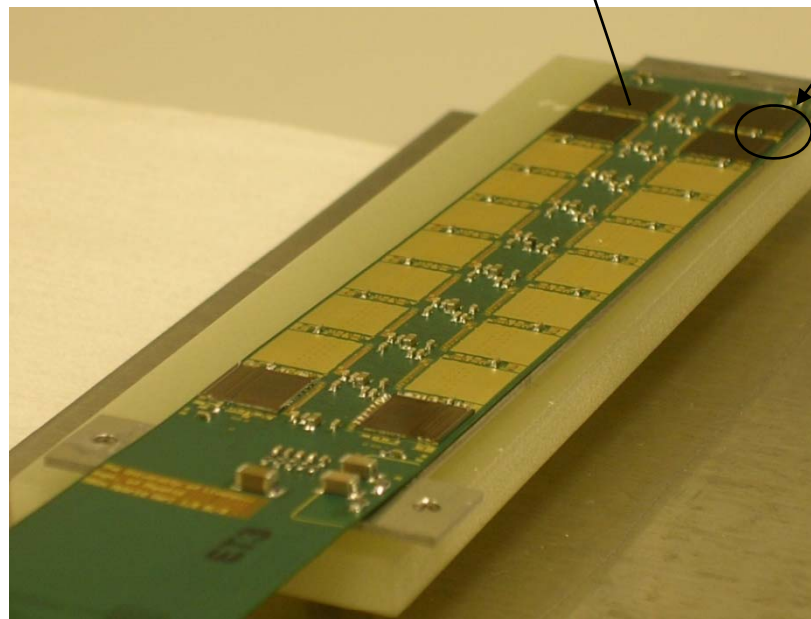
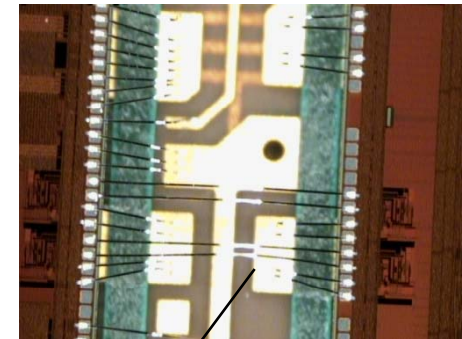


Fully populated hybrid

Neighbouring ABCNs wire bonded



Inter-chip bonding



Hybrid Stuffed with Passives and 6 x ABCNs

Weight $\leq 2g$
(unpopulated)

Production Results

- First batch (15 off) of flex circuits received in the last week of Oct'08.
- 2 panels of 18 circuits made (36 total) at Stevenage circuits (UK).
 - 10 day delivery
 - Yield of 89% achieved.
 - Should increase to $\leq 98\%$ during a production run (achieved by process tuning).
 - Yield enhancement part of original design stage
 - High yield translates into a more reliable object.
- Currently have 4 fully populated hybrids, 20 x ABCNs, being exercised successfully.
 - Hybrids have been wire-bonded at 2 sites with no problems.
 - Have been primarily used for DAQ development & ASIC evaluation.
- Have yet to find any (major) hybrid layout or related problems.
- Very reasonable costs
- Minimum £1500 per submission
- <£25 per circuit for large quantities



Stevenage Circuits Ltd and Tru-Ion Printed Circuits Ltd are the leading manufacturers of printed circuit boards (PCBs) used worldwide in medical, aerospace and defence applications, industrial instrumentation, and high end telecoms.

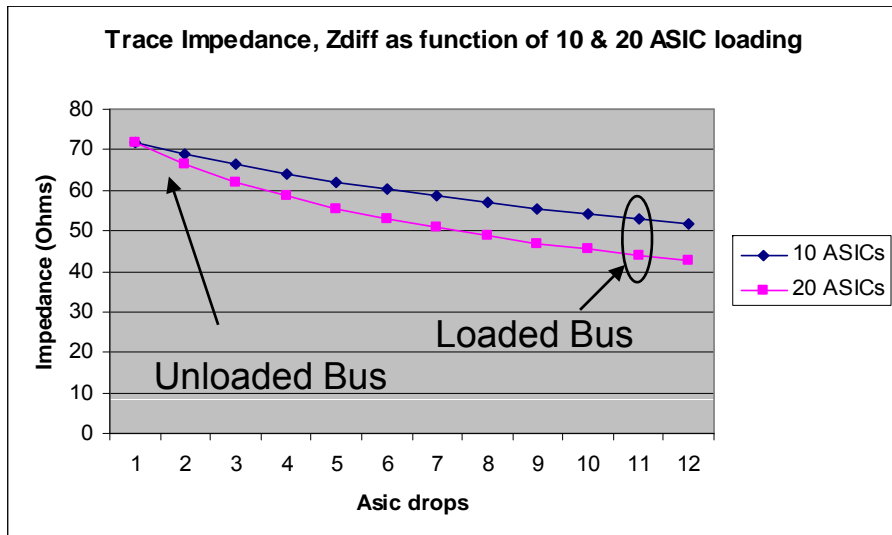
From prototype to production volume, Stevenage Circuits Group engineers work to develop and supply high-layer count multilayer, flex-rigid and flexible PCB's including HDI with blind and buried microvias, RF and metal backed PCB's.

- Privately owned
- Established 1971
- Tru-Lon Printed Circuits (Royston) acquired 1999
- Group turnover circa GBP 11 million (€16 million)
- 140 staff within 100,000 sq. Ft (10,000 sq. M) facilities

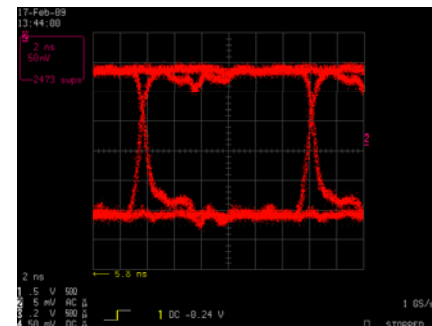
NO:	PRODUCT NAME	CIRCUIT		SERVICE	BATCHES	TOOLING PRICE	Bare Board Tested
		QTY	PRICE (each)				
1	Hybrid Solid Ground iss -	25	£55.30	20 Days	1	£0.00	YES
Construction Type 'Flexi ML04 Standard', Construction Name 'Flexi 04 AP8525R + 5um foil + 50um B/P', Min Track/Gap = 111µ/76µ, 987 Through holes (Min size 0.15mm), Solder Resist Std Green Both sides, BBT, Circuit Size 145.2mm x 24mm, Electroless Ni/Au.							
2	Hybrid Solid Ground iss -	50	£34.10	20 Days	1	£0.00	YES
Construction Type 'Flexi ML04 Standard', Construction Name 'Flexi 04 AP8525R + 5um foil + 50um B/P', Min Track/Gap = 111µ/76µ, 987 Through holes (Min size 0.15mm), Solder Resist Std Green Both sides, BBT, Circuit Size 145.2mm x 24mm, Electroless Ni/Au.							
3	Hybrid Solid Ground iss -	100	£26.90	20 Days	1	£0.00	YES
Construction Type 'Flexi ML04 Standard', Construction Name 'Flexi 04 AP8525R + 5um foil + 50um B/P', Min Track/Gap = 111µ/76µ, 987 Through holes (Min size 0.15mm), Solder Resist Std Green Both sides, BBT, Circuit Size 145.2mm x 24mm, Electroless Ni/Au.							
4	Hybrid Solid Ground iss -	200	£23.47	20 Days	1	£0.00	YES
Construction Type 'Flexi ML04 Standard', Construction Name 'Flexi 04 AP8525R + 5um foil + 50um B/P', Min Track/Gap = 111µ/76µ, 987 Through holes (Min size 0.15mm), Solder Resist Std Green Both sides, BBT, Circuit Size 145.2mm x 24mm, Electroless Ni/Au.							

Trace Impedance and Performance

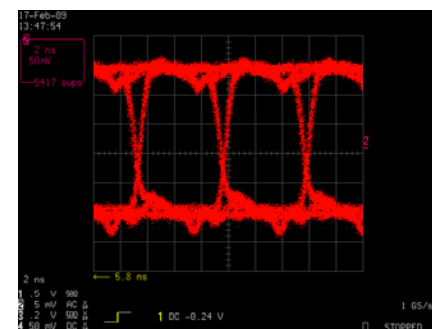
- Trace impedance set by width, thickness of dielectric and dielectric constant.
- Hybrid topology makes use of embedded edge-strip geometry for LVDS transmission.
- For proposed build using 100 μ m track and gap with 50 μ m dielectrics, $Z_{DIFF} \sim 71\Omega$.
 - But this does not take into account ASIC receiver loading (see plot below).
- 20 ASICs on bus reduces impedance to <50 Ω .



Eye Diagrams for 20 ASIC loading

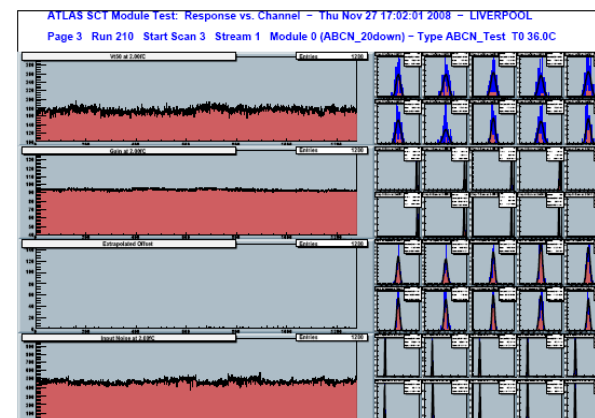
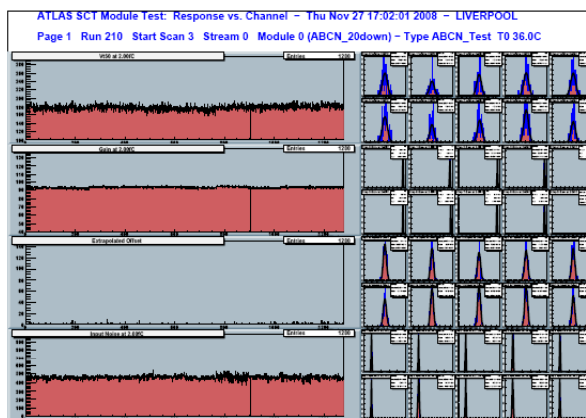
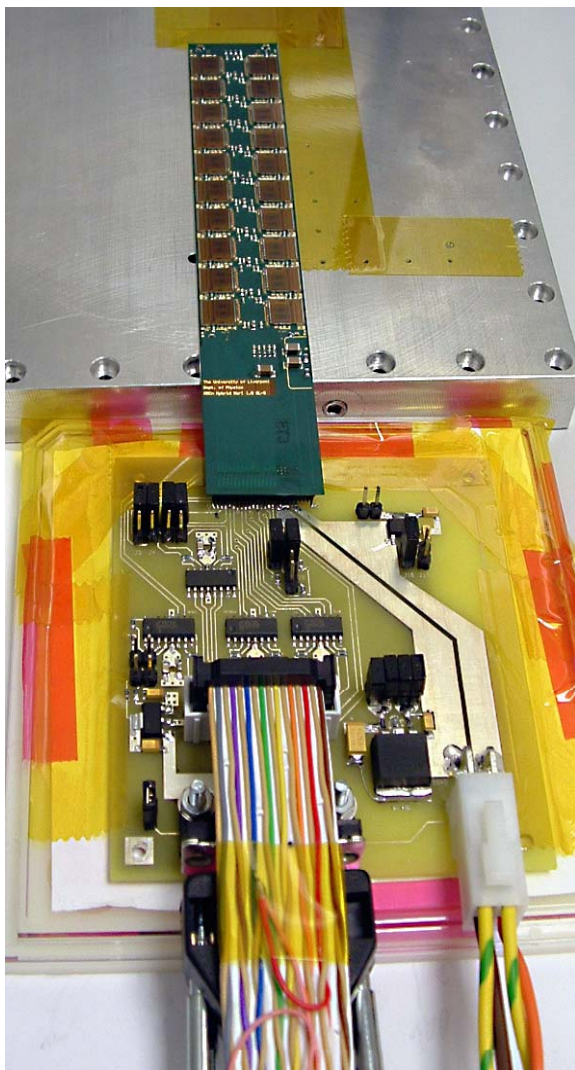


80Mbit/s PRBS
51 Ω end termination
(2ns/Div, 50mV/div)



160Mbit/s PRBS
51 Ω end termination
(2ns/Div, 50mV/div)

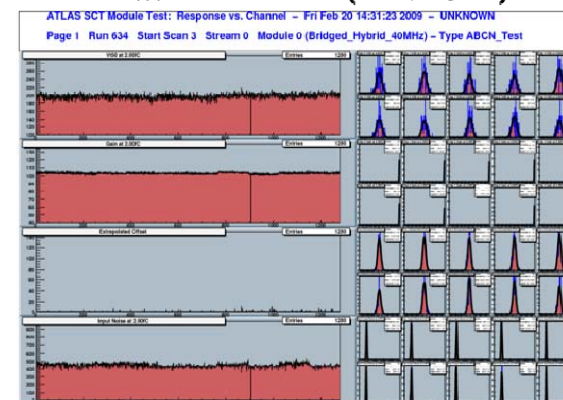
Electrical Performance



SCT DAQ Read-out adapted for ABCnext by Cambridge, RAL, Liverpool

Gain: 100mV/fC
 Input Noise: ≤ 400 enc
 Threshold variation before trimming: 5.5 mV
 after trimming: 1 mV

80MHz data rate (10 × ABCn)

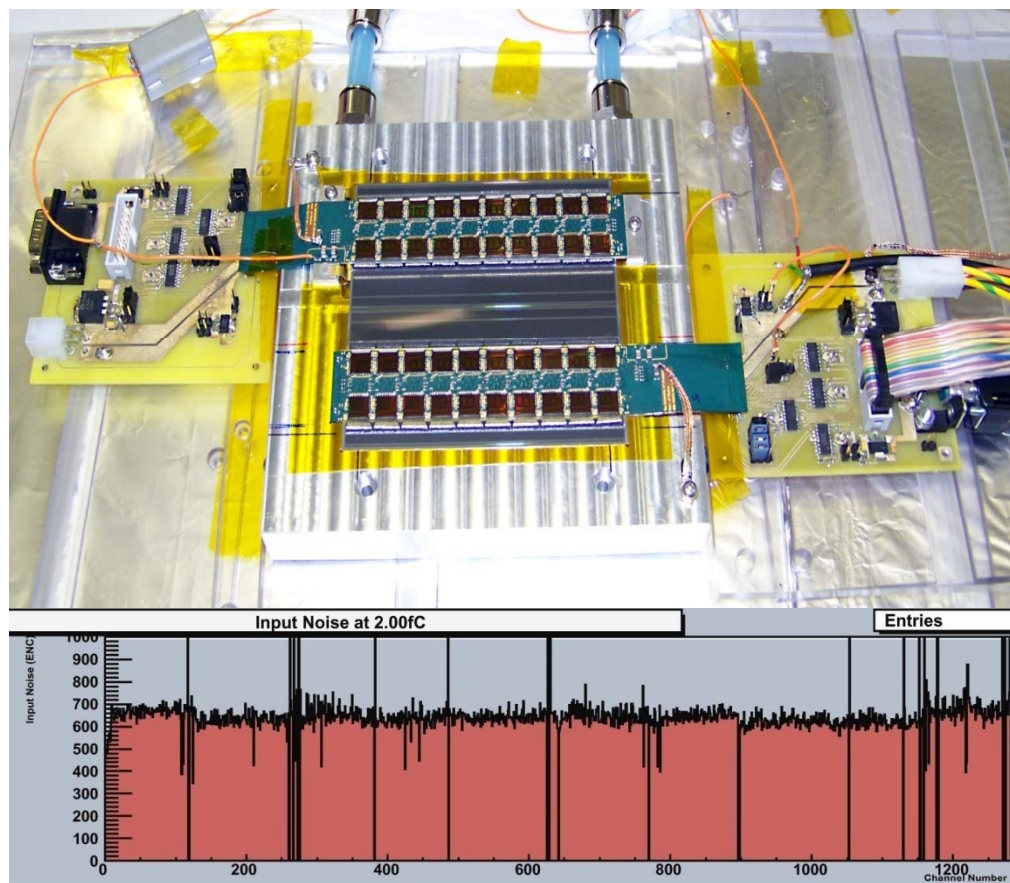


ASICs and hybrids working extremely well with remarkably high yield

- Gain and Input noise show very little change.
- Data/token passing works at 80MHz.
- Tested using Front-end regulator enabled.

First SLHC Short-strip Module Demonstrator

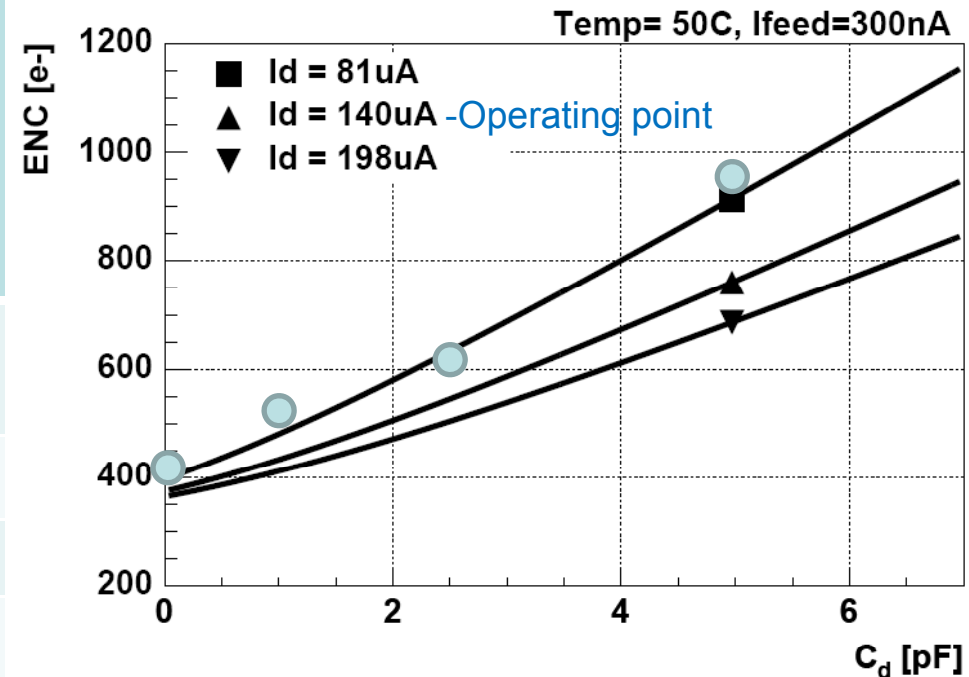
- Aluminium plate with machined bridge legs and cooling pipe (10 °C glycol + water)
- Sensor glued directly to fixture
 - 2 layers of 75 μm thick kapton between AL and sensor
 - HV connection through tab silver-epoxied to backplane
- AL plate referenced to ground of hybrid
- First hybrid bridged with 1 mm thick AL
- Second hybrid directly glued to sensor



- Noise as expected ($\sim 650 e^-$)
 - More open/shorts due to AL bridge
 - More shorts at chip edges due to bonding angle

Preliminary Noise Slope Results

	With separate analogue/digital power	With analogue regulator
Bare Hybrid	450 e ⁻	450 e ⁻
1 pF		525 e ⁻
2.5 pF	605 e ⁻	575 e ⁻
5 pF	986 e ⁻	952 e ⁻
7.5 pF	1364 e ⁻	1313 e ⁻

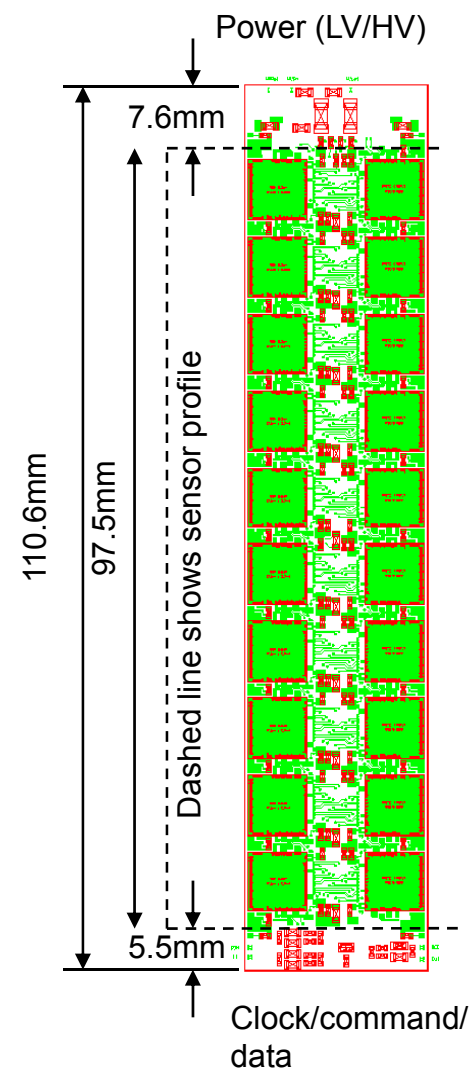


Noise prediction from Jan Kaplon with no detector leakage

We see slightly higher noise than expected from simulation. Direct charge injection measurements and noise slope measurements with discrete capacitors are in process to confirm measurement expectations.

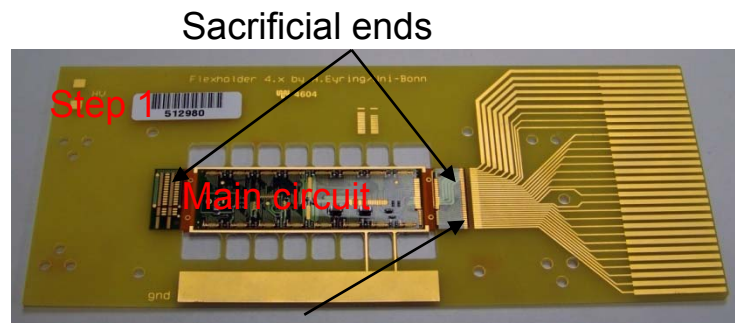
Stave Hybrid: Considerations

- New flex circuit will be glued directly to sensor without substrate.
 - Minimizes unnecessary mass
 - Majority of current design will remain the same, e.g. ASIC location, TTC bus routing etc.
 - Use of ASIC-to-sensor bonding fixes most of the geometry of hybrid.
 - Ends change to match to stave
 - Design will be optimized to stuff passives/ASICs and wire-bond industrially
 - Need high yield/reliability/throughput
 - Prototype of full-scale production module production (~10000 modules in 2 years)
 - Start learning how to assemble modules quickly and precisely
 - Necessary to include shield layer to prevent pickup to sensor
 - Flexibility needed for reference point
 - Solid, non-perforated backplane for gluing
 - Concern about the proximity of the hybrid ground to sensor HV (towards the sensor edges)
 - Propose 2 passes of solder resist on the back of the flex (results in ~50 μ m resist)
- Slightly more aggressive with ground/power
 - 4 layer build
 - Top layer
 - Signal/power
 - Ground
 - Shield



Current Substrate-less Hybrids

- Initiated a program at beginning of year to investigate working with rigidless hybrids
 - Try to learn as much as possible from Pixel community
 - Kindly sent jigs to show steps involved in their module construction, see below

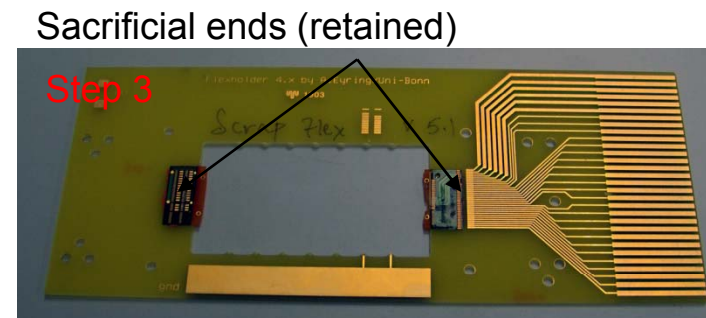


Bond Pads for connection to 'outside' world

- Flex circuit composed of 2 components
 1. Main active circuit (non-glued)
 2. Sacrificial ends which are glued to FR4
- Circuit sits flat on a rigid FR4 base
 - Drilled for vacuuming down



FR4 base removed to allow mounting of circuit onto sensor + wire-bonding

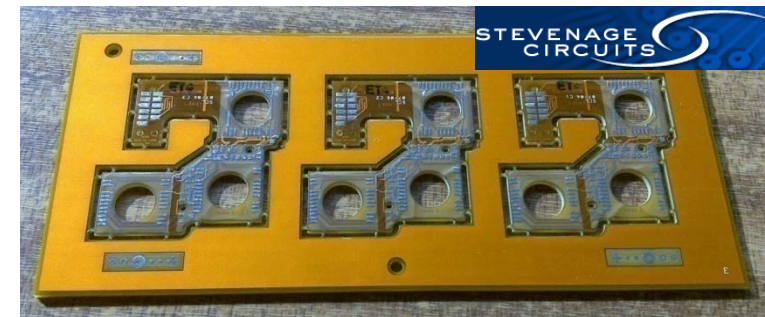
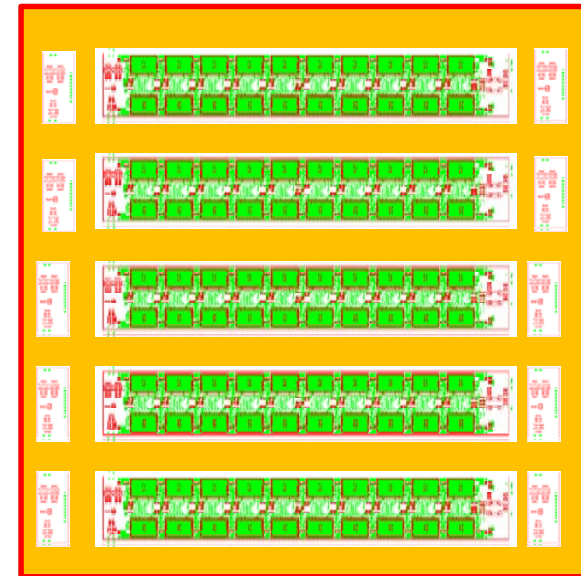


Final step, circuit + sensor removed

Try to industrial process and modify for strip needs (~2000 vs. ~16000 hybrids)


Hybrid Production Plans

- In discussions with industrial partners
 - Stevenage Circuits, LTD UK (flex circuits)
 - Hawk Electronics, LTD UK (population)
- Produce 4-8 hybrid circuits in A4-size panel
 - “Waste” area patterned to allow hybrid testing in panel
- Panel is then laminated onto 1.6 mm thick FR4 carrier with holes in bond-ply where active circuits are located
 - Two edges routed (laser/mechanical) to allow for “easy” removal on circuit
 - Location holes added to module production
- Panels is then sent to industry to be populated by re-flow technique
- Hybrids are wire bonded and tested in panel
- Vacuum pickup tool located by holes in panel, attaches to ASIC site.
 - Once held, remaining material holding hybrid in place cut out
- Hybrid now free to be glued to sensor



Flex circuit held in FR4 panel
(circuits not laminated to FR4)

Conclusions

- For the SLHC upgrade, it is important to plan for manufacturability and reliability from the beginning
- Open communication during design phase between ASIC, hybrid, and sensor designers is a must!!
- Contact industrial partners early as well
- So far hybrid operation and testing has shown no problems.
 - Performance is as expected (for bare die).
 - It works! 
- Very soon hope to converge to a hybrid design for integration on a stave.
 - Involve minimal changes to routing of the present hybrid.
 - Modifications are being made to enable population and wire bonding in industry
 - Could be ready for a submission in the very near future...