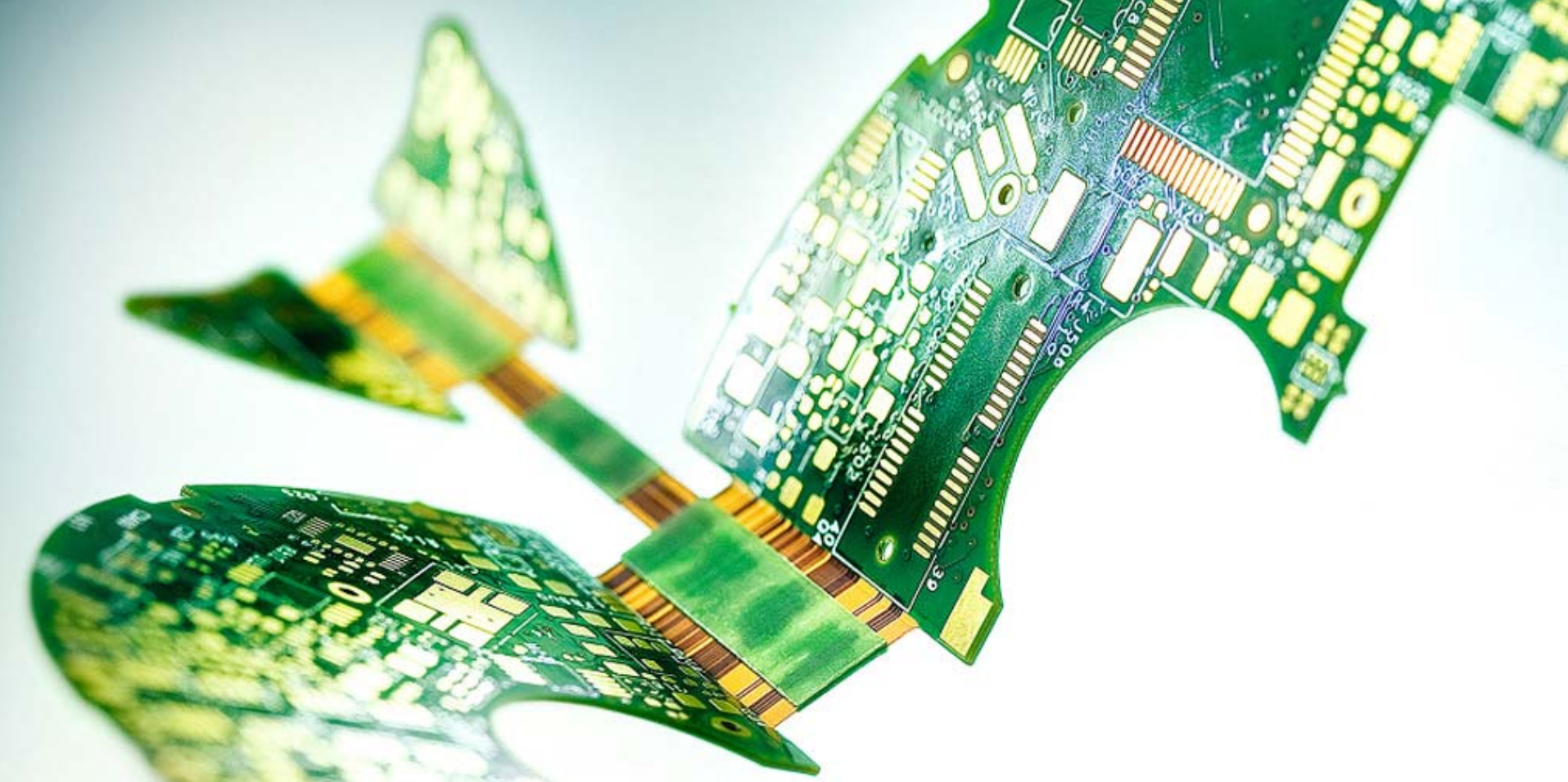

Current capabilities and future developments for flex hybrids

SWISS PCB

Author

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- PCB Manufacturing

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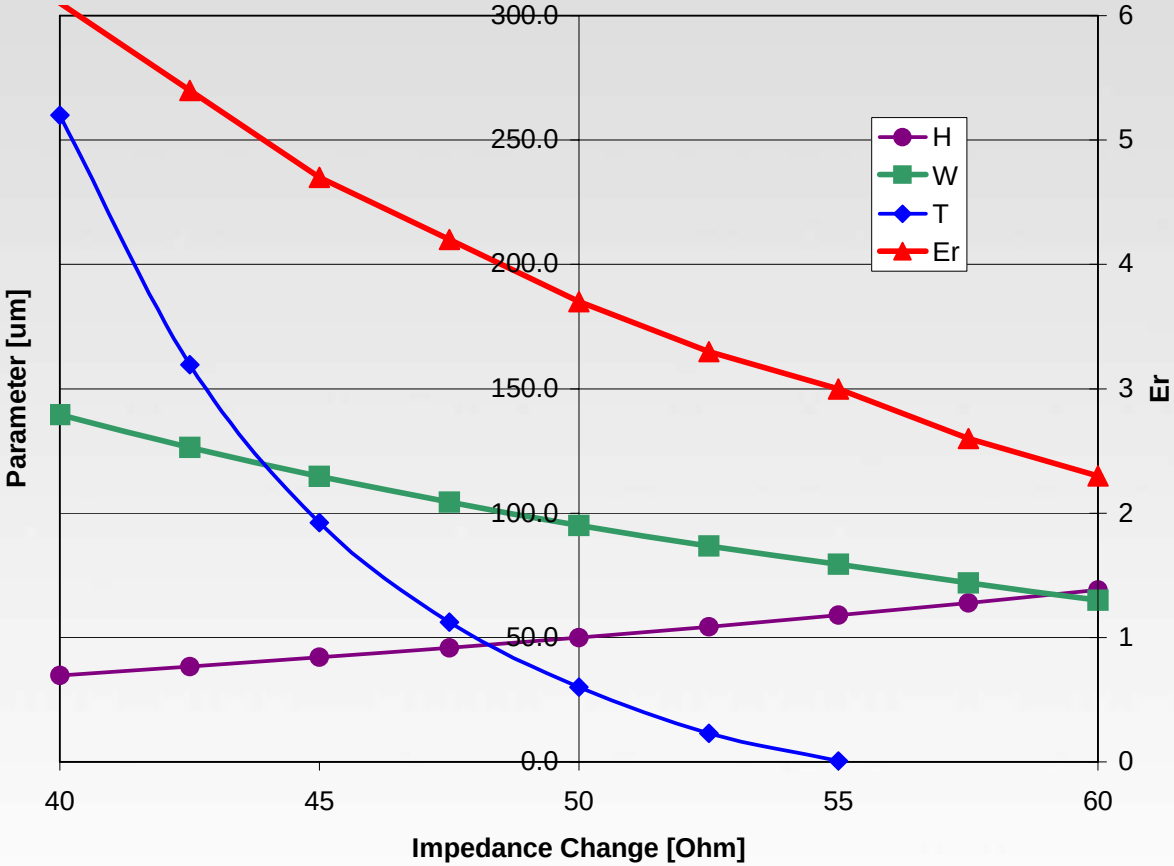
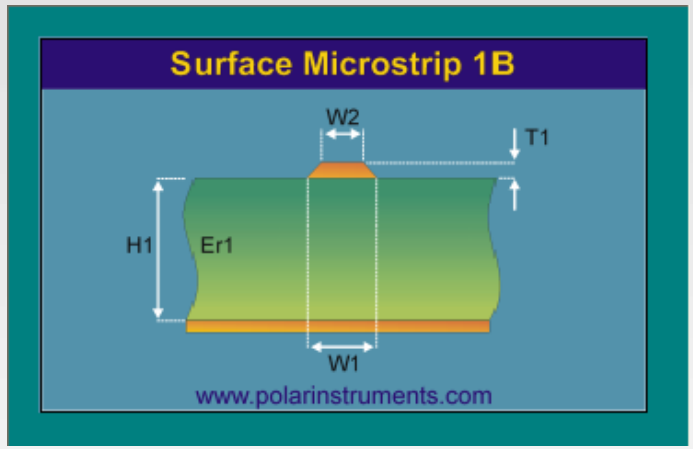
Table of Contents

Clock Speed and RF Frequency

- Ensure geometrical reproducibility of art work
- Extract S-Parameters for better models and to account for parasitics
- Find flex materials with good radio frequency properties
- Material must posses good properties with respect to PCB manufacturing

Micro Strip Line





Influence of geometrical variation on impedance

S-Parameter extraction required

- Supplier value for ε_r in FR4 is around 4.2-4.5
  → fitted values are closer to 3.7 ???

- Polar is de facto industry standard SW & measurement

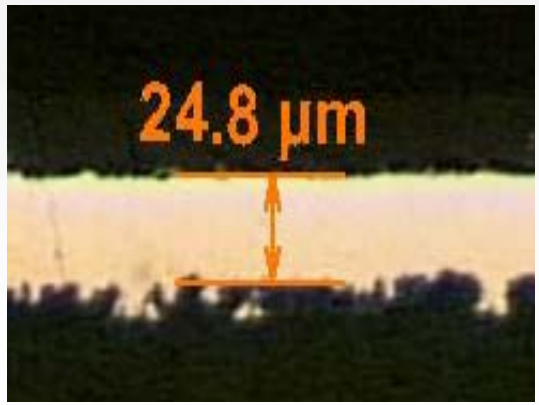
→ Polar calculates around 1 MHz

→ Polar measurements done in time domain

- S-Parameter extraction required for better models

→ Broader frequency range and parasitics

→ Skin effect & radiation due to treatment taken into account



Better flex materials required, i.e., LCP

- Better mechanical stability
- Low moisture absorption (stability, vacuum)
- Better RF characteristics

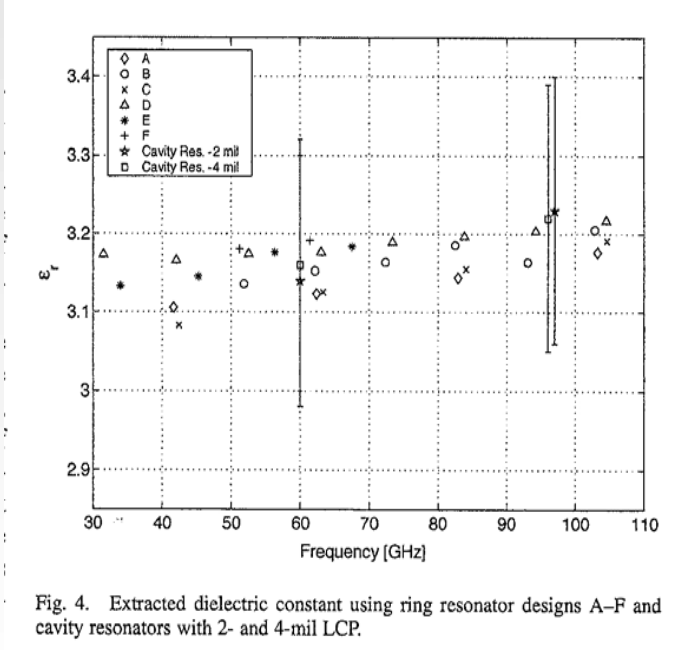


Fig. 4. Extracted dielectric constant using ring resonator designs A–F and cavity resonators with 2- and 4-mil LCP.

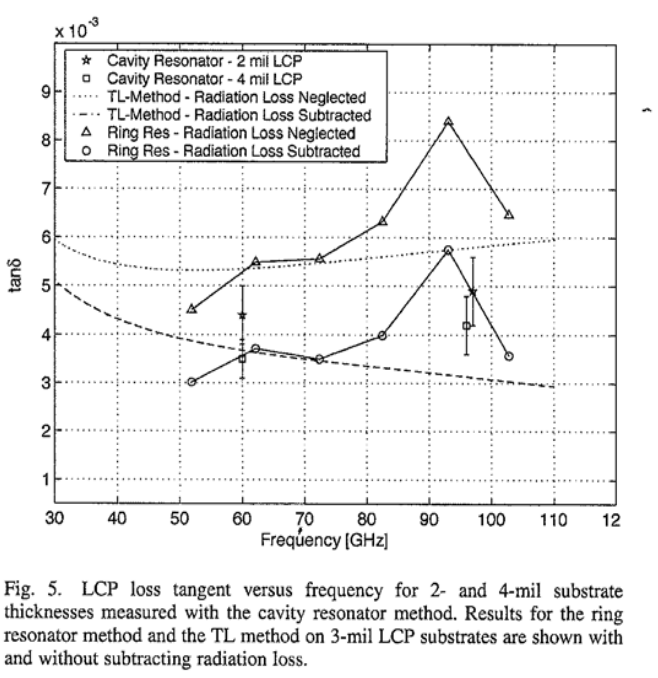
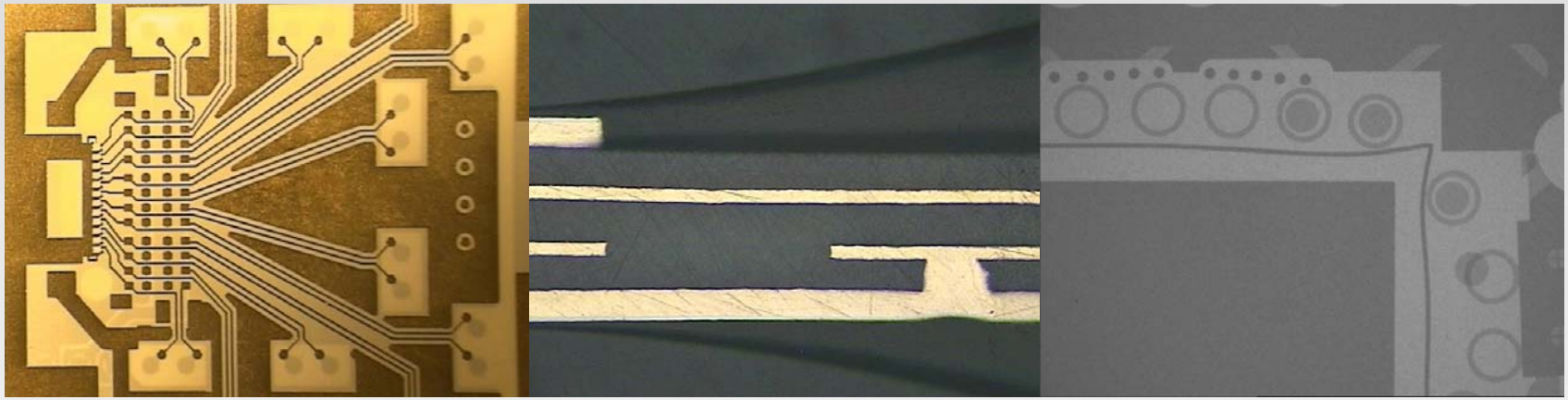


Fig. 5. LCP loss tangent versus frequency for 2- and 4-mil substrate thicknesses measured with the cavity resonator method. Results for the ring resonator method and the TL method on 3-mil LCP substrates are shown with and without subtracting radiation loss.

Tentzeris et al., IEEE Transactions on Microwave Theory and Techniques, Vol. 52, No.4, 2004

Example of LCP Substrates



- LCP currently broadly used as high speed flex layer in hybrid build ups (LCP combined with other materials)
- Full LCP build not readily available because of lamination problems, pattern dependence
- Supply:
  Rogers, Nippon Steel (Espanex), and now Dupont

Density / Miniaturization

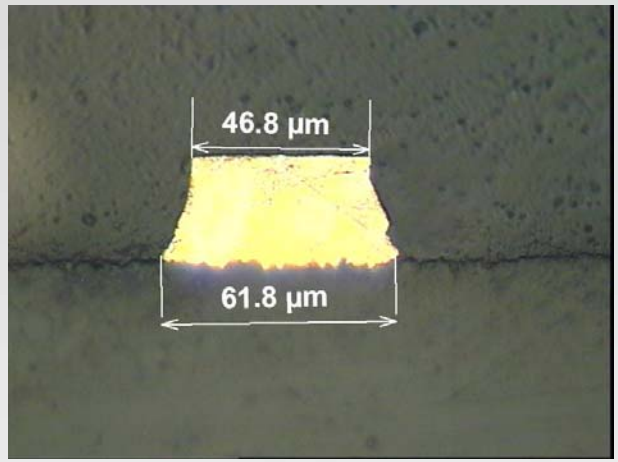
- Main problem is **isotropic** nature of wet chemistry etching
- Subtractive process vs additive process
  (panel plating vs pattern plating)
- Stacked vias are reducing amount of real estate required for interconnects
- Annular rings are required because of drill scatter even with CCD camera positioning
- Defect density (defects per m2) is limiting availability of fine pitch PCBs

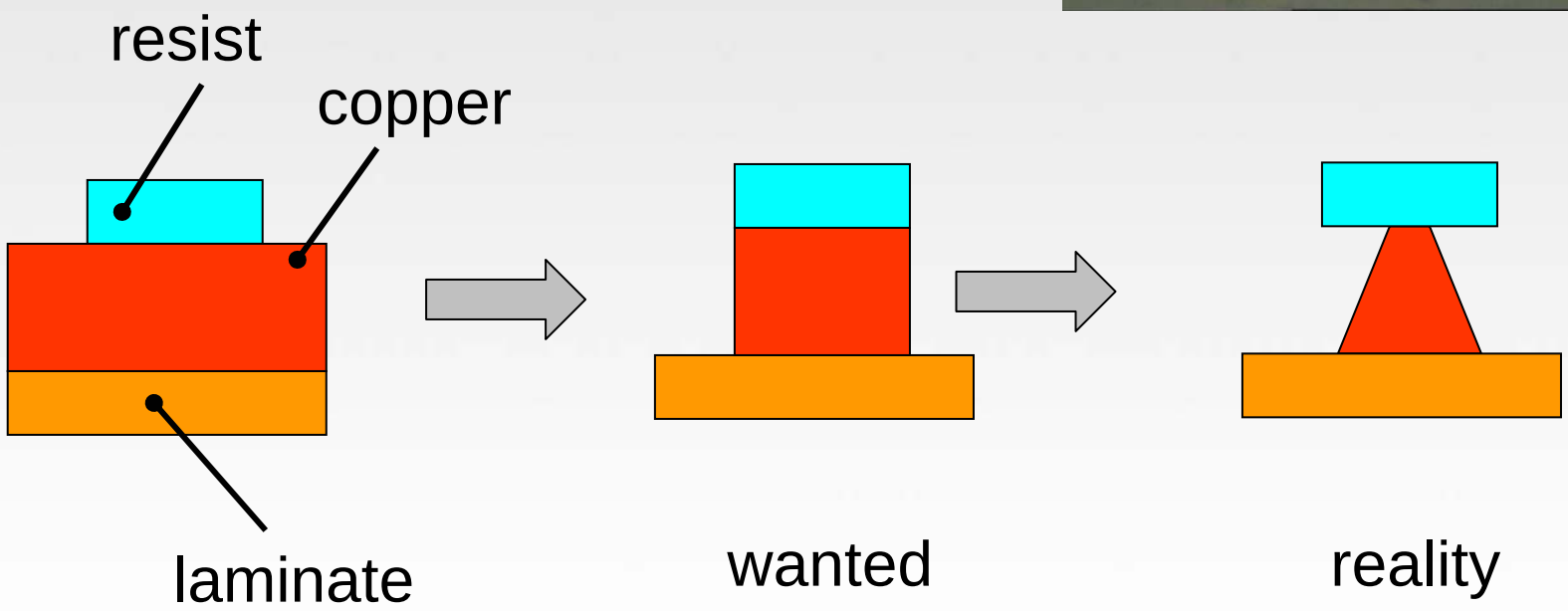
Subtractive Process

- Easy process flow, economical
- Pitch (p) limited to

$$p > 3*T$$

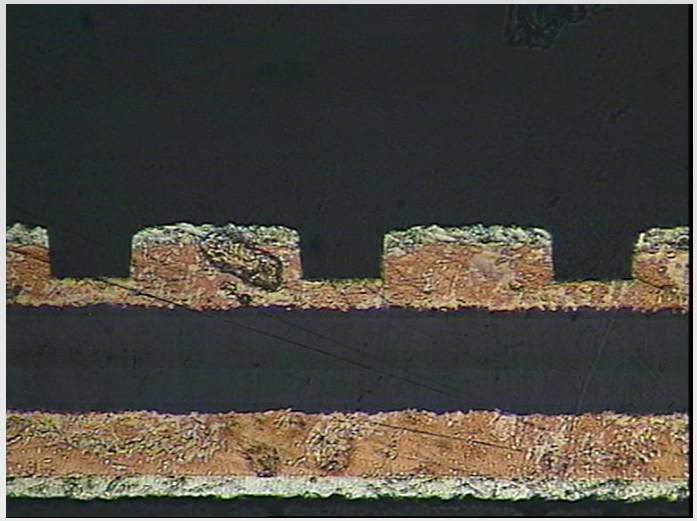
T = Cu + resist thickness

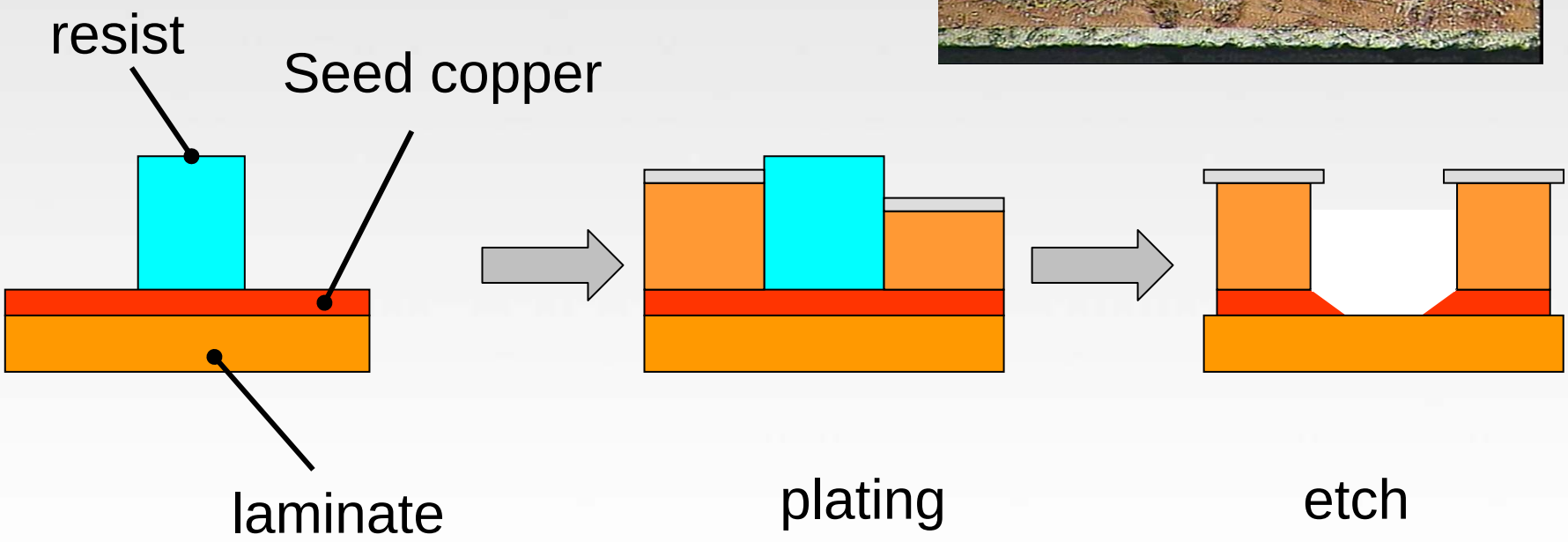




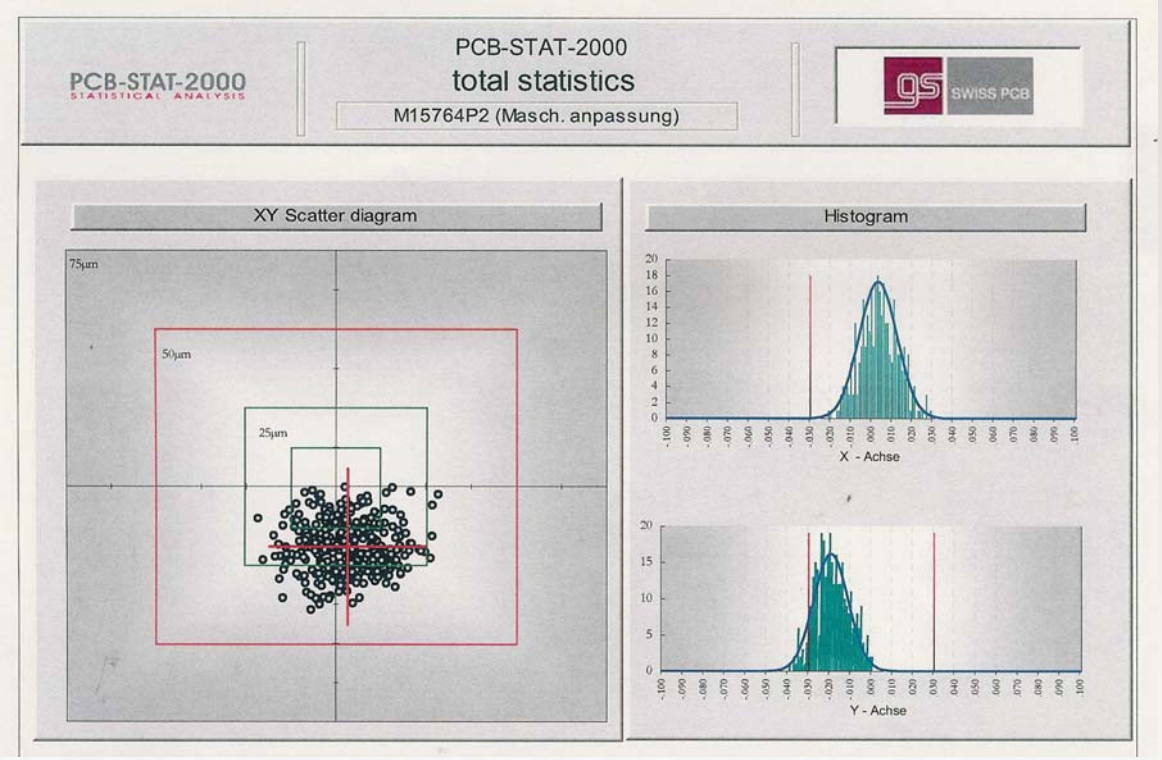
Additive Process

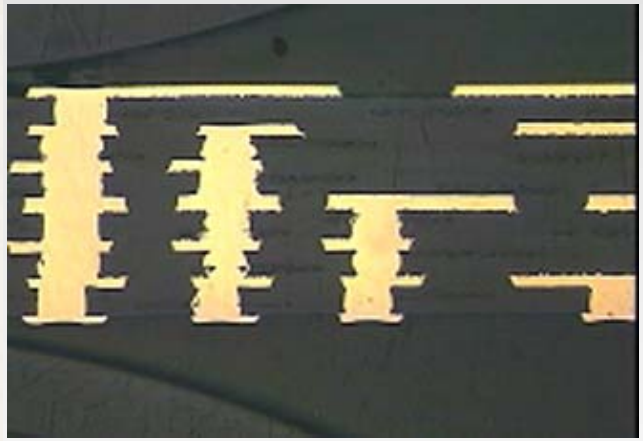
- Advanced process flow
- Pattern dependence





Vias, Annular Ring and Catch Pad





- → Pads must be considerably larger than via diameter
- → Blind via must have aspect ratio > 1:1
- → Stacked via enables real estate saving, no break-outs

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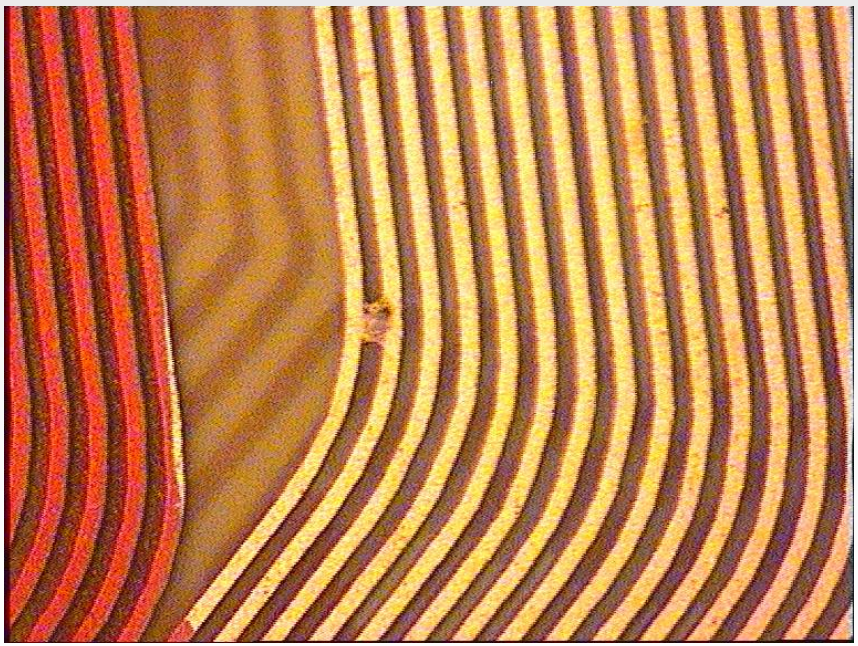
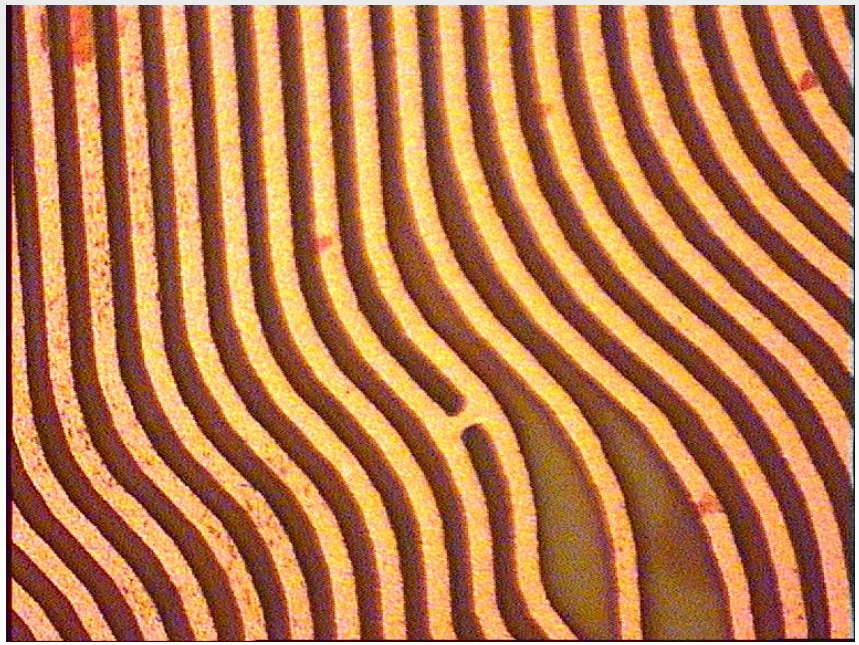
What is limiting fine pitch processes?

- Availability of thin seed layer materials (Hofstetter AG)
- Defect density is not yet well controlled

→ Currently 100μm pitch is available for small PCBs (3x3 cm)



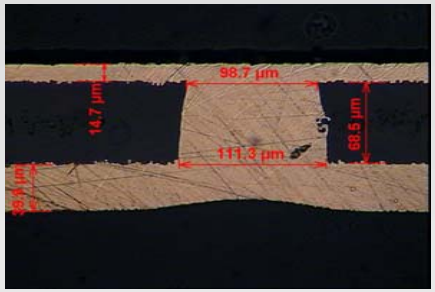


Current Capabilities and Road Map

		Production	R&D
Thickness		25 µm – 4.8 mm	10 µm – 4.8 mm ?
Trace Width		50 µm (2 mil)	25 µm (1 mil)
Space		50 µm (2 mil)	25 µm (1 mil)
Microvia	Laser Mechanical	50 µm (2 mil) 75 µm (3 mil)	25 µm (1 mil) 50 µm (2 mil)
Layers	Multilayer Rigid-flex Flex	up to 16 up to 14 up to 8	up to 24 up to 24
EP Cu Microvia Filling		yes	
AOI & E-test		100%	

SWISS PCB

Reliability & Metrology

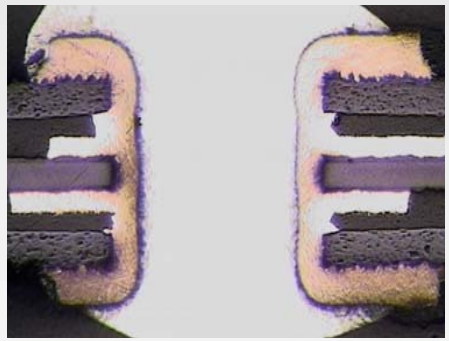


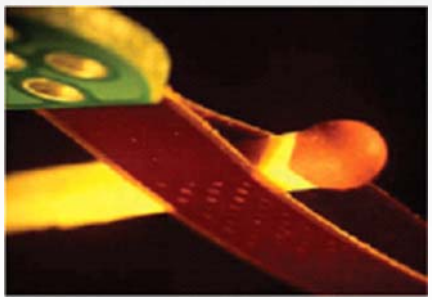
Stacked Vias expected to exhibit higher reliability

- Base line and test in progress
- Already used in implantable devices

Metallization Problems

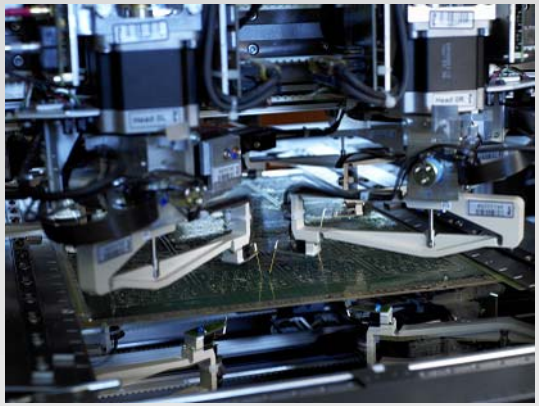
- Plating is well understood
- Choose a reliable vendor





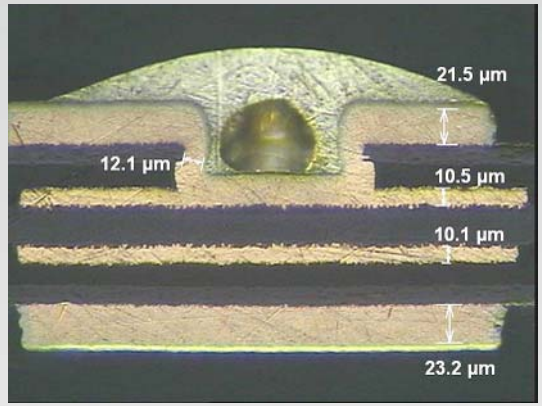
Full Flex and Rigid-flex

- High reliability applications (aerospace)
- Hearing Instrument hybrids as full – flex modules
- Reduce interconnection complexity and connector failures



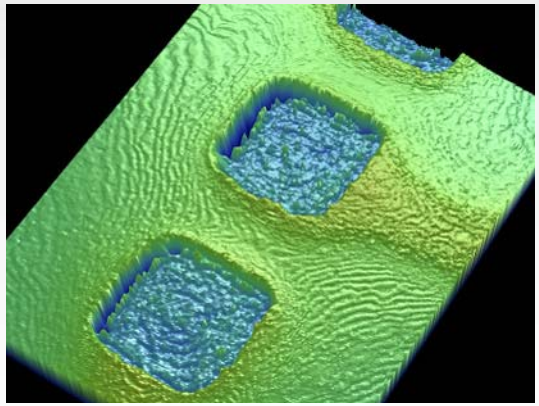
E-Test

Polishing of
Micro Section



Micro Section

Final Inspection



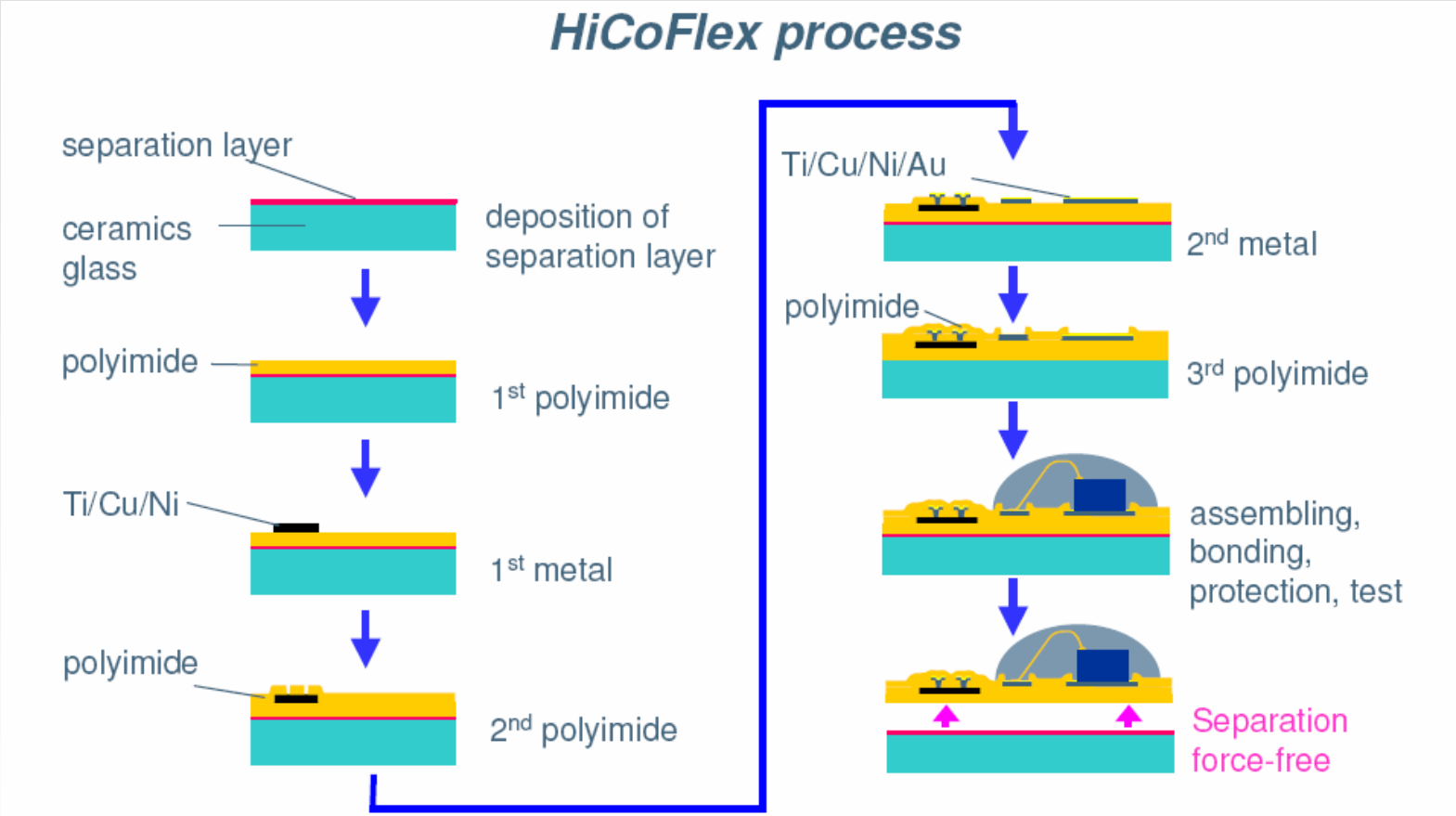
3D Image

FAIR

Some other Developments

- HiCoFlex (SHIFT, Hightec MC)
- Embedded Components (VISA, HERMES,
  embedded chip (Würth, AT&S, Imbera, etc.)
  embedded interposer (Schweizer etc.)
  embedded passives
- Embedded fibre-optics (Varioprint, PPC Cham)
- Inkjet printed PCBs (cheap, but low performance)

HiCoFlex: Thin spin-on polyimide



H. Burkhard, Hightec MC, Lenzburg, 6./7. September 2007

HiCoFlex

- Spin-on polyimide film guaranties thin layer
- Very fine etching possible due to sputtered seed layers

- One sided assembly only
- Panel size to increase from 6x6 inch to 12x24
- Single Source !

3-layer HDI flex
CMS experiment at the Large Hadron Collider (LHC) at CERN

Assembled barrel modul for
66560 pixels on 67mm x 26mm
(courtesy of PSI, Villigen)

Embedded Die

- Thermo-sonic flip chip embedded in PCB substrate
- Laser cavity enables placement of thinned die

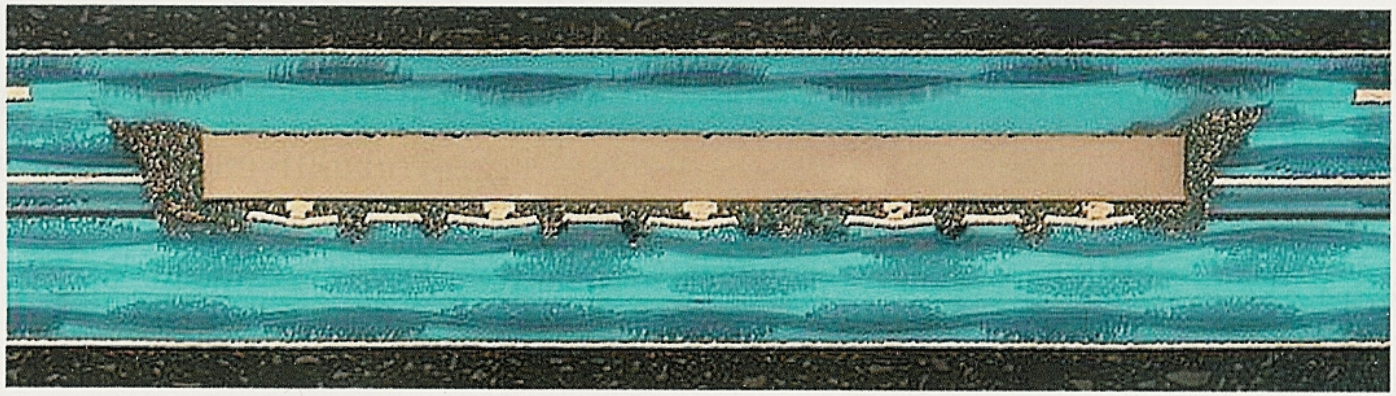
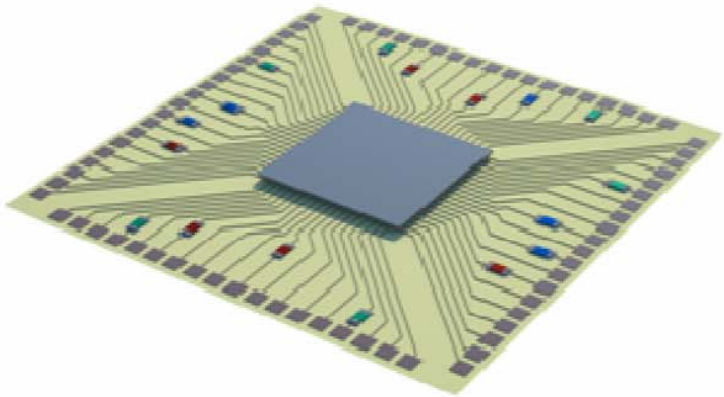


Abb. 8: Querschliff durch einen embedded Flip Chip in einer Lasercavity in einem Multilayer. Die Außenlagen stehen zur konventionellen Bestückung zur Verfügung

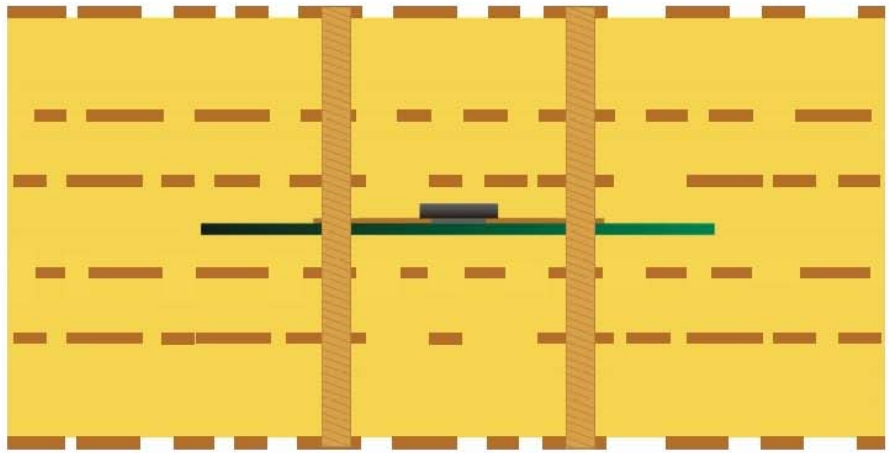
R. Schönholz, Würth Schopfheim, Plus 2/2009, Leuze Verlag

Embedded Interposer

- Lamination of interposer board into Multilayer
- Testability, Known Good Interposer



Interposerelement mit bestücktem Chip und diskreten, passiven Bauelementen.

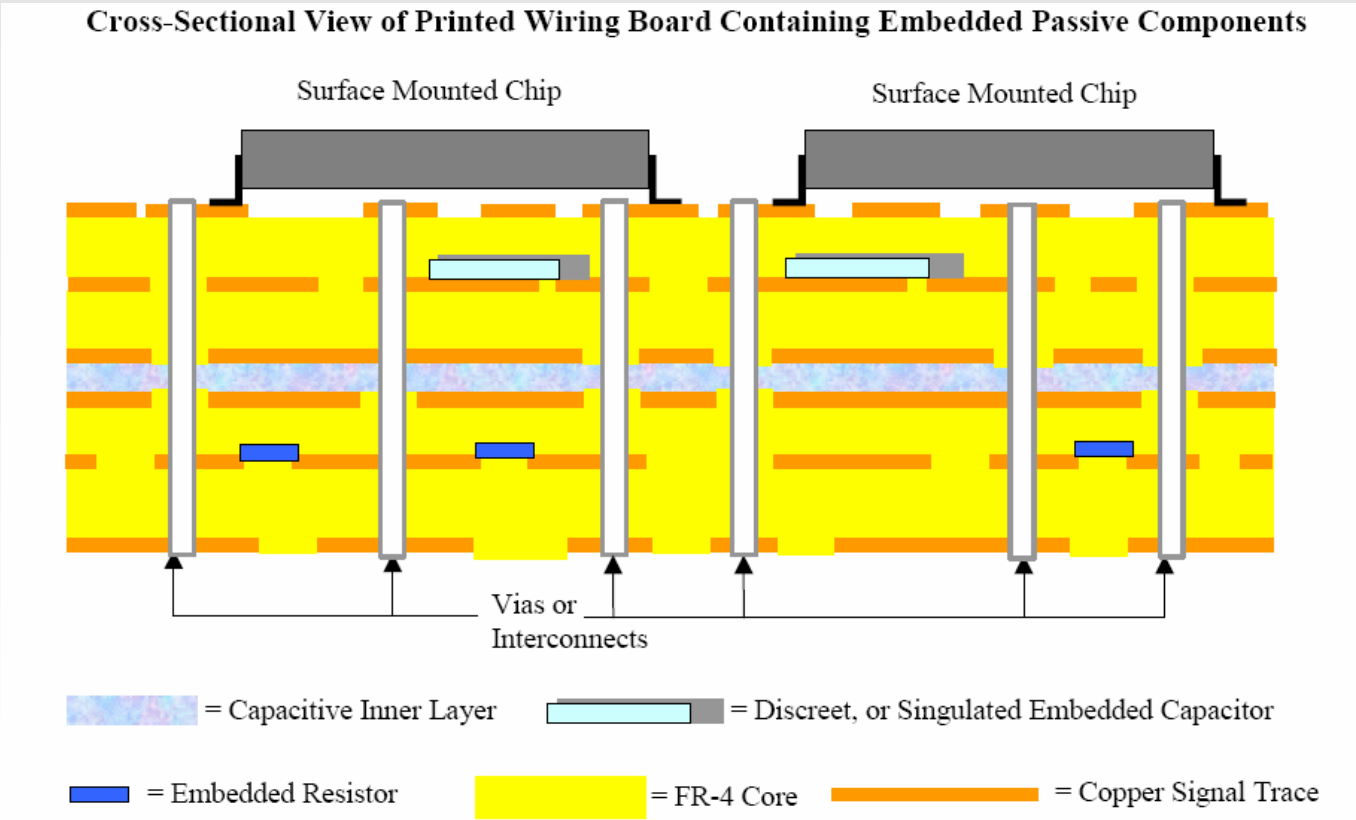


Multilayeraufbau, 6 Lagen, als Schweizer iBoard (eine von vielen Möglichkeiten)

T. Gottwald et al., Schweizer Electronic AG, Plus 2/2009, Leuze Verlag

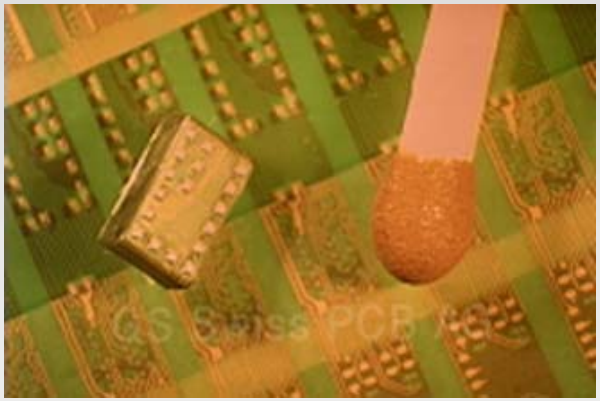
Embedded Passives

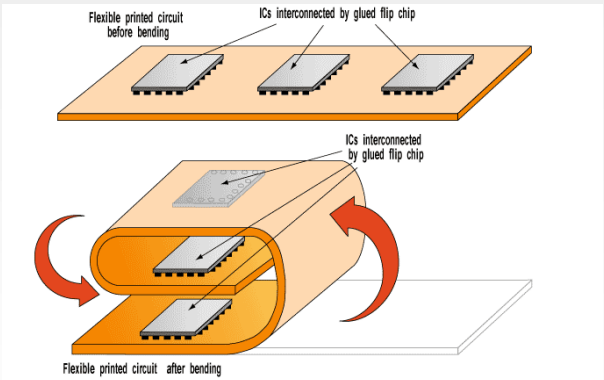
- Resistive and capacitive layers within multilayer
- Embedded ceramic components



W.J. Borland et al., Dupont iTechnologies

Folded-in instead of embedded !





2. Miniature electronic components supplied by Valtronic enabled the design of a suitably sized SiP probe tip for an implanted pacemaker.

GS Swiss PCB / Phonak

- Two layer flex PCB for flip chip (COF)
- SiP for medical application
- Polyimide thickness: 25 µm

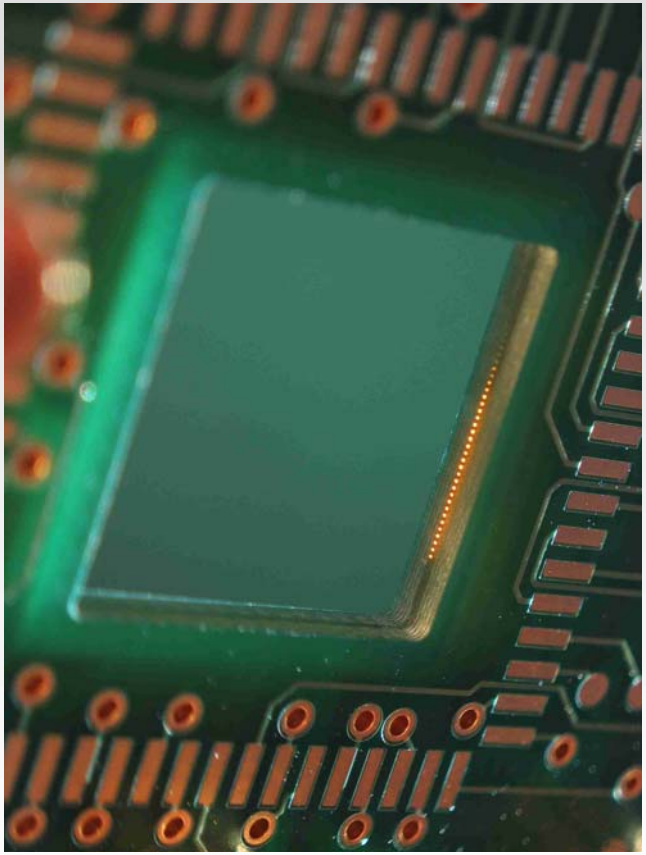
→Better testability of MCM

→Better form factor as dielectric is thinner than standard pre-pregs

→Easier supply chain integration

→PCB yield does not push up electronics cost

Embedded Optical Waveguides



Varioprint / IntexyS Photonics

- Embedded polymer wave guide
- High End Server backplane solution

http://www.zurich.ibm.com/news/06/photonics_d.html

Summary

- PCB technology is faced with the challenge of reducing the widening gap of silicon pitch and board pitch
- Ever higher clock rates require precise artwork etching, often beyond current IPC Class 3 requirements
- Reduction of foot print will evolve gradually, no revolutionary technology in sight
- Material technology to evolve to include better RF properties, thinner dielectrics and thinner copper cladding
- Increase in electrical function density to be expected with the use of embedded components, either active or passive, however, the jury is still out!

Thank you for your attention.
Questions ?

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