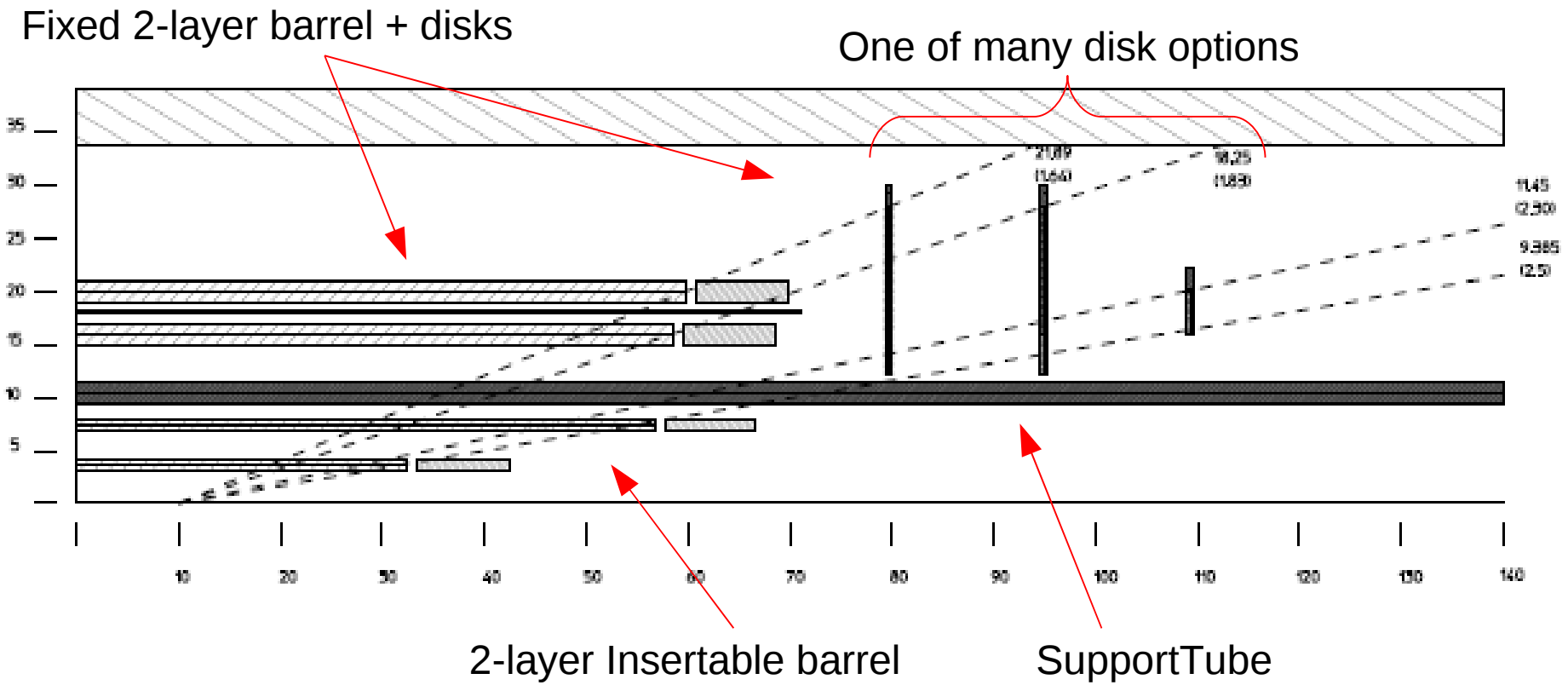
Phase 2 ATLAS pixel system architecture and requirements

Work in progress

- Pixel upgrade system task force started in 2008 to draft specifications and system architecture recommendations (chair A. Grillo)
- Work still in progress
- Will show selected tables from working draft

Detector layout

- System requirements are based on this basic working layout
- The final layout will surely be different



Radiation dose in pixel region

- Done with PHOJET pp event generator and FLUKA particle transport code.
- In pixel region, 3000fb^{-1} prediction fit well by $\left(\frac{270}{r^2}+\frac{14}{r}\right) x\,10^{15}$
- Negligible z-dependence.
- Use smaller safety factor for insertable layers

Layer	Ionizing dose in MRad (included safety factor)	NIEL dose x10 ^{15} (included safety factor)	SEE Flux (for SEU) particles / cm ^{2} /s
0	750 (1.5)*	13.4 (1.0)	1.2 x 10 ^{9} (1.15)
1	275 (1.5)*	4.5 (1.0)	0.5 x 10 ^{9} (1.15)
2	150 (2.5)*	2.5 (2.0)	0.2 x 10 ^{9} (1.15)
3	105 (2.5)*	1.8 (2.0)	0.1 x 10 ^{9} (1.15)
disks	150 (2.5)*	2.5 (2.0)	0.2 x 10 ^{9} (1.15)

(*) ionizing dose based on older estimates => bigger safety factor

Readout chip and pixel size

- In addition to layout, a readout chip format is assumed based on the FE-I4 now under design for Phase 1.
- FE-I4 active area = 1.68 x 2.0 cm^2
- Pixel surface area x recovery time must be compatible with hit rate for total dead time < 1%
- Pixel aspect ratio is a matter of preference
  - FE-I4 values are: 50um x 250um x 400ns
  - Assume these values where occupancy allows

Number of components

Layer	Radius or Z (cm)	N. of staves or wedges	Modules / stave or wedge	Chips / module	End cards / stave or wedge
0	3.7	16	32	1	2
1	7	16	24	4	4
2	16	36	32	4	4
3	21	44	32	4	2
disk 1	140	8?	16?	4	2
disk 2	150	8?	16?	4	2
disk 3	160	8?	16?	4	2
disk 4	170	8?	16?	4	2
disk 5	180	8?	16?	4	2

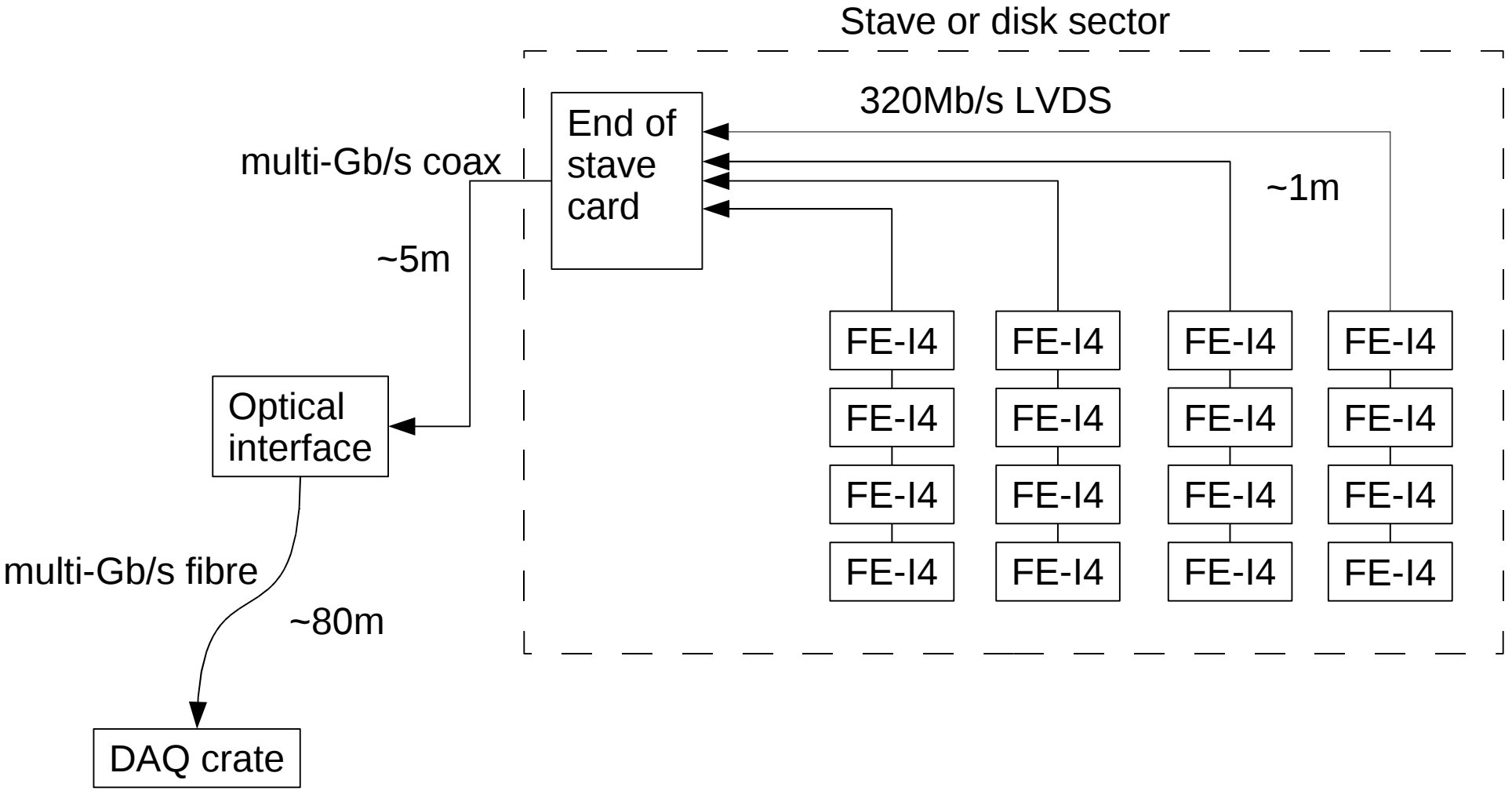
Maximal disk system

Total number of FE chips = 15,000
Total active area = 5.0 m^2
Estimated chip power = 13 KW (~twice present detector)
(nominal for FE-I4)

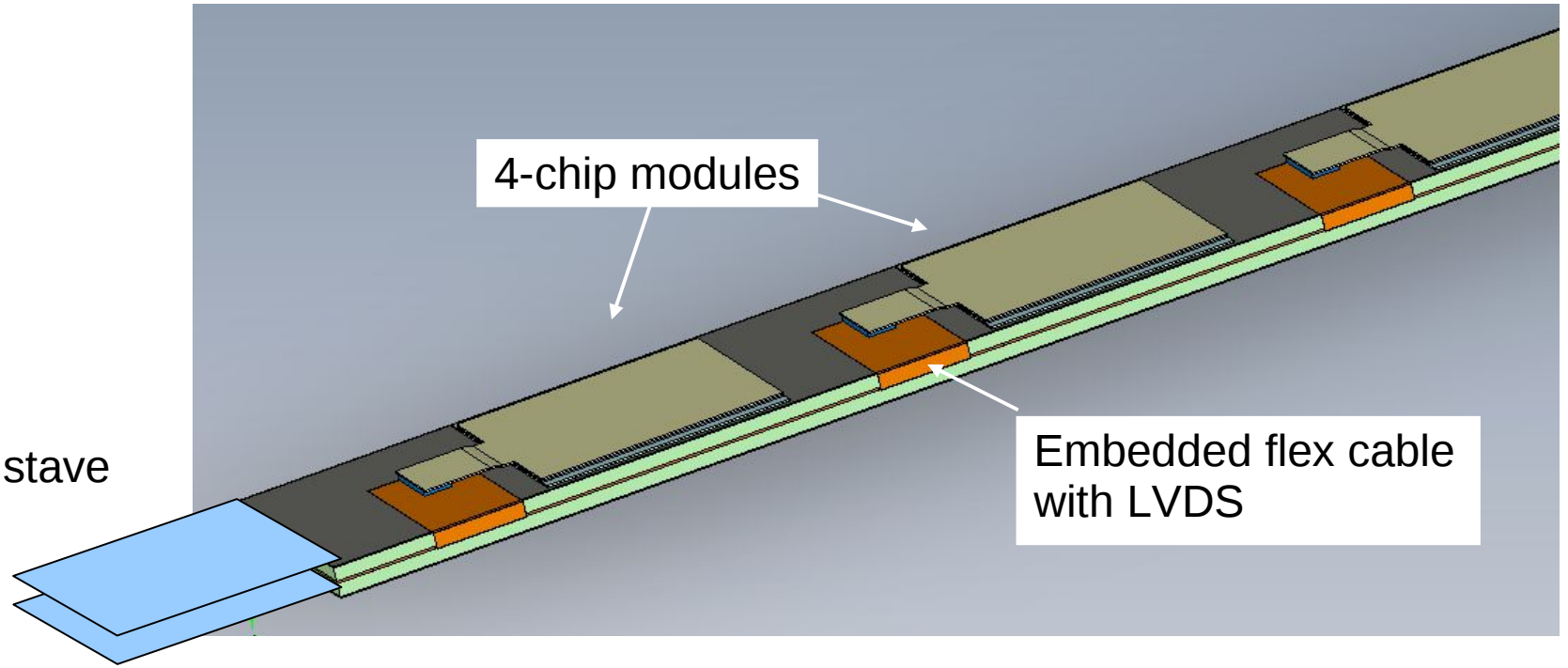
Power delivery

- A constraint for the new detector is that it must be able to use the cable plant of the present detector
  - Can take this literally to mean re-use same cables where possible
  - Or simply that it must fit into the same space and no more.
- But total power is X2
- And FE chip internal voltage is ~ /2
- This means supply current is X4 at chip
- =>To keep the same power loss in the cables, need on-detector power conversion of at least factor of 4.
- Options under consideration are
  - Serial power (8 modules in series, but could be 4)
  - 2 stage DC-DC conversion, factor of 2 in chip x another 2 or 4 near detector
  - Both options have ratio in the 4-8 range and can look remarkably similar to rest of system (cables only care about ratio, for example)

Readout system architecture



Example of stave concept



Data output parameters

Trigger rate	100 kHz
Interactions per crossing	400
Max. trigger latency	256 x 25ns
Sensor model used in simulation	260um planar, unirradiated
Comparator threshold	4000e
Output format for analog data	Fixed frame dynamic 2 pixel phi pairing
Bits / pixels per analog output frame	26 / 2
Output format for binary data	Fixed frame dynamic 2 pixel phi pairing (L2, L3) Fixed frame dynamic 4 pixel group (L0, L1)
Bits / pixels per binary output frame	24 / 4 (L2, L3) ; 20 / 2 (L0, L1)
Encoding, parity, redundancy or headers	None
Design margin	Factor of 2

Data rate requirements

Layer	comp. firing per cm^2 per BX	Required bandwidth per chip (Mb/s) (analog / binary)	chips/ module	320Mb/s LVDS outputs / module (analog / binary)	**EOS card data volume (Gb/s) (analog / binary)**	FE-I4 chip data losses (*) x 10^{-4}
0	60.0	749 / 454	1	3 / 2	12.0 / 7.3	n/a + 3
1	18.4	230 / 140	4	3 / 2	5.5 / 3.4	n/a + 1
2	6.6	75 / 58	4	1 / 1	2.4 / 1.8	18 + 0.5
3	3.9	42 / 32	4	1 / 1	2.7 / 2.1	10 + 0
disks		80 max?	4	1	2.9?	10 to 20?

50x250u x400ns pixel pileup

>1%

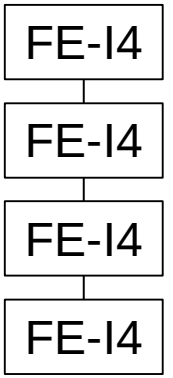
<1%

- Outer is a good match to FE_I4 chip under design and to data links like GBT
- Inner is not a “solved problem” yet. Plan a further IC design generation Pixels must be smaller, or faster, or both

- SEU corruption of hit data inside the chip is not an issue

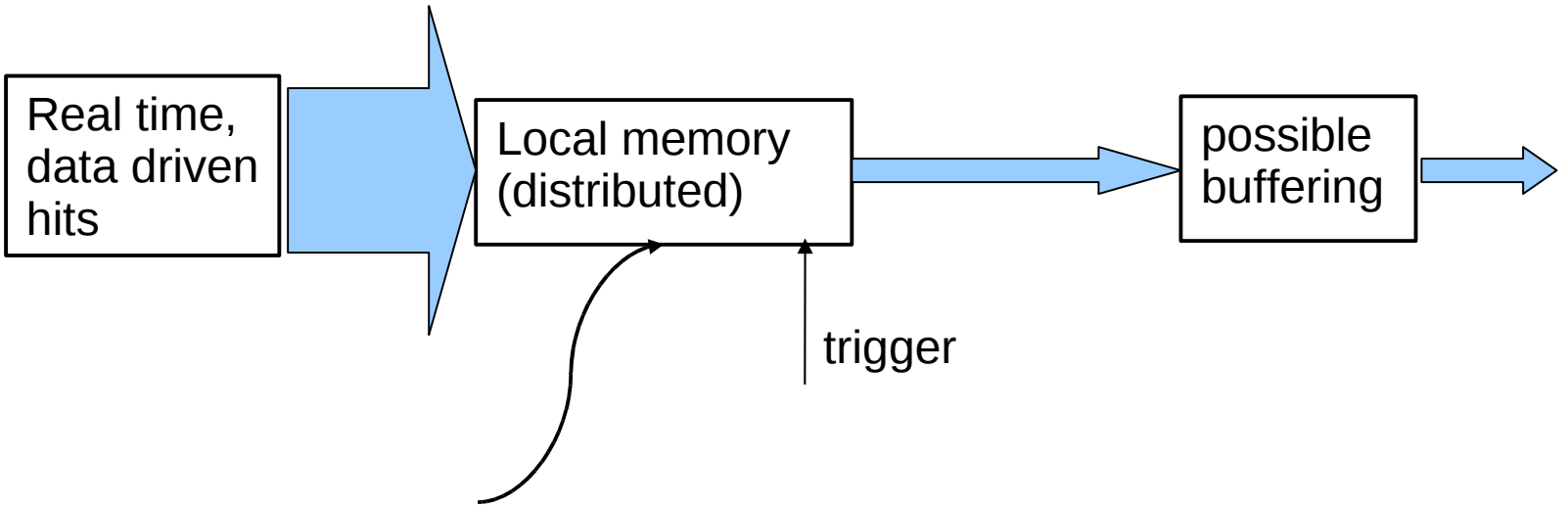
Token passing

- Recall this from a few slides ago:



- Concept is that 4 FE chips share one single LVDS output
- A read token passing scheme is necessary
- Various options under study for LVDS rate of 320Mb/s
- Could be shared bus (4 tri-state drivers), daisy chain (1 repeater per chip), or star (1 master and 3 slaves).

Trigger Latency

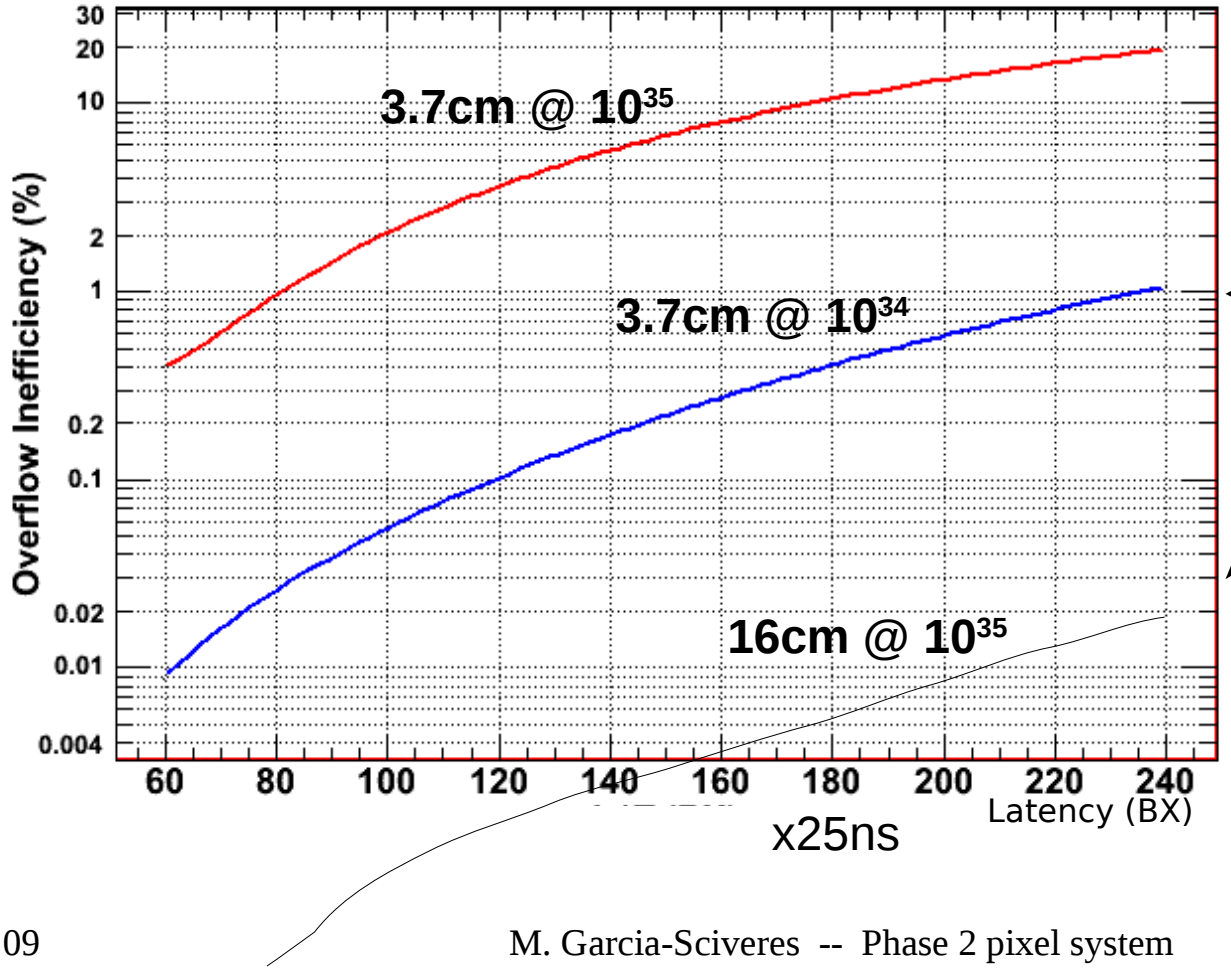


- Local memory size ~ Latency * hit_rate
- Memory size limited by pixel size
- Will have as much as can fit, no more
- => Latency * hit_rate limit given by IC technology

Memory overflow inside FE-I4 chip

(see M. Barbero talk, Wednesday for more details)

- This is basically a source of dead time.
- Increases ~1 order of magnitude with every latency doubling.
- This is a representative simulation, not the final FE-I4 architecture



Want to stay below 1%

Expect something down there for 16cm layer FE-I4 at SLHC

From D. Aritunov, Bonn

Control and monitoring

3-Level approach

<u>Detector safety interlock</u>
Always on- cannot fail
Low granularity

<u>Control feedback</u>
during operation- good reliability
same granularity as control

<u>Diagnostics</u>
On request during calibration
Maximum granularity

Control and monitoring specific cases

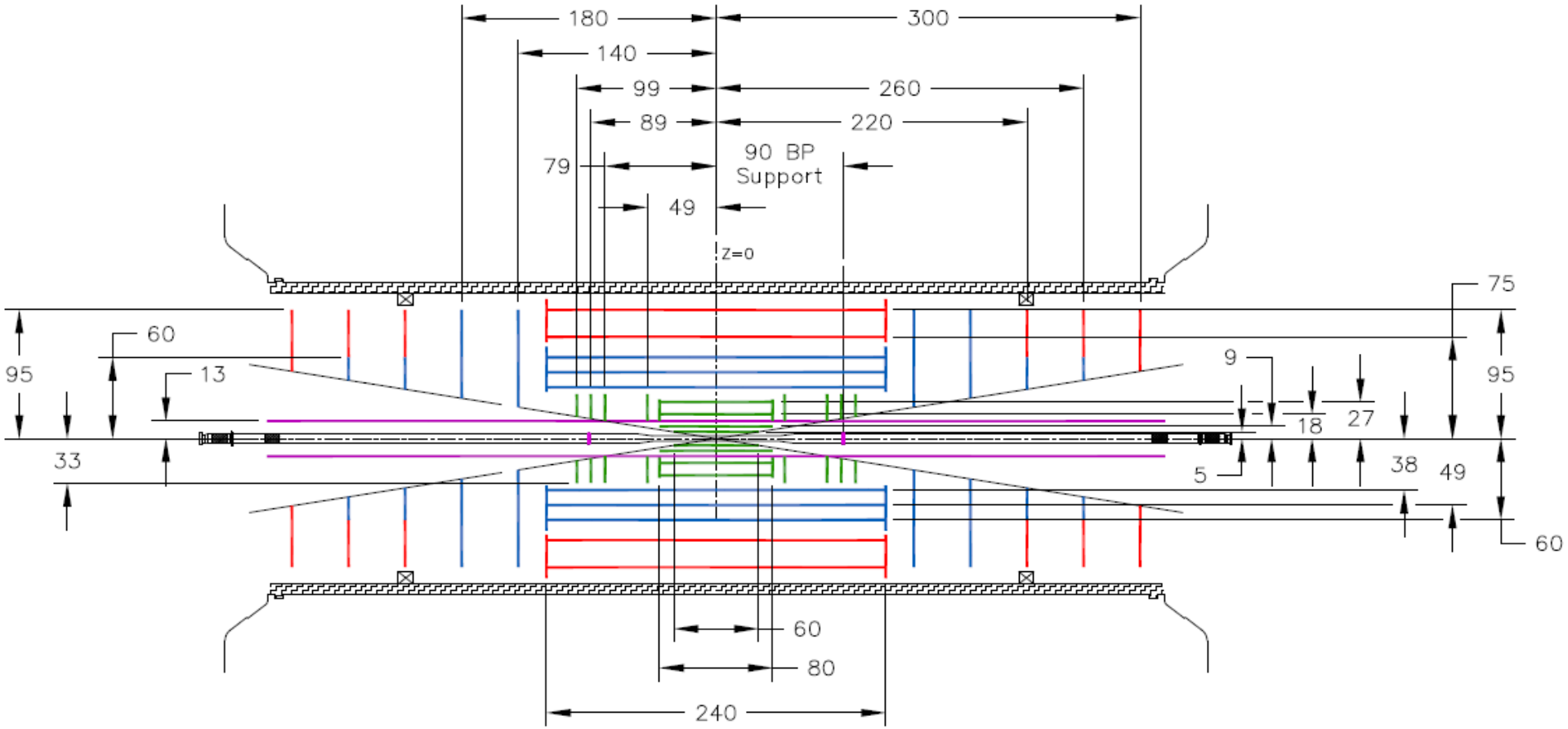
Function	Reliability	processed where	smallest group	largest group	Live time
HV bias on/off, set voltage	very high	@ power supply	sensor tile	SP stage	All use cases
feedback HV voltage & current readings	high	@ power supply	sensor tile	SP stage	All use cases
switch LV current on/off, set current	very high	@ power supply	half-stave	half-stave	All use cases
feedback LV voltage reading	high	@EOS card	4-chips	SP stage	All use cases
SP stage bypass switch on/off	high	@EOS card	SP stage	SP stage	All use cases
monitor chip LV	low	in FE chip	1 chip	1 chip	upon request
temperature interlock on module NTC	very high	off-detector	sensor tile	half-stave	always
feedback temperature reading of module NTC	high	@EOS card	sensor tile	1/4 stave	All use cases
monitor chip temperature	low	in FE chip	1 chip	1 chip	upon request

Summary

- ATLAS pixel system requirements taking shape for present upgrade concept
  - Some options and details to be resolved
  - But concept, physics needs, can still change
- Technology development for outer layers rapidly converging
- Inner layers need more R&D
- Did not cover trigger or details of power delivery – whole sessions devoted to these
- Did not cover mechanical issues- mass, cooling.

BACKUP

ID layout



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