CMS Pixel Upgrade

2nd ACES workshop, CERN

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3.3.2009

Scope

- Phase I (~2013):
  - CMS pixel detector designed for fast insertion/removal
  - Can replace system during normal shutdown
  - Planned to insert new 4 layer system in 2013
- Phase II (>2017):
  - For pixels, there is no proposal yet, nor a strawman design
  - This talk gives general considerations and personal thoughts
  - Assume that the same 4 layer/3disk mechanical structure as for Phase I will be used

Outline

- Phase I:
  - Layout of 4 layer / 3 disk system
  - Electronics upgrade
- Phase II:
  - Overview of present front end and ist limitation
  - ROC considerations
  - Hit / data rates
  - Powering scheme

Outline

- **Phase I:**
  - **Layout of 4 layer / 3 disk system**
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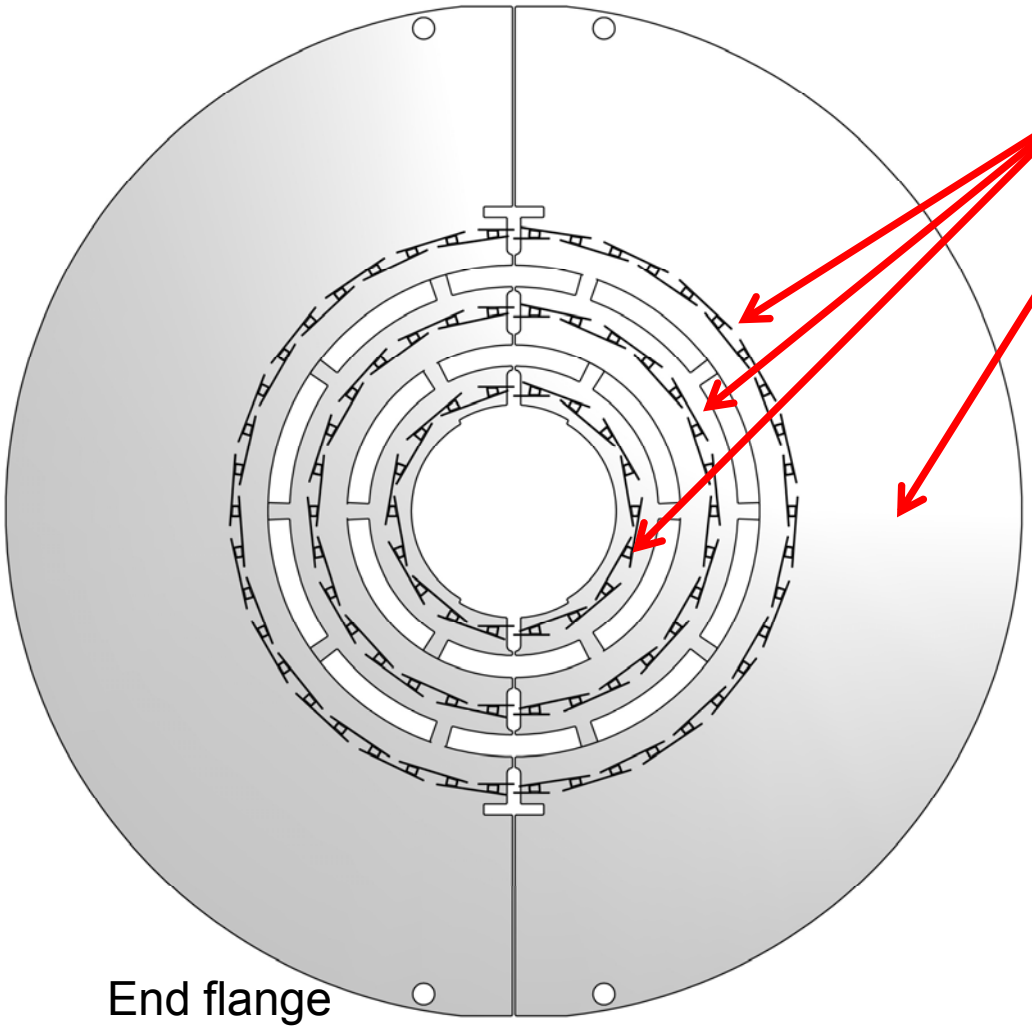
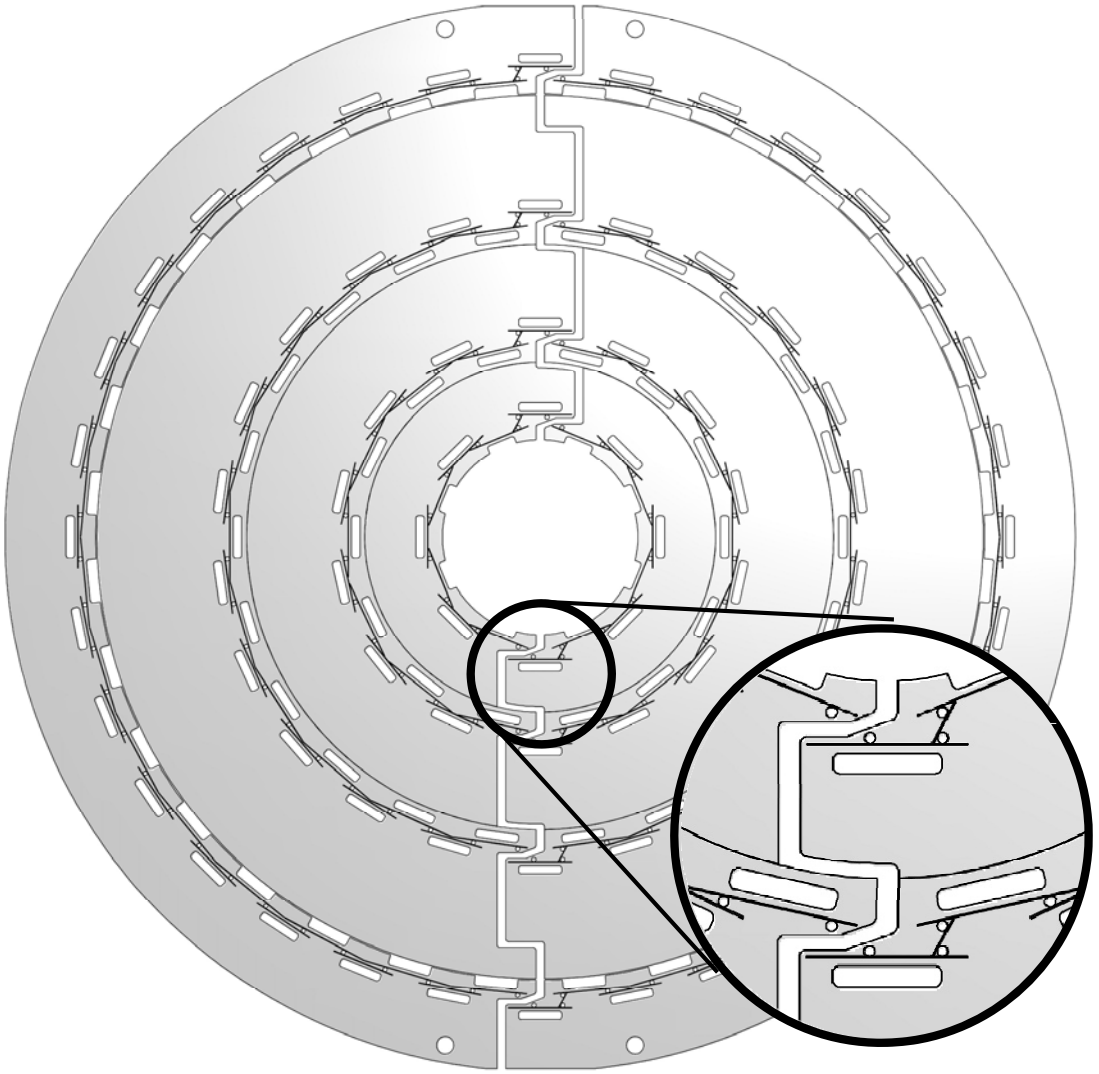
Present barrel layout



End flange

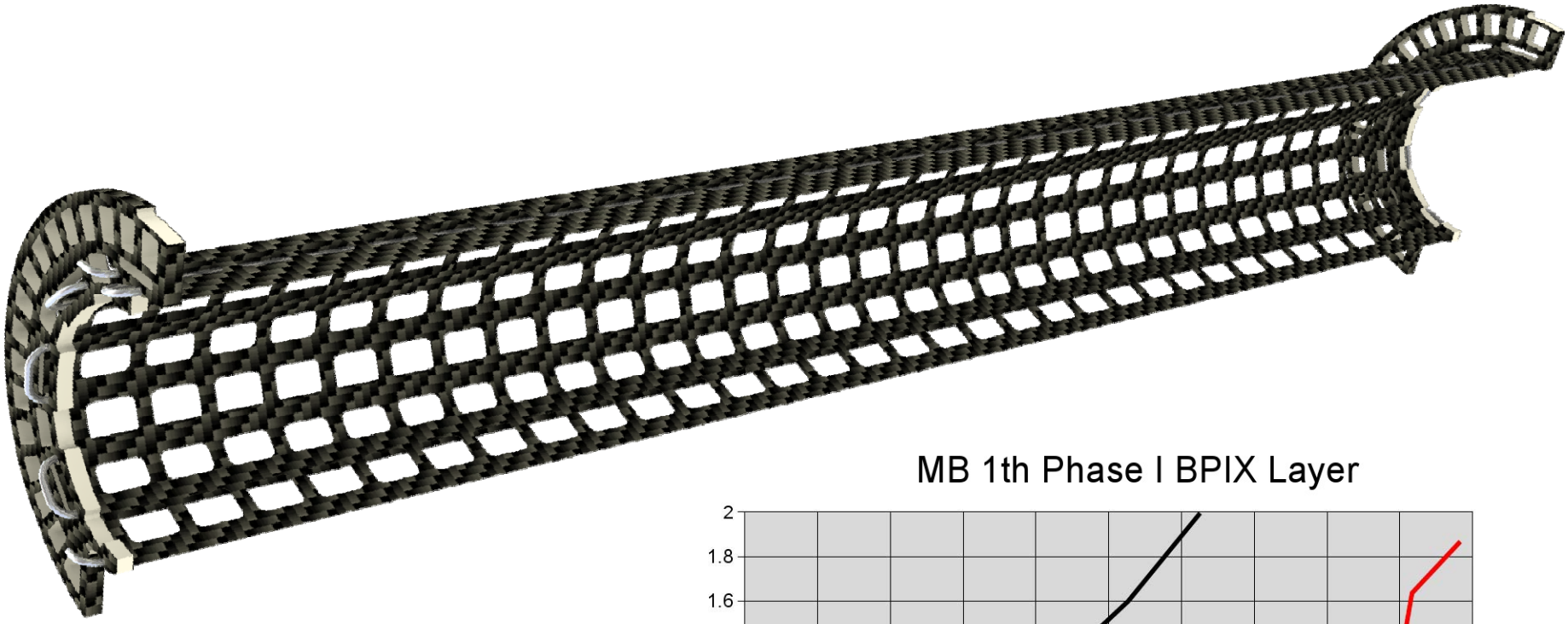
- Two identical half shells
- 3 layers at R = 4.3, 7.2 and 11cm
- Empty volume
  - Strip tracker starts at R = 20cm
  - Track seeding in pixels. Have to extrapolate through ~9cm gap
  - More difficult at higher track rates
- A = 0.75 m^2, 784 modules
  - 1 type of full module
  - 2 types of half modules
  - At least 100 different cable lengths

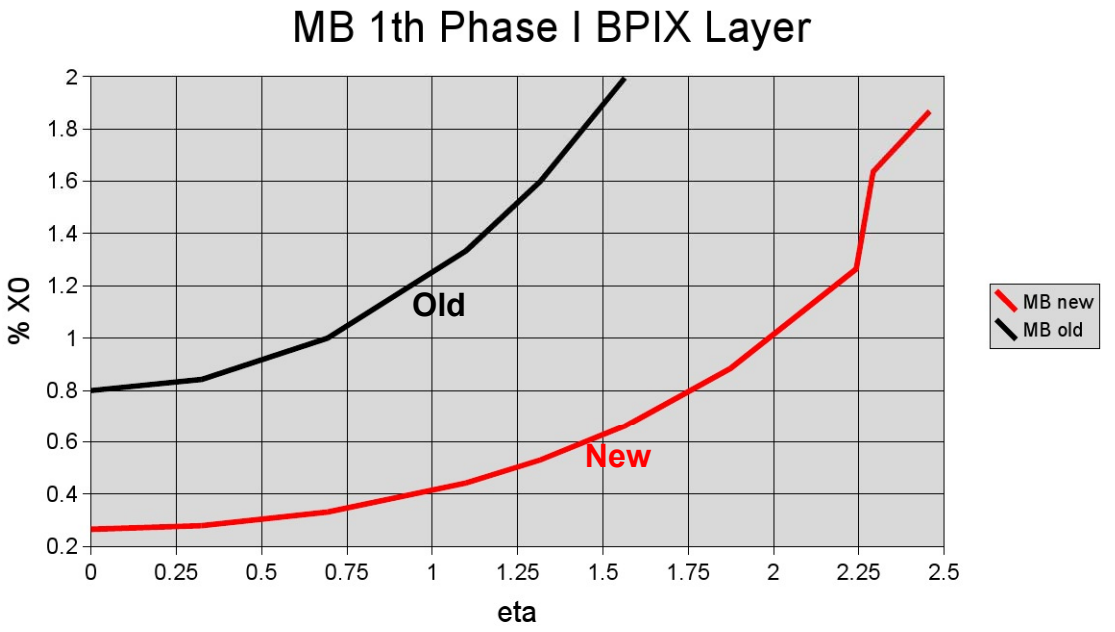
New 4 layer layout



- Two identical half shells
- 4 layers at R = 3.9, 6.8, 10.9, 16.0 cm
- No large empty volume, excellent pointing precision of track seeds
- A ≈ 1.21 m^2, 1216 modules
  - Full-modules only
- Clearance to beam-pipe 4mm

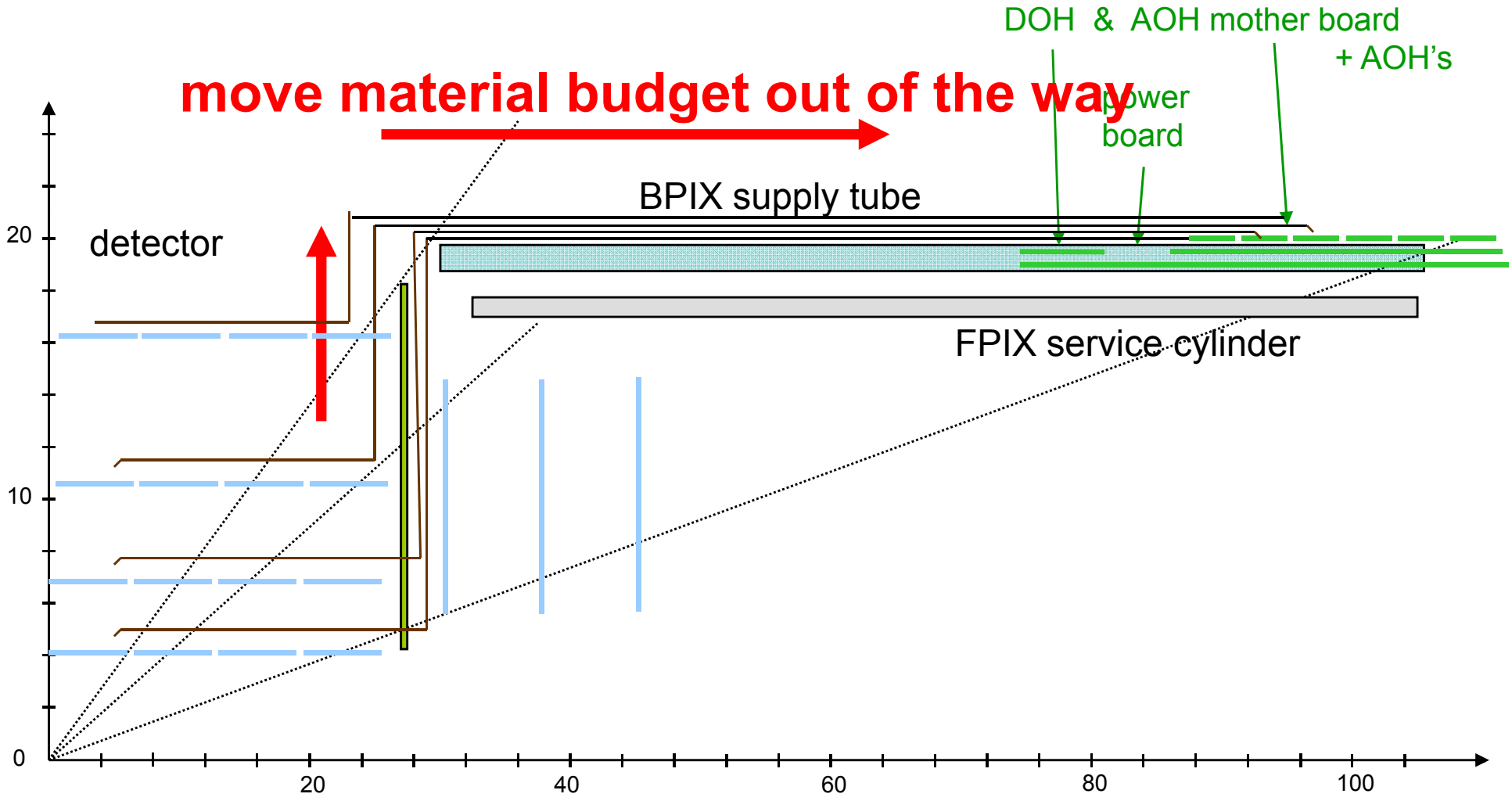
New layer 1 mechanics



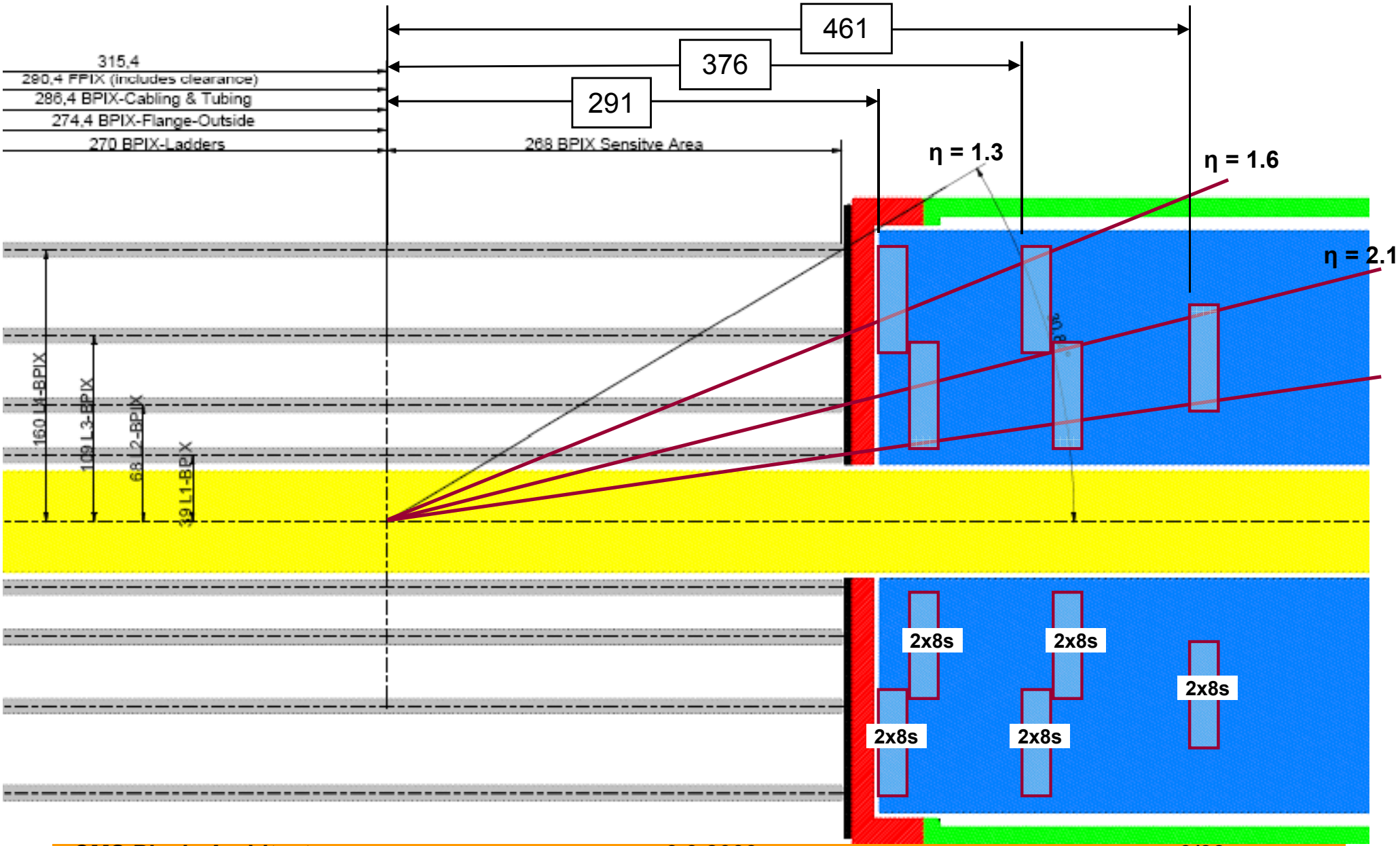


- New material budget is 30% of current barrel
- → new 4 layer system will have smaller MB than present 3 layer system

- Cooling C_6F_{14} → CO_2
- Modules with long pigtails (1.2m) **CCA μ-twisted pairs** 16x(2x125μ)
- Move DOH & AOH boards back by 50-60cm



Third disk


461
376
291
315,4
280,4 FPIX (includes clearance)
286,4 BPIX-Cabling & Tubing
274,4 BPIX-Flange-Outside
270 BPIX-Ladders
268 BPIX Sensitve Area
η = 1.3
η = 1.6
η = 2.1
160 L4-BPIX
109 L3-BPIX
68 L2-BPIX
39 L1-BPIX
2x8s
2x8s
2x8s
2x8s
2x8s

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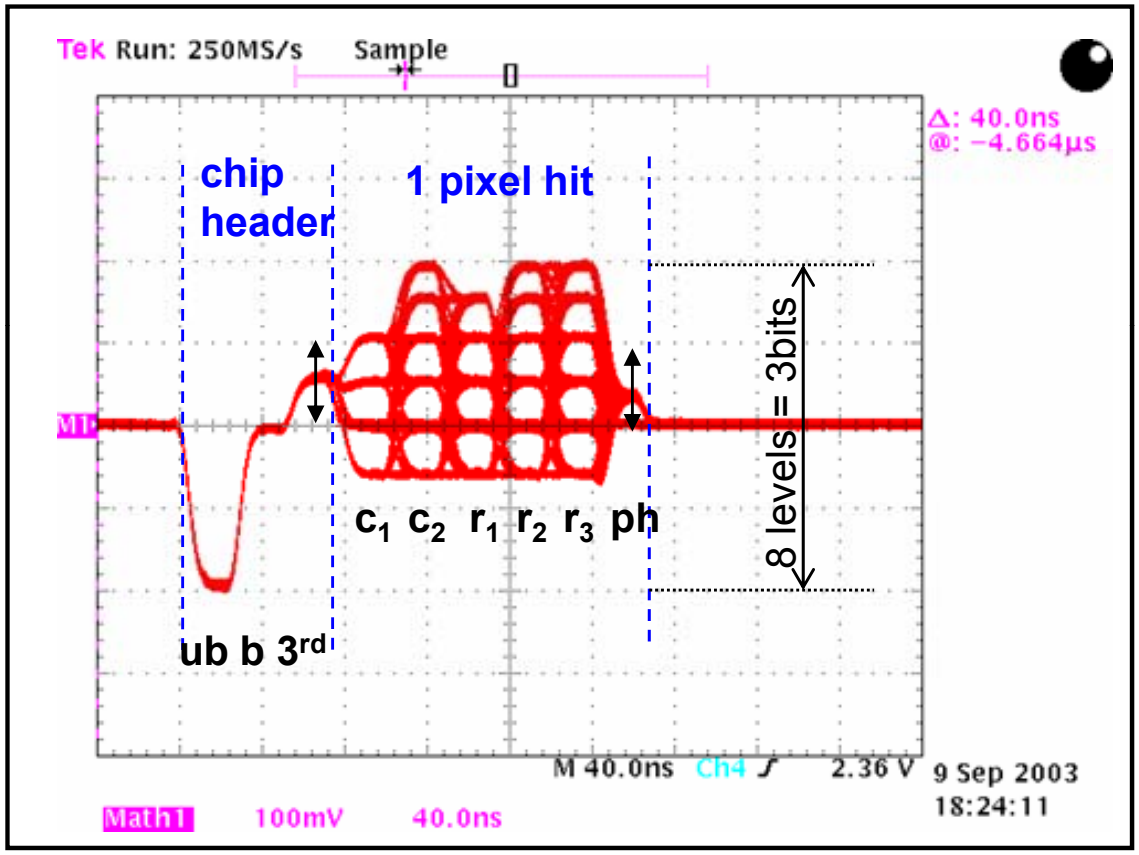
Present analog link



Pixel uses analog coded digital pixel readout

Pixel address 5 x 3 bit

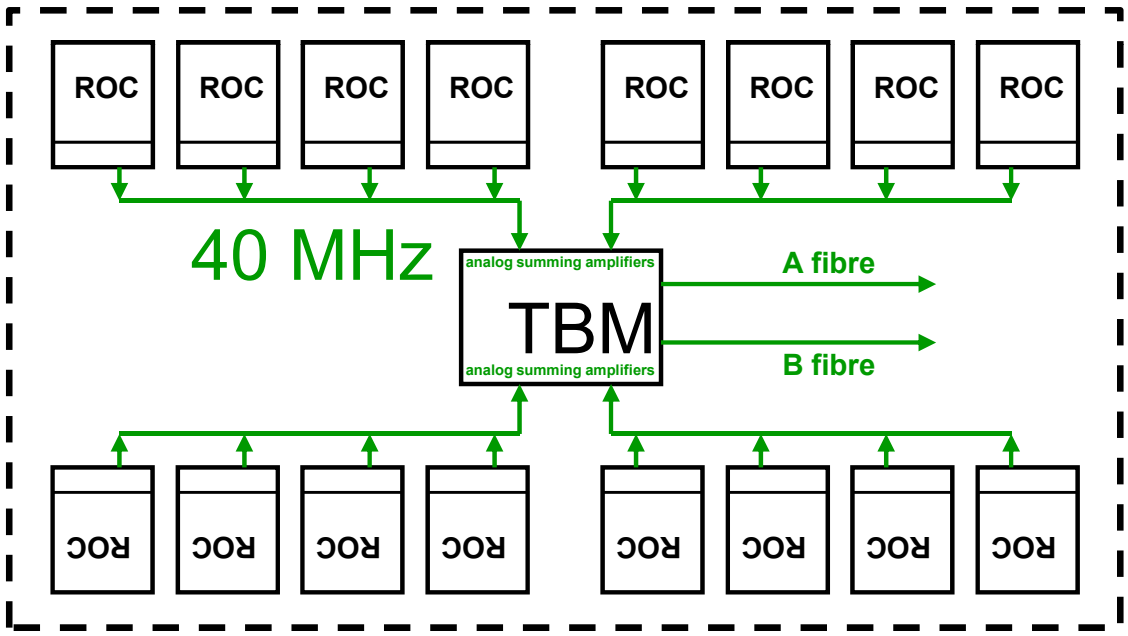
Pulse height 1 x 8 bit

→ **total 23 bits/ pixel hit**
in 6 clock cycles

→ 160 Mbits/sec link speed

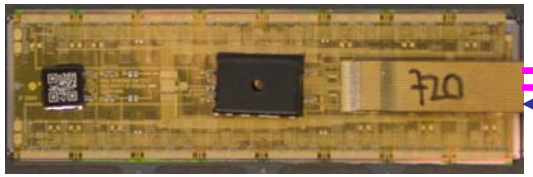
Present module readout

ROC → TBM : 40 MHz analog readout
TBM → pxFED : 40 MHz analog readout



Layer 1& 2 → 2 fibres A & B
Layer 3 → 1 fibre A

Pixel System (old)



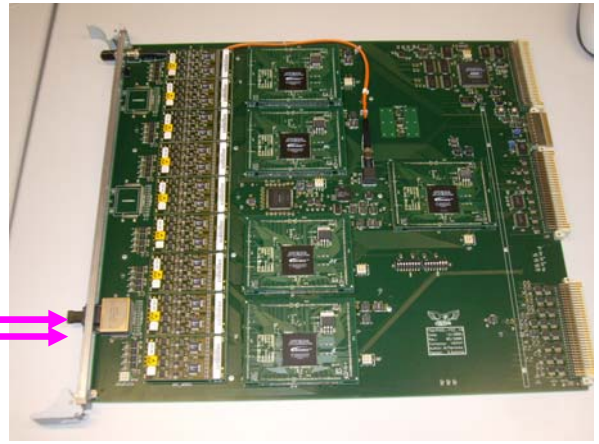
40 MHz analog out electrical

A

B

px-AOH

40MHz analog optical



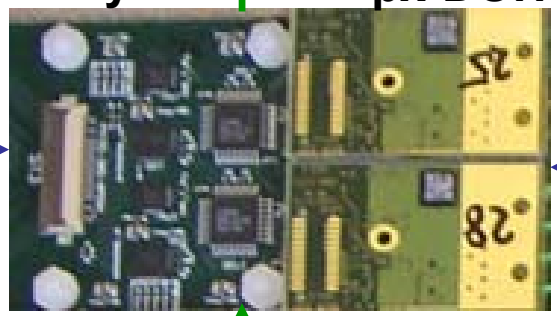
px-FED

I²C

PLL Delay25

px-DOH

crt, 40MHz fast I²C



px-FEC

I²C

CCU

trk-FEC

Three Systems:

1) Laser, PLL, Delay25 programming

2) pixel TTC & pixel ROC programming

3) 0-suppressed analog coded data readout at 40MHz

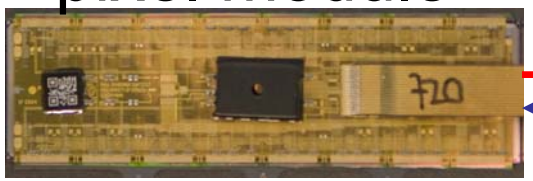
New digital readout

- In 4 layer barrel pixel system we will have 1216 modules (128 / 224 / 352 / 512)
- We will have to re-use existing fibres from PP1 out.

  1536 fibres mounted (including spares)

  → can only use one fibre per module everywhere. (now 2 fibres per module for layer 1 and 2)
- Present analog links too slow. Hard to make faster.
- New readout with 320 MHz digital links (160 MHz from FE to TBM)
  - Development of fast very low power copper links at PSI (see talk W. Erdmann)
  - Development of fast low power ADC, clock-multiplier with PLL at PSI (see talk of R. Horisberger)

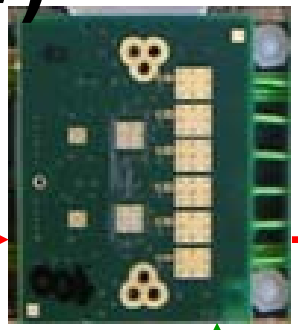
Pixel System (new)



pixel module

320 MHz binary electrical

px-AOH



320 MHz binary optical

Deserializer on daughter card

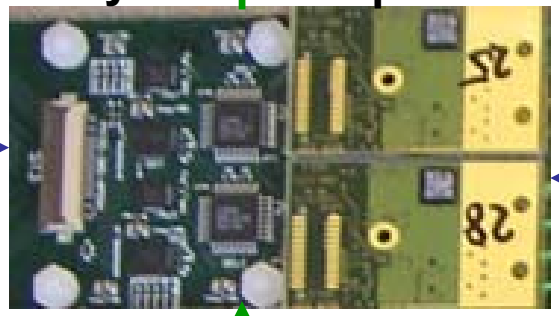
px-FED

I²C

PLL Delay25

crt, 40MHz fast I²C

px-DOH



px-FEC

I²C

CCU

trk-FEC

Three Systems:

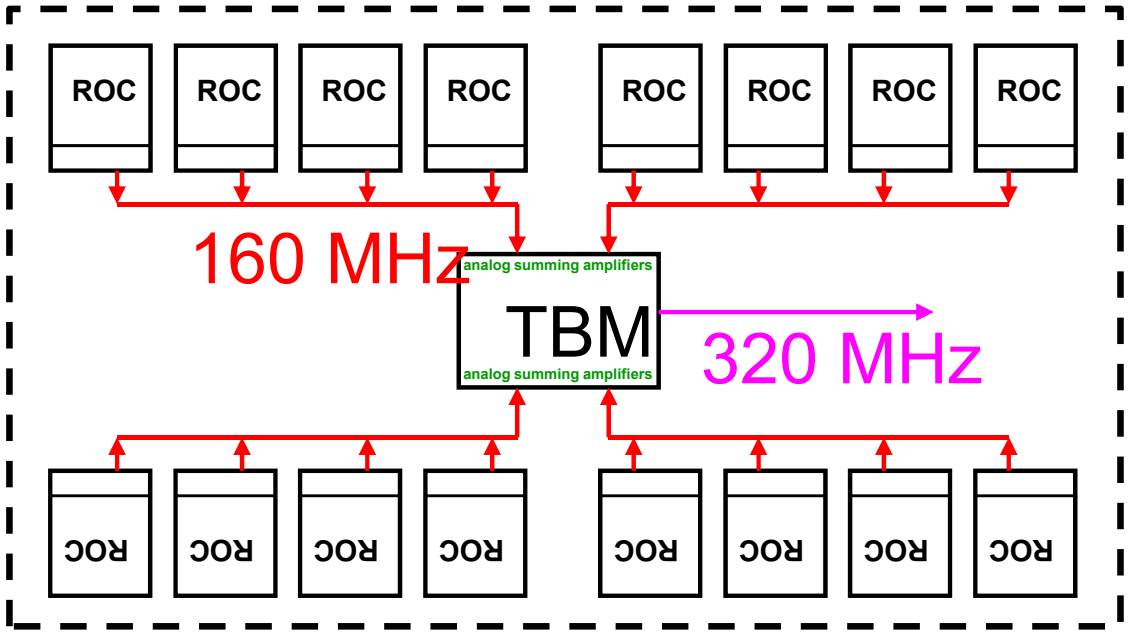
1) Laser, PLL, Delay25 programming

2) pixel TTC & pixel ROC programming

3) 0-suppressed serial binary data readout at 320MHz, same data structure

New digital module readout

ROC → TBM : 160 MHz digital readout (digitized Pulseheight, 8b
TBM → pxFED : 320 MHz digital readout (digitized Pulseheight, 8b

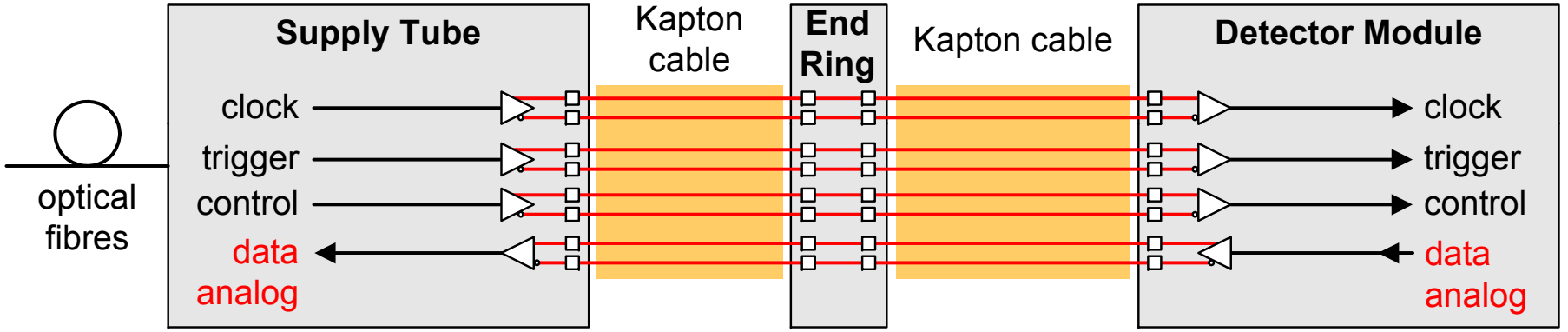


Layer 1 - 4 → 1 fibre/module

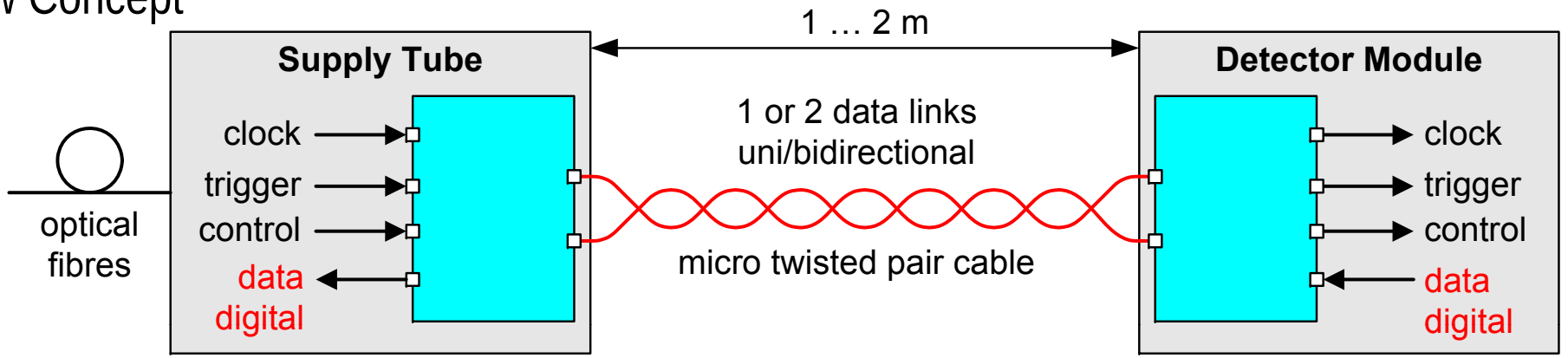
New copper links

Idea: reduce connectivity (no endring prints) and material

Existing System in CMS Pixel Detector

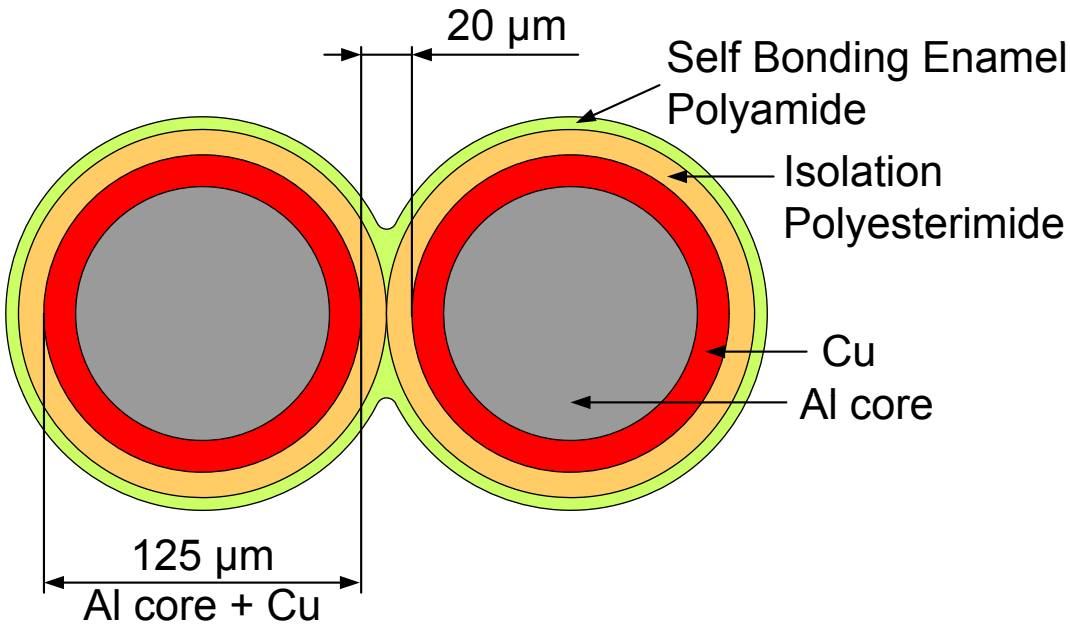


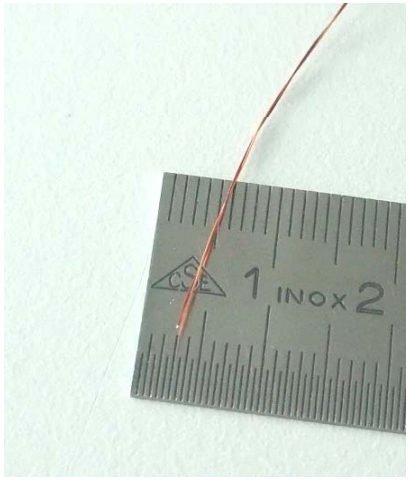
New Concept



Micro Twisted Pair Cable

cross section





First Choice:

- twisted pair self bonding wire
- 125 µm wire diameter (4um Cu)
- 10 mm per turn

Electrical characteristics:

- Impedance: 50 Ohms (very low for differential line)
- Impedance change: 1.3 Ohms per 1 µm distance variation
  (Calculation done with ATLC by Sandra Oliveros UPRM)
- $v = 2/3\ c_0$ (5 ns/m)
- C = 100 pF/m, L=250 nH/m

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Readout Chip PSI46V2

0.25 mm technology

Pixel size 100x150μm²

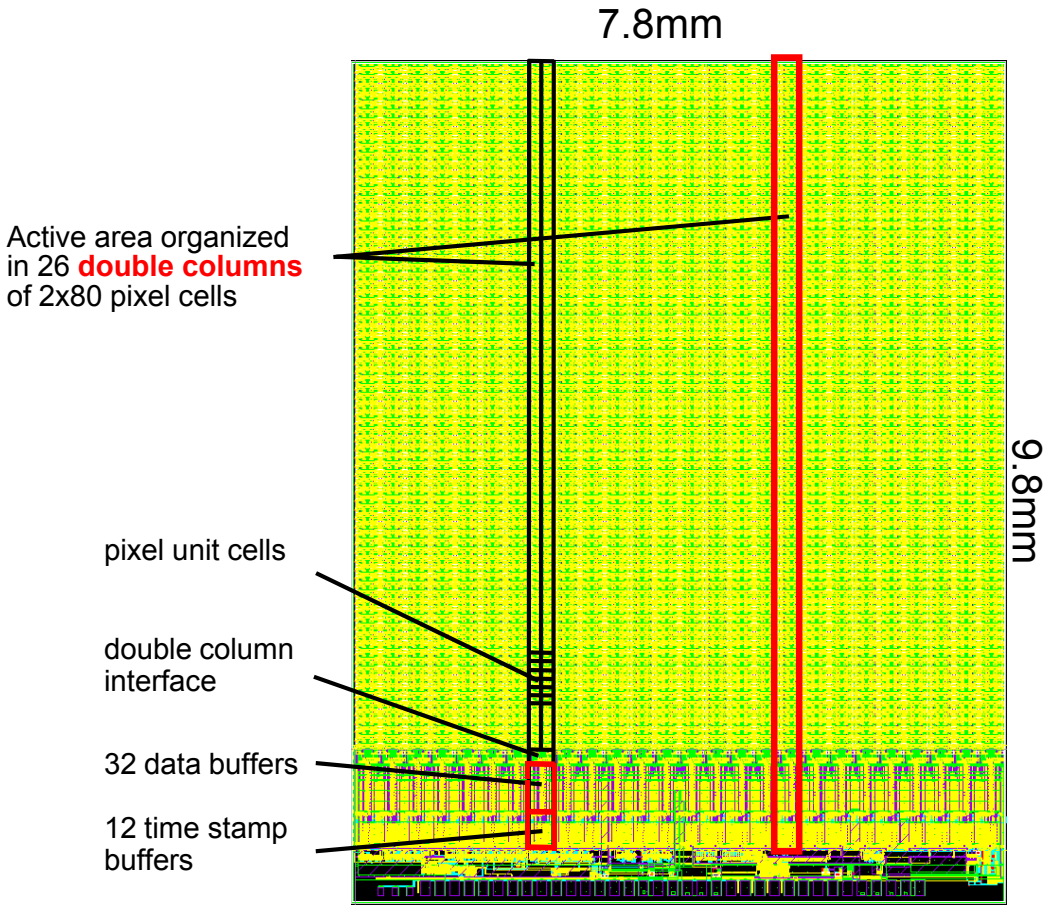
4160 pixels in array of 52x80

Pixels organized in double columns.

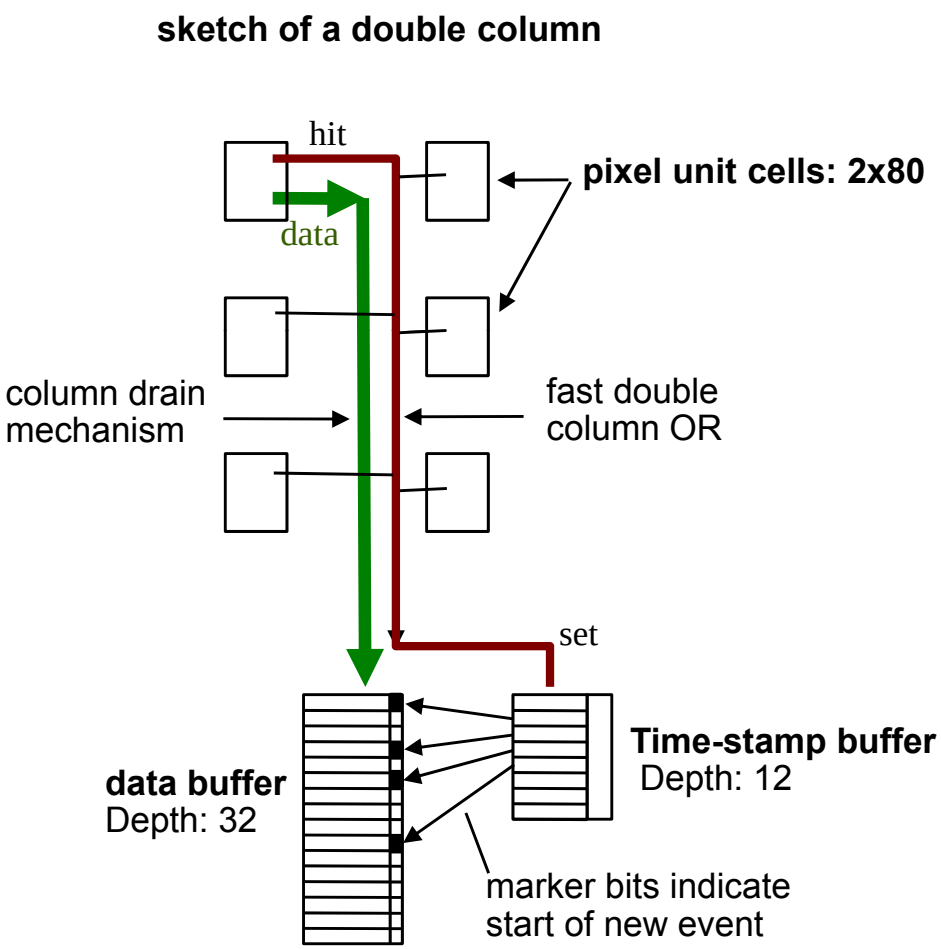
Column drain architecture

Size of double column periphery: 900μm. **Mainly due to time stamp and data buffers (800μm)**

Chip periphery contains voltage regulators, fast I²C interface, 28 DACs for chip settings



Column drain architecture

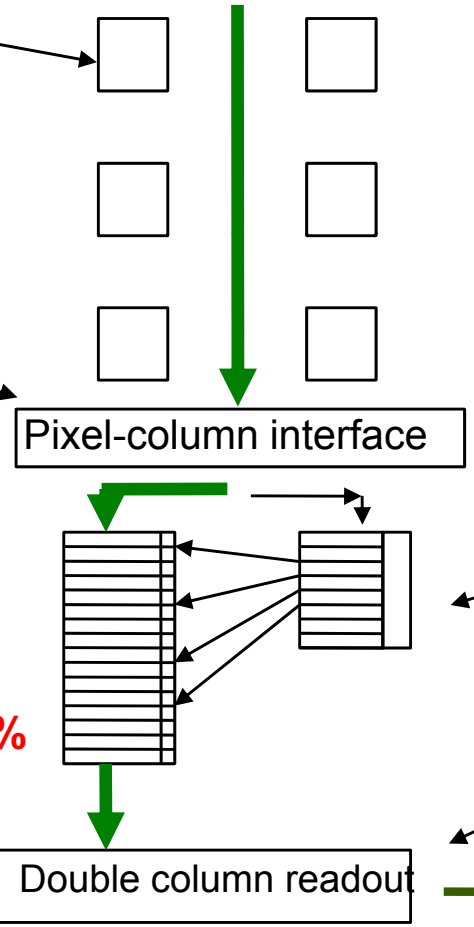


- Designed for 10% occupancy (≈7cm layer at 10^{34})
- Pixel hit information transferred to time stamp and data buffers
- Kept there during L1 trigger latency
- Double column stops data aquisition when confirmed L1 trigger → dead time
- Double column resets after readout →loosing history
- Serial readout: Controlled through readout token passing from chip to chip and double column to double column. Chips daisy chained 8 (16) ROCs.

Data loss mechanisms

Pixel busy:
0.04% / 0.08% / 0.21%
pixel insensitive until hit transferred to data buffer (column drain mechanism)

Double column busy:
0.004% / 0.02% / 0.25%
Column drain transfers hits from pixel to data buffer. Maximum 3 pending column drains requests accepted



For Luminosity: 1 x 10^{34} $cm^{-2}sec^{-1}$

Radii = 11 cm / 7 cm / 4 cm layer

Total data loss @ L1A =100kHz

- 0.8%
- 1.2%
- 3.8%

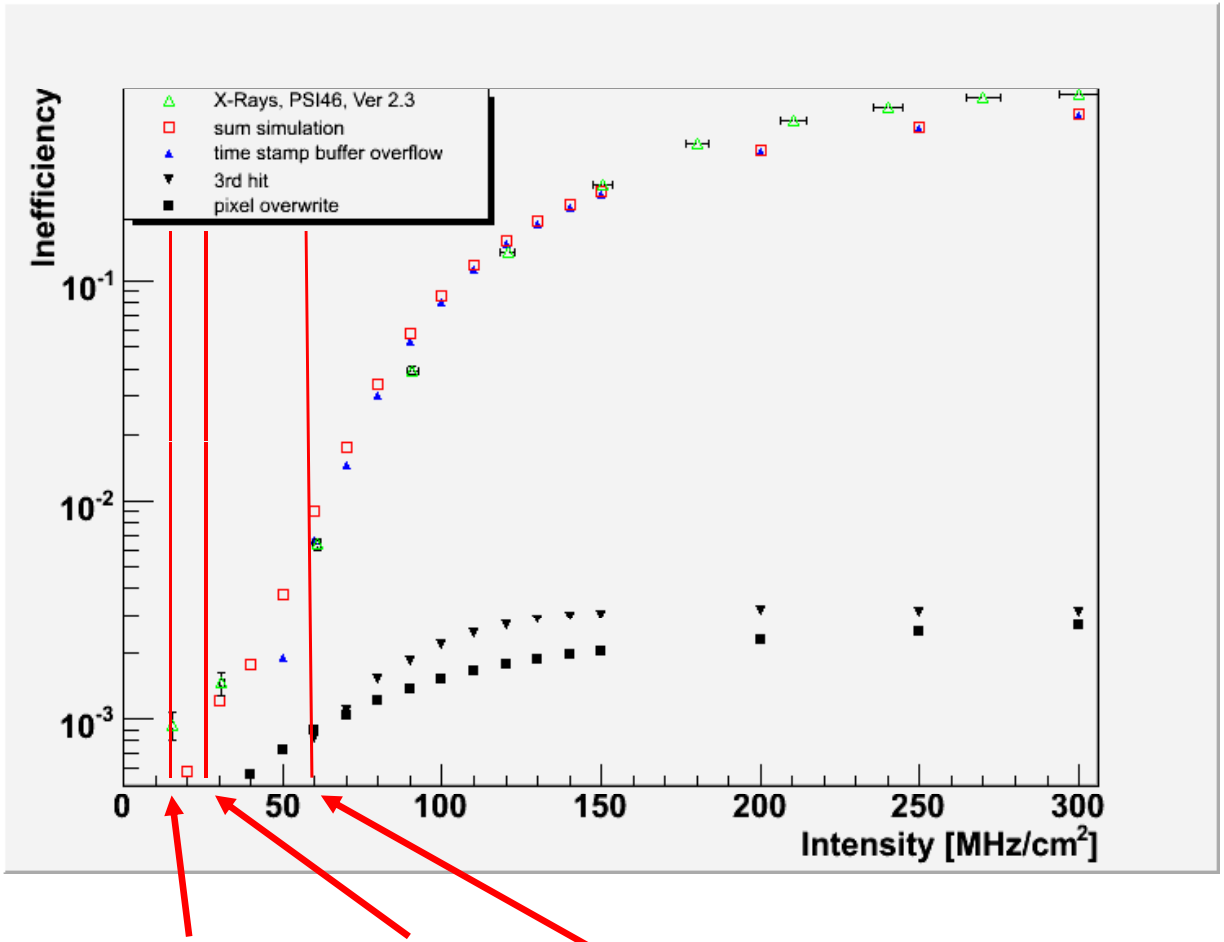
Timestamp Buffer full:
0 / 0.001% / 0.17%

Data Buffer full:
0.07% / 0.08% / 0.17%

Readout and double column reset:
0.7% / 1% / 3.0%
for 100kHz L1 trigger rate

Contributions to data loss

- Entirely dominated by **timestamp buffer overflows**
- In experiment also data buffer overflow (higher pixel multiplicity)
- Steep rise of inefficiency due to buffer limitations
- Extension of buffer sizes is trivial (no R&D)

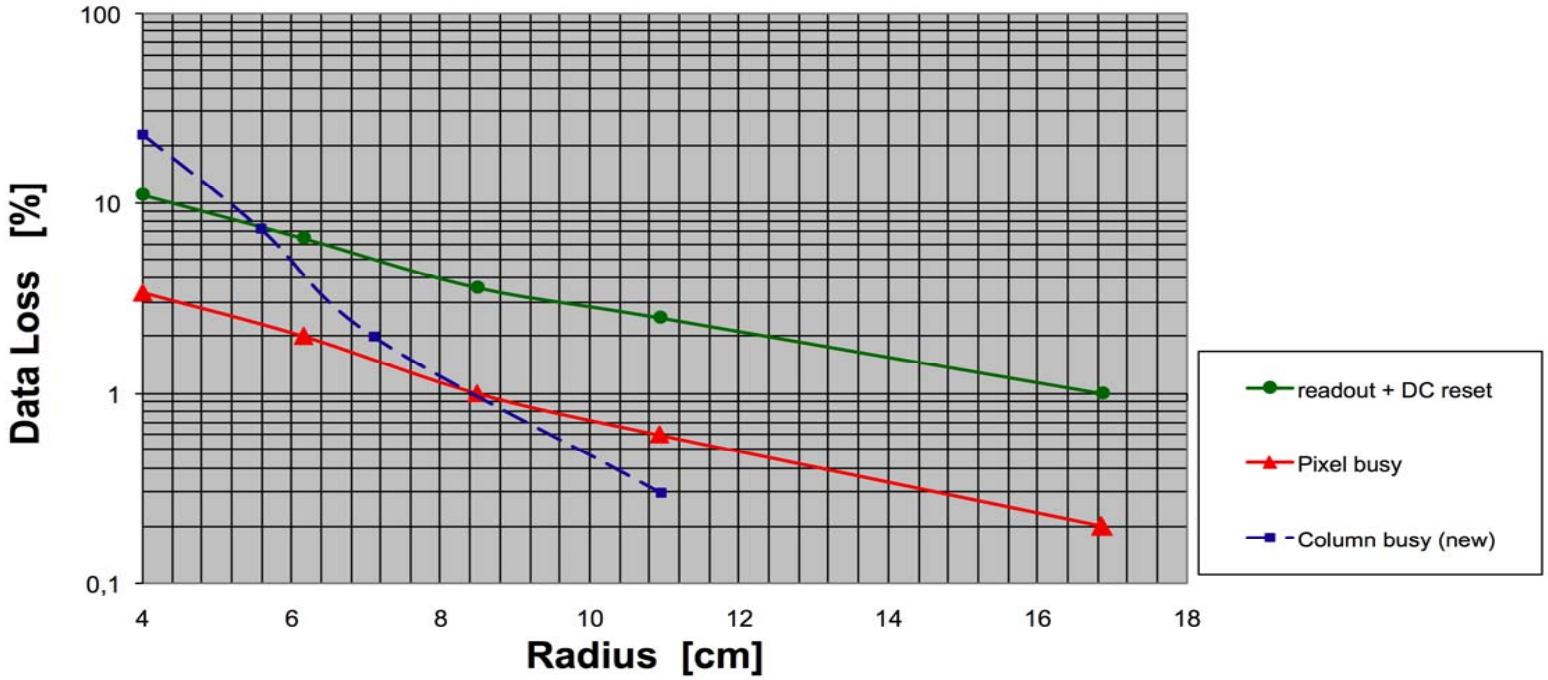


LHC (10^{34}cm^{-2}s^{-1}): 11cm 7cm 4cm

SLHC rate data losses strongly dominated by finite buffer sizes !

Inefficiency vs radius for SLHC rates

Buffers can be enlarged (trivial). What is next?



1. Next dominating effect are readout losses. The column is stopped after a L1 accept and reset when read out
2. Column drain is overloaded at low radii
3. Pixel size not really an issue

Need for new architecture

- Readout losses can be reduced by more intelligent buffer logic, such that column can contineously take data (not trivial, but feasible)
- What stays is the busy column drain. All hits are copied down to the perifery → huge data traffic
- **Column drain architecture breaks down below 8cm at SLHC rates**
- **Need entirely new architecture for SLHC**
- **No proposal yet**

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Pixel size

- Has impact on track resolution and data traffic. Should be as small as possible for physics (less (no) charge sharing after heavy irradiation), but this will increase data traffic
  - Can be reduced by using thinner sensors (i.e. 225μm)
- We want to keep good z-resolution. Physics benefit from 3D vertexing. New pixel size could be 75 μm x 100 μm (half the area of today)
  - Has to be studied in detail, but: must be considered together with FE architecture from the beginning.

Future ROC

Column drain architecture as in present ROC doesn‘t work. Two options:

1. Broader buses for column drain (CD)
   - More metal layers allow for higher connectivity
   - DMILL (2.5 metals): analog CD needed due to limitation in connectivity
   - IBM 0.25µm (5 metals): address digital in CD, 9 bit bas
   - 130/90nm (up to 8 metals): could go to broader buses, eventually recover CD
2. Store hits in pixel during trigger latency (preferred)
   - Only ≈ 0.2% of hits need to be read out, but column drain copies all hits to periphery
   - This data traffic needs power and time

   →Store hit in pixel cell.

   →have to distribute clock across whole chip. Power penalty decreases for smaller technologies (C/2 V^2)

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Estimated data rates

Assumptions:

- Peak lumi = 10^{35} $cm^{-2}s^{-1}$
- Trigger rate = 100 kHz
- 32 Bits/hit (8 ROC address, 16 pixel address, 8 pulse height
- GBT: 2.5 Gbit/s per link usable for data

Layer	Area [cm^2]	Pixel hits [MHz/cm^2]	Pixel readout [MHz]	Bit rate [Gbit/sec]	GBT links	% of total bandwidth
3.9 cm	1280	1400	4480	143	57	31
6.8cm	2236	690	3857	123	50	27
10.9 cm	3514	380	3338	107	43	23
16.0cm	5112	220	2812	90	36	19
Total	12142			463	186	

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Powering

Have to supply (a lot) more power through **existing cables**

- Baseline concept is DC-DC conversion to reduce currents (serial powering still pursued at lower priority as backup solution)
  - Design studies of 3:2 step down converter with switched capacitors at PSI (see talk B. Meier). Idea: put converter in FE chip. Reduce number of supply voltages (i.e. generate analog voltage from digital supply).
    - Cons: cannot regulate, works only for small currents (or efficiency drops too low)
  - Other solution: DC-DC conversion on supply tube
    - Need higher currents/power
    - Charge pump (→LBL, M. Garcia)
    - Inductor based converter

      → air coil is difficult to build for high power

Conclusion

CMS plans to replace pixel system ~2013 with new 4 layer barrel + 3 disk system

Will reuse parts for Phase II

- •Mechanical structure with CO_2 cooling
- •Low power copper links
- •ADC, PLL (migration to new technology)

For Phase II we will need entirely new FE architecture
To deliver the higher currents through the existing cables, CMS plans to use DC-DC converters on the detector