CMS strip tracker at SLHC Requirements and Architecture

Karl Gill

Outline

- Perspective of existing CMS Si-strip Tracker and electronic system
- Upgrade roadmap
- Requirements
  - General CMS Outer Tracker requirements
    - Tracking
    - Trigger
    - Environment
  - Boundary conditions
    - P5 existing services
- Progress on Architecture
  - Outer tracker readout (more details from Mark Raymond)
- Conclusion

Thanks to G. Hall, M. Raymond, D. Abbaneo, M. Pesaresi and other TK colleagues

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WARNING : WORK IN PROGRESS

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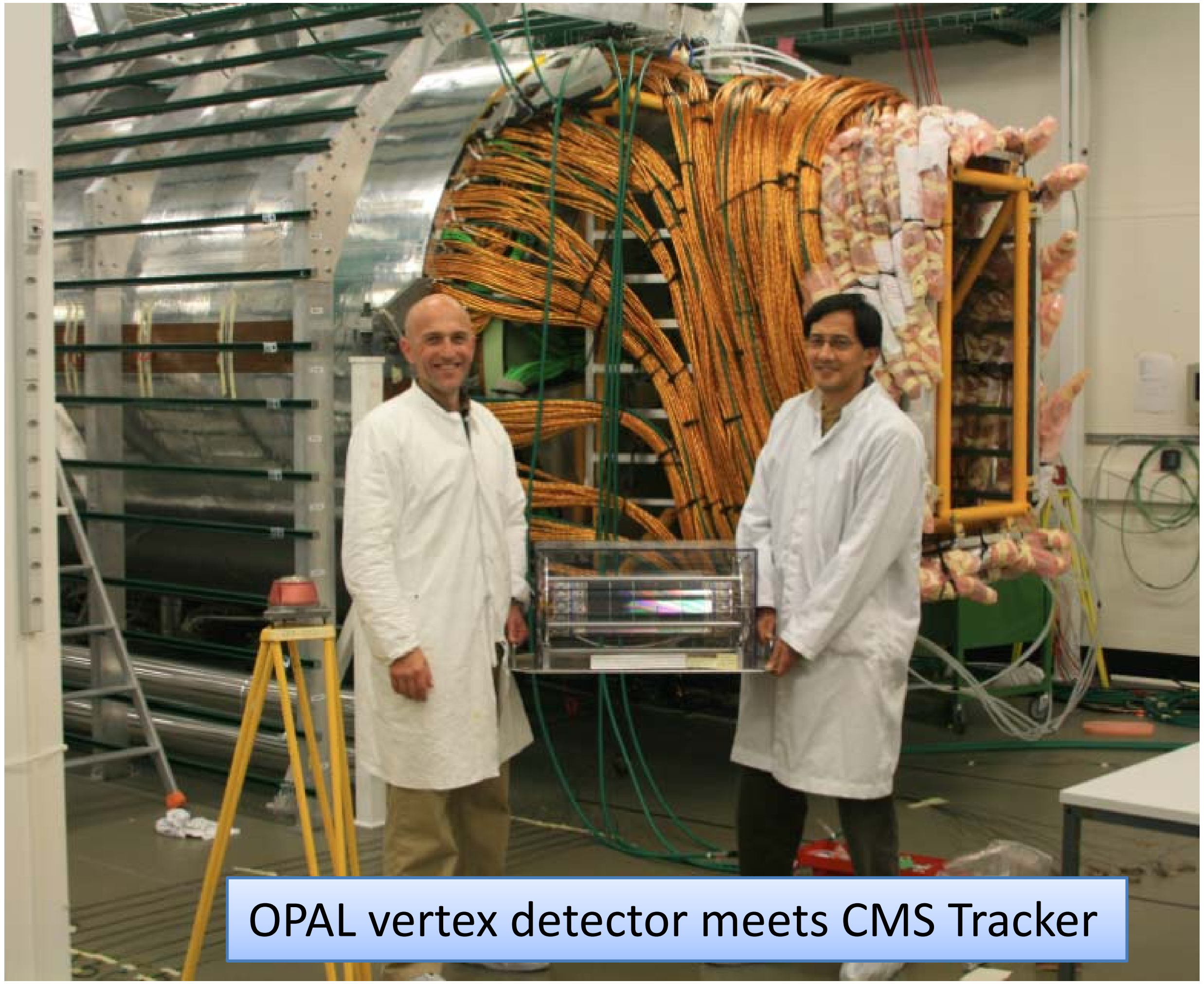
Experience with the current CMS strip Tracker

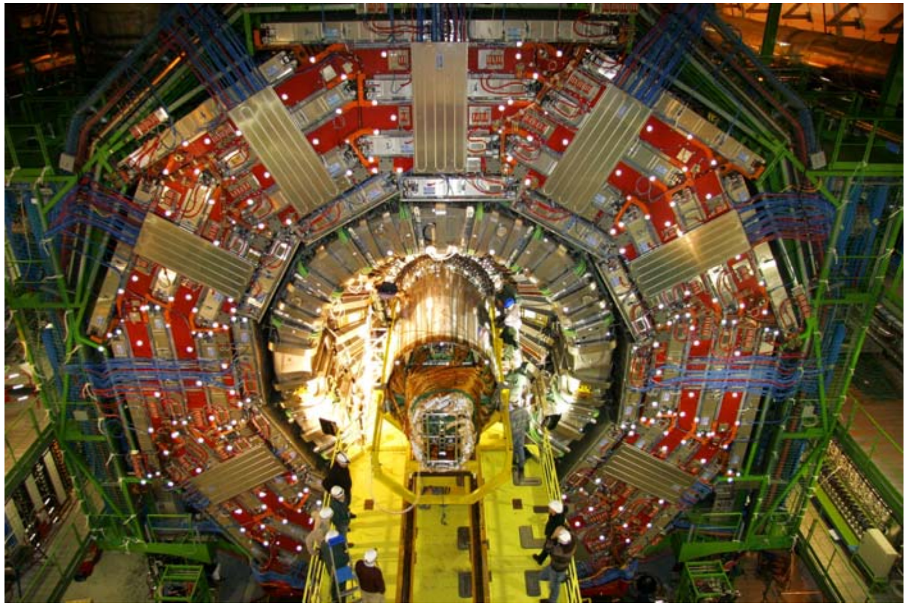
Current CMS Si-StripTracker

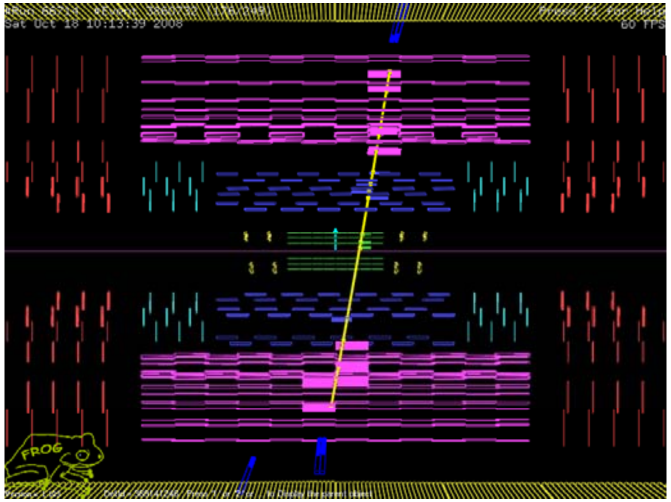
- $200m^2$ Silicon in $22m^3$
  - 300-500μm thickness
- 9.3M channels
  - 50μm to 180μm
  - Occupancy ~1%
  - η coverage up to 2.5
- 16,000 Modules
  - 27 types
- 73k APV Chips
  - 250nm IBM CMOS
- 40k Optical link channels
- 440 Front End Drivers
- 2000 Power Supplies and power cables
  - P=33kW inside TK, 20kW in cables, I=15kA
- 180 Cooling Loops
  - (C_6F_{14}, TK to -30°C)

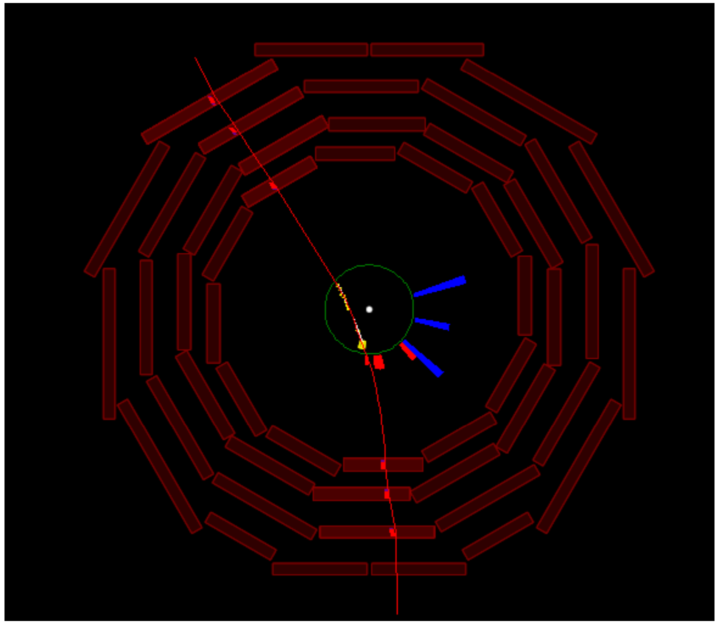
- Including pixels
  - >500 Physicists and Engineers
  - 54 Institutes in 10 Countries



CMS Si-Strip Tracker 2008/9







- 15 years R&D, Production, Assembly and Testing
- 1 day to install, 3 months to connect
- 3 months to commission (99%)
- 3 further months practising operations
  - Including 1 month cosmic running at 4T (CRAFT).
  - Very successful experience
    - 96% TK up-time, >98% TK working, 8M events with TK tracks
    - S/N >25, alignment to 25 μm in barrel, 70 μm in endcaps
    - Efficiency per layer >99%

http://cms-tracker.web.cern.ch

Current strips electronic system

- Readout System
  - Unsparsified, synchronous analogue front-end
    - 100kHz readout, 3.2μs trigger latency
  - 73k readout chips
    - Noise spec <2000e-, 50ns shaping,
    - Deconvolution or Peak mode
  - 38k optical links
    - Most novel development
  - 440 FEDS
    - 40MSamples/s
    - 10 bit resolution, 8MSB kept
- Digital Control System
  - 44 FECs
    - Token ring@ 40Mbit/s
    - 3k optical links
    - I2C at front end
    - BER < 10^{-12}
- Also TTC and APVE (x4 partitions)
- Commercially available technologies
  - Used rad-tolerant parts (eg IBM 250nm)
  - Rad tolerant system design (eg links)

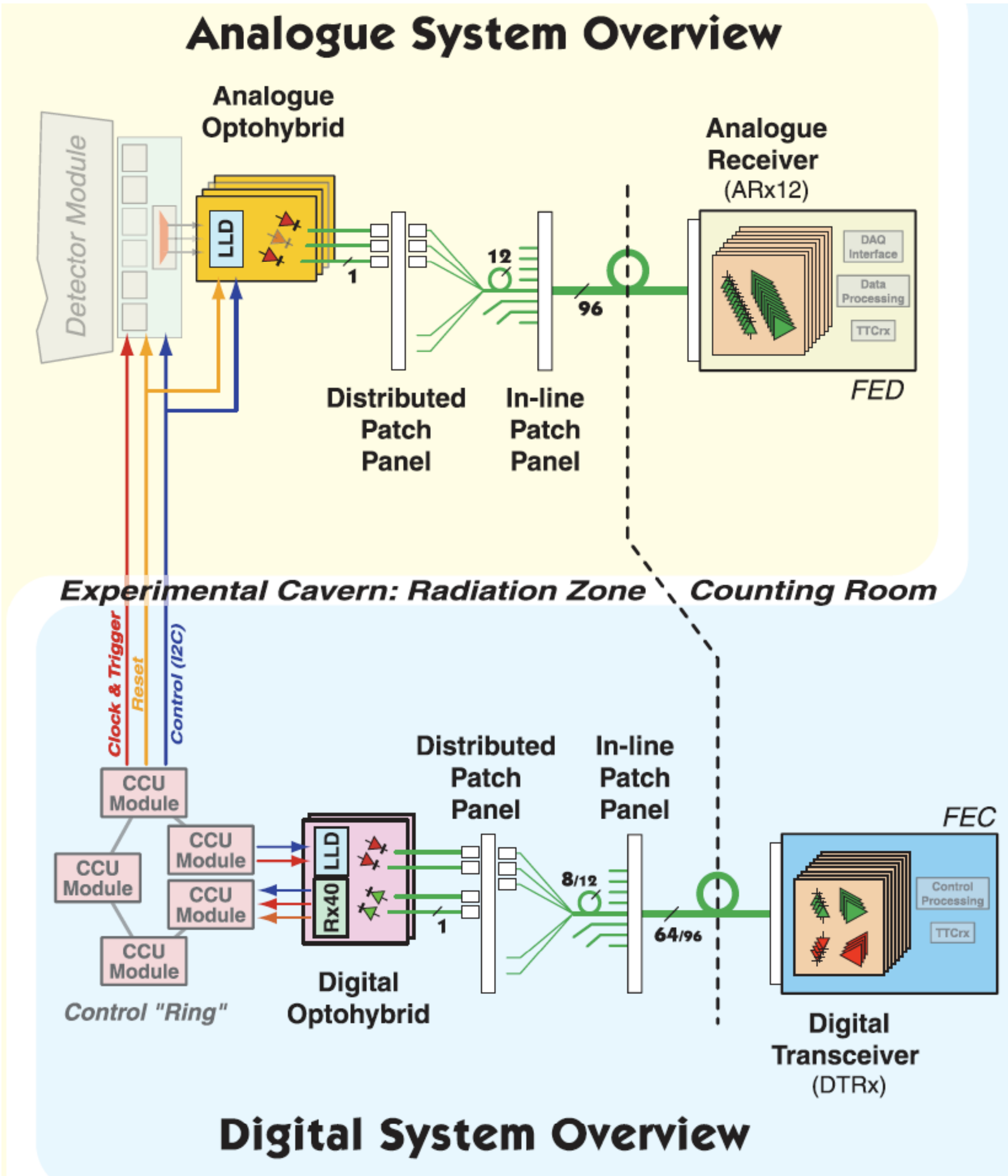


Fig: Jan Troska, NSS 2003

Some of the lessons learned

- Development/Production/Construction
  - Profited from good relationships with industrial partners and strong QA/QC
    - Maintain good contacts, make use of proven technologies
  - To ease logistics during production, assembly and reduce cost of spares
    - Minimise number of variants at front-end
  - Make common development (only) where appropriate
    - eg optical links
      - Many same parts across readout and control system
      - Also across systems: CMS TK strips (then pixels, ECAL, EE,..)
- Operations
  - Complexity/scale of system:
    - (Re-)Commissioning time is long
      - Days/weeks, should not increase
    - (Re-)Configuration time is long at start of run
      - ~minutes, should not increase
    - Electronic system proving to be high quality and robust
      - Only relatively few experts needed to operate and maintain

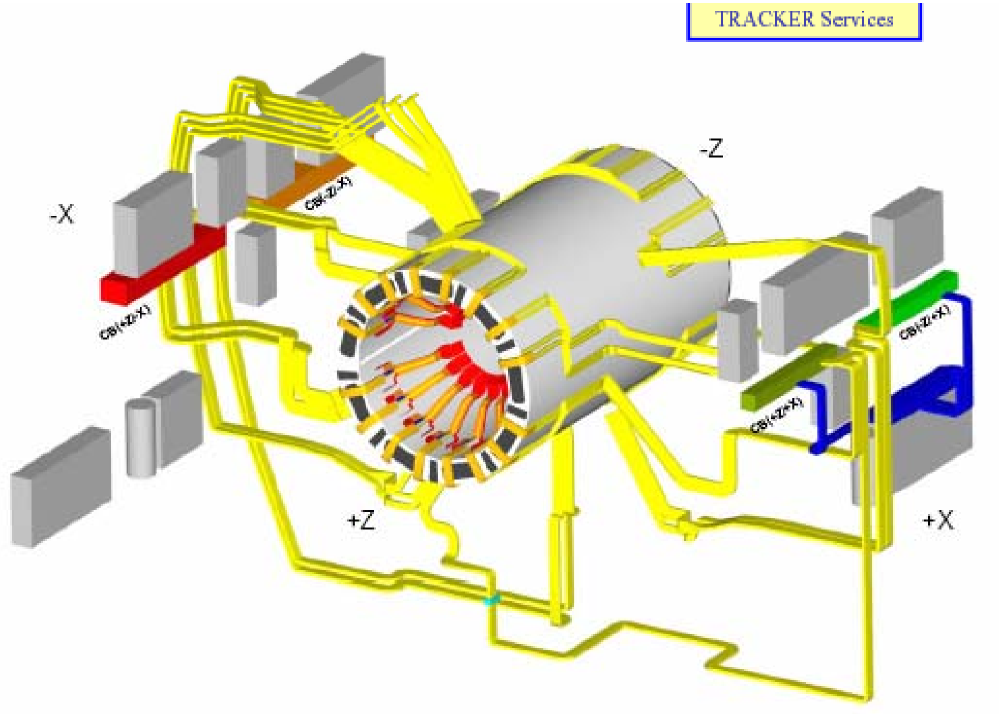
Some of the lessons learned (ctd)

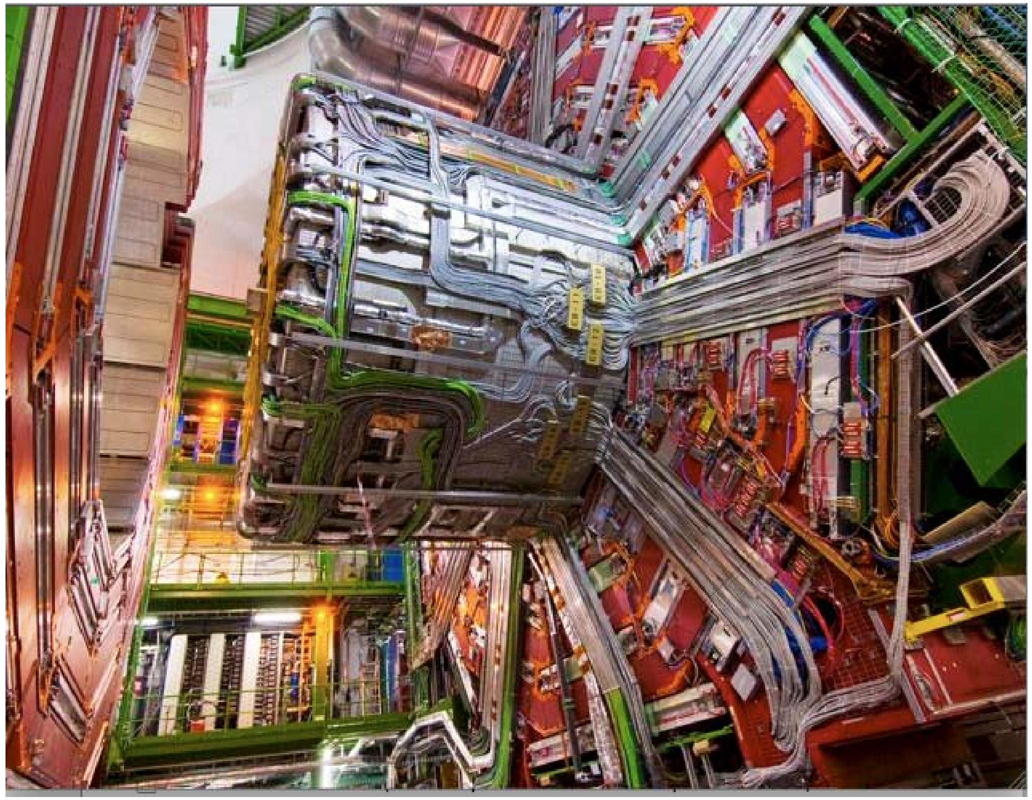
- Architecture choice (readout): Synchronous, analogue system worked well
  - Minimal power dissipated inside Tracker, intelligence put mainly at back-end (FED)
  - Power consumption is stable and uniform
  - Tracker always in known state
  - Robust against overflow
    - APV emulator (and FED) can throttle L1
  - Few problems in operation (credit of course also to developers)
    - Setup,checkout, calibration, synchronization, debugging and diagnostics
  - Scaled well from smaller test-systems to final system
    - Modest test system can still used for deep investigations and development
- Tracker digital control ring system also works very well
- Have to find best way to build on these solid foundations

Boundary conditions for upgrade: Re-use of existing TK services

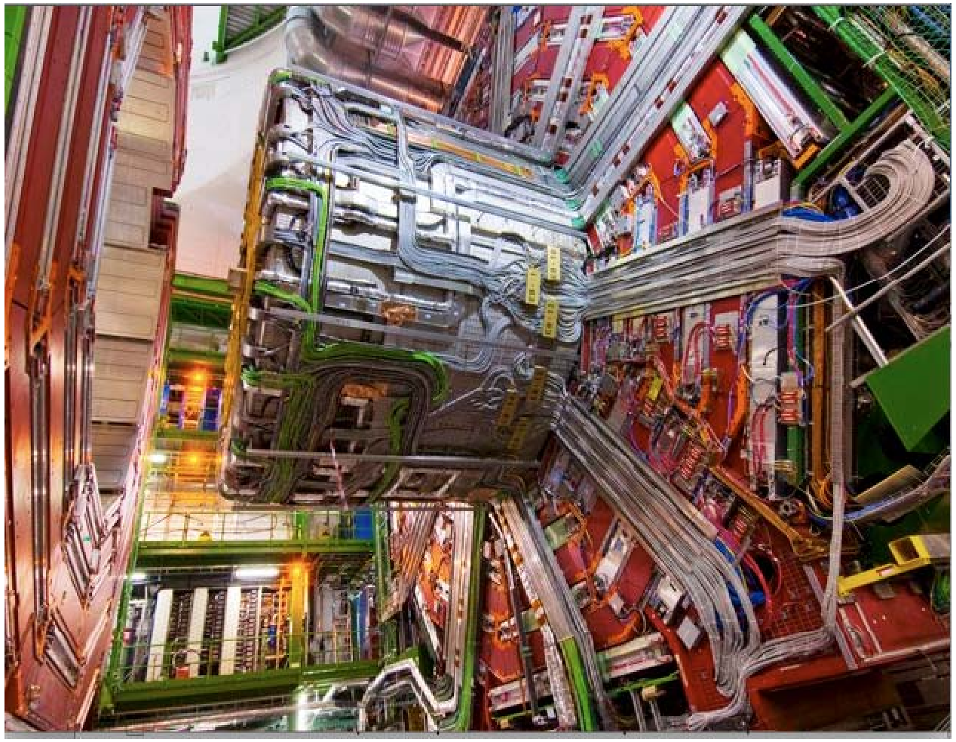
Services constraints

- Power cabling
  - From TK PP1 to 33 specific racks distributed across 6 balconies
    - Impossible to remove and re-route
- Optical cabling
  - From TK PP1 to 14 racks in USC
    - Impossible to reroute on YB0 or in UXC
    - Difficult also to re-route in USC
- Cooling
  - Pipes (2x 91 circuits) for TK cooling available
  - Current monophase C_6F_{14}
    - 33kW inside TK, 20kW in cables
    - Near limit (pipes, cables)
  - Hope to upgrade to biphase CO_2 cooling
    - building on pixel Phase 1 R&D
      - Cannot take this for granted today
- Tracker PP1 patch panels inside solenoid
  - See extra slides





Efficiency for re-use?

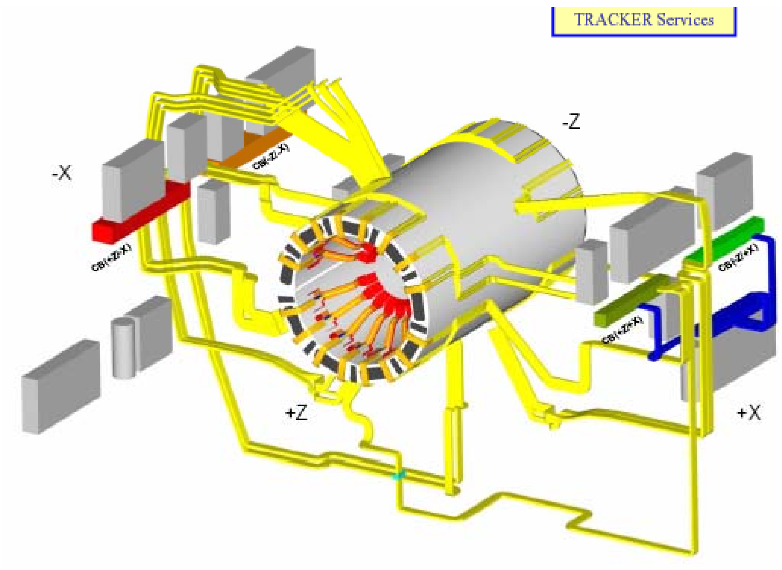


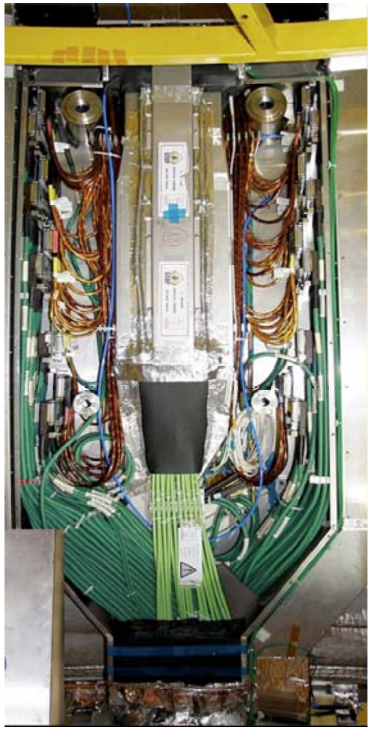
- Conclude we have to live with what we have now
  - from PP1 patch-panel outwards

- It was (and will be again) a daunting task to make sensible combined grouping of cooling, power, control and readout channels throughout the Tracker.
  - Optimised for operation and reliability as well as power, material
  - Should do as soon as we arrive at a good layout
  - Feed back into detail specification and design of mechanical structures and cooling

- Guess efficiency factor for re-use?
  - Power cables, crates and racks
    - e.g. aiming high $0.9^3 \approx 0.7$
  - Then add in fibres, pipes

- An impressive puzzle!



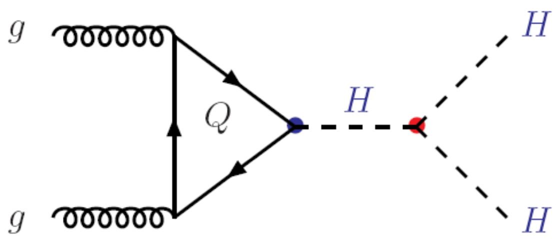


Roadmap for CMS Tracker Upgrade

Physics case

- Essentially unknown until LHC data come
  - general guidance as for LHC – granularity, pileup…
  - Improve statistics in rare and difficult channels

- eg: whatever Higgs variant is discovered, more information on its properties than LHC can provide will be needed



- Expected HH production after all cuts in 4W -> $l^{+/-}l^{+/-}$ + 4j mode
  - σ = 0.07-018 fb for m_H = 150 – 200 GeV
  - with 3000fb^{-1} ≈ 200 – 600 signal events
  - plus significant background

- An excellent detector is essential…
- …even better than LHC to cope with particle density & pileup
  - which should also be flexible to adapt to circumstances

Overall CMS Upgrade Scope

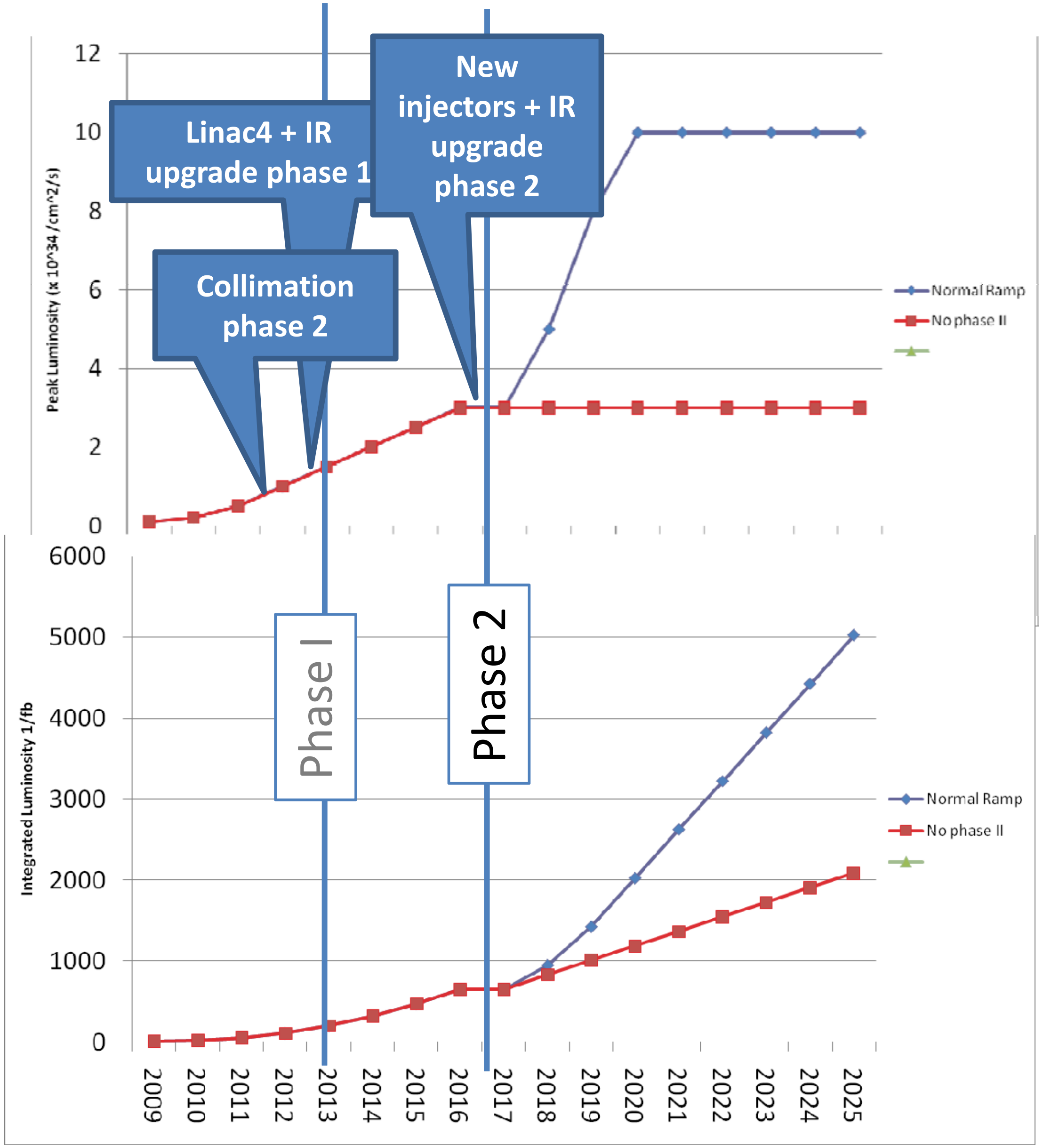
System	Phase 1	Phase 2
Pixel	New Pixel Detector (1 or 2 iterations?)	
Tracker	FEDs?	New Tracking System (incl Pixel)
HCAL	Electronics + PD replacement	HF/HE?
ECAL	TP (Off Detector Electronics) ?	EE?
Muons	ME4/2, ME1/1 ,RPC endcap, Minicrate spares, some CSC Electronics	Electronics replacement
Trigger	HCAL/RCT/GCT to μTCA	Complete replacement

Outer Tracker should be robust enough to survive Phase 1

CMS Tracker Upgrade Roadmap

- **Phase 1**
  - Replace pixels after radiation damage
  - Opportunities:
    - Add 4th barrel layer pixel
    - Ultra-light mechanics
    - Light copper links
      - Move connections further away
    - CO_2 cooling
    - Upgraded power system
      - 60% increase inside detector
      - DC-DC attractive
  - Good flexibility for when to do this upgrade in terms of (de)installation
    - Rapid removal/installation procedure
  - Also, maybe Si-strip FEDs need upgrade (TBC)

- **Phase 2**
  - Totally new TK and pixel systems
    - Higher granularity outer TK
    - L1 Trigger capacity
    - Improved cooling
    - Improved power
      - DC-DC
    - New high speed readout and control

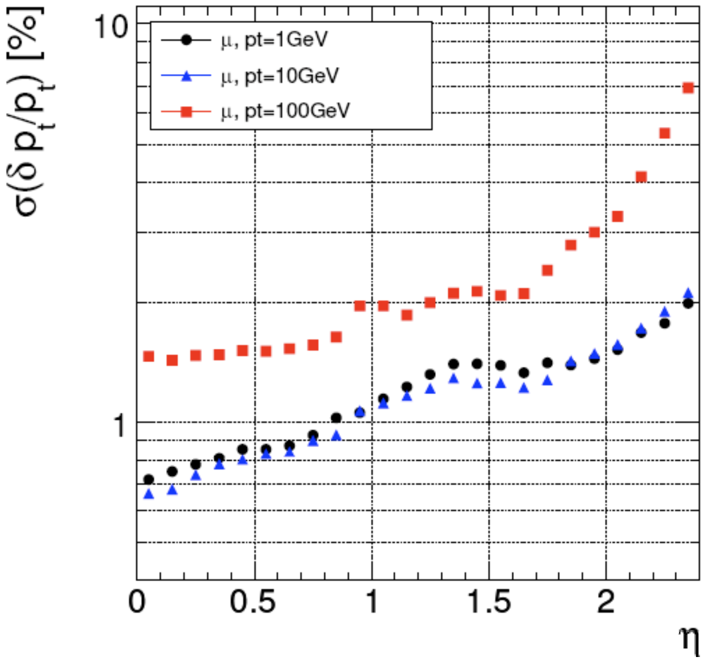


- *L. Evans, SLHC-PP 27-2-09*

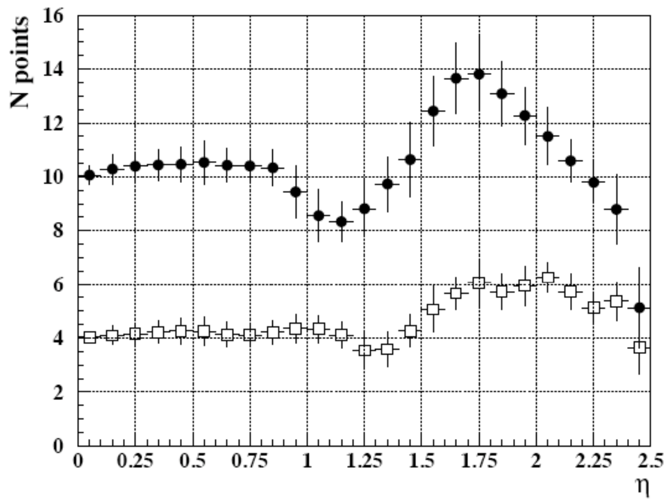
SLHC Outer Tracker requirements

Tracking performance

- Maintain current TK performance
  - Reconstruct all tracks >1GeV in η<2.5
  - P_T resolution ~1% for 100GeV muons
    - Pitch remains the same
    - Strip length has to decrease to keep occupancy <few %



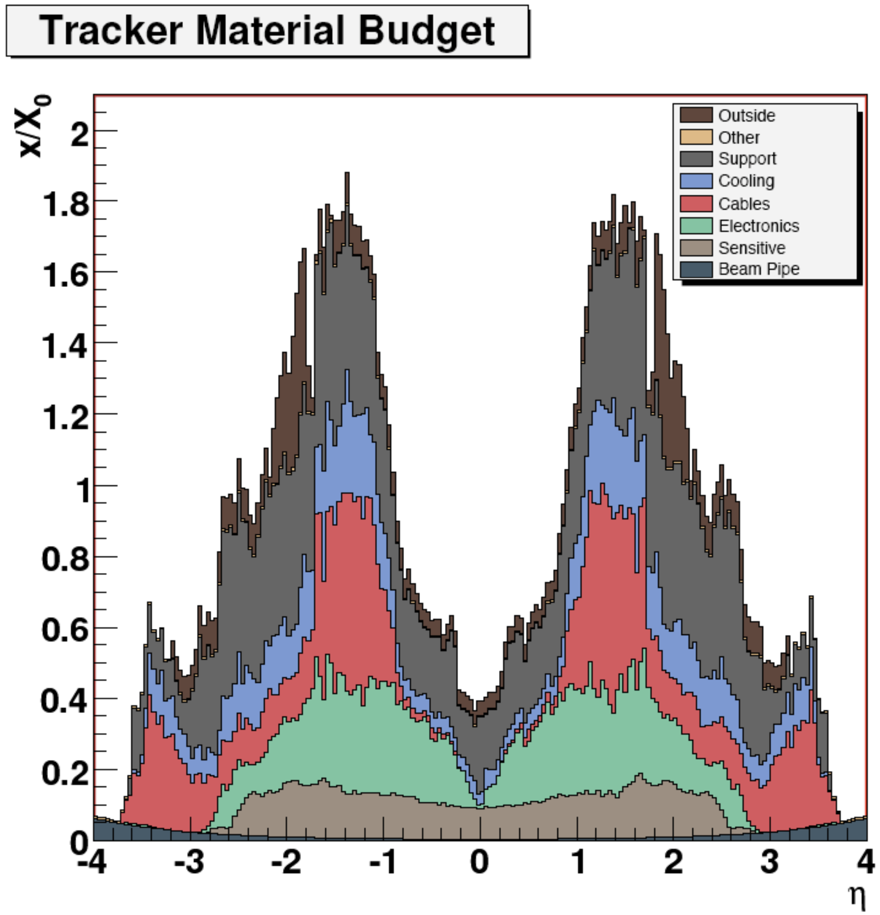
- Resolve primary vertices
  - To be seen whether stereo layers still needed in outer barrel, or if 4 layer pixel sufficient

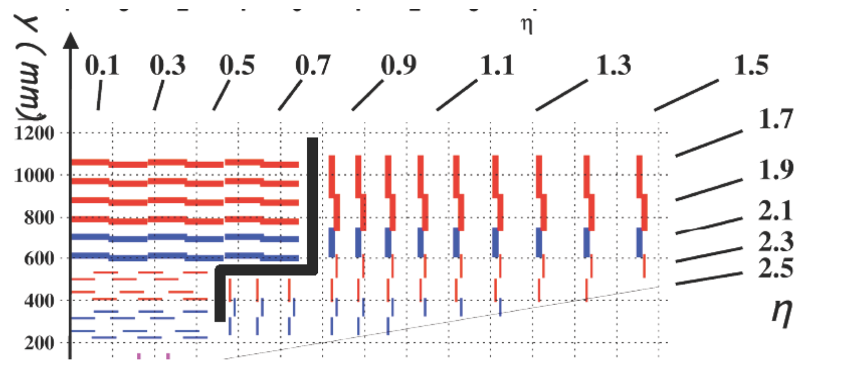


CMS paper, JINST, 2008

Material budget

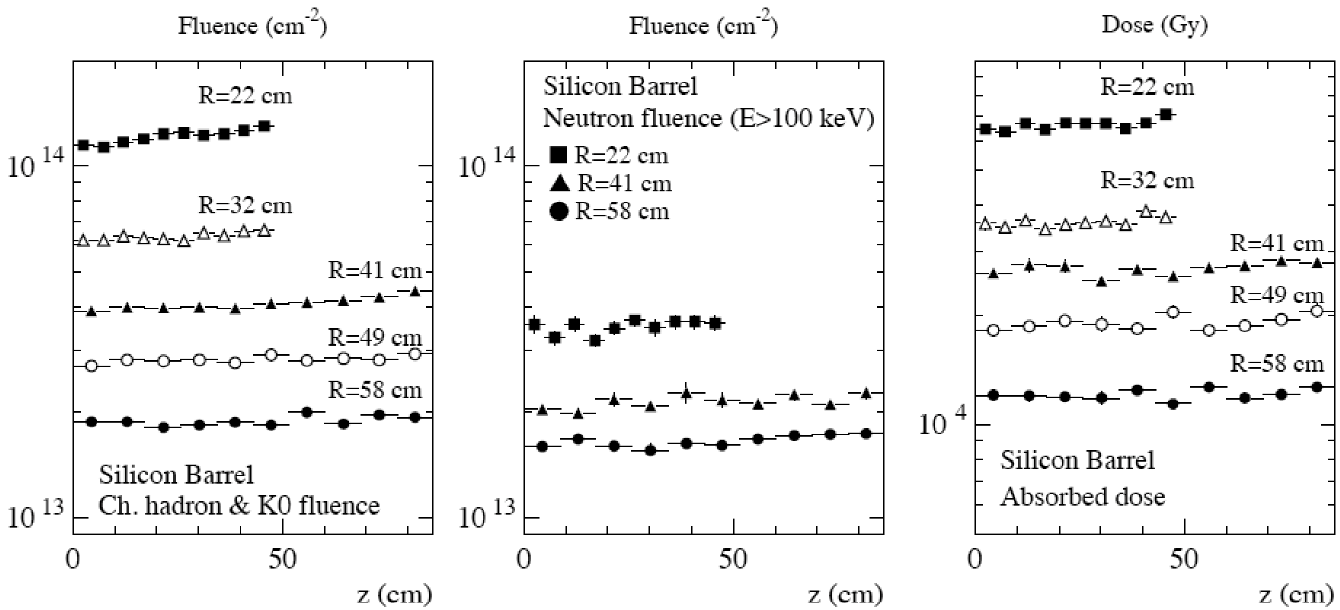
- Where we should try hard
  - May be only way to improve tracking performance
- Aggressively minimise material
  - Optimise layout and mechanics
    - Support structure and PCBs
    - Cooling pipes and thermal contacts
- Minimize power dissipation, optimise:
  - Layout, granularity
  - Front-end functionality
  - Data transfer inside TK
  - Use of data link capacity
    - Data concentrator needed?





Tracker Environment

- Expect to be able to scale up factor 10 total from LHC estimates of radiation levels
- Will still need to run cold to avoid reverse annealing (<0°C)
  - and possible thermal runaway
- CMS Magnet to remain at 3.8T



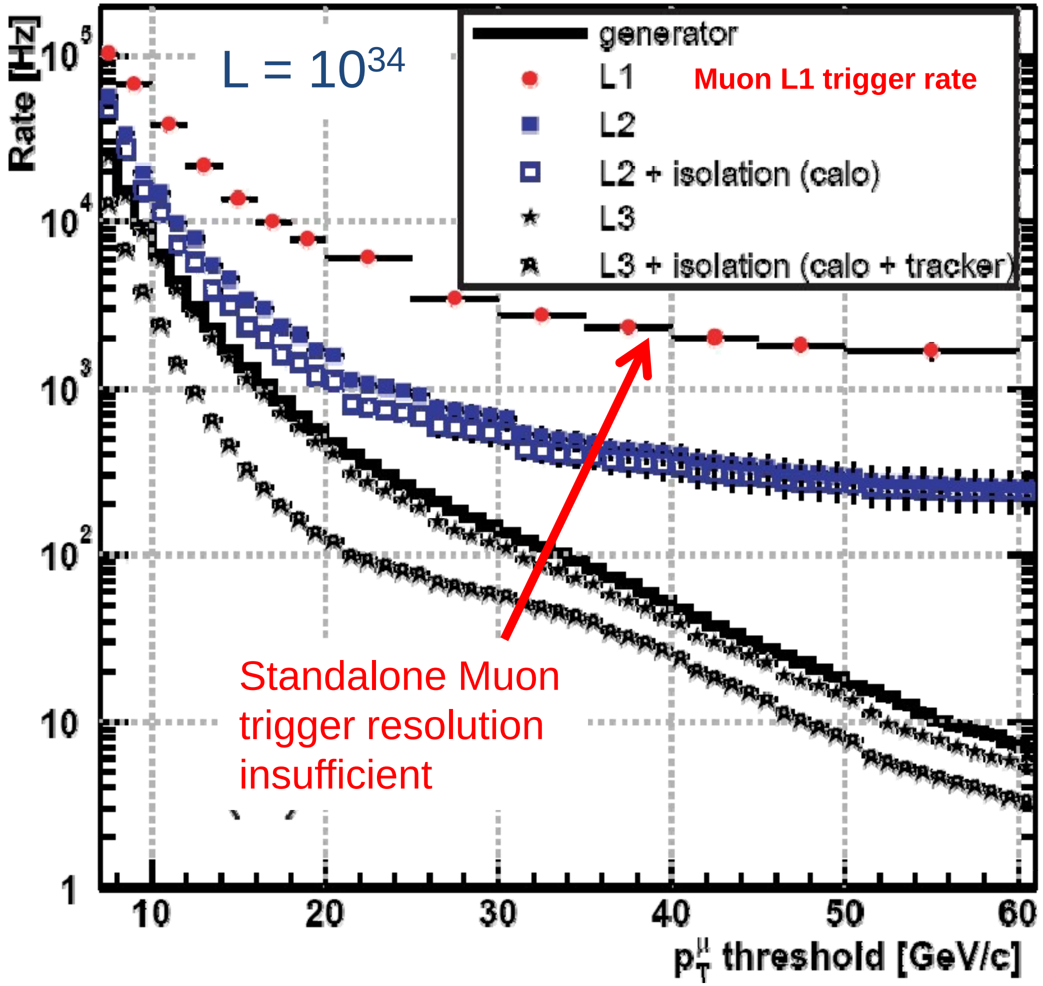
Fluences and doses after $500fb^{-1}$ (LHC lifetime)
Totals are factor 10 higher at SLHC
Inner layers dominated by ~200MeV pions
M. Huhtinen, CMS TK TDR, 1998

Detector will be, like now, inaccessible once installed
Need lifetime of parts to be qualified for 10yrs operation in this environment.
Deep QA Programme needed. COTS issues will resurface.
Must apply ALARA principles to upgraded TK installation.

SLHC Track-Trigger requirements

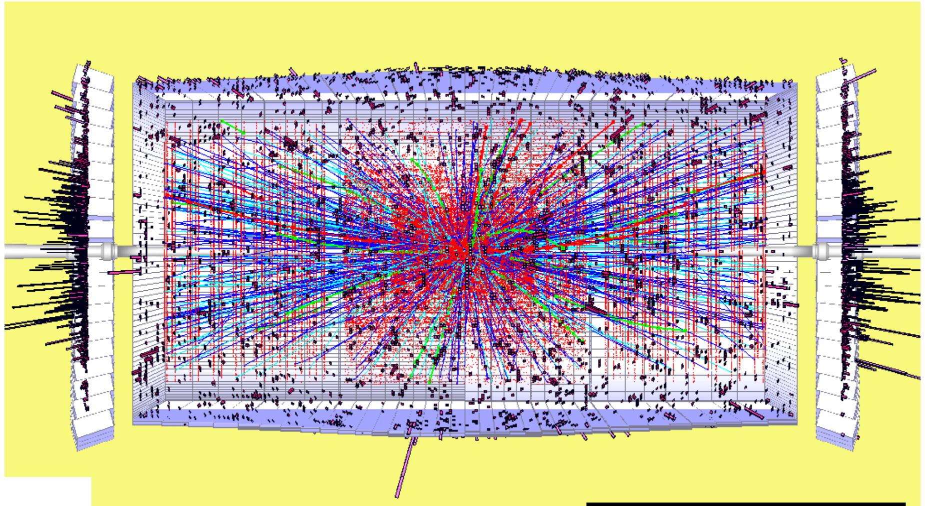
SLHC: Track Trigger Requirement: Muons

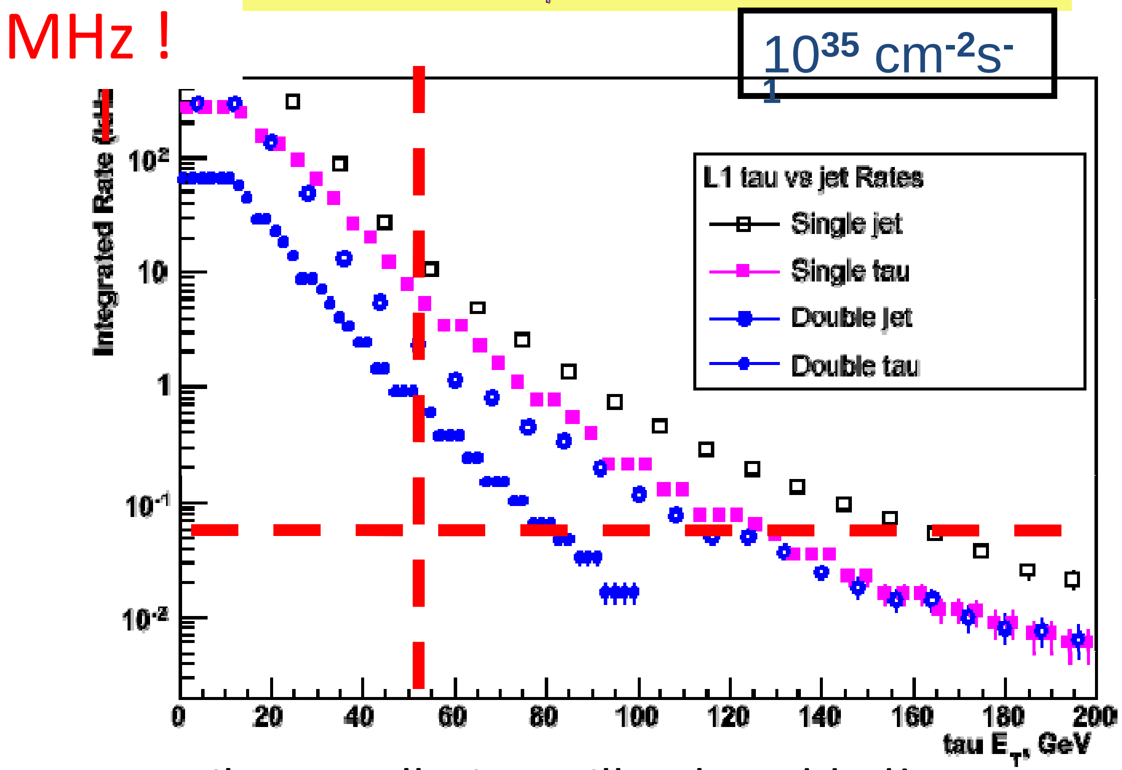
- Standalone L1 muon rate too high at $10^{35}cm^{-2}s^{-1}$
- HLT currently brings in TK info, giving efficient P_T discrimination
- TK should provide info in L1
  - trigger primitive up to η=2.5
  - high P_T track 'stub' at precise η, ϕ
    - To see if 1 or 2 doublet layers suffice



SLHC: Track Trigger Requirement: e, τ

- Normal isolation cuts will not work
  - Problem of combination of backgrounds plus pile-up
    - jet rejection against τ lost
    - fluctuations in pile-up fake τ !
- e/γ QCD backgrounds
  - ECAL trigger towers never empty
- Need primary vertex info, plus tracks > ~1GeV to recover isolation cut
- Hundreds of primary vertices!





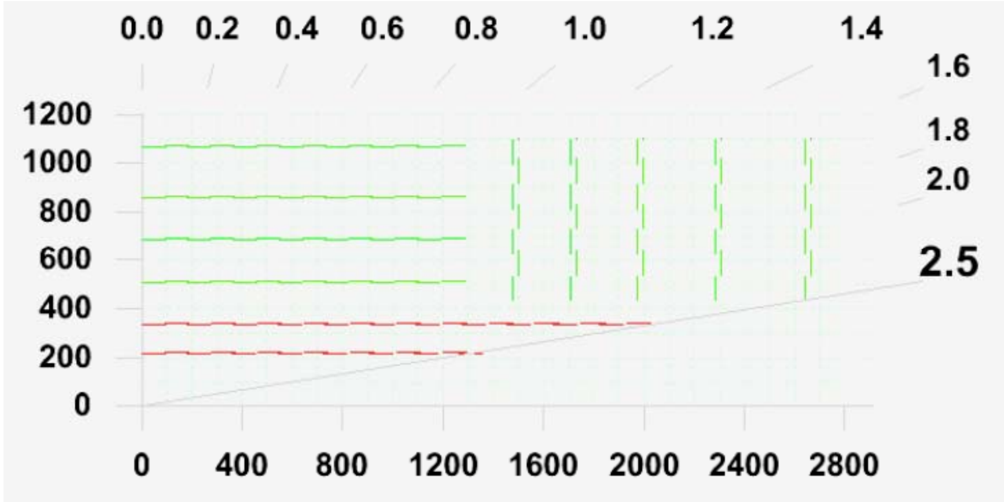
Pile-up pollution still to be added!

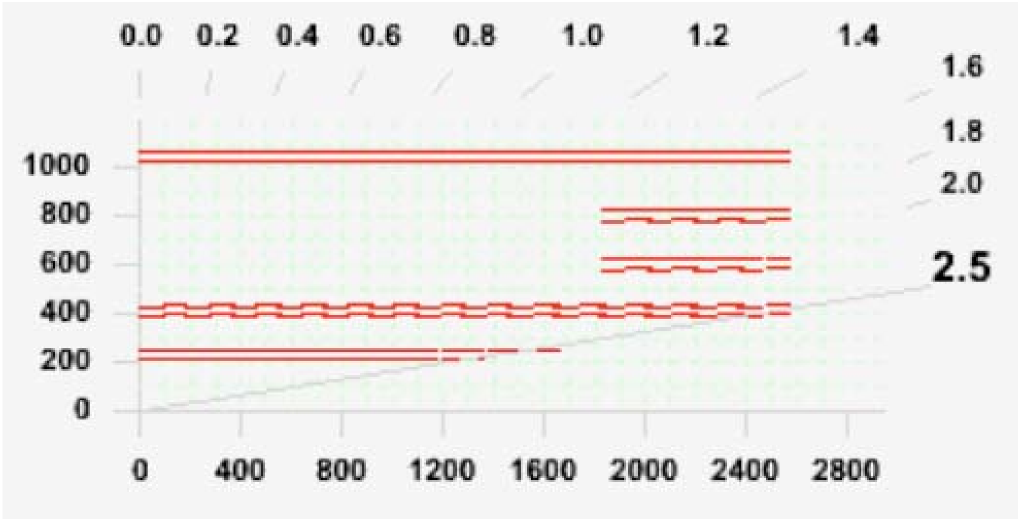
Track-Trigger impact on Outer TK system

- The location and geometry of the "P_T layers" have to be integrated into the layout of the 'outer' Tracker
  - These layers the most challenging
  - Will require very dense services: power, cooling, readout
  - Note, P_T layers should also contribute to 'regular' tracking
- Number of dedicated P_T layers and their position within the "outer Tracker" being studied
  - Layout, Simulation and Trigger Task Forces

- Strawmen under study (besides development of the study tools, already a lot of work in itself)
  - Full η coverage
    - Long-barrel PT layers
      - 2x2 layers at ~20cm, 30cm radii
    - Full long barrel outer tracker of stacked triggering layers (FNAL strrawman geometry)
- Outer barrel only
  - Stacked layers (several ideas)
  - Cluster size method

- Aim to converge on best geometry
  - providing the needed rejection at L1
  - Other criteria good tracking performance (power, material budget), costs, and challenges





http://abbaneo.web.cern.ch/abbaneo/tkgeometry/summaries/

Layout geometry tool

- Produce layouts from parameter set
  - Size, pitch, radii, …
- Calculates occupancy, power estimate
- For a given architecture estimate readout bandwidth
- Rough cost estimate
- Material budget to be added soon to tool

Modules

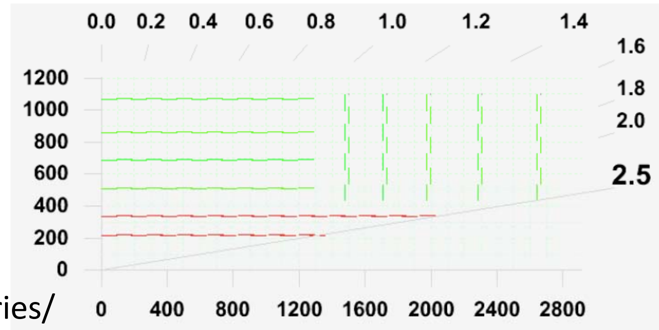
	B_1	B_2	B_3	B_4	B_5	E_7	Total
Tag	PTBARRELL1	PTBARRELL2	TOBL1	TOBL2	TOBL3	ENDCAPR7	
Type	pt	pt	rphi	rphi	rphi	rphi	--
Area (mm^2)	8580.5	8580.5	--	--	--	--	**26.9(m^2)**
Area (mm^2)	--	--	8580.5	8580.5	8580.5	8516.7	**87.7(m^2)**
Occup (max/av)	0.7/0.3	0.3/0.2	4.3/3.4	2.4/2.1	1.5/1.4	1.4/1.3	--
Pitch (min/max)	90	90	120	120	120	108/119	--
Segments x Chips	48x8	48x8	2x6	2x6	2x6	2x6	--
Strip length	1.9	1.9	46.3	46.3	46.3	48.7	--
Chan/Sensor	49152	49152	1536	1536	1536	1536	--
N. mod	512	1056	1120	1344	1680	760	**12640**
N. sens	1024	2112	1120	1344	1680	760	**13408**
Channels (M)	--	--	1.72	2.06	2.58	1.17	**17.01**
Channels (M)	50.33	103.81	--	--	--	--	**154.14**
Power (kW)	5.0	10.4	1.0	1.2	1.5	0.7	25.6
Cost (MCHF)	17.6	36.2	3.8	4.6	5.8	2.6	88.9

Cost estimates:

Pt modules: 200.0 CFH/cm2 - Strip modules: 40.0 CHF/cm2

Power estimates:

Pt modules: 0.10 mW/chan - Strip modules: 0.60 mW/chan



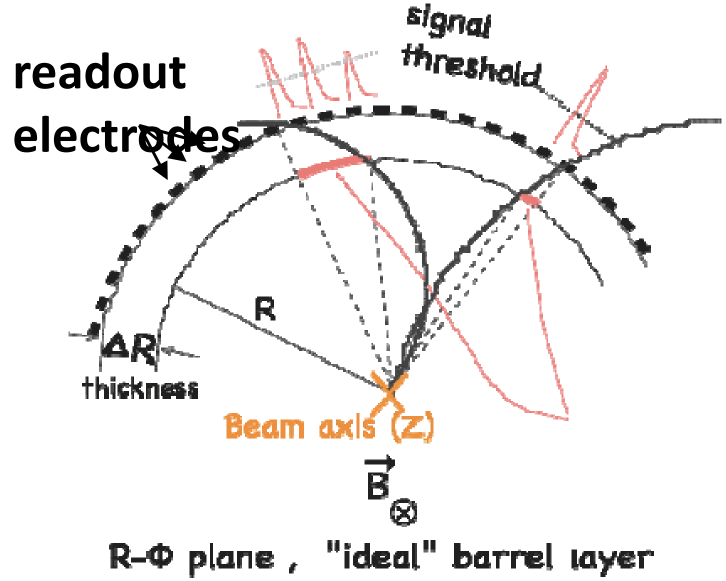
http://abbaneo.web.cern.ch/abbaneo/tkgeometry/summaries/

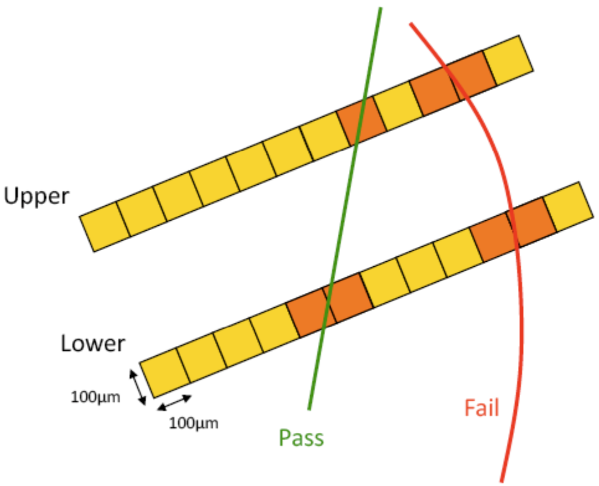
P_T-layer approaches

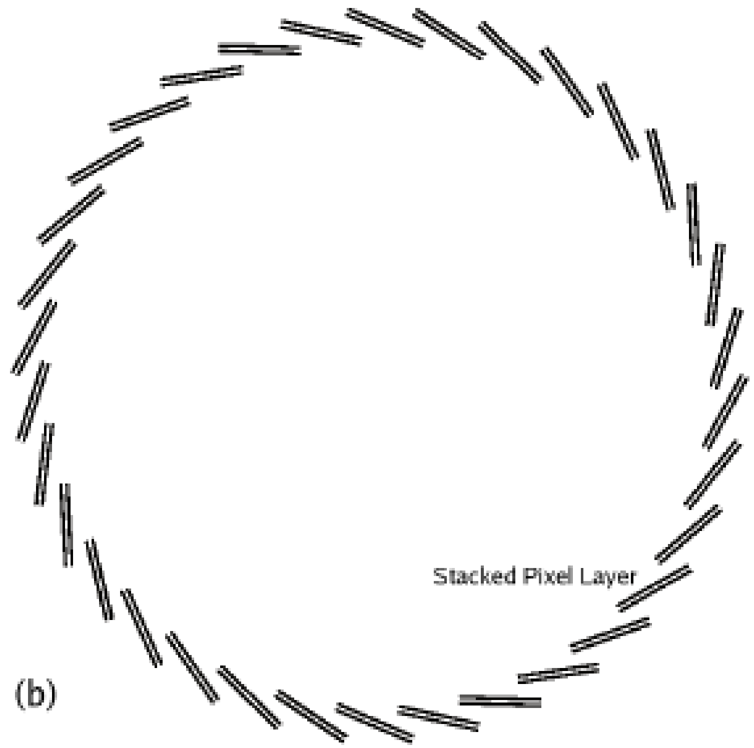
- Limited number of proposals so far
  - try to send reduced data volume from detector for further logic
  - eg factor 20 with p_T > few GeV/c

- (A) Use cluster width information to eliminate low p_T tracks (F Palla et al)
  - simple but thinner sensors may limit capability

- (B) Compare pattern of hits in closely spaced layers
  - p_T cut set by angle of track in layer







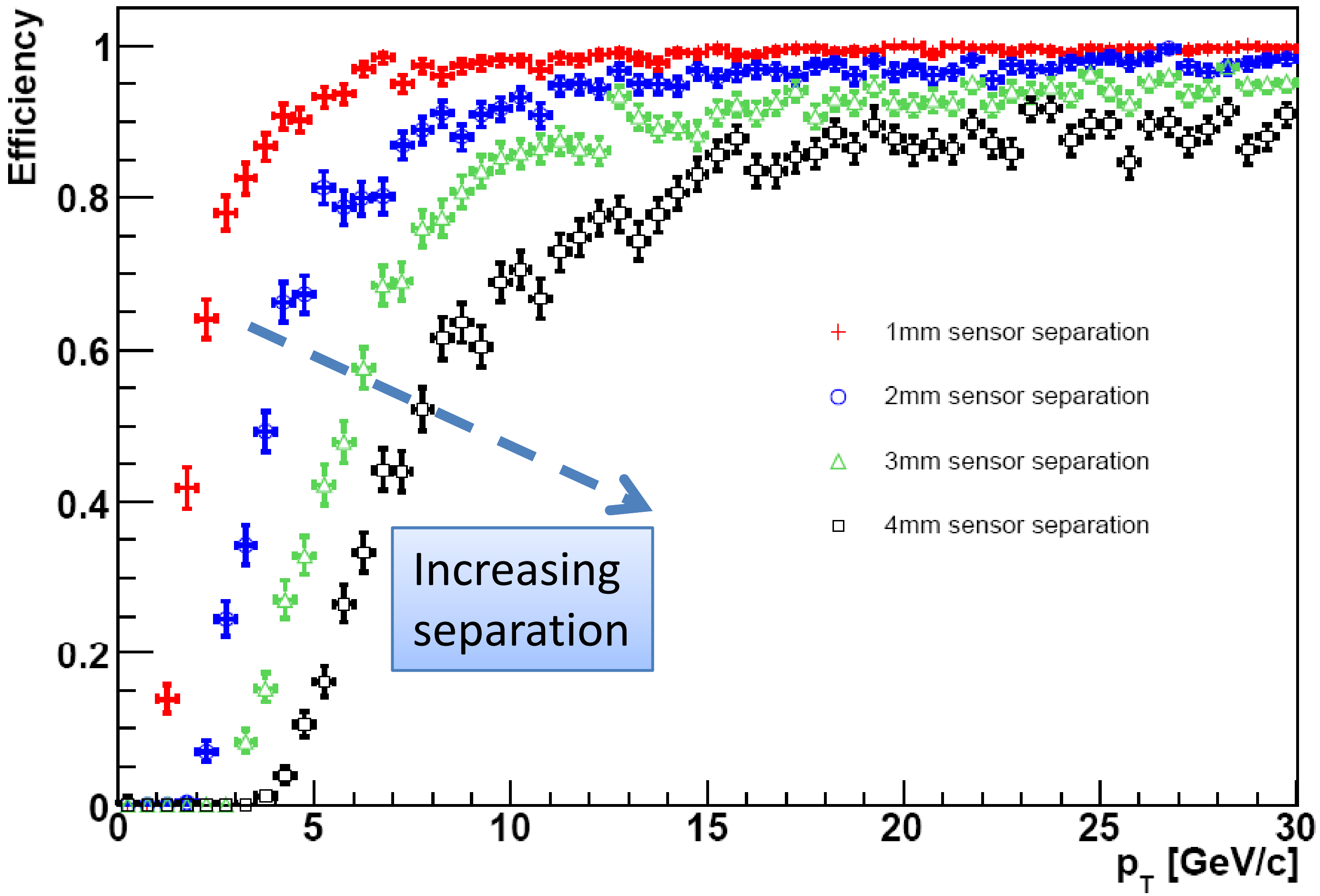
Stacked Layer Algorithm Performance

Sensor separation is again an effective cut on p_t

Again, the width of the transition region increases with separation.

Due to:
- pixel pitch
- sensor thickness
- charge sharing
- track impact point

Efficiencies decrease with sensor separation due to the larger column window cuts – sensor acceptances and fake containment are issues



p_T discriminating performance of a stacked layer at r=25cm for various sensor separations using 10,000 di-muon events with smearing

Cuts optimised for high efficiency:
Row window = 2 pixels
Column window = 3 pixels @ 1mm, 2mm; 4 pixels @ 3mm; 6 pixels @ 4mm

Architecture for Track Trigger system

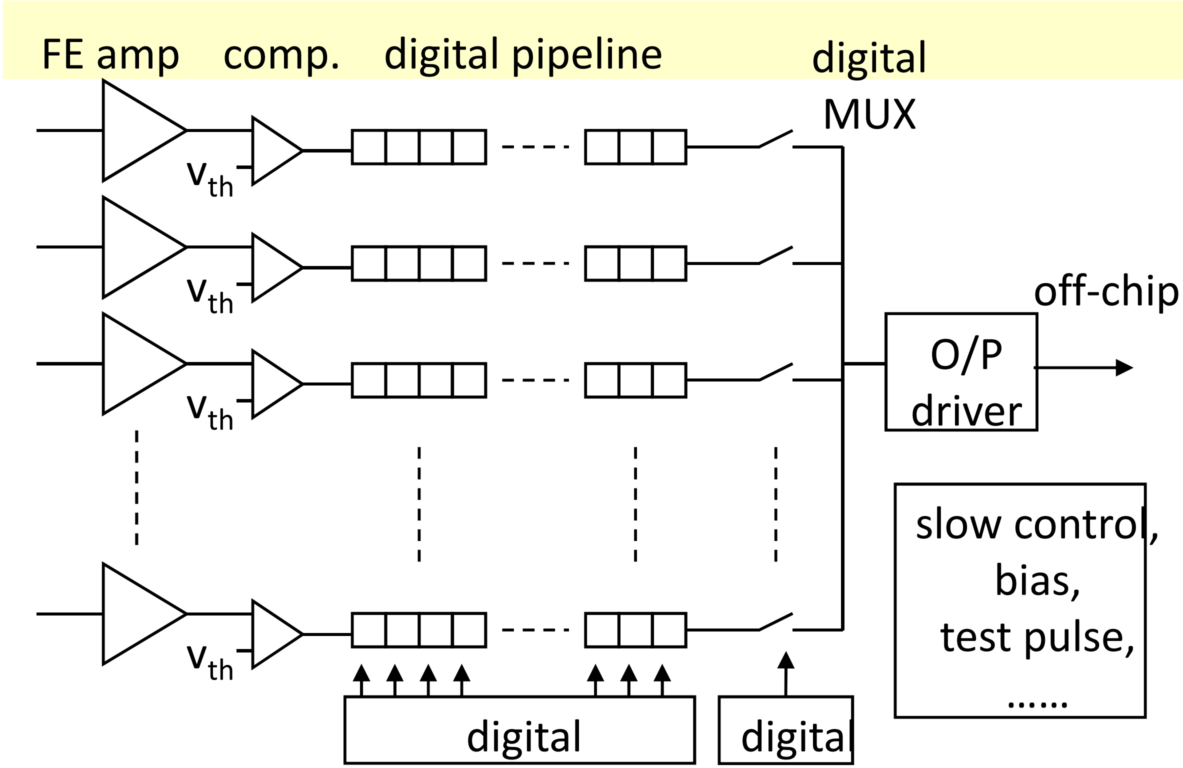
- Must respond quickly to every (40MHz) bunch crossing with signal to L1 with minimal latency and dead time
  - Expect to be binary, sparsified
- Correlator ASICs needed near front-end
  - Position to be decided (heat removal, powering…)
  - Must be programmable to cover different configuration needed for different locations in detector
- How many high speed optical links needed?
  - For two barrel doublets up to η=2.5
    - Estimated to be ~200 candidate stubs (~1% of tracks, plus fakes) to be readout each 40MHz
    - How to gather gather and multiplex data into link branchs (eg GBT 80MBit/s branches)
- If >1 doublet stack used, make inter-stack correlation of track-stubs to back-end?
  - Save power, keep flexibility, profit from reduced development time
- Generate signals efficiently from both isolated high P_T tracks and high P_T tracks in jets
- How to get out 'regular' tracking data from same layers
  - 100kHz readout
  - Maybe only need to readout one layer of a doublet
  - Favouring binary, unsparsified for rest of system
  - Try to match trigger layers 'standard' readout with rest of detector?
  - Try to use same TTC, slow control system as rest of Tracker

Progress on ‘standard’ Outer Tracker readout architecture

Outer readout

- Recall present architecture
  - analogue, unsparsified, analogue optical links, synchronous
  - external digitisation, cluster finding, zero suppression
  - 0.25μm CMOS, FP edge-emitting lasers, single-mode fibres
- Pros
  - works extremely well and easy to use with excellent diagnostic capability and noise robustness
  - occupancy insensitive – few power fluctuations
  - synchronous system easy to model and understand
  - cost effective, despite customisation
- Possible cons for future
  - Not enough bandwidth at front-end, new optolinks TX and RX required – analogue not an option
  - if analogue information to be preserved, on-detector ADC

binary architecture – un-sparsified



what about binary un-sparsified?

much simpler than "digital APV"
particularly for pipeline and readout side

need fast front end and comparator
=> more power here

but no ADC power and simpler digital functionality will consume less

allows retention of features we like

simpler synchronous system
no FE timestamping
data volume known, occupancy independent
(so no trigger-to-trigger variation)

but less diagnostics (can measure front end pulse shape on every channel in present system
some loss of position resolution, common mode immunity)

binary, un-sparsified is an option we are considering

Readout: Operating Requirements

- Trigger rate up to 100kHz
  - Latency = 6.4us (ECAL chip buffer size)
  - Trigger rules and coding ?
- Bigger event size
  - More bandwidth needed at backend for transmission to global DAQ (FED output)
- Run Control/Configuration
  - Start-up, re-start configuration should be fast (~minute whole system)
  - Synchronization (internal to Tracker then adjust global phase?)
- Straightforward scalability from small to large systems
  - Ability to use substitute parts to reduce costs, e.g. electrical links on test benches rather than optical where appropriate
- Monitoring
  - Want to have simple interfaces and functions to monitor state of system and correct functionality, e.g
    - Slow control
    - Emulator
    - Spy channel
    - DQM

The role of monolithic detectors

- Can they be major contributors to new Tracker?
- Pros
  - a single concept providing tracking and trigger functions would be easier to build a common effort around
- Cons
  - the technology is unproven and unlikely to mature rapidly
  - there are many unknowns which will require time and effort
  - the R&D cost may be high, since deep sub-micron processes
- If good progress could be shown in ~2 years, it will not be too late to review the tracker design
  - significant power or functional advantages would be a strong motivation to adopt a new technology, even if late

Conclusion

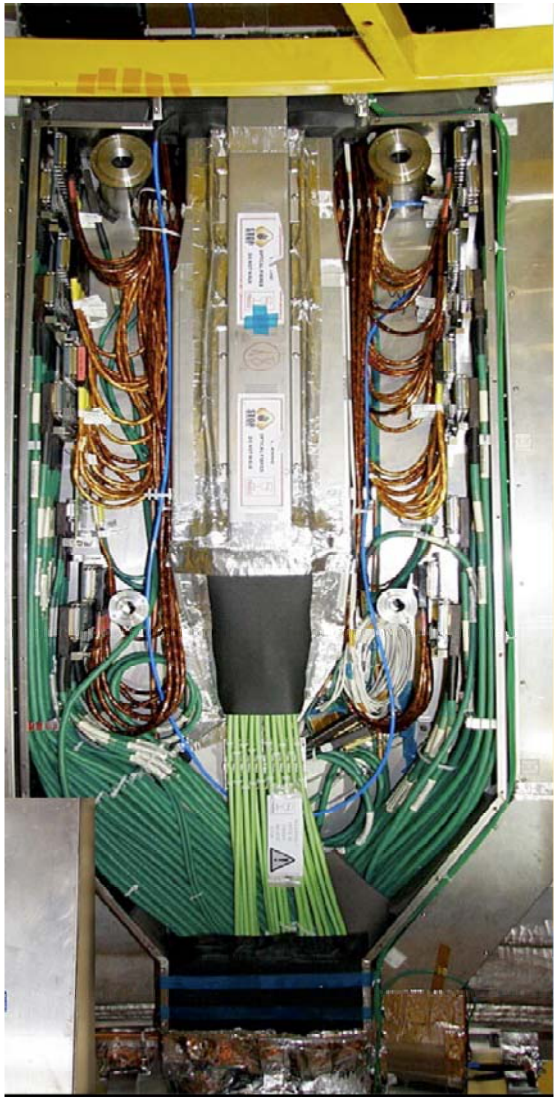
- Upgrade to CMS Tracker will be again a complex, long project on a large scale
  - Additional challenge of the operating environment
  - New requirement for triggering functionality
  - Must profit from lessons learned, feeding these back into Requirements, Specs, QA Programme, budgets, plans…
    - Aim to obtain functionality with good margin whilst aiming for high yield for minimum power, material, costs (including spares)
- Requirements definition for CMS SLHC Tracker very much a work in progress
  - Some requirements we have to wait for Physics
    - e.g. radiation environment, occupancy, physics requirement
  - Track trigger efforts gathering momentum
    - iterate between simulations and layout tool
    - Iterate between TK and CMS (Trigger, Physics and other subdetectors)
- Good progress on outer Tracker readout architecture
  - Favouring synchronous binary, un-sparsified readout
    - Simplicity here should free up resources for other work needed

Extra slides

TK Connections inside CMS detector

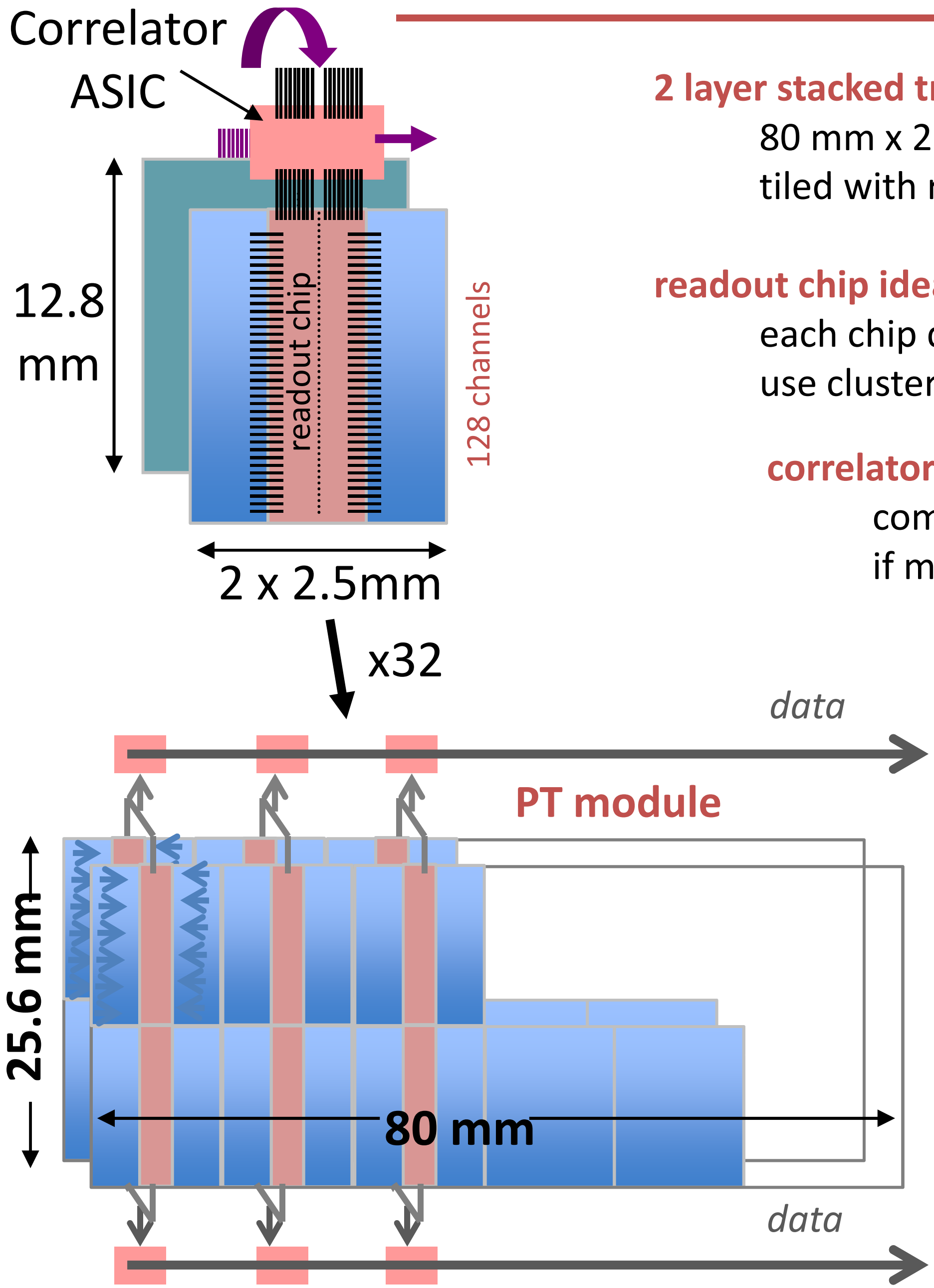
- Integration inside CMS detector volume (YB0)
  - Tracker PP1 patch panel, 2x16
    - ~ 90 power/control cables, 20 multi-ribbon fibre cables, 12 Cu pipes
  - PP1 are permanent fixtures, as are cables from PP1 outwards
- To complicate matters, many ancillary systems in all PP1s
    - Environmental Sensing, Heater wires, Dry air, Cable channel water
  - Plus, in ‘special PP1s’
    - Pixels services, BCM, PLT, Laser Alignment, Thermal screen
- Also Endcap (TEC) connections at TK bulkhead to work on

- Complicated situation raises ALARA concerns for future
  - 3 months to connect
  - Has to be disconnected carefully (since re-using services)
- Have documented all connections and have a PP1 mockup
  - How will different teams manage in ~10 years time.
- Must purchase (soon?) stock of new connectors
  - MFS for fibres, custom electrical connections



G Hall, M Pesaresi
M Raymond

possible PT module for inner layer



2 layer stacked tracking approach

80 mm x 25.6 mm sensors segmented into 2.5 mm x 100 µm pixels
tiled with readout chips – could be wire bonded for easy prototyping

readout chip ideas *(see *)*

each chip deals with 2 x 128 channel columns
use cluster width discrimination to reduce data volume

correlator

compares hit pattern and address from both layers
if match then shift result off-detector

data volumes

need to transmit all correlated hit patterns every BX
predicted occupancy + reduction from correlation
=> 1 link can serve 2 PT modules

link power

need ~ 3000 PT modules for 3m length cylinder, r=25cm
so 1500 links (@2.56 Gbps) => **3 kW** @ 2W / link

readout power

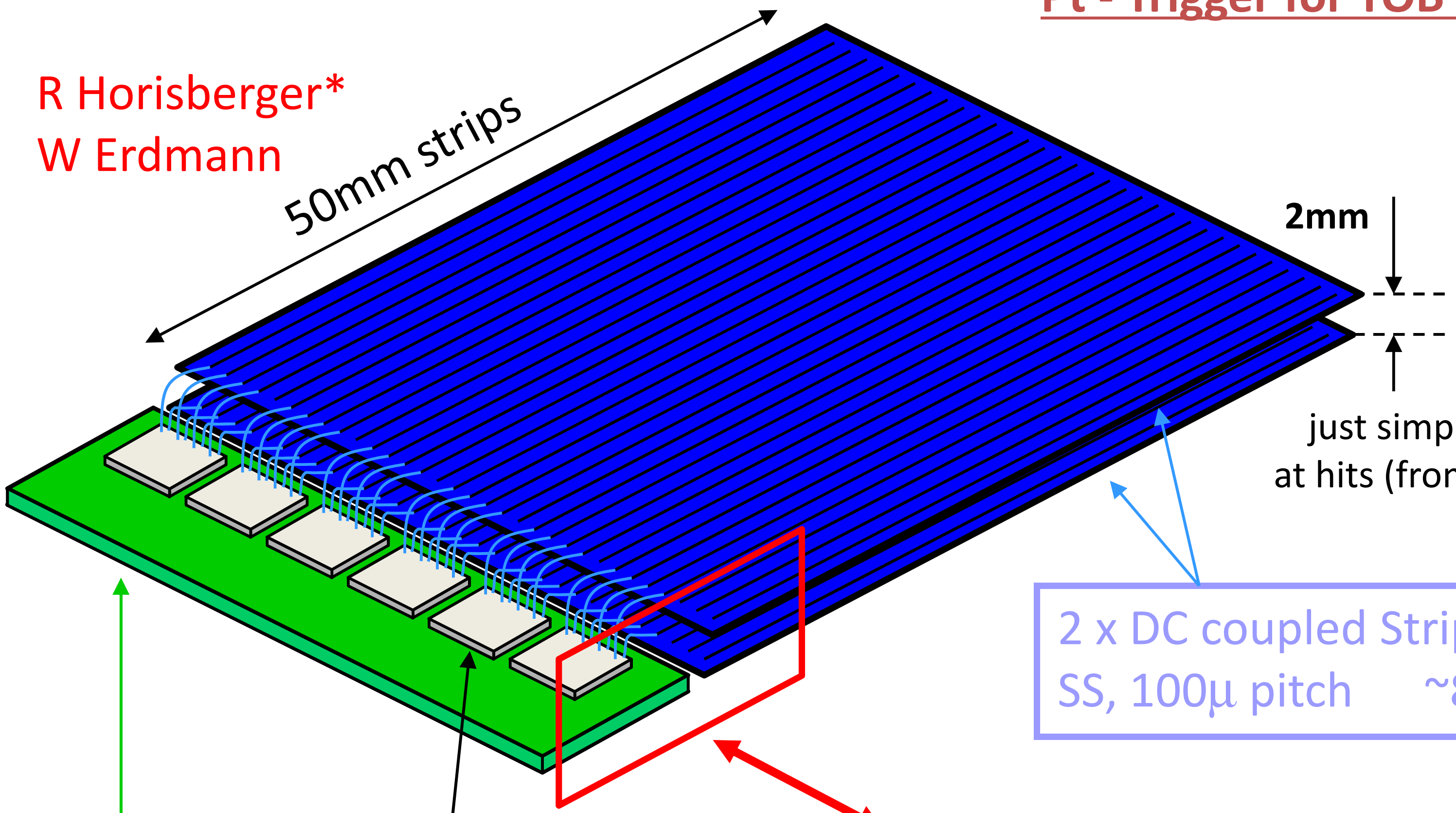
50 µW / pixel (extrapolate from current pixels)
=> **2.4 kW** for 8192 x 2 x 3000 channels

=> **this will not be a low power layer**

http://indico.cern.ch/getFile.py/access?contribId=15&sessionId=2&resId=1&materialId=slides&confId=36581

Pt - Trigger for TOB layers

R Horisberger*
W Erdmann

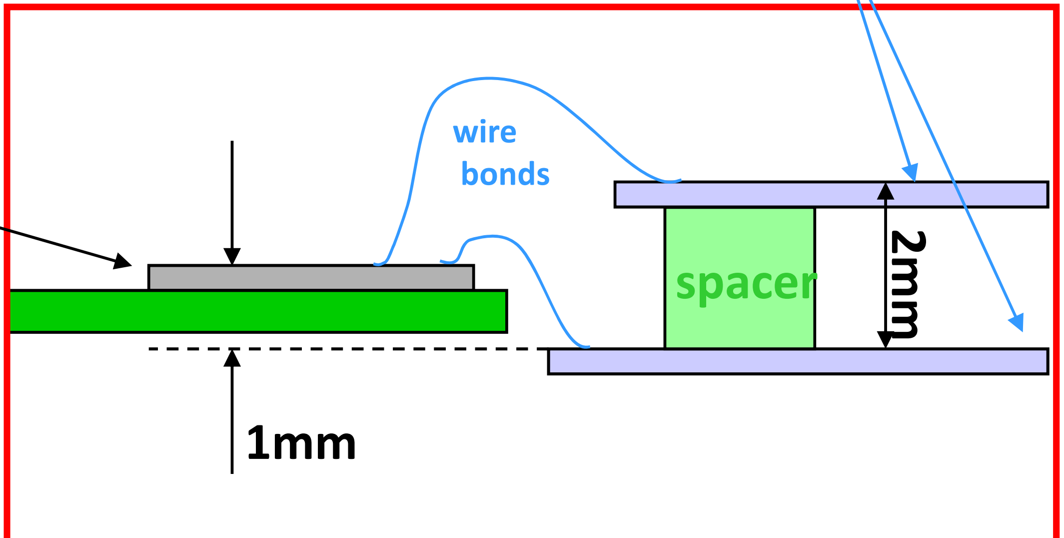


Two-In-One Design
bond stacked upper and lower sensor channels to adjacent channels on same ASIC
no interlayer communication
no extra correlation chip
just simple logic on readout chip, looking at hits (from 2 layers) on adjacent channels

2 x DC coupled Strip detectors
SS, 100µ pitch ~8CHF/cm^2

Strip Read Out Chip
2 x 100µ pitch with
on-chip correlator

Hybrid



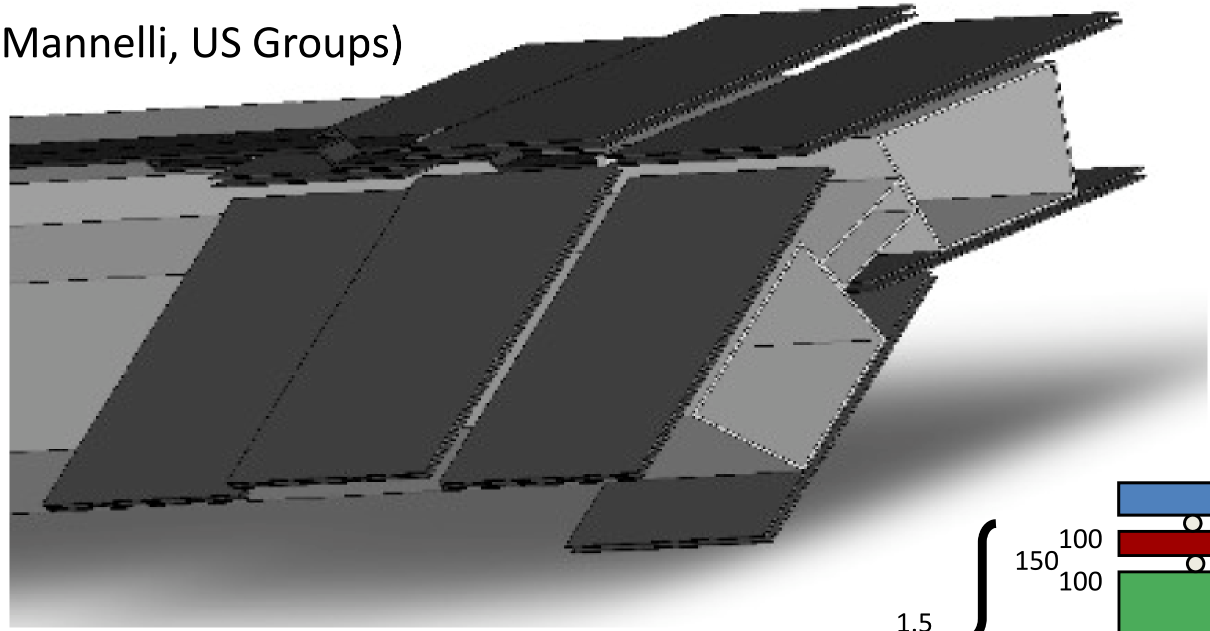
track angular resolution ~20mrad

→ good P_t resolution

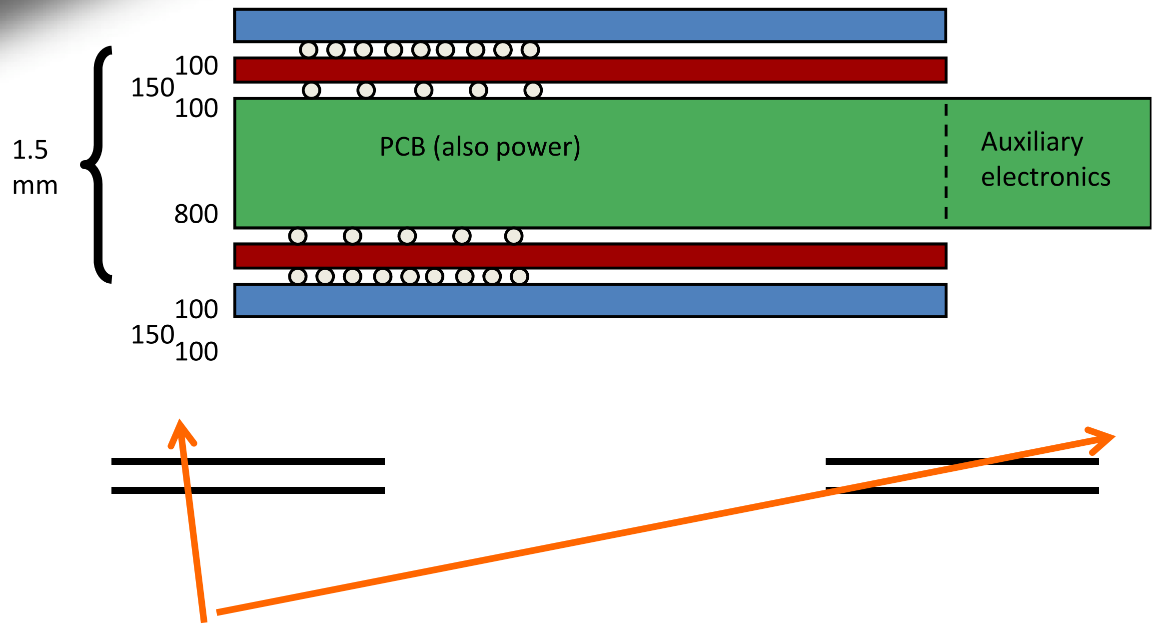
* *http://indico.cern.ch/getFile.py/access?contribId=3&sessionId=0&resId=0&materialId=0&confId=36580*

Other approaches to stacked layers

(M. Mannelli, US Groups)



(A. Marchioro)



Transmission top-bottom as effective as possible

PCB covers 100% of the sensor surface

Need correlation capability to cover z displacement

Barrel layers only

estimated link power contribution

no. of chips / link depends on estimations of data volume – some details in backup slides

	link speed	# of 128 chan. chips/link	power per link	link power/ sensor chan.
LHC unsparsified analog	0.36 Gb/s (effective)	2 / analog fibre	60 mW	230 μW
SLHC digital APV no sparsification	2.5 Gb/s	32 / GBT	~ 2W	490 μW
SLHC digital APV with sparsification	2.5 Gb/s	256 / GBT	~ 2W	60 μW
SLHC binary unsparsified	2.5 Gb/s	128 / GBT	~ 2W	120 μW

LHC unsparsified analog

230 μW / sensor channel: ~ 10% of overall channel budget
need to do better at SLHC (e.g. 10% of 0.5 mW = 50 μW)

SLHC digital APV without sparsification not viable

link power contribution too high (no. of channels will increase at SLHC)

SLHC digital APV with sparsification appears best

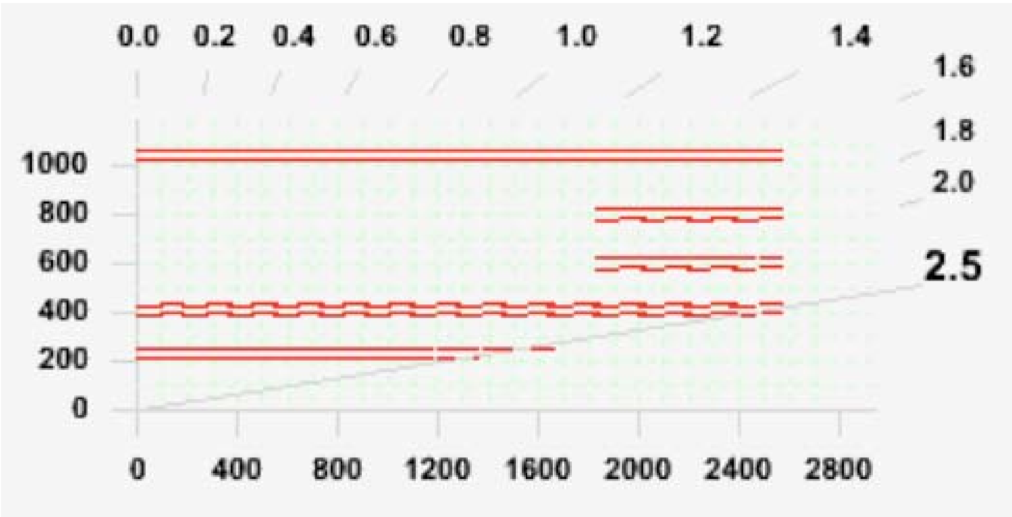
but can only be achieved with extra buffering between FE chips and link
more chips to develop, some additional power

SLHC binary unsparsified next best

has strong system advantages

Layout tool output (continued)

- Stacked layer long-barrel geometry
  - Strawman proposed at FNAL workshop, 11/2008



Layers and disks

Layer r	L1	L1	L2	L2	L3	L3	L1	L1	L2	L2
	270	231	450	410	1080	1040	640	600	840	800

Disk Z

Ring r

1

2

Modules

	B_1	B_2	B_3	B_4	B_5	Total
Tag	BARRELL1	BARRELL2	BARRELL3	SHORTL1	SHORTL2	
Type	pt	pt	pt	pt	pt	--
Area (mm^2)	8580.5	8580.5	8580.5	8580.5	8580.5	**288.7(m^2)**
Area (mm^2)	--	--	--	--	--	0.0(m^2)
Occup (max/av)	0.7/0.3	0.2/0.1	0.0/0.0	0.0/0.0	0.0/0.0	--
Pitch (min/max)	90	90	90	90	90	--
Segments x Chips	48x8	48x8	48x8	48x8	48x8	--
Strip length	1.9	1.9	1.9	1.9	1.9	--
Chan/Sensor	49152	49152	49152	49152	49152	--
N. mod	1400	3584	8512	1408	1920	**16824**
N. sens	2800	7168	17024	2816	3840	**33648**
Channels (M)	--	--	--	--	--	0.00
Channels (M)	137.63	352.32	836.76	138.41	188.74	**1653.87**
Power (kW)	13.8	35.2	83.7	13.8	18.9	165.4
Cost (MCHF)	48.1	123.0	292.1	48.3	65.9	577.4

Cost estimates:

Pt modules: 200.0 CFH/cm2 - Strip modules: 40.0 CHF/cm2

Power estimates:

Pt modules: 0.10 mW/chan - Strip modules: 0.70 mW/chan