Requirements of the ATLAS Strips at SLHC

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In behalf of the ATLAS Upgrade community

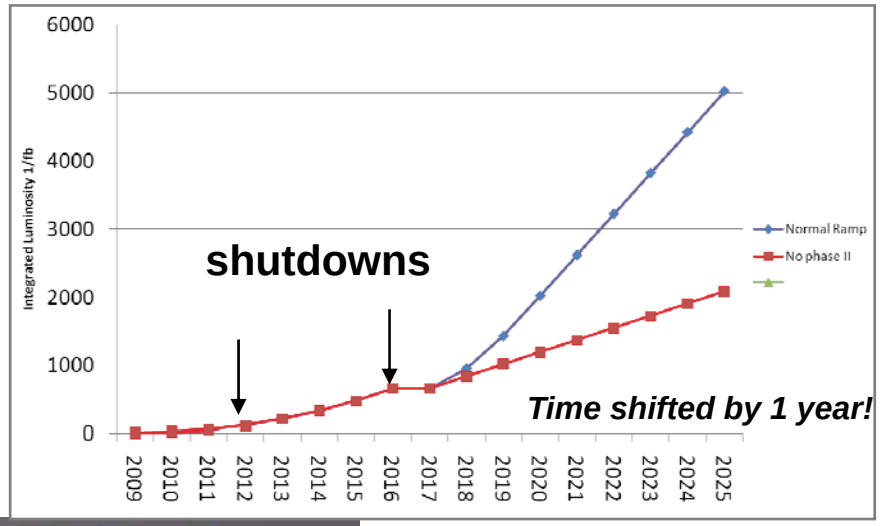
ACES09, 3-4 March 2009 at CERN

Outlines:

- Machine and detector upgrade plans
- Layout and challenges
- Module integration
- Silicon sensors & FE readout
- Powering schemes
- Readout architecture overview
- Service constrains
- Summary

Machine Scenario

Parameters	SLHC – Phase II	
	Scenario 1	Scenario 2
Bunch spacing [ns]	50	25
Proton/bunch Nb[10^{11}]	4.9	1.7
β* at IP1&5 [m]	0.25	0.08
Longitudinal profile	Flat	Gaussian
Rms bunch length σ_z[cm]	11.8	7.55
Peak luminosity [10^{34} $cm^{-2}s^{-1}$]	10.7	15.5
Effective luminosity (5h) [10^{34} $cm^{-2}s^{-1}$]	3.5	3.6
Peak events per crossing	403	294



Year	Normal Ramp Peak Lumi (x 10^{34})	Normal Ramp Annual Integrated (fb^{-1})	Normal Ramp Total Integrated (fb^{-1})	No phase II Peak Lumi (x 10^{34})	No phase II Annual Integrated (fb^{-1})	No phase II Total Integrated (fb^{-1})
2009	0.1	6	6	0.1	6	6
2010	0.2	12	10	0.2	12	10
2011	0.5	30	48	0.5	30	48
2012	1	60	108	1	60	108
2013	1.5	90	198	1.5	90	198
2014	2	120	318	2	120	318
2015	2.5	150	468	2.5	150	468
2016	3	180	648	3	180	648
2017	3	0	648	3	0	648
2018	5	300	948	3	180	828
2019	8	420	1428	3	180	1008
2020	10	540	2028	3	180	1188
2021	10	600	2628	3	180	1368
2022	10	600	3228	3	180	1548
2023	10	600	3828	3	180	1728
2024	10	600	4428	3	180	1908
2025	10	600	5028	3	180	2088

Collimation phase 2

Linac4 + IR upgrade phase 1

New injectors + IR upgrade phase 2

Radiation damage limit ???

Expected shutdowns:
- 6 to 8 months in 2012
- 18 months in 2016

B-Layer replacement

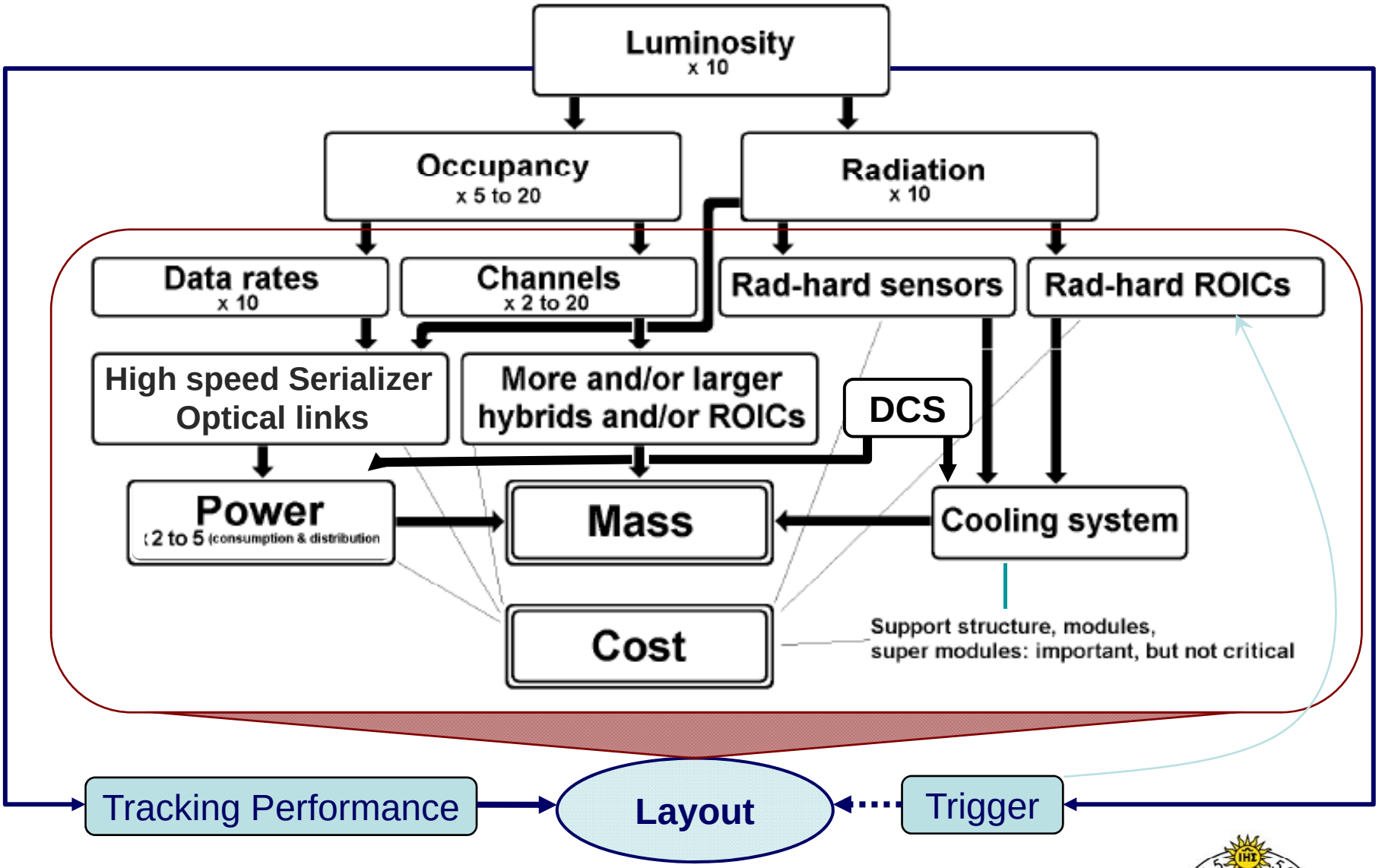
Detector Upgrade

Detector Upgrade Plan

- **Current ID is designed to survive ~600fb^{-1} integrated luminosity** expected for 2016
- **New ID is therefore planned** for installation/operation in 2018 with a higher yearly integrated luminosity of 600fb^{-1}
- **Many challenges and critical issues**: Under investigation for most of them
- **Schedule:**
  - End of 2009: Letter Of Intend
  - 2010: Technical Proposal
  - 2011: Costing and MOU by April and TDR by December
  - 2012: PRRs
  - 2017: Installation at the end of the year
- **Upgrade organization:** Executive bodies, Steering Group, Technical Coordination, Project Office and Working groups

The Upgrade community has to keep in mind the detector challenges at SLHC…

Challenges

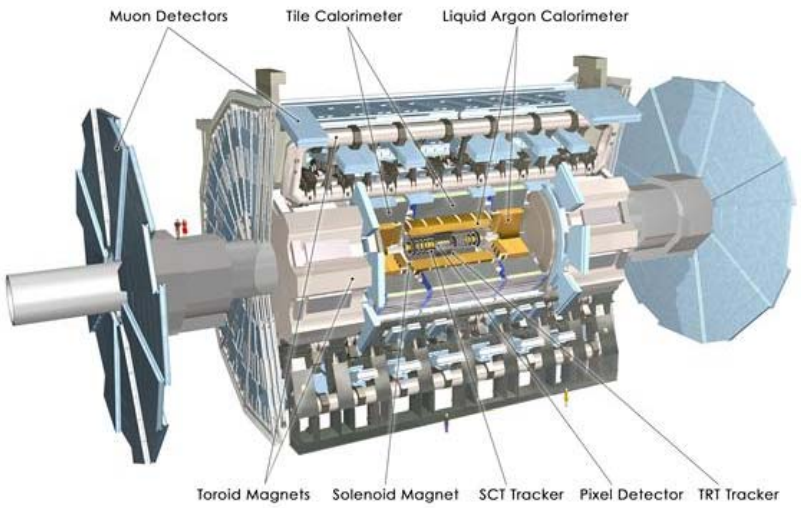

Luminosity
x 10
Occupancy
x 5 to 20
Radiation
x 10
Data rates
x 10
Channels
x 2 to 20
Rad-hard sensors
Rad-hard ROICs
High speed Serializer
Optical links
More and/or larger
hybrids and/or ROICs
DCS
Power
2 to 5 consumption & distribution
Mass
Cooling system
Cost
Support structure, modules,
super modules: important, but not critical
Tracking Performance
Layout
Trigger

Detector Upgrade Issues

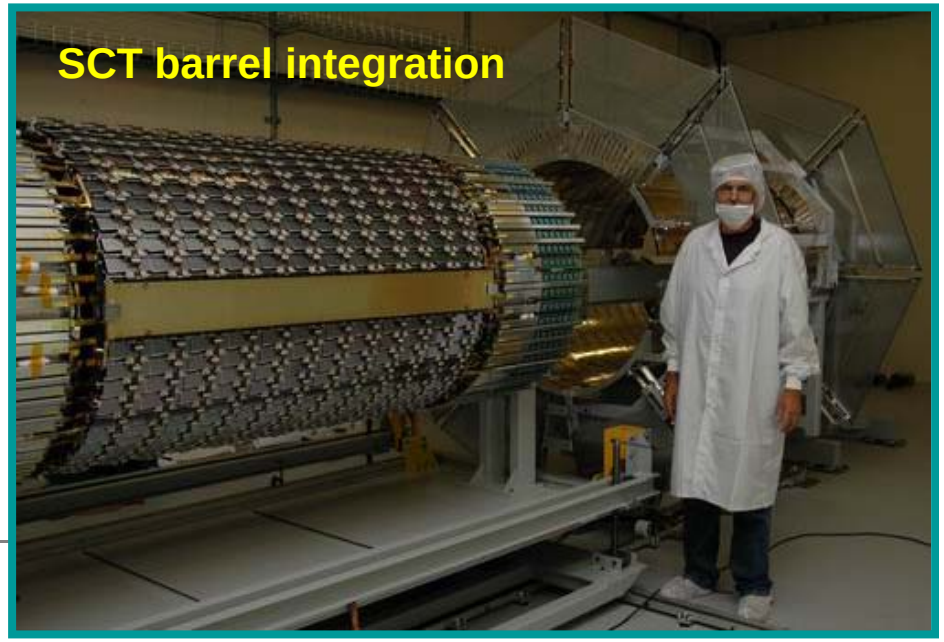
Topics under investigation for the tracker upgrade:

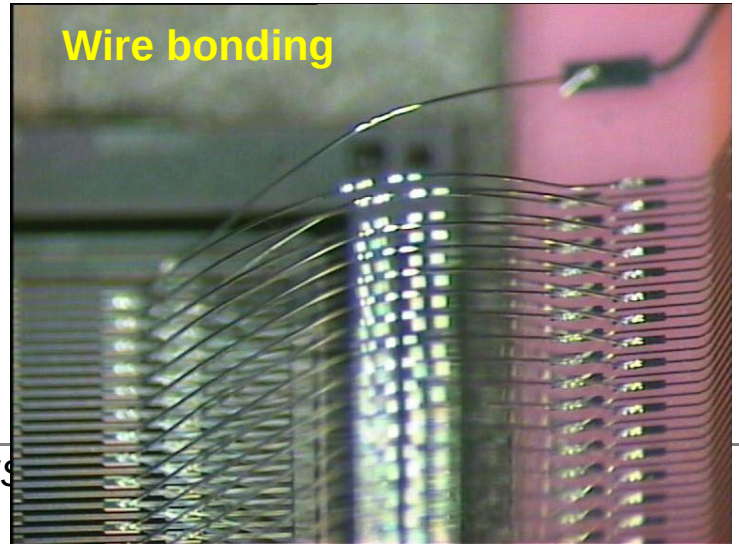
- **New ID layout:** Only silicon pixel and strip detectors ↔ Simulations
- **Trigger:** Need to workout on a TDAQ/Detector interface specification
- **New detector technology:** n-in-p planar for strips
- **New ASICs technologies:** Deep submicron 250 nm →130nm or 90 nm
- **Cooling with more headroom:** Silicon temperature below -20°C
- **New powering scheme:** Serial powering or DC-DC for parallel powering
- **Faster readout:** FE asics (160/320 Mbps) and optical link (5Gb/s)
  SCT 1.3 kch/link → Upgrade 123 kch/link
- **Module integration** will be grouped on a stave or a super-module structure
→ performances
- **DCS** is proposed to be partially integrated into the readout architecture
- **Engineering:**
  - Assemble and commission the complete ID in a surface building
  - Service reuse of cables between counting room and detector
- **Installation:** Limited access time inside the cavern

Strip Detector Today



~60 m2 of silicon installed today
→ 16 years from LOI to readiness!





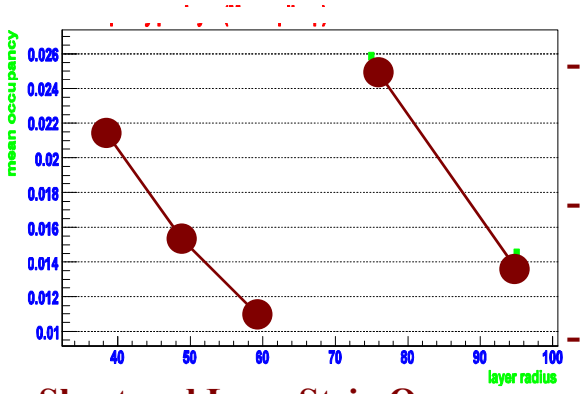
ID Upgrade Layout

Evolution of Strawman Layout since 2006 →
Fixed length barrel Stawman08

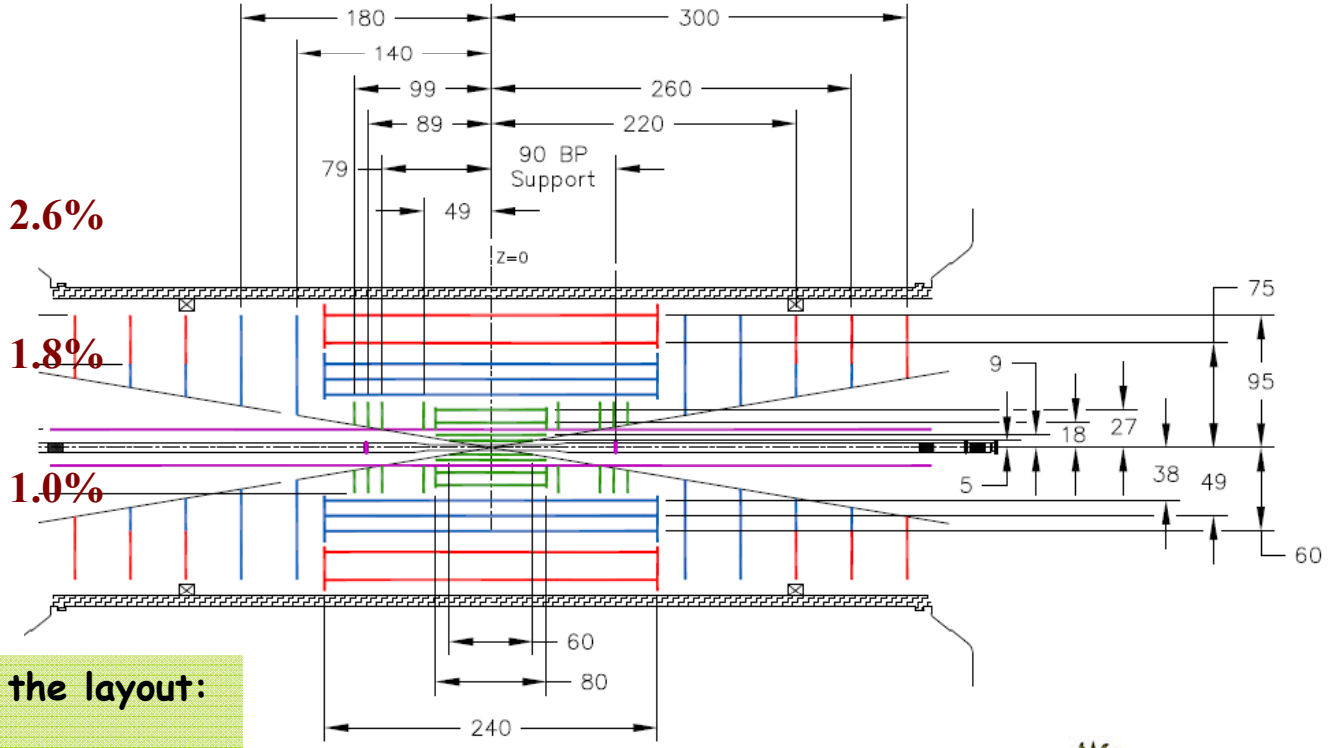
2 layers - long strips (~10 cm x 80 μm)
3 layers - short strips (~2,5/5 cm x 80 μm)
4 layers - pixels (0,2/0,4 mm

Including disks this leads to:
Pixels: 5 m², ~300,000,000 channels
Short strips: 60 m², ~30,000,000 channels
Long strips: 100 m², ~15,000,000 channels

V13—Fixed Length (Proposed)



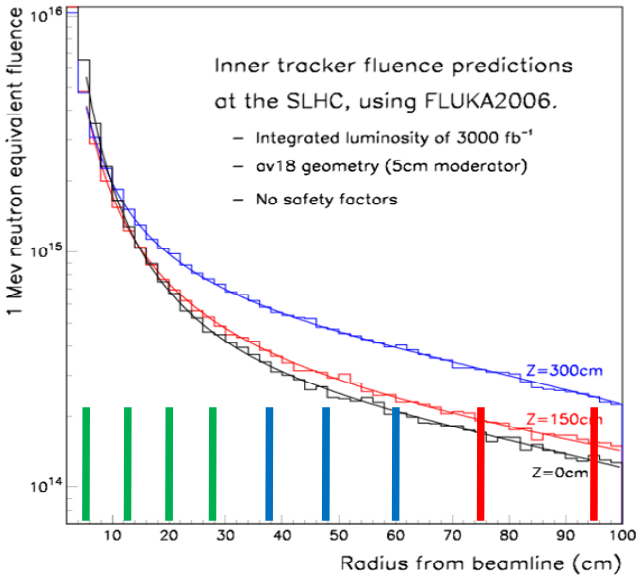
Short and Long Strip Occupancy (400/BCO)



Simulation G3, G4 should drive the layout:
- Reasonably low occupancy
- Good tracking efficiency, low fake rate

6 months Layout TF led by L. Rossi

Radiation Background in ID at SLHC



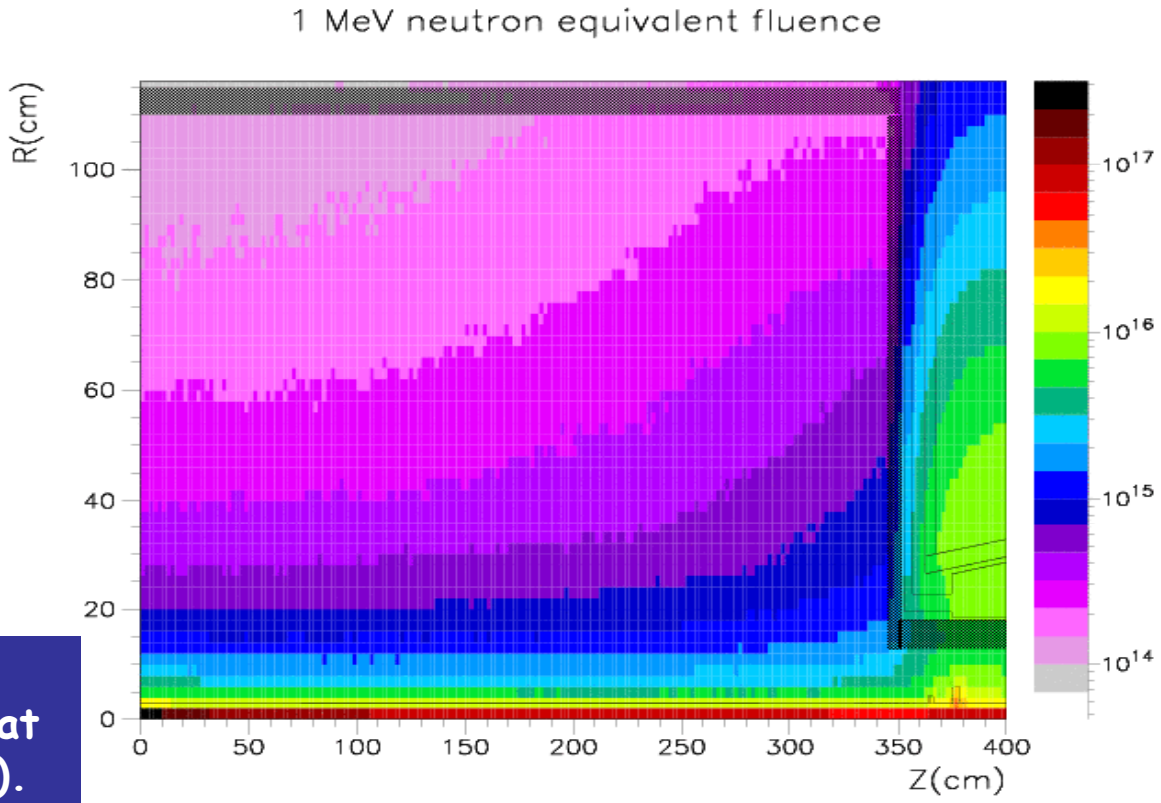
Issues

→Thermal management and shot noise. Silicon looks to need to be at less than -20°C (Thermal runaway).

Si power: 1W @ -20°C
4W @ -10°C
10W @ 0°C

→ High levels of activation will require careful consideration for access and maintenance.

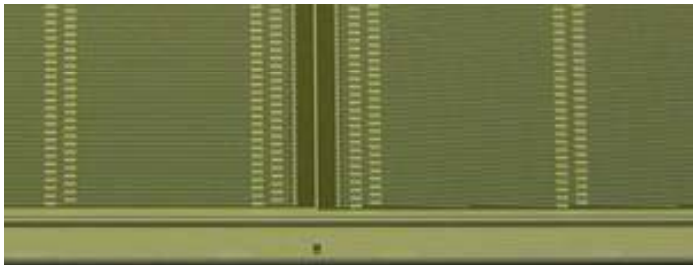
Simulation using FLUKA2006



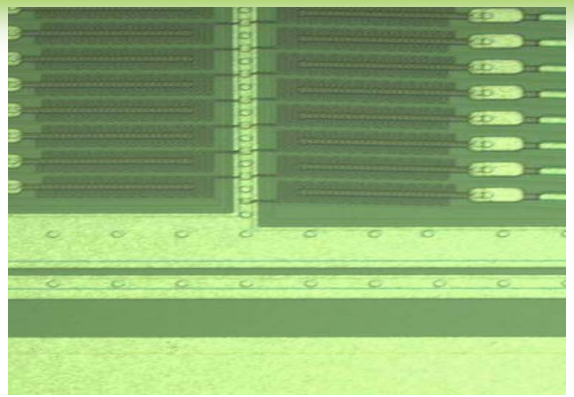
1 MeV equivalent neutron fluences assuming an integrated luminosity of 3000fb^{-1} and 5cm of moderator lining the calorimeters (reduces fluences by ~25%)

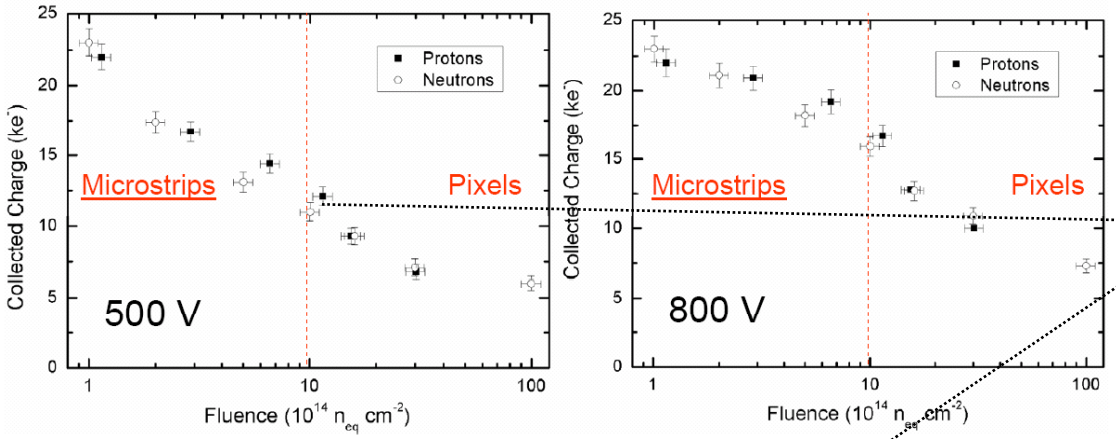
→ With safety factor of 2 Si-strip has to withstand 9.$10^{14} n_{eq}/cm^2$

Silicon Sensors

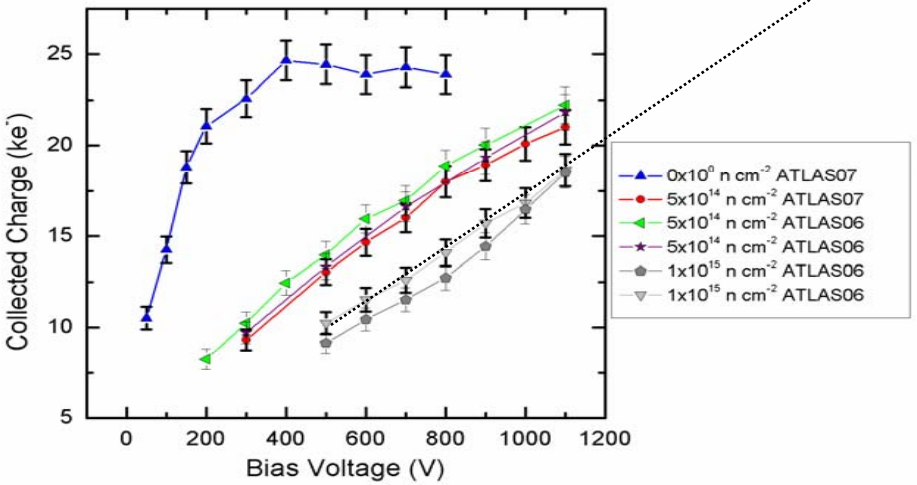


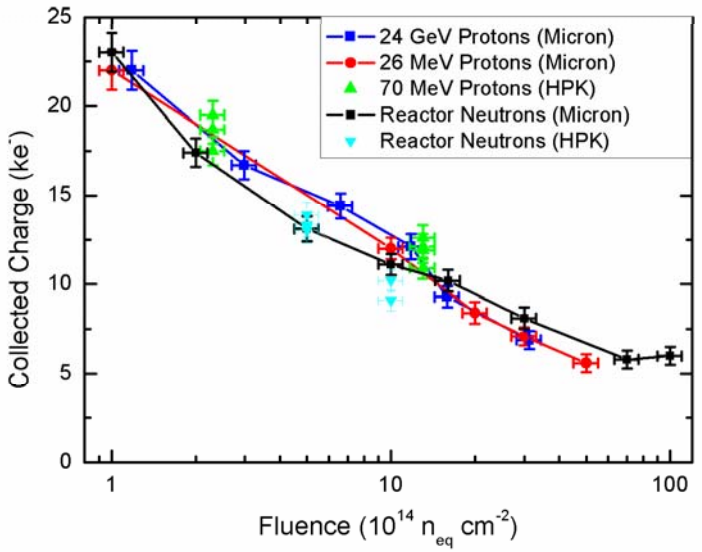
Hamamatsu ATLAS07
4 short strips: ~2.3 cm
20 mrad on 1side
Straight on the other side



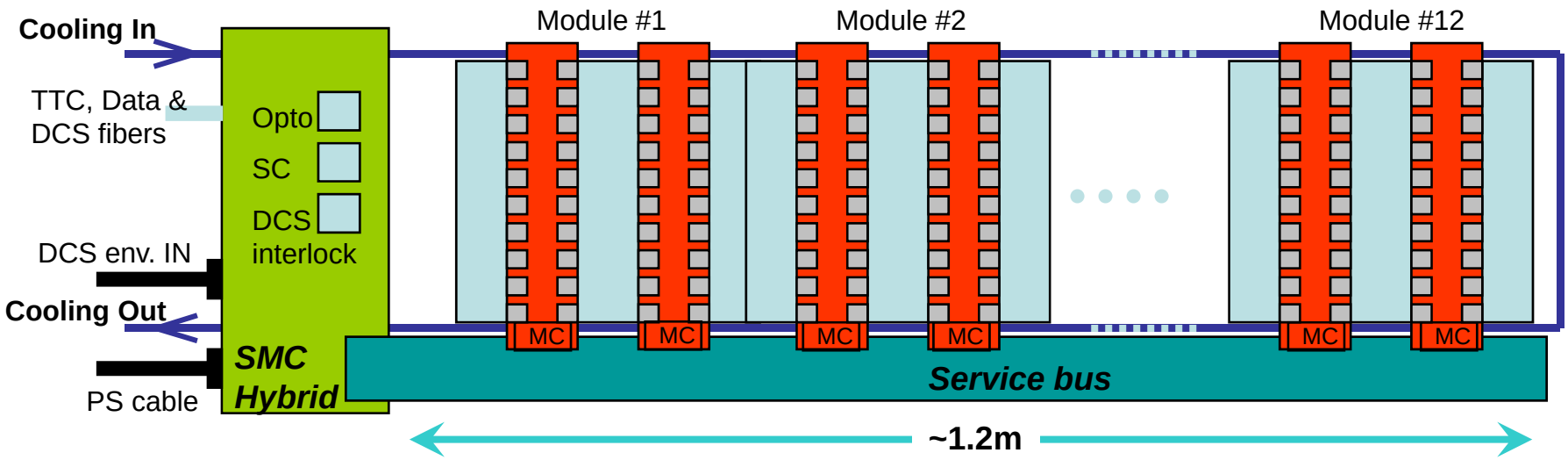


New trackers required to survive 6000fb^{-1} ie short strip detectors to withstand $9\times10^{14}n_{eq}/cm^2$ at 500V With 750e$^-$ noise, → S/N ≈12-15 (0.9µA/strip @ -15°C)





Module Integration

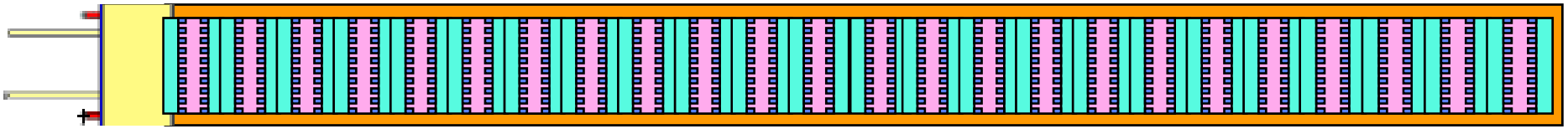


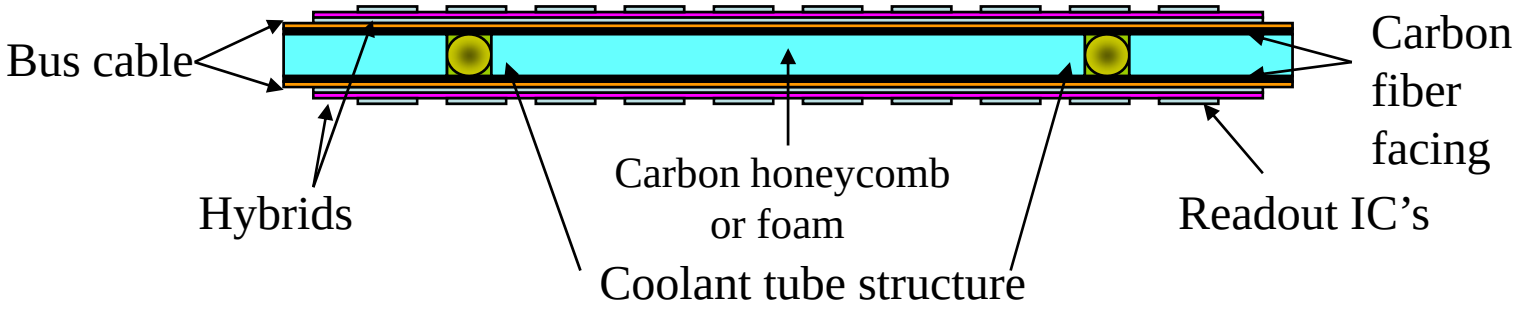
Key features:

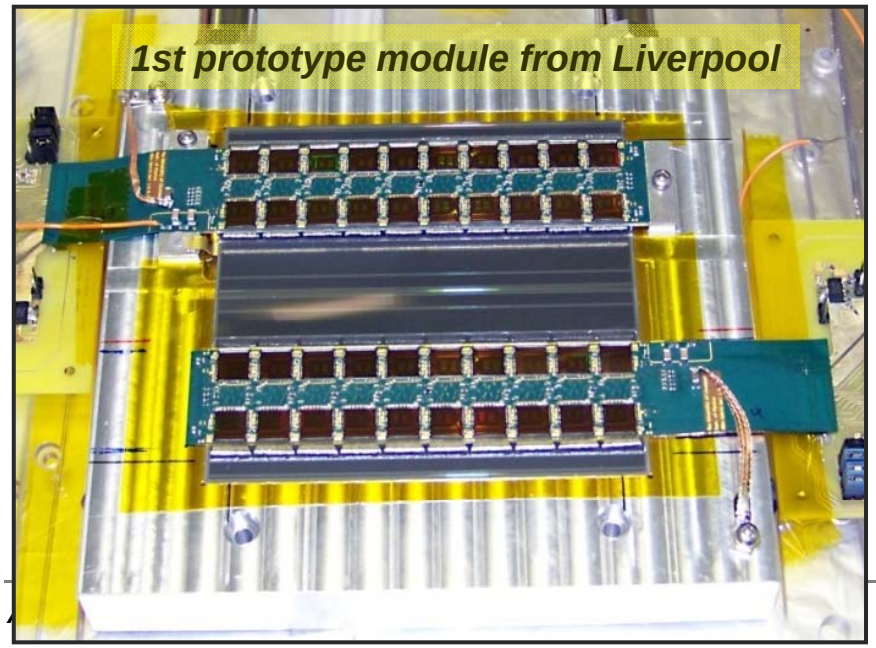
- Integrates all the functionalities and the requirements like: Sensor, FE, service bus, powering, DCS, cooling, mechanical precision and stability, controller cards, optical readout link, connectors and fittings…
- Low material budget with design and technology optimization
- Precision: built-in accuracy and mechanical stability
- Thermal management is critical to prevent runaway on the silicon
  → cooling, design, material and performance to be optimized
- Manufacturability, yield and cost

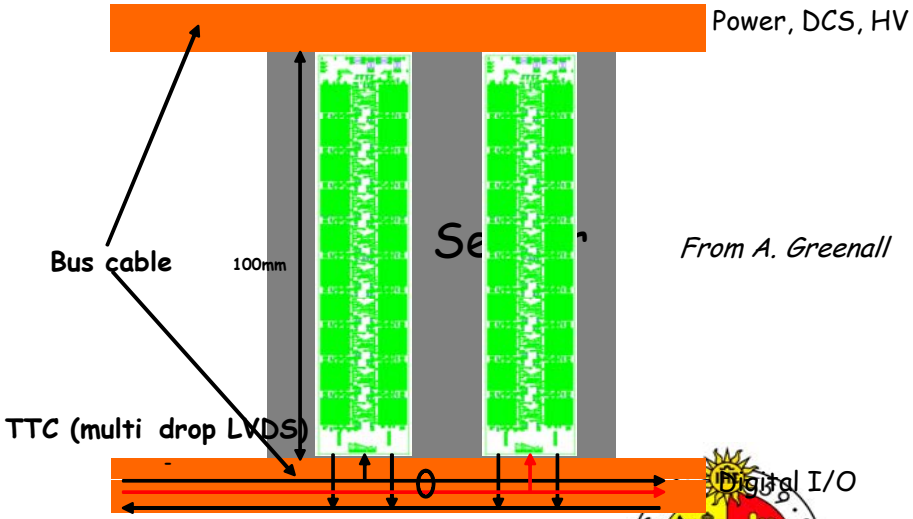
Module Integration - Stave

Short Strip Double-sided Stave - Baseline



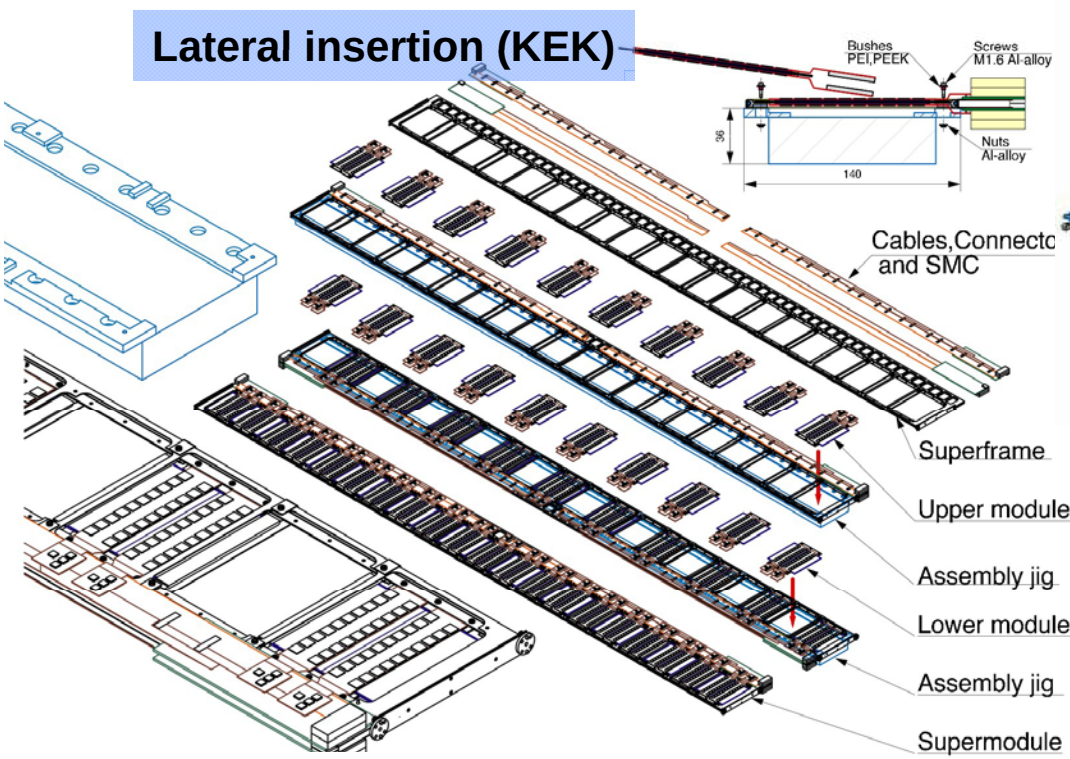


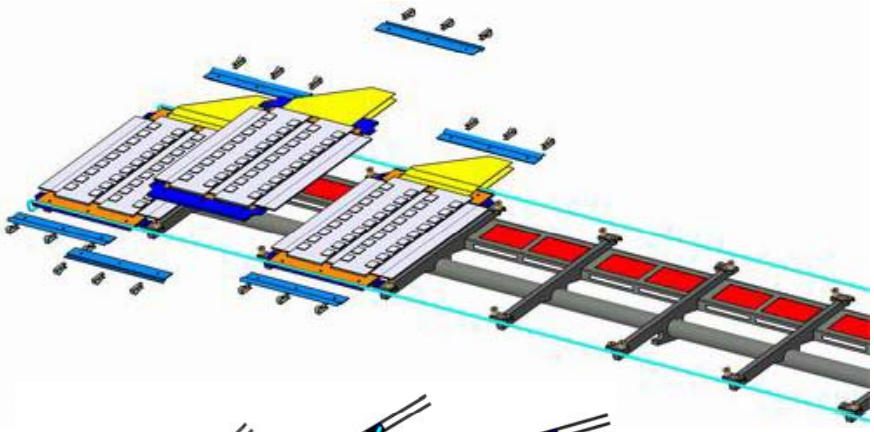


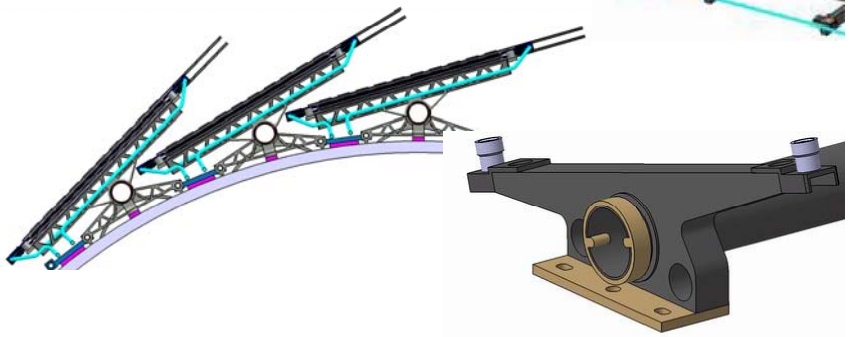


Double-sided Module - Backup

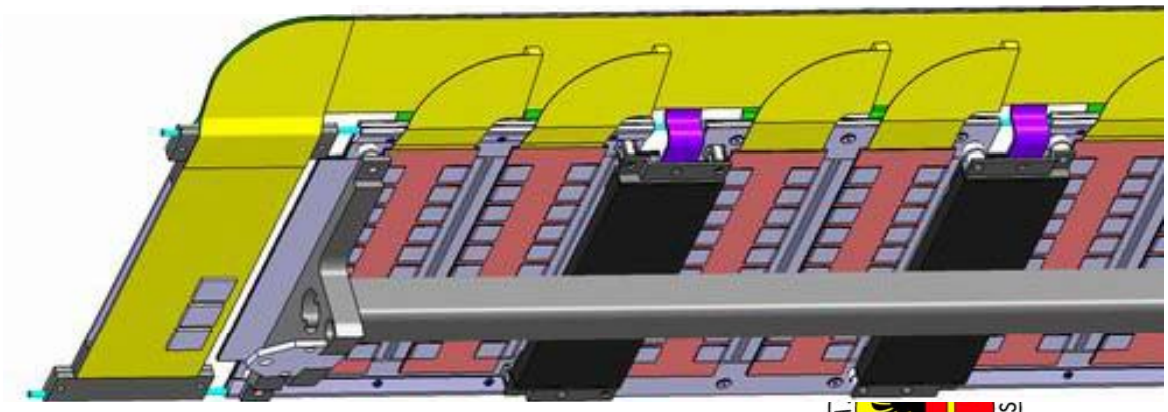
Lateral insertion (KEK)

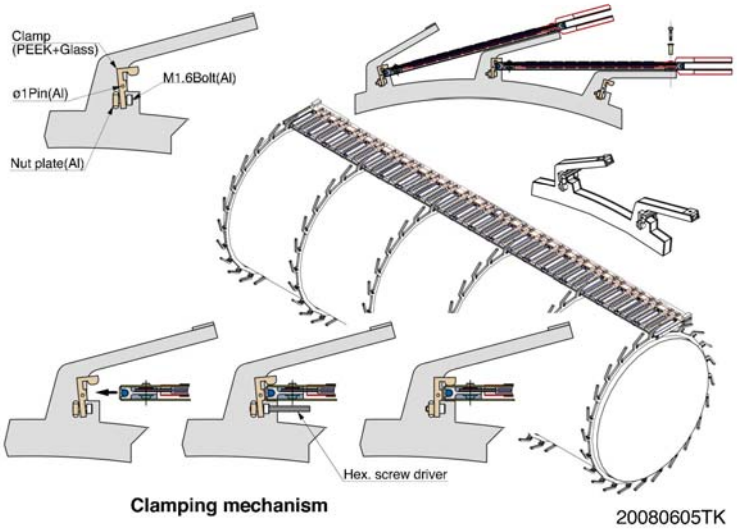






End insertion (Geneva)





Clamping mechanism

20080605TK

Endcap Petals

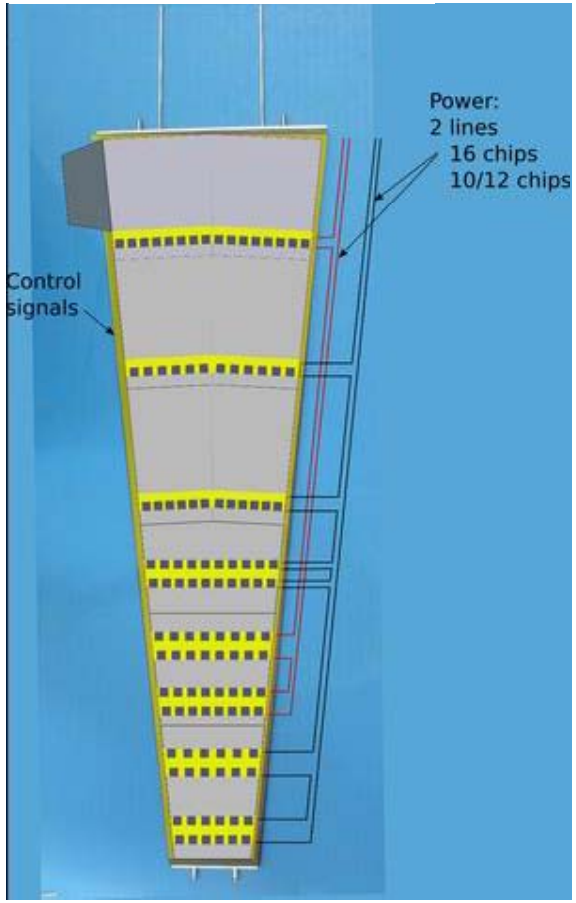
Endcap strip:

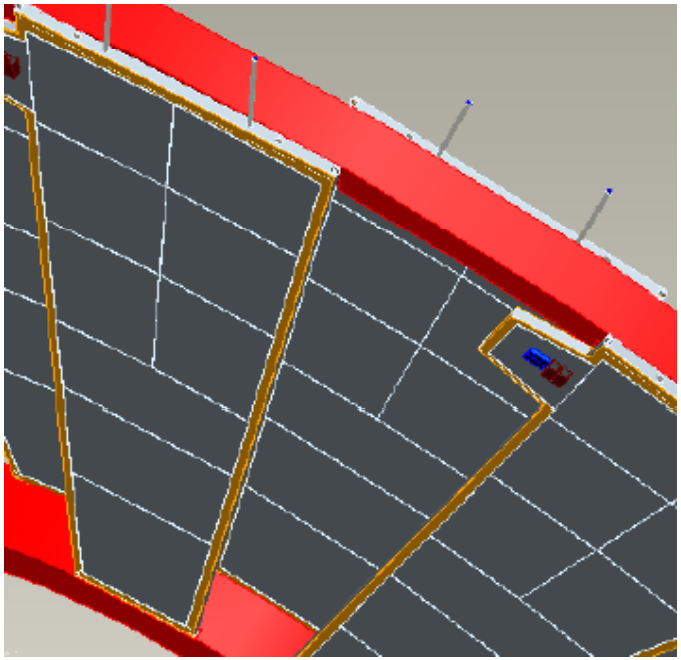
- 5 discs on each side
- 32 petals/disc
  - ➔ 4 different petals (325mm<R<950mm)
- 6 different detector types mounted on petals
  - ➔ Max 18 sensors/petal
  - ➔ Min. 12 sensors/ petal
- 8 hybrid types

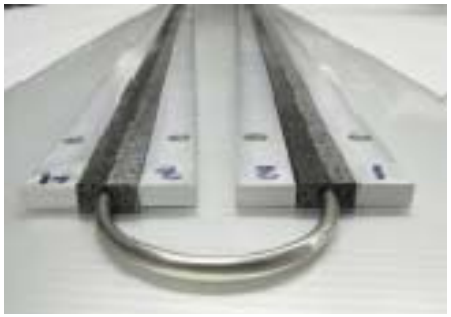
➔ Issues: Layout, modularity, powering…

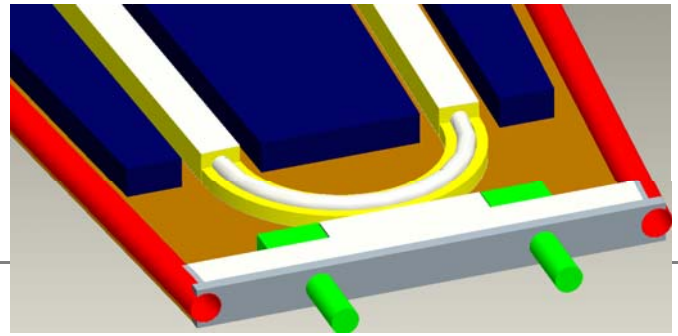
C. Lacasta IFIC

Serial Powering Lines









Readout Electronics - IC

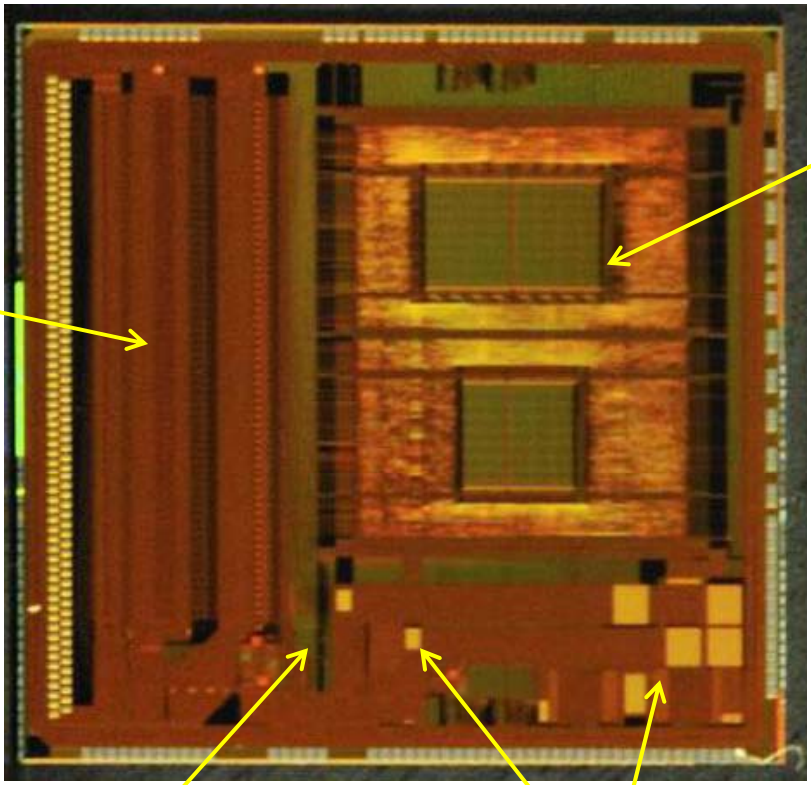
CMOS [130nm or 90nm] is the commercial technology choice for the Upgrade:
- Known for the radiation hardness (Transistors with GAA)
- Good for large volume production
- Good for low power consumption

Current Asics program → **Strip:** ABCN 250nm → 130nm **@ 160/320 MHz**

Issues:
- Technology choice for a production in > 3 years: 130nm, 90nm?
- Number of channels per FEIC is left opened so far: More than 128 may have some advantages
- Power consumption (Strips):
  - 250nm (ABCN) → Measured 3.6 mW/ch @ 40MHz
  - 130nm → Max target 1 mW/ch @ 160MHz (expected 0.5-0.6 mW/ch)
- Single Event Upset (SEU):
  130 nm technology seems to be 10 times more sensitive than 250 nm
- Need to consider new readout protocol
- Design → prototype and tests → manufacturability on a fixed timescale
- Design and tools of 130nm or 90nm are more complex

FE - ABCN

128
Channels
Front-End opt.
for Short Strips
0.7mW/channel



Digital part : reuse of existing SCT protocols, SEU protections, 80Mbits/sec output rate, power control , 2mW/channel @2.5V

ABCN 250nm is an intermediate version of the FE chip for modules prototypes developments

F. Anghinolfi

Serial regulator to provide analogue from a unique digital+ analogue power source

Shunt regulators (2 options) to exercise 2 different serial powering systems

ABCN in 250nm

ABCN program:

- Test and validate the current chips in 250nm technology
- Use those chips for prototypes
- Work on the final choice technology

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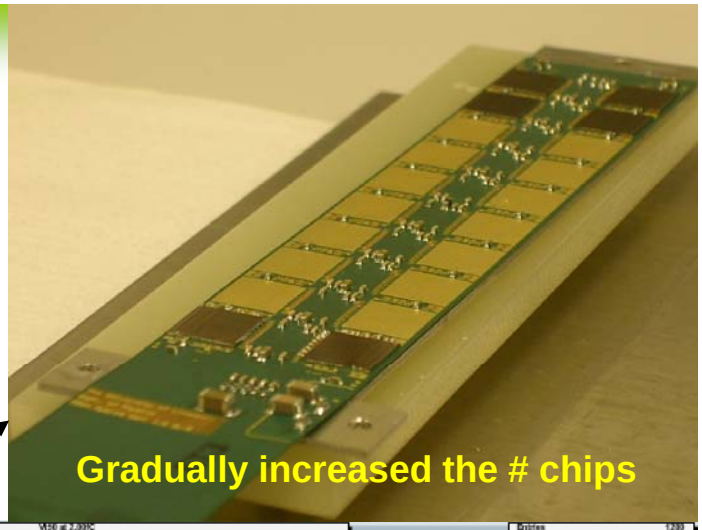
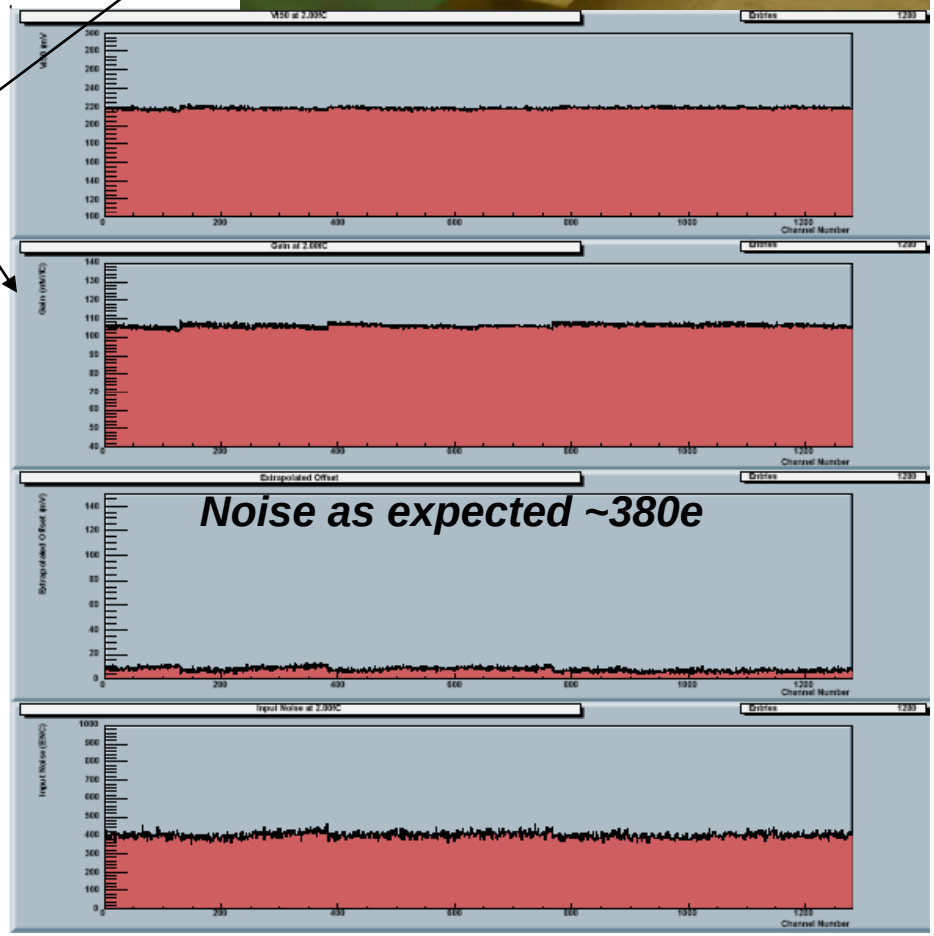
Subset of a result of a 20 chip ABCN Liverpool hybrid





Good progress so far in testing:

- Digital and analog performance as expected
- No malfunctioning found
- Yield seems good
-Functionality and performances to be tested @80MHz
- Wafer screening under investigation

Silicon with ABCN-250nm

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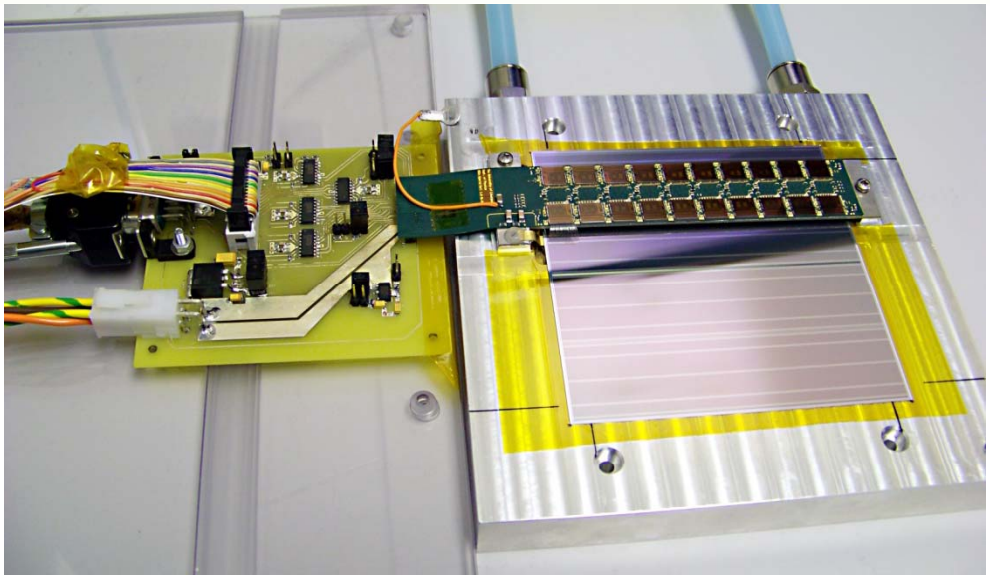
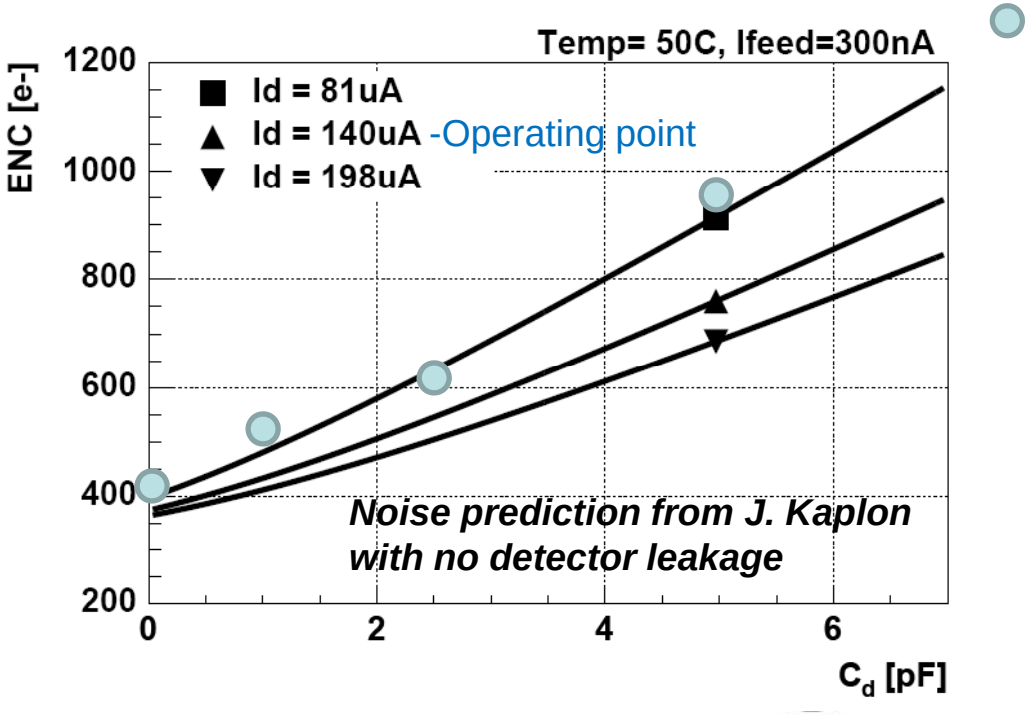
Divided first ABCN into three sections connected to 2.5 cm, 5 cm, 7.5 cm silicon strips



	With separate analogue/ digital power	With analogue regulator
Bare Hybrid	400-450 e^-	400-450 e^-
1 pF		525 e^-
2.5 pF	605 e^-	575 e^-
5 pF	986 e^-	952 e^-
7.5 pF	1364 e^-	1313 e^-



Module Controller (MCC)

From M. Newcomer

Features:

- Single Point interface between hybrid FEIC's and Stave distribution of TTC and ROD read out signals.
- DCS Monitoring
- Power Management ??
- Short and long strip readout clock: 160 and 80 MHz respectively

Stave Bus

SC → MCC **L1, BC, CMD** Bussed to all MCC
For the Serial Power (SP) option the MCC needs AC coupled receivers.

SC ← MCC Hybrid **Data** Direct Link / MCC
For the SP option the Stave Controller needs AC coupled receivers.

Hybrid Bus

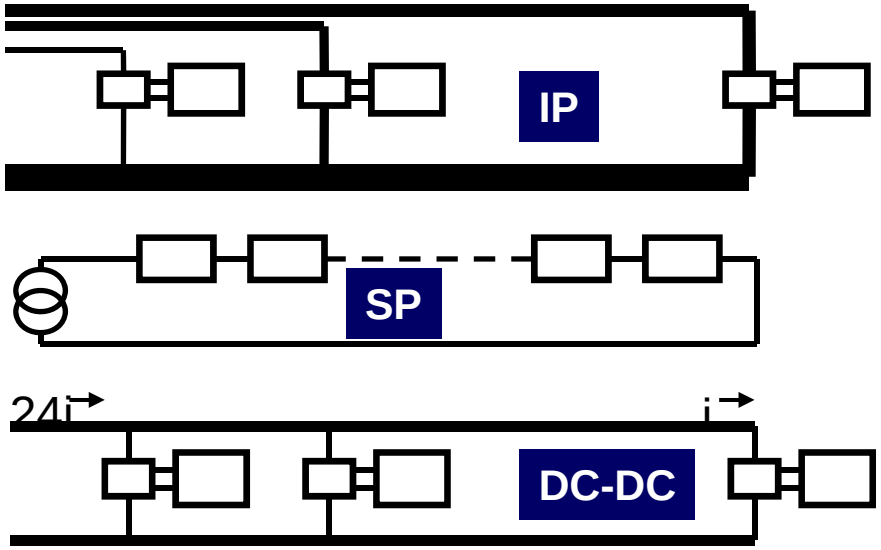
MCC → FEIC **L1, BC, DC, CMD** Bussed to FEIC's

MCC ← FEIC FEIC **Data**
@128ch/FEIC Multiple Loop Bi-directional Serial.
@512ch/FEIC Dedicated Lines to MCC ??

Powering

ID Upgrade has a lot of more channels to power than current ID

2 options are considered: - Serial powering
- DC-DC conversion



ABC-Next 250 nm : ***Vcc = 2.2 V, Icc = 0.036 A***
Vdd = 2.5 V, Idd = 0.12 A
0.38W/FE → 30.4W/module → 365W/stave

ABC-Next 130 nm : ***1mW/ch expected***
0.13W/FE → 10.2W/module → 123W/stave

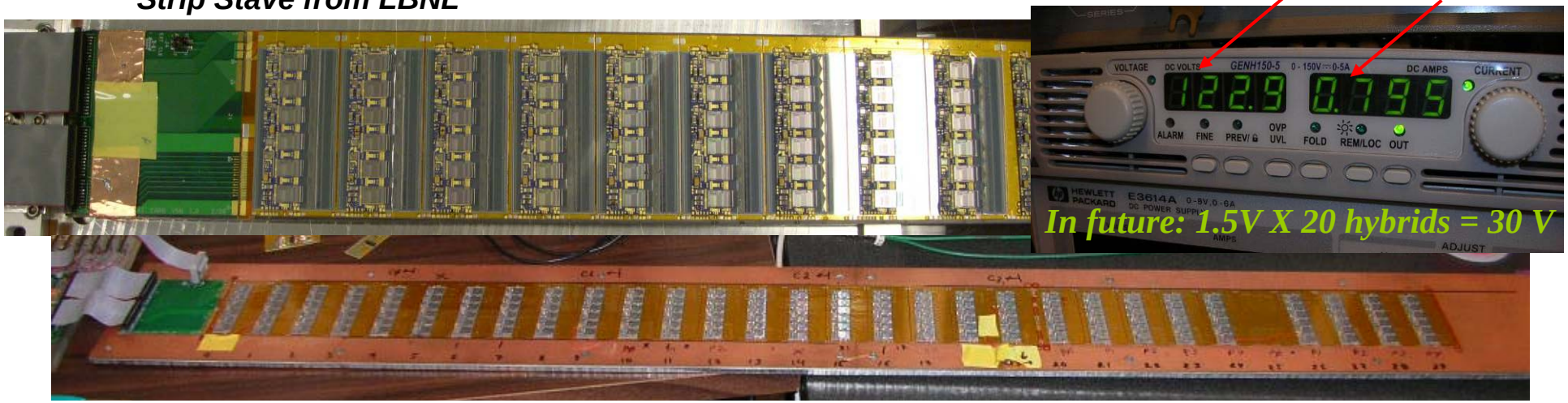
IP → ~2 order of magnitude higher of line width than SP or DC-DC

Issues:
- DC-DC: EMI (switching noise); radiation-hardness; high gain/efficiency
- Serial Powering: System aspect, Optimize protection/by-pass circuitry, Evaluate custom circuitry and identify best architecture
- System: Work out cable budget; LV & HV distribution, schedule…

Serial Powering

4 V x 30 hybrids = 120 V (0.8 A)

Strip Stave from LBNL



Tested so far:

1) Pixel stave with FE-I3 (old, published)
2) 6 SCT modules in series with ABCD
3) 6 module stave with ABCD
4) 30 module stave test vehicle and stave

Electrical performance is excellent in all tests. Multi-drop AC- LVDS coupling works

On work:

- Several options are considered: Shunt integrated in the FE, Shunt outside and transistor in the FE, Shunt and transistor outside FE

Tested with ABCN and SPi

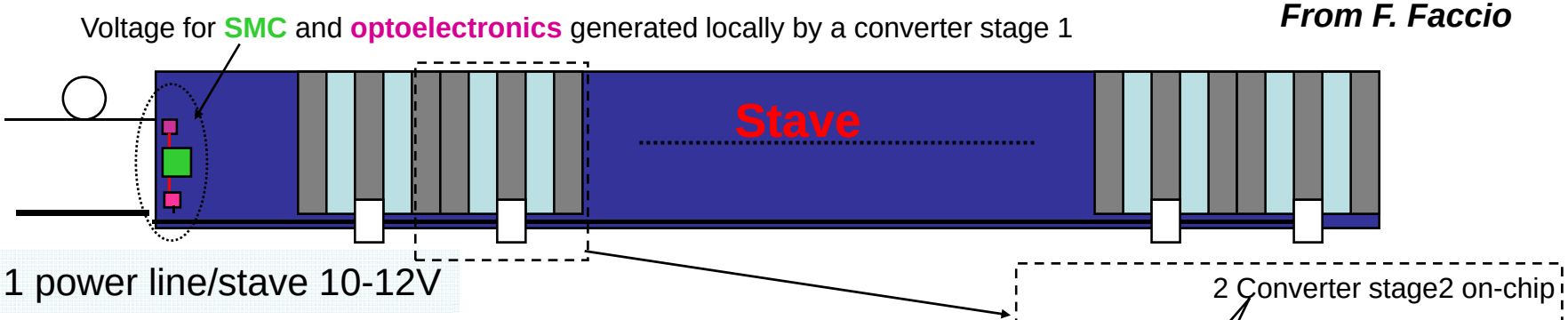
- Overvoltage protection and enable scheme to be worked-out and tested

DC-DC Powering

Key features: Efficiency, modularity, flexibility

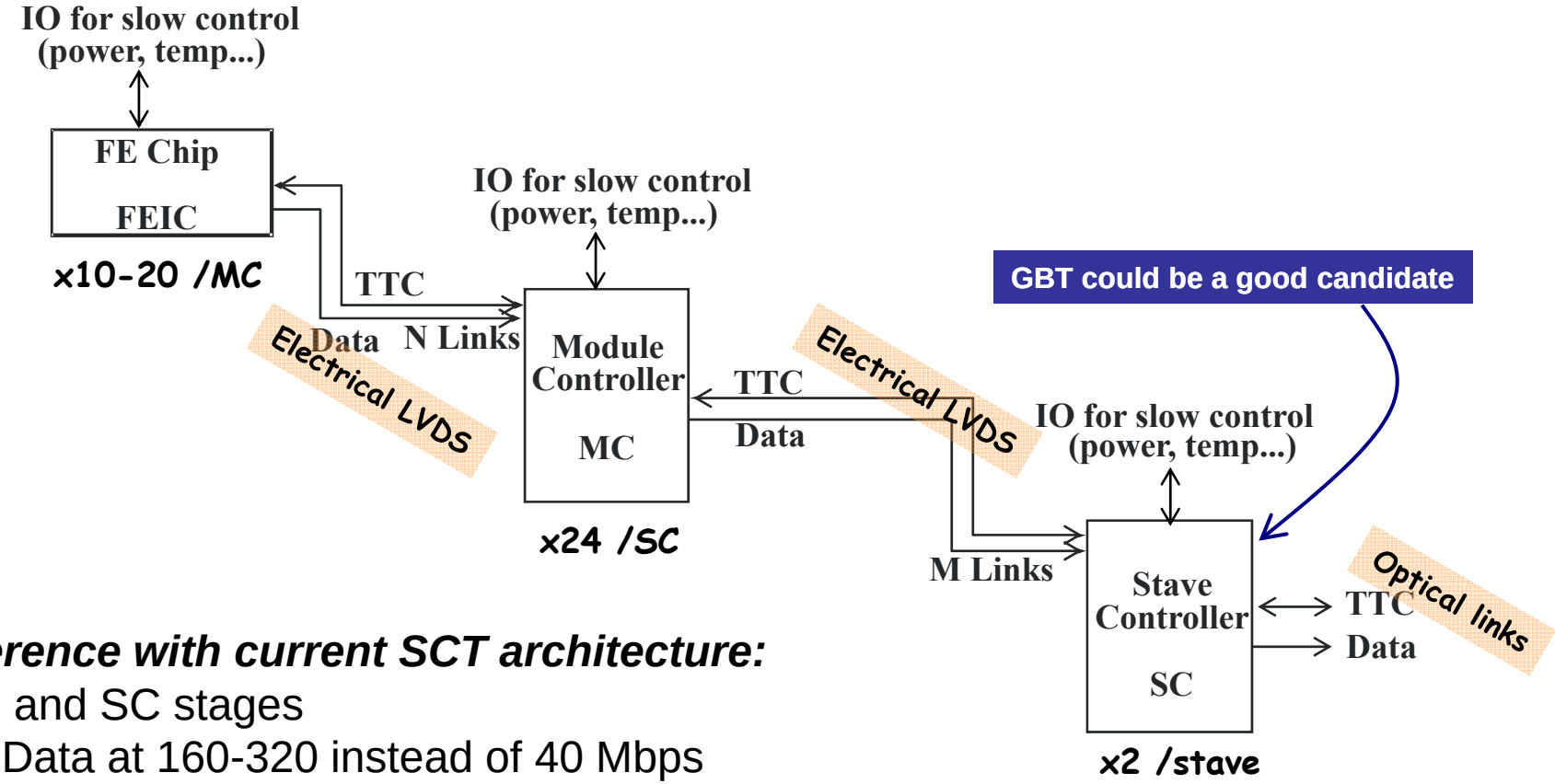
Work development common at CERN for ATLAS and CMS

From F. Faccio



- **Distribution with 2 conversion stages**
- **Stage 1:**
  - 2 converters: 2.5V analog and 1.8V digital
  - Higher efficiency if more hybrid powered
  - Integrated into a modular circuit board
- **Stage 2:**
  - Directly integrated into the FE asics
  - Switched capacitor converter with fixed conversion ratio = 2
  - 2 converters one for analog and one for digital

Readout Architecture



Difference with current SCT architecture:

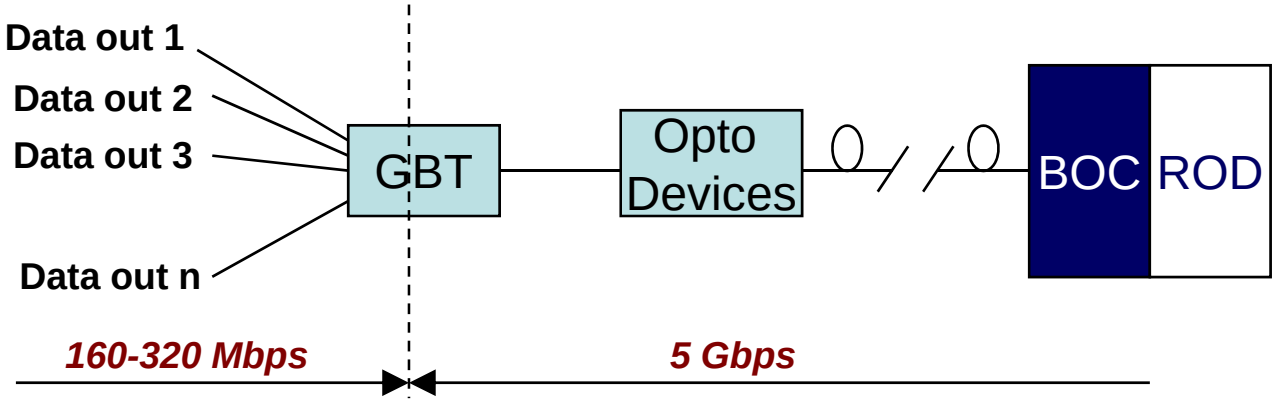
- MC and SC stages
- FE Data at 160-320 instead of 40 Mbps
- Data to off-detector will transit via high speed links

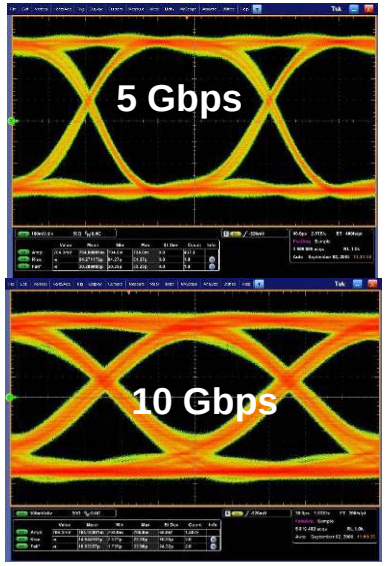
  Short-strip stave → bandwidth 3.84 Gbps Max needed for strip project
- Top and bottom side readout are decoupled
- DCS diagnostics data possibly integrated into the readout chain
- FE redundancy scheme is differently implemented (No bypass)
- Readout protocol has to be different (avoid token, data coding,…)

Optical Transmission

Work focus on high speed data link @ 5Gbps to minimize the number of fibers

The data transmission will be done for half stave (Strip)





Challenges and investigations:

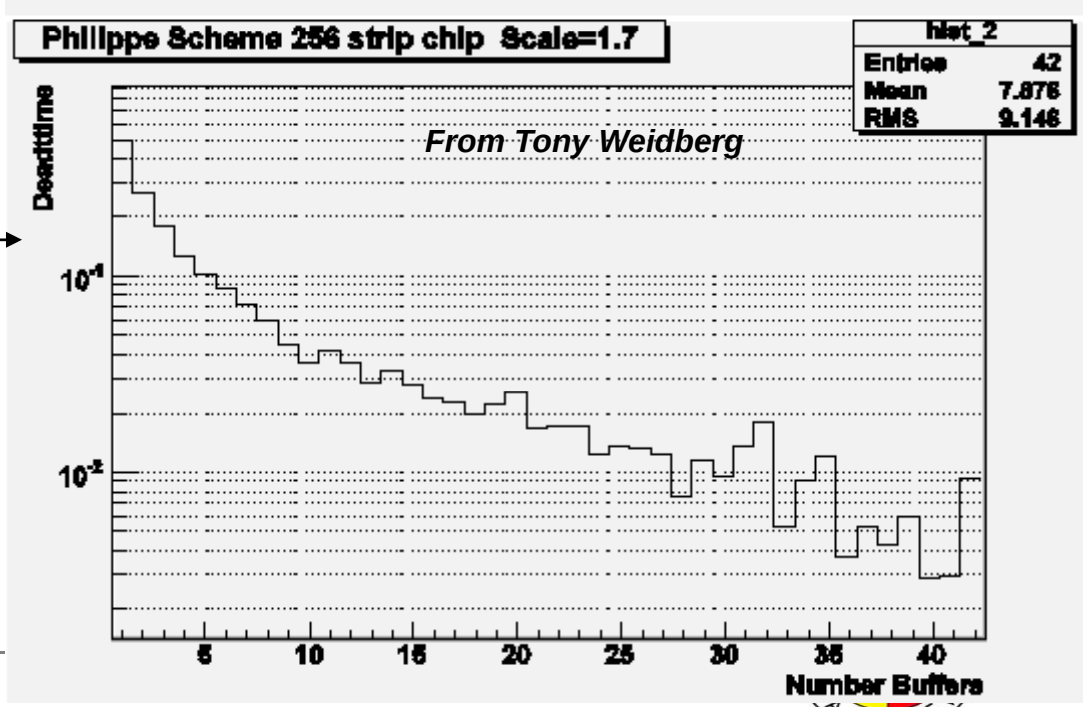
- Opto-devices not enough radiation hard for the pixel region BUT OK for strips
- Radiation harness of all the components especially at low temperature -20°C
- Bit Error Rate (BER) versus SEU → Error correction mandatory at sLHC
- Wavelength study: 850nm versus 1310 nm (more radiation hard)
  → 1310 SM VCSELs becoming available now which are being investigated
- Versatile link working group well structure (common to ATLAS and CMS)

Possible Requirements

- Redundancy scheme to be considered at all the stages of the readout chain from FEIC to SC and Opto-electronics
- Readout protocol and the data format has to cope with high speed readout, the easiness and the occupancy
- SEU robustness is essential → Replica logic has to be integrated where it is necessary
- Need at maximum an effective data rate of 3.84 Gbps at the optical interface (short-strip stave)
- An error correction scheme should be necessary due to BER in the optical interfaces

Dead time versus buffer depth

Here occupancy increased by a factor of 1.7 for a dead time of 1%



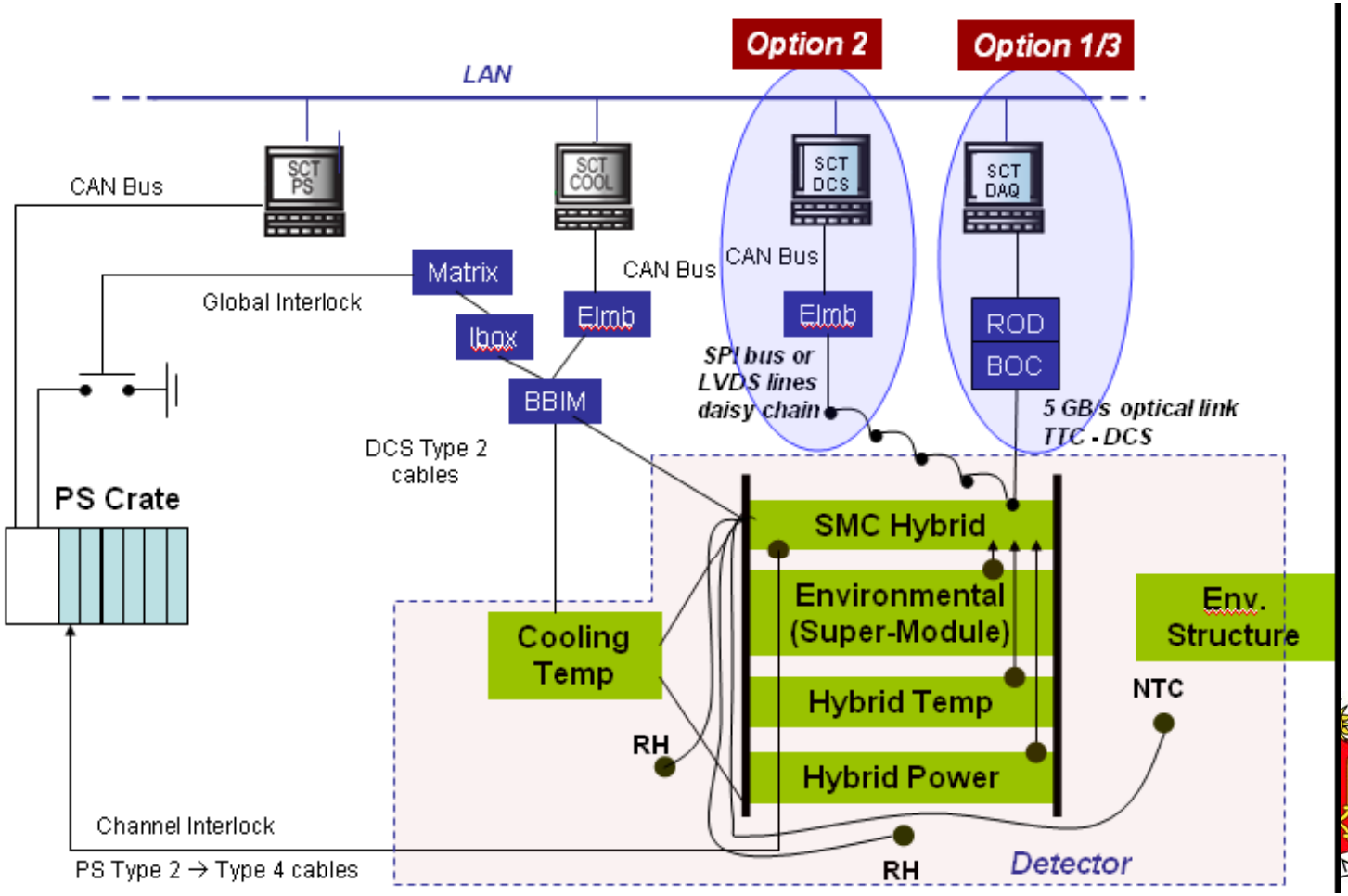
- Trigger Rate <L1> = 100 kHz
- Assume 20 MHz BC → <pile up> = 400
- 256 channels/FEIC
- Readout through 1 MCC
- Look at short strip detector only (worst case)

DCS Architecture

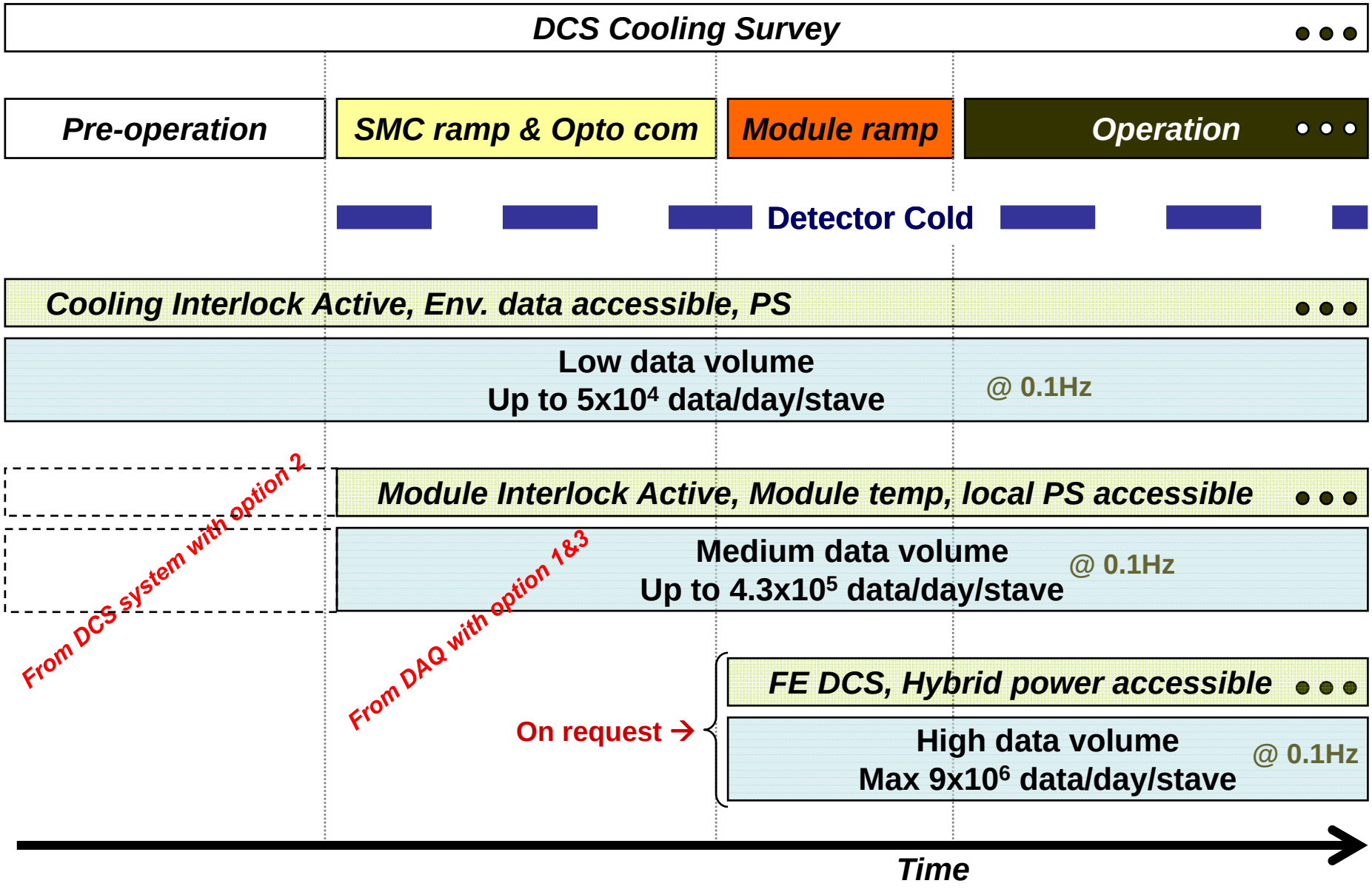
Mainly 2 options proposed so far:

- Option 1: - All the Hybrid and FE chip DCS info are readout via Fiber
  - One hybrid temp per stave is independently readout
- Option 2: Same as option 1 except that all the hybrid temperatures are readout independently via an independent DCS chip

NB: In all options interlock based on NTC cooling loop, Environmental, SMC temp are separated from data readout



DCS versus Operation



Services

It is where there is a lot of constrains!

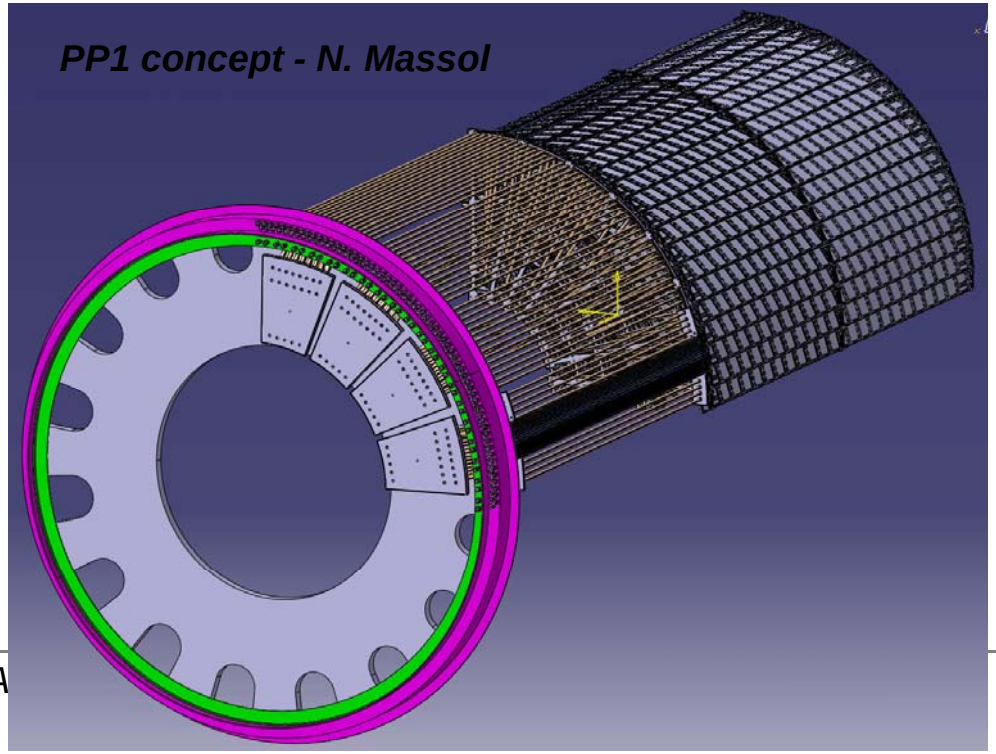
Constrains:

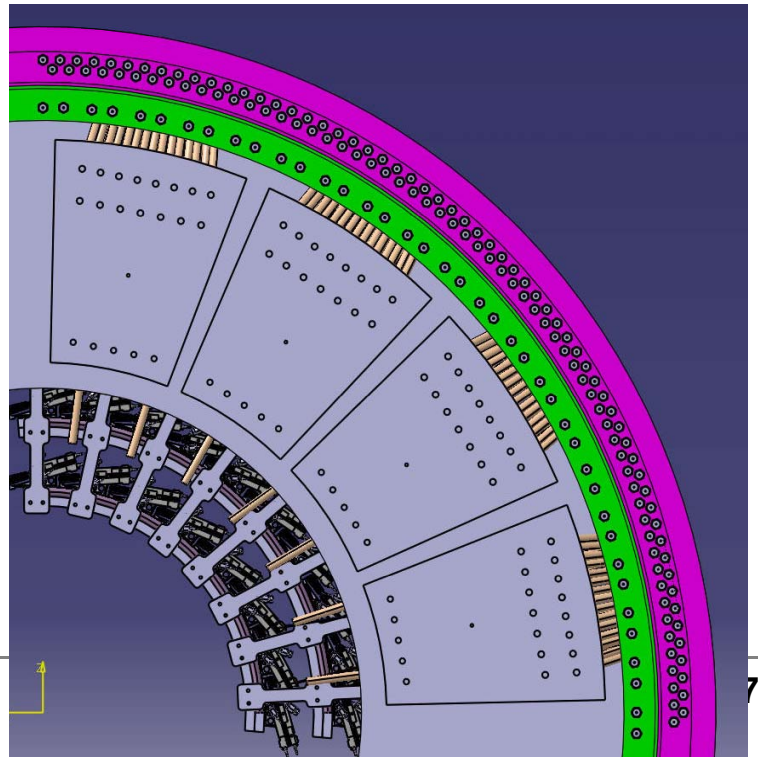
- Low mass inside the ID volume required
- Connection to the ID flanges should be fast and reliable (Limited access due to radioactivity level)
- Have to deal with the existing cables from counting rooms to PP2
- It has been excluded to reuse all the services at the various PP1 position
- For cooling pipes the cooling choice will strongly define what to do and the possible recycling

Electrical service available:

- SCT: - 4088 cables (LV, HV)
  - 144 fiber ribbons
- Pixel: - 1808 cables (LV, HV)
  - 84 fiber ribbons
- TRT: - 40128 cables (LV, HV, signal)

NB: Fibers have to be reinstalled to suit with bandwidth of ~5Gbps





Conclusions

• 3 ID Strawman layout versions have been investigated but a new baseline is expected in fall and to be presented at the LOI (early in 2010)
• Need also to deal with the possibility of a change in the layout with a track trigger → Implication on the readout architecture?
• The strip community are investigating the short (2.5cm) and the long strips (10 cm) for barrel and EC with stave or petal concept
• A strip readout Task Force has been initiated and is led by P. Farthouat. Specifications for the complete readout chain has to come soon to progress
→ Interim document “Architecture of the Readout Electronics”
• So far ABCN in 250nm is working well and the noise performance is as expected
• Many interleave fields: powering, readout, opto-electronics, DCS, services
• Prototyping is vital and all the future new ICs have to be tested on a real size stave/petal object
• Schedule is tight for a TDR in 2011

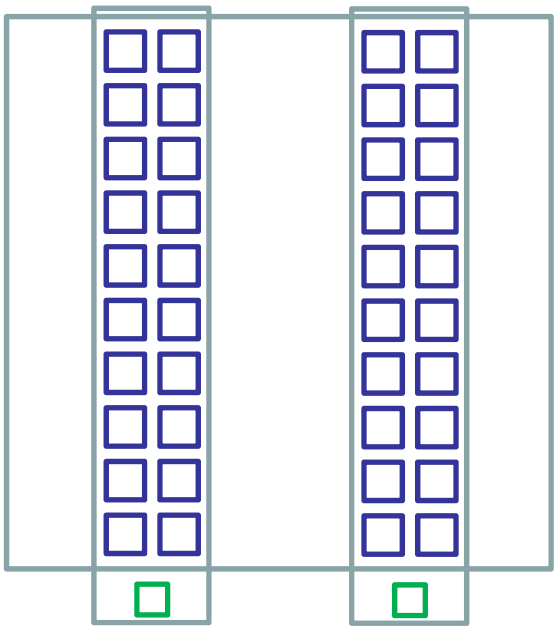
→ Need soon to freeze the FE technology, the readout protocol, the powering scheme and the DCS options.

Backup Slides

Backup Slides

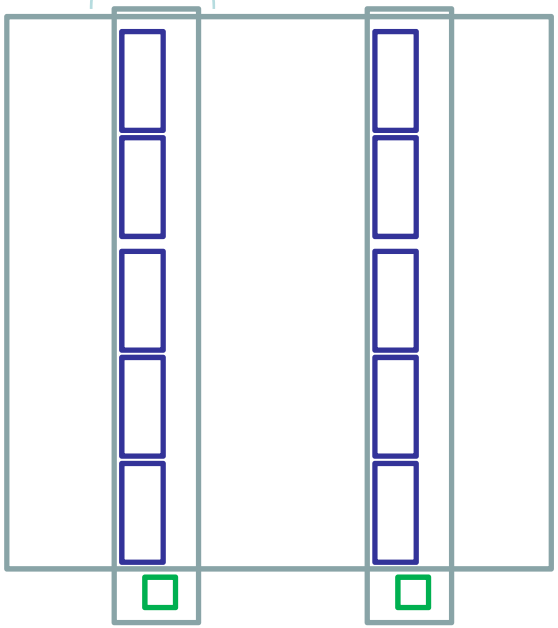
SHORT STRIPS

2 x 10
128
channels



Module arrangement, Short strips,
128 channels ABCN

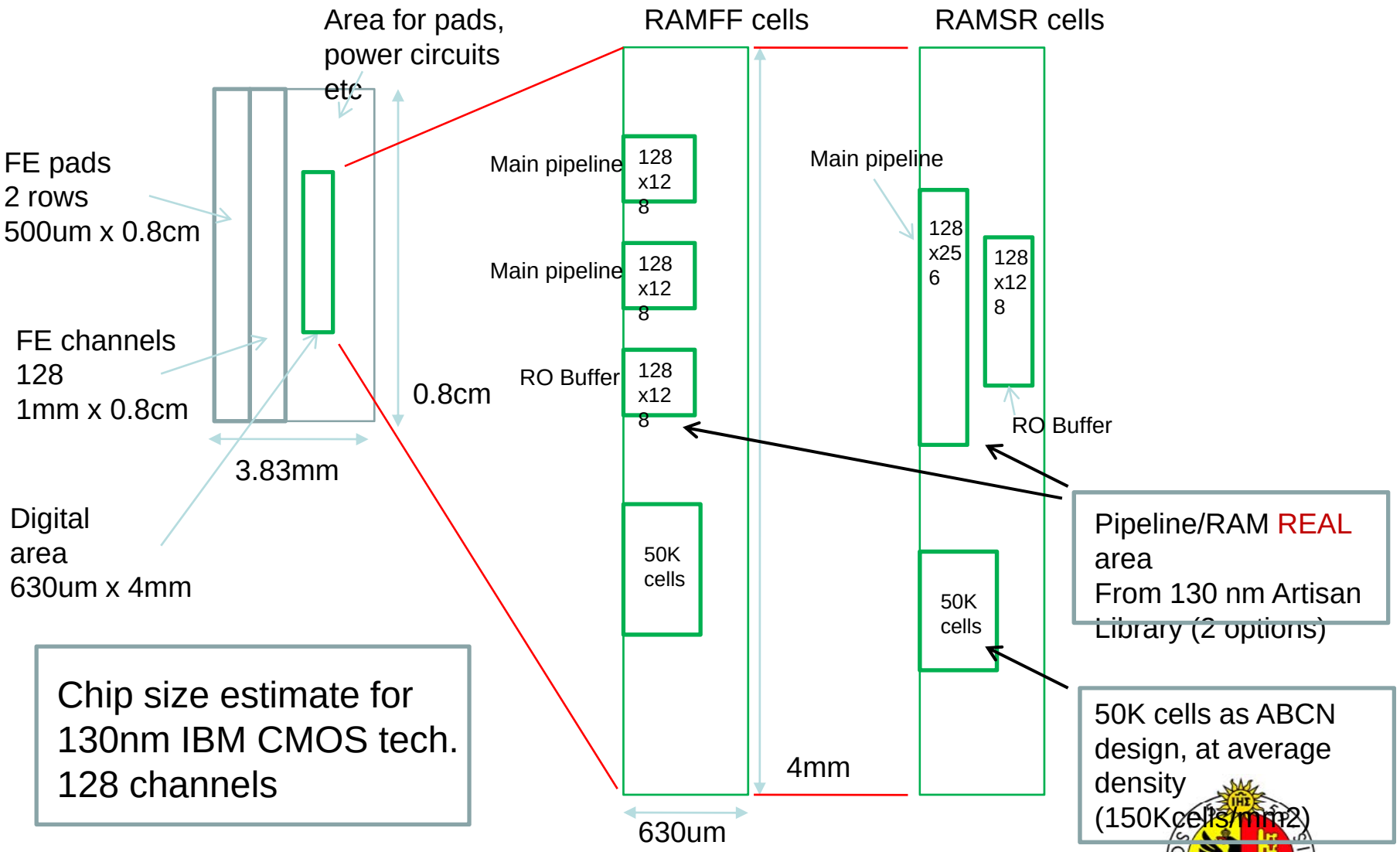
5 times
512
channels



Module arrangement, Short strips,
512 channels ABCN

128 ch FEIC layout

Variations on channel number

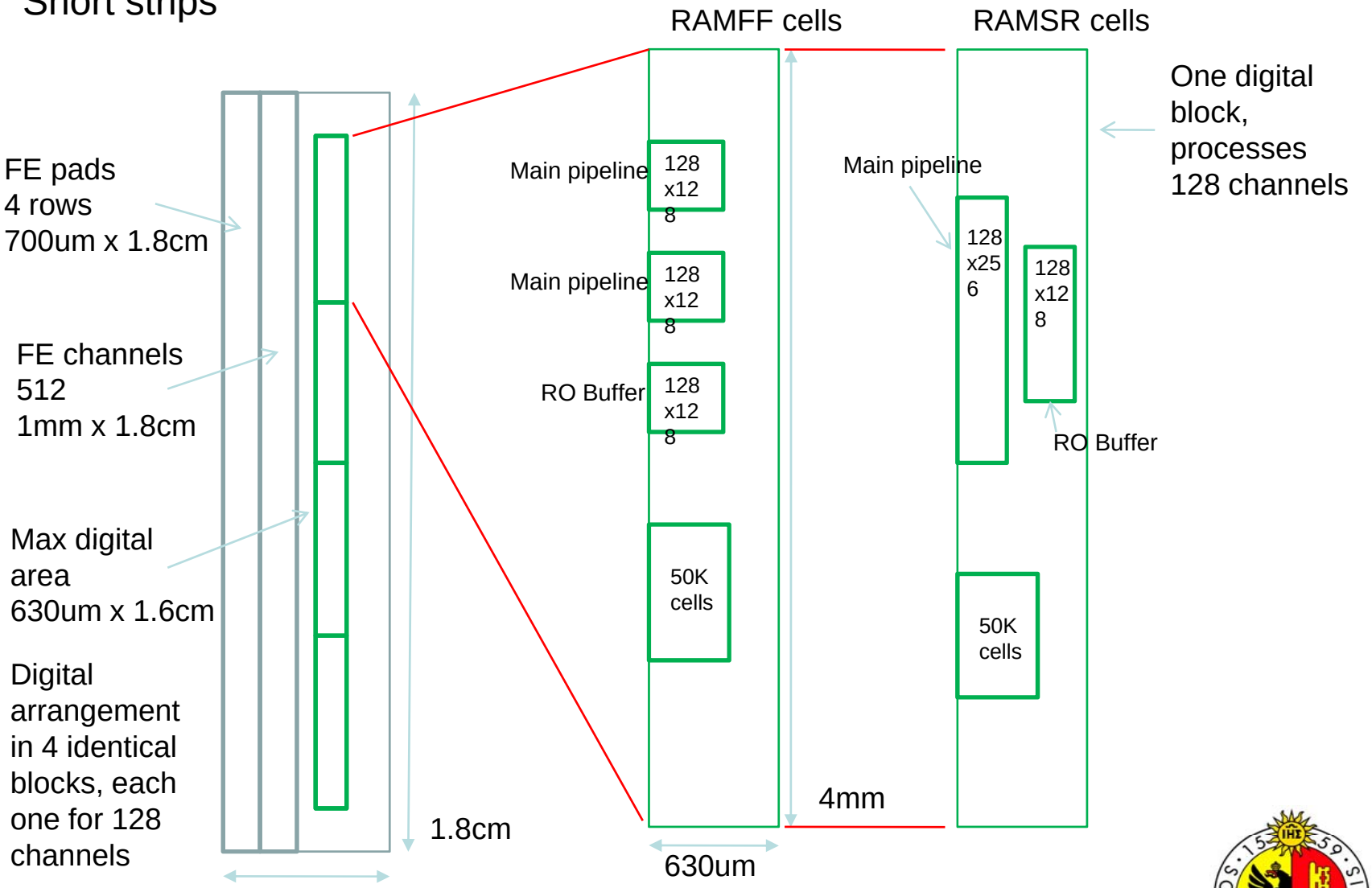


Chip size estimate for 130nm IBM CMOS tech.
128 channels

512 ch FEIC layout

512 channels chip option, Short strips

ABCN : NEXT STEPS



Interim Report

ATLAS project	Architecture of the Readout Electronics for the ATLAS upgraded silicon strips detector Interim report of the Strip Readout Working Group		
ATLAS Project Document No:	*Institute Document No.*	*Created:* 01-Oct-2008	*Page:* 1 of 35
ATL-P-EN-00xx		*Modified:* 13-Jan-09	*Rev. No.:* 1.0

Architecture of the Readout Electronics for the ATLAS upgraded silicon strips detector
Interim report of the Strip Readout Working Group

Abstract

This document describes the basic architecture of the readout electronics of the ATLAS upgraded silicon strips detector, summarises the conclusions drawn by the strip readout working group and lists next topics to be addressed.

Prepared by:	*Checked by:*	*Approved by:*
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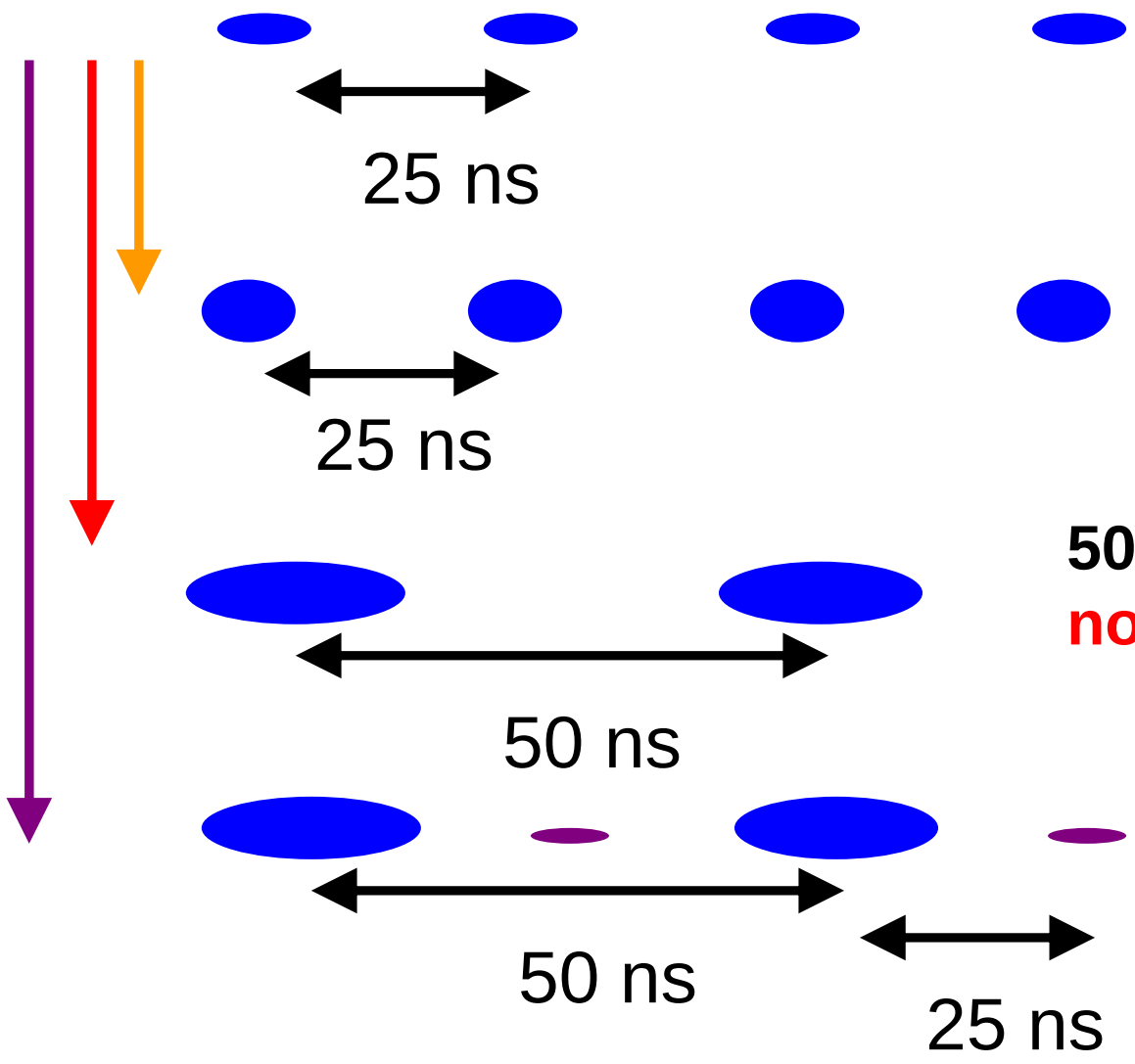
Distribution List

Upgrade Bunch Pattern

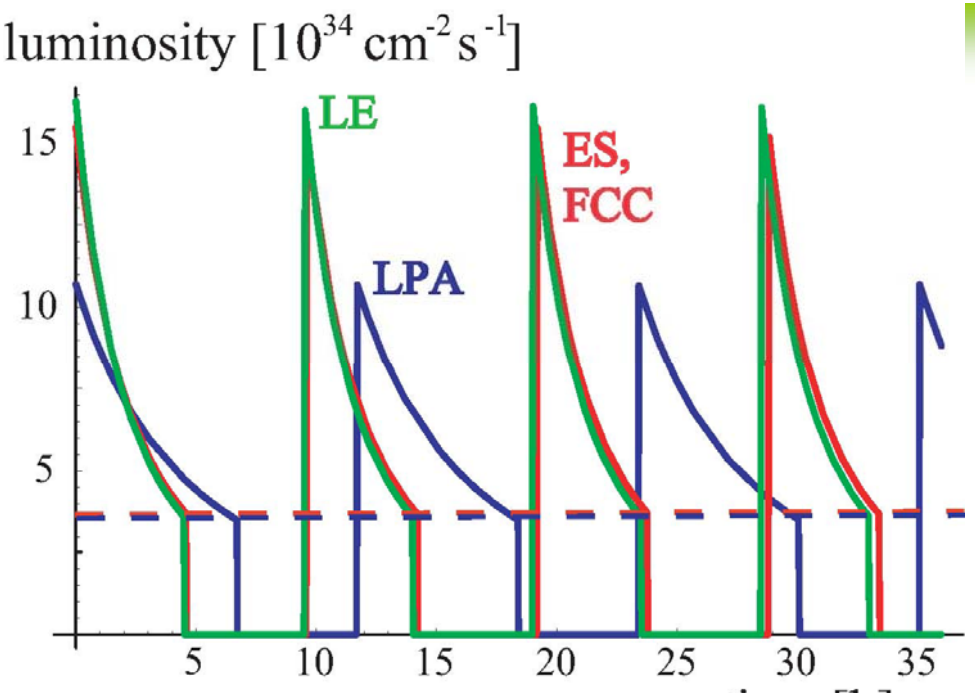


nominal

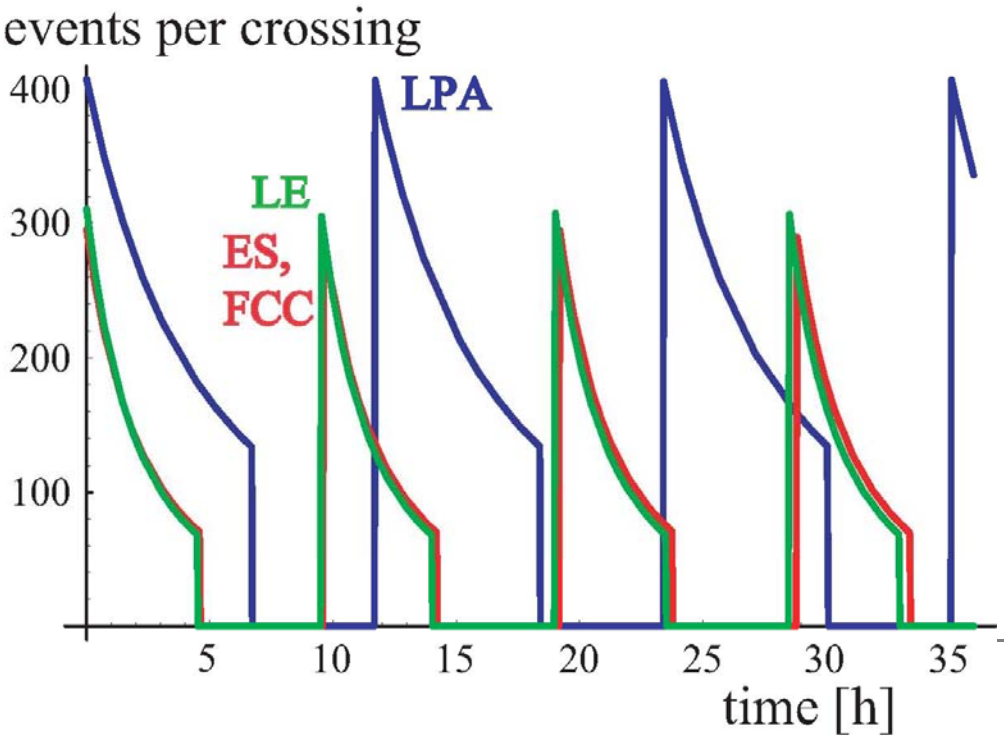
ultimate
& 25-ns upgrade
(ES, FCC, & LE)

50-ns upgrade (LPA),
no collisions in LHCb!

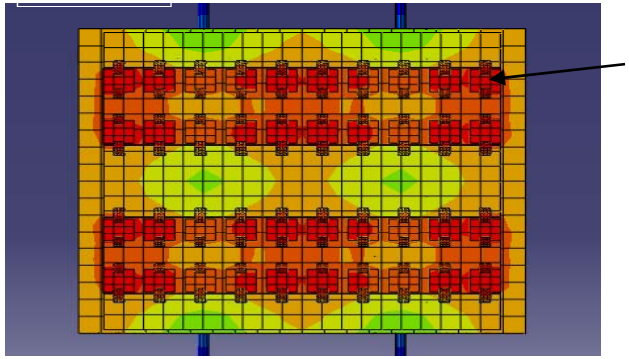
50-ns upgrade with 25-ns collisions in LHCb



Average luminosity



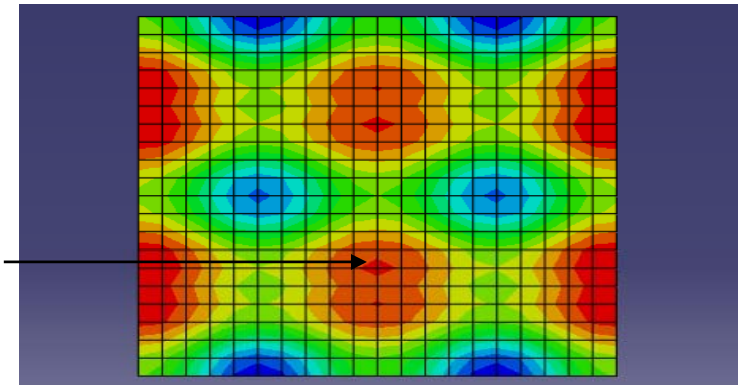
Thermal Runaway



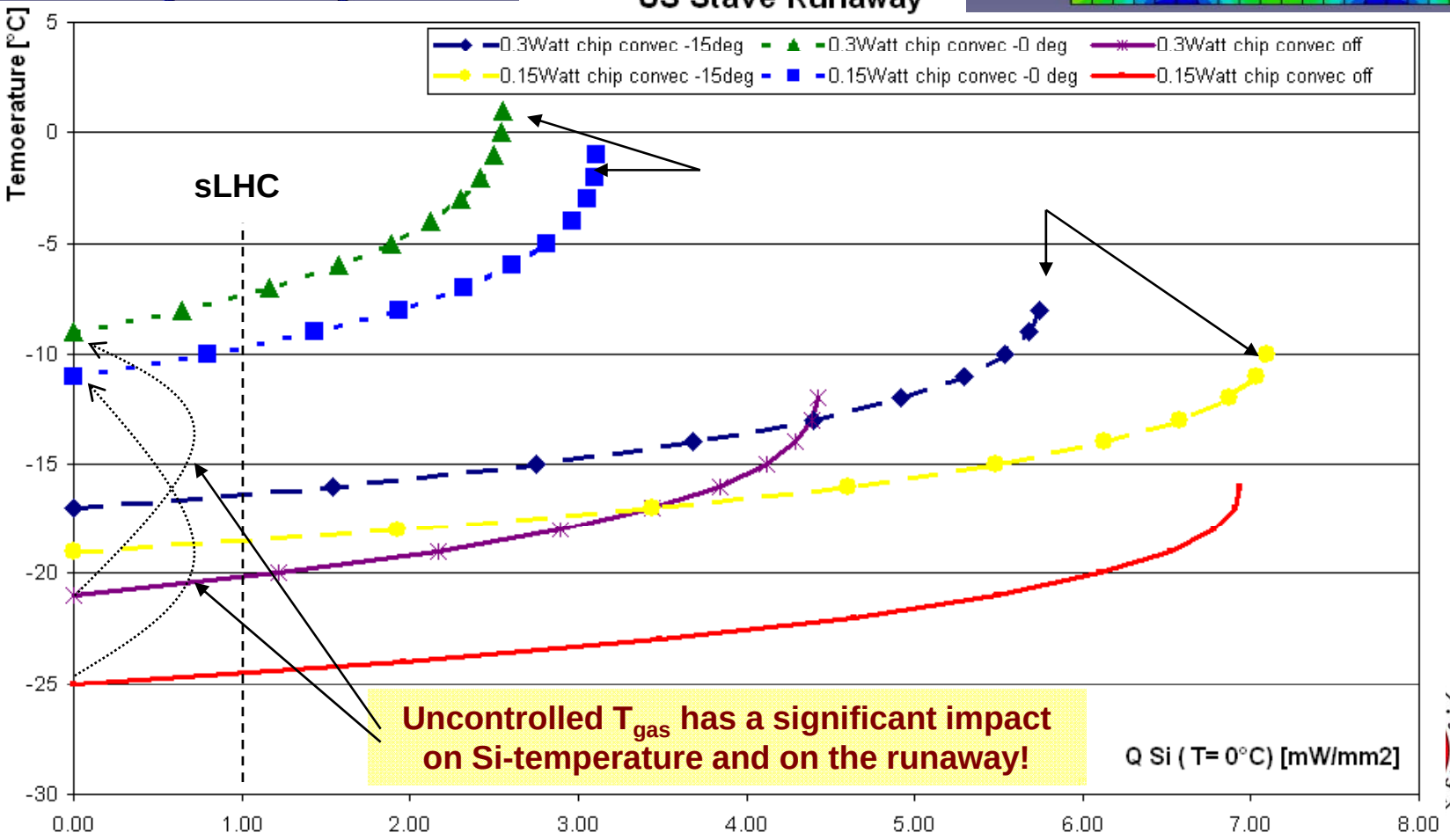
Tmax (FE)= -19.4°C

Cooling @ -30°C with CO_2

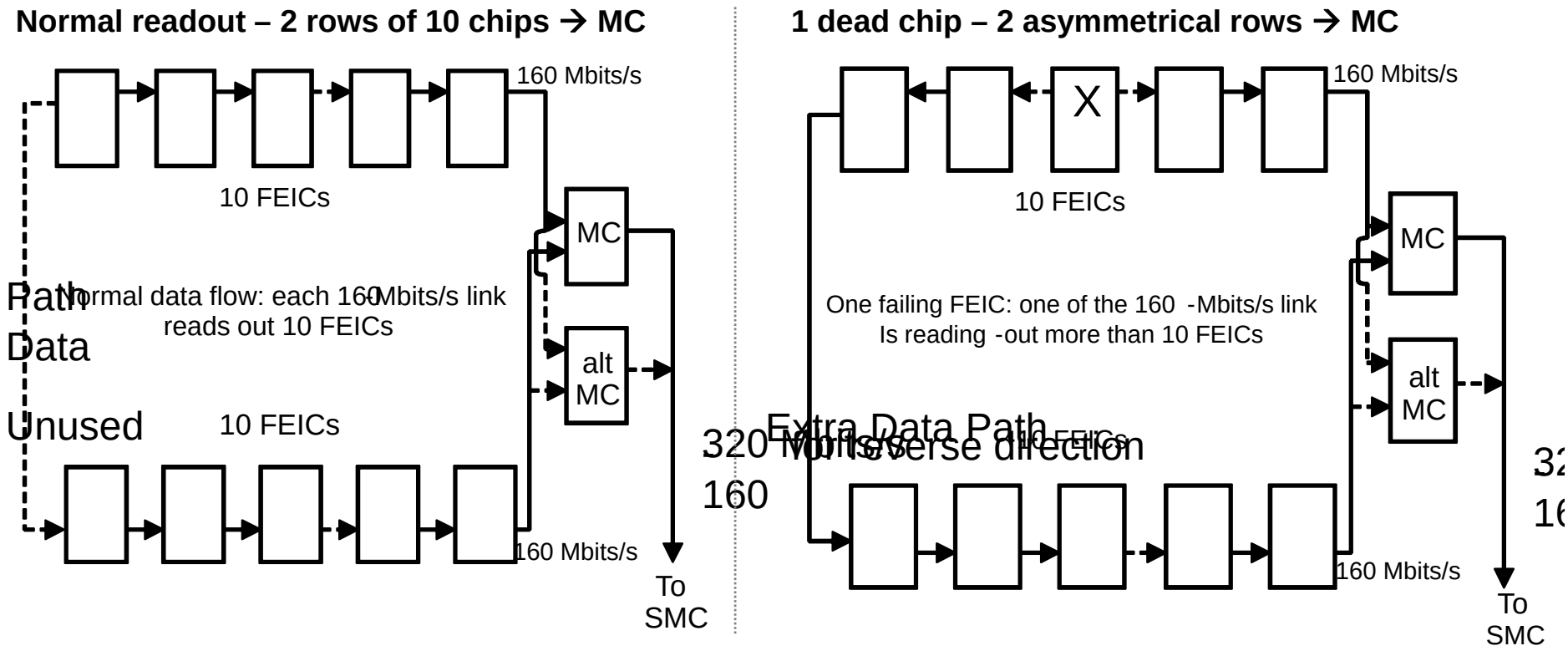
Tmax (Si)= -20.7°C



US Stave Runaway



Readout Scheme - Redundancy



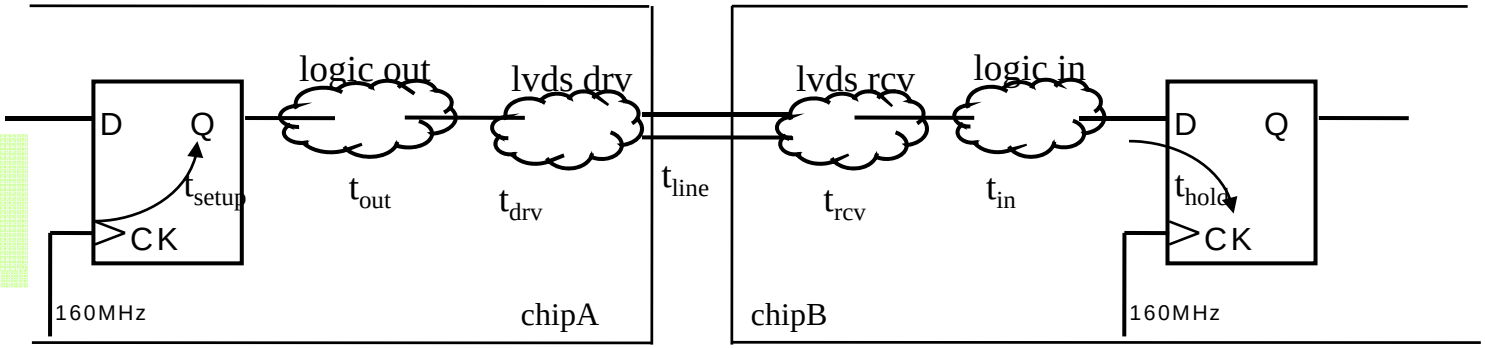
Other stages of the readout chain:

- **MC:** 2 chips are installed per hybrid and 100% fail safe scheme can be adopted
- **SMC:** Similar scheme as MC could be specified
- **Opto:** To be defined – One option could be to link the TTC and the data with the SMC of the other side of the stave → Bandwidth?

Readout Protocol

Option 1

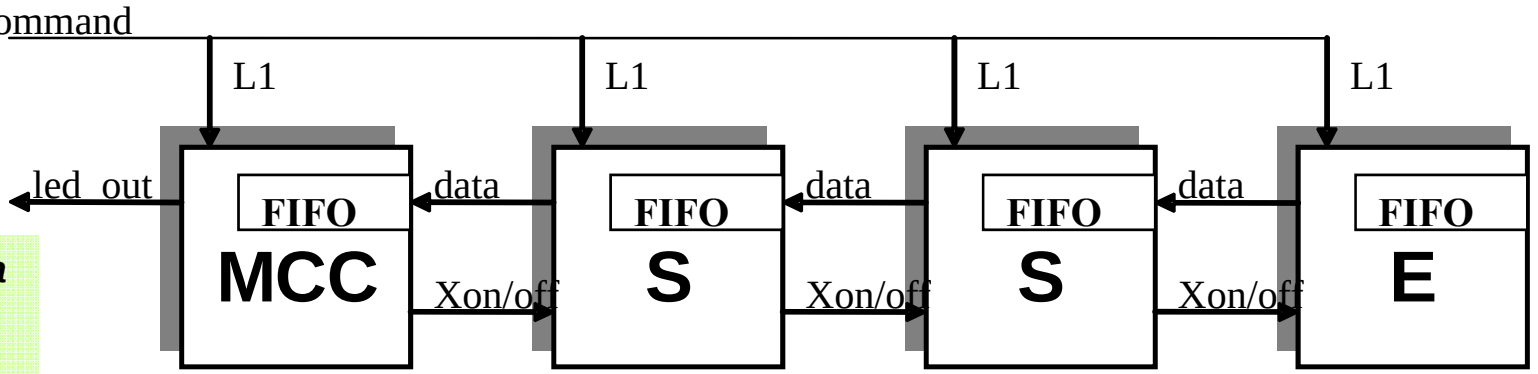
Token mechanism currently used with ABCD and ABCN



NB: At 160Mbps: 2.8ns remains to t_{out} and t_{in}… Not enough for any logic @ 250nm!

Option 2

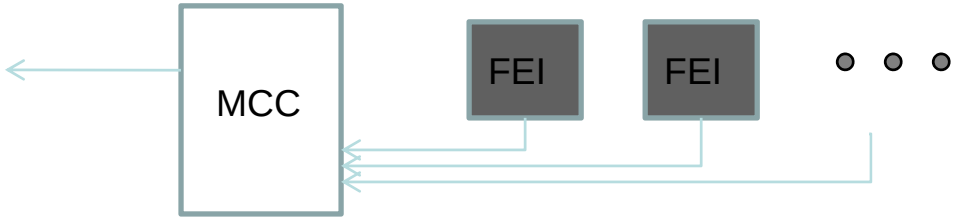
Word enable via Xon/Xoff line(s) → No synchro.



NB: Data are pushed from left to right into the FIFO. Xoff is up when the FIFO is full!

Option 3

- No synchro
- Robust if dead FEI



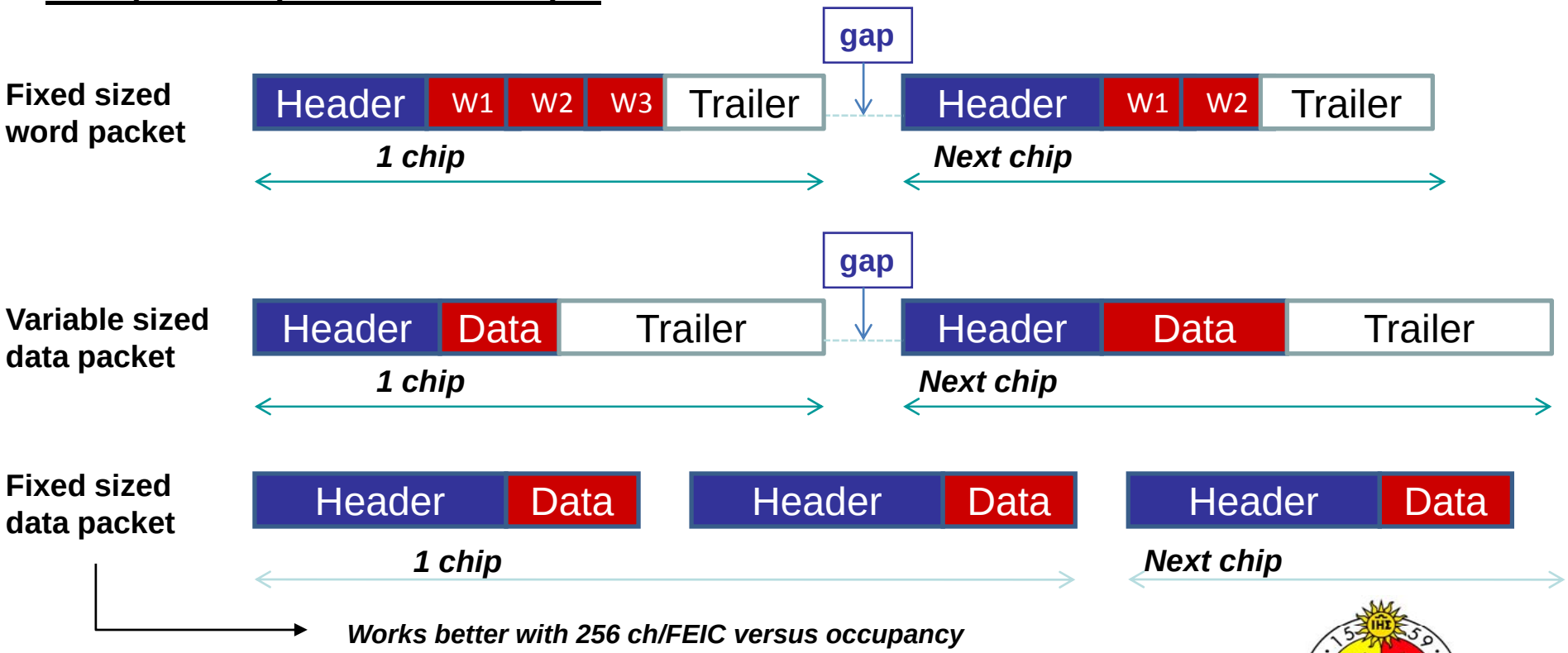
Star configuration – Data concatenation into MCC

Readout Protocol – Data Packets

Still to be defined: How to encode the data and bandwidth expectation?

{Header}{+ L1_ID}{+ BC_ID}{MC_ID}{+ Chip_ID}{ + CH_ID + Data}{+ Trailer}
… {+ Reg_ID +Data} … ← ***DCS***
… {+ ErrorCode} …

Data packet options for all chips:



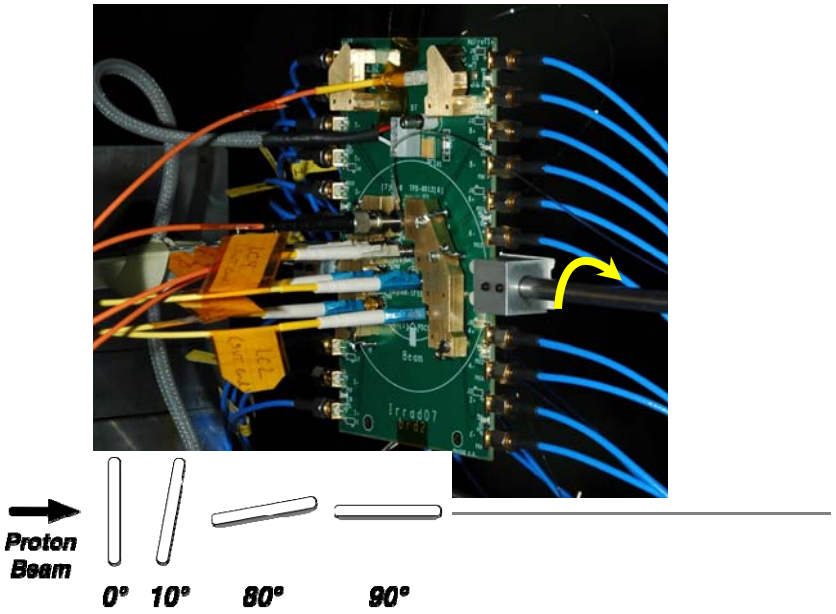
SEU & BER

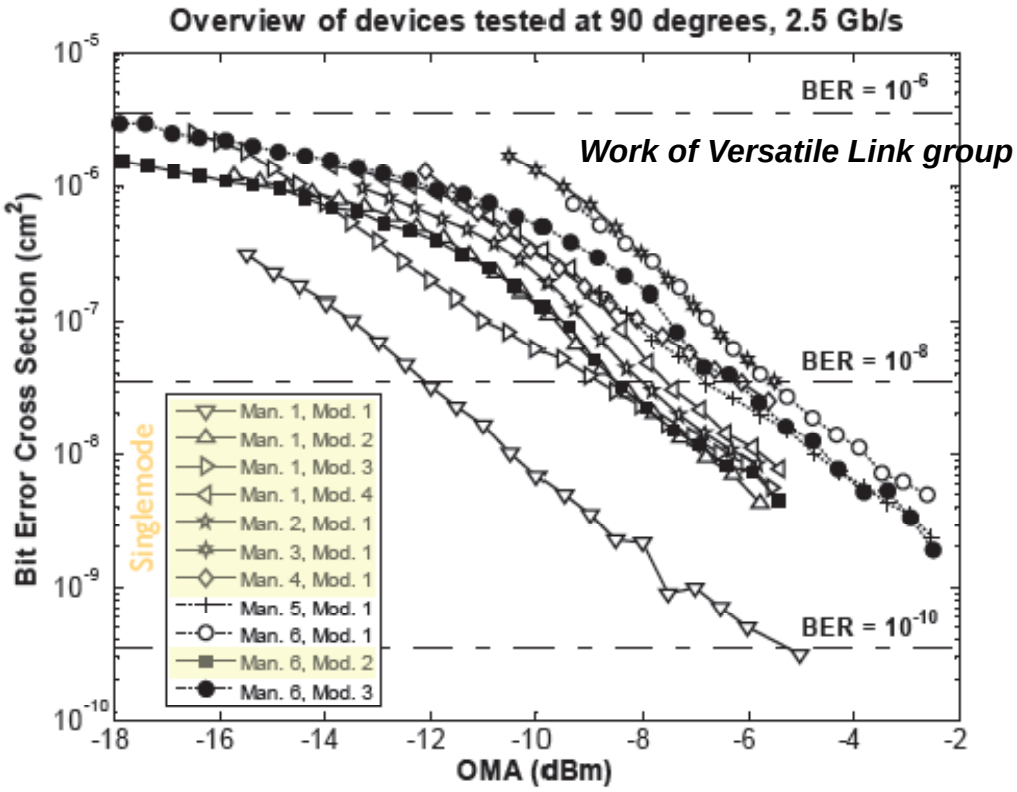
Absolute requirement is to prevent the readout chain against off-state due to SEU

→ Smooth run & operation

- 130 nm technology has higher SEU cross-section due to smaller geometry and smaller digital voltage
- Need to implement replica logic (triple vote logic) to increase SEU tolerances
- Replica logics consume 3 times more space and therefore has to be used where it is absolutely necessary
- P-I-N diodes and BER versus SEU has been studied by Versatile link teams

Measurements obtained with a test system at PSI





Cooling

One of the keys in the operational success!

Issues:

- Define the fluid coolant: CO_2 versus C_3F_8
- Service reuse and segmentation
- Manifolding and impact on the system
- Module design is directly dependent of the cooling choice
- Requirements and specifications to be well defined and written-up

Known:

• **C3F8:** We learnt a lot and still may be a lot to learn in long term operation!

→ Already a plant running BUT would it still be satisfactory in 10 years

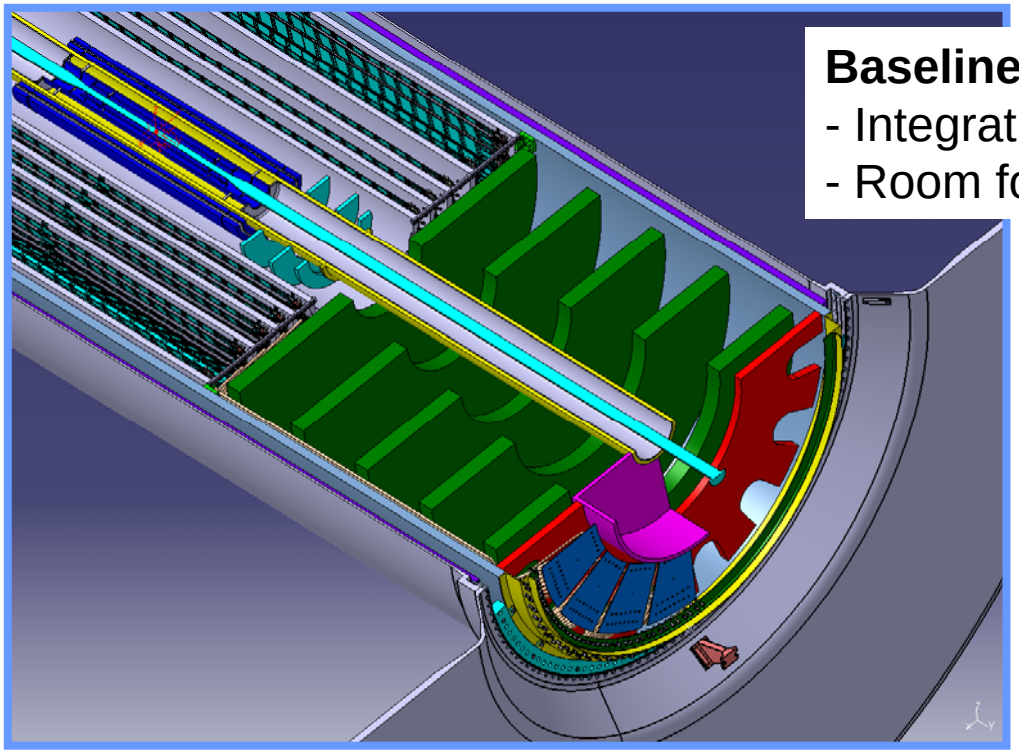
→ Need to improve the pressure drop in the exhaust to allow a temperature close to -30°C.

• **CO2:** LHCb, AMS have it! Looks good but not easily scalable to ID Upgrade but fine for IBL!

→ Less material for pipes, fittings and manifolds inside the ID volume

→ More safety margin for Si temperature.

Integration



Baseline:
- Integration of a 7 m long ID on the surface
- Room for insertable/removable b-layer

Issues:
• Layout not defined yet → Engineering is based on 1 layout (not optimized)
• Analysis (FEM) and dimensioning of main structural elements
• Critical points under investigation:

- Service space inside the ID volume critical between EC and Barrel strips and in the flange region
- End of barrel strip where SMC and dense service region is expected
- Cooling distribution and manifolds
- Thermal management OC and Poly-moderator
- Pixel optoboards position
- PPF1 connection area and arrangement

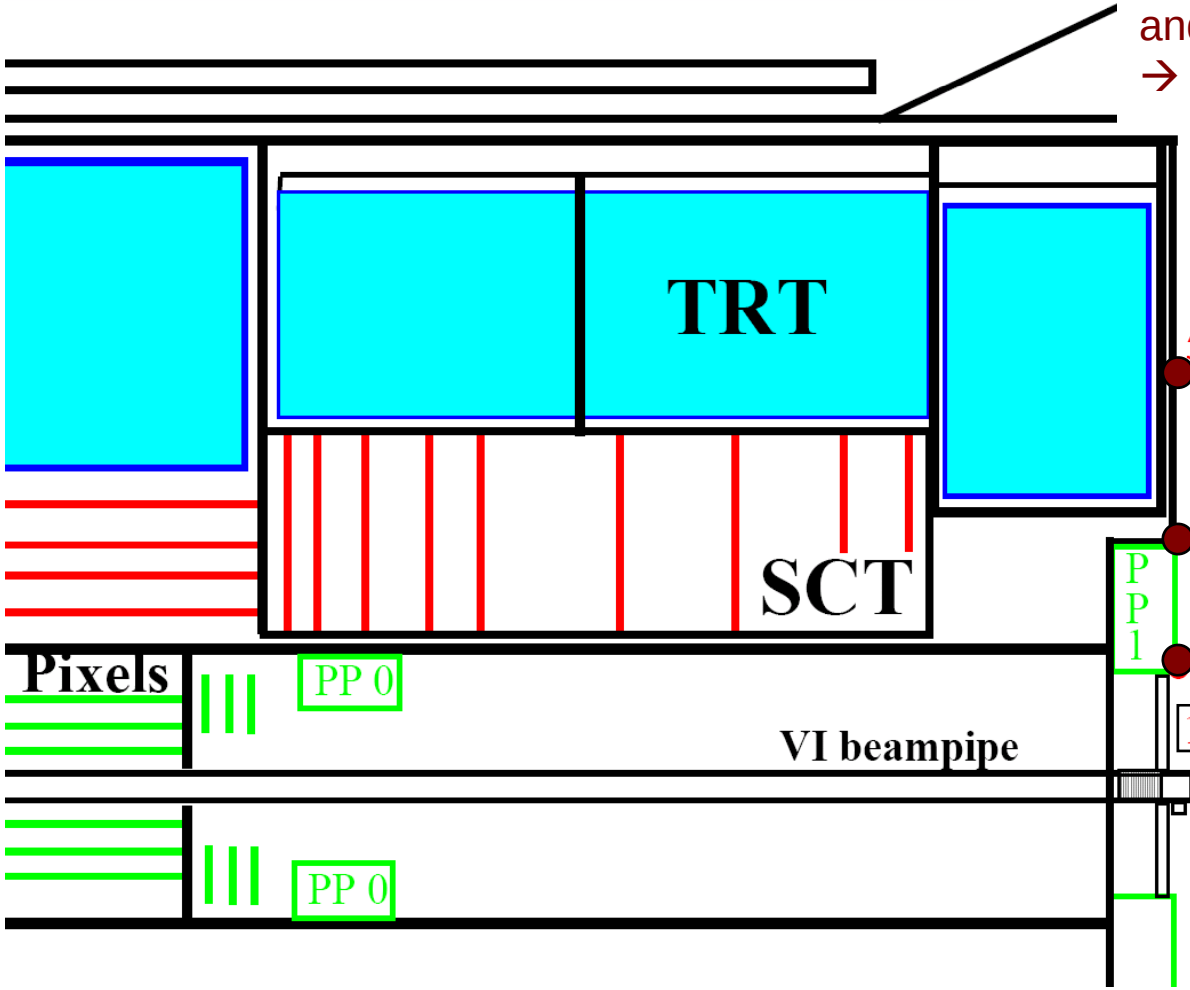
Radiation Level

LAr Calorimeter

Dose rates after 10 years of running and 30 days of cooling.

Issue:
Requirements to reuse much of ATLAS and the levels of activation anticipated:
→ greatly complicate installation

→ Minimize the tasks



	Pixels	SCT	TRT	LAr	VI
58 μSv/h:	37	8	4	8	1
Neut. act.:	29%	42%	29%	23%	0%
Services:	78%	86%	64%		

	Pixels	SCT	TRT	LAr	VI
73 μSv/h:	51	8	3	8	3
Neut. act.:	18%	41%	30%	25%	0%
Services:	59%	84%	63%		

	Pixels	SCT	TRT	LAr	VI
144μSv/h:	118	9	3	8	6
Neut. act.:	4%	41%	30%	25%	0%
Services:	9%	82%	62%		

→1 week for catA (<6mSv/y)
→ 2.5 weeks for catB (<15mSv/y)