



System implementation of a power distribution scheme based on DC-DC converters

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Outline

- Foreword and objectives.
- Distribution Scheme.
 - Proposed scheme.
 - On-module distribution.
 - Example of power-up sequence.
 - On-stave distribution.
 - Protection features.
- Integration issues.
- Noise issues.
- Conclusion.

Foreword

- Requirements:
 - To deliver increased amount of power.
 - To contain or even reduce thermal losses.
 - To minimize the material needed to bring the power in.
 - Cables
 - Boards
 - To be compatible with the environment
 - Radiation,
 - Magnetic field
 - Space

- All images shown here are examples for ATLAS SS staves

An Optimal DC/DC Scheme

- The scheme proposed here results from the optimization of several parameters in different converter topologies:
 - Conversion ratios less than 6 per stage.
 - Efficiency above 80% per stage.
 - Switch frequency that minimizes the size of components.
 - Granularity:
 - That enables scalable control system.
 - That provides individual control to each front-end ASIC.
 - Reduction of losses in cables and copper traces.
- This resulted in a two stage scheme based on a buck converter per module, followed by individual switch capacitors converters in each front-end ASIC.

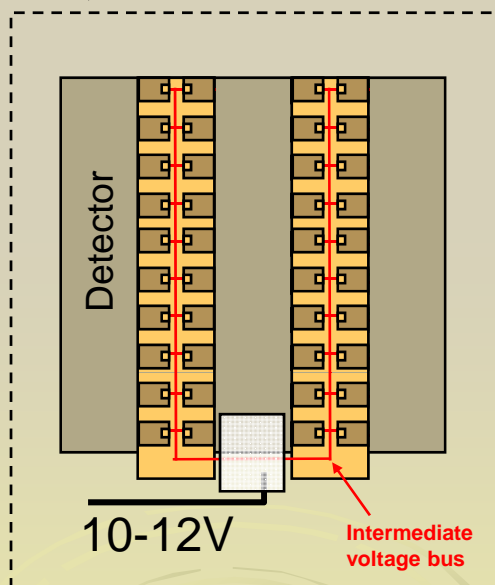
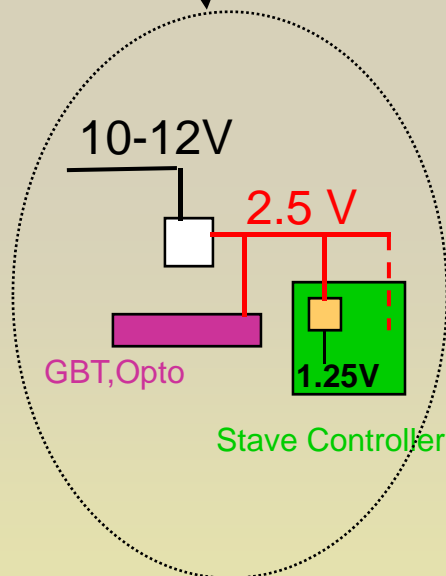
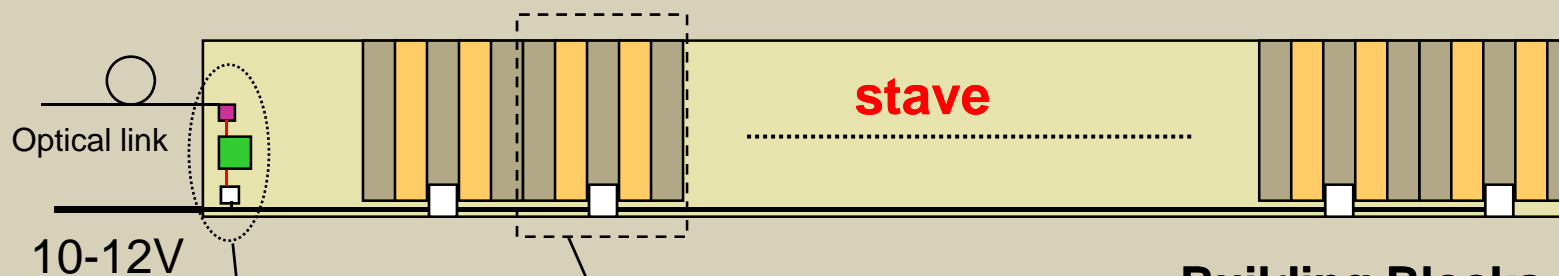
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Proposed distribution scheme (1)

Distribution based on 2 conversion stages

Example design shown for ATLAS short strip concept



Building Blocks

Stage1:

- Inductor-based buck
- $V_{in} = 10-12\text{ V}$
- $V_{out} = 2.5-1.8\text{ V}$
- $P_{out} = 2-4\text{ W}$

Stage2:

- On-chip switched capacitor
- $V_{in} = 2.5-1.8\text{ V}$
- Conversion ratio $\frac{1}{2}$ or $\frac{2}{3}$
- $I_{out} = 20-100\text{ mA}$

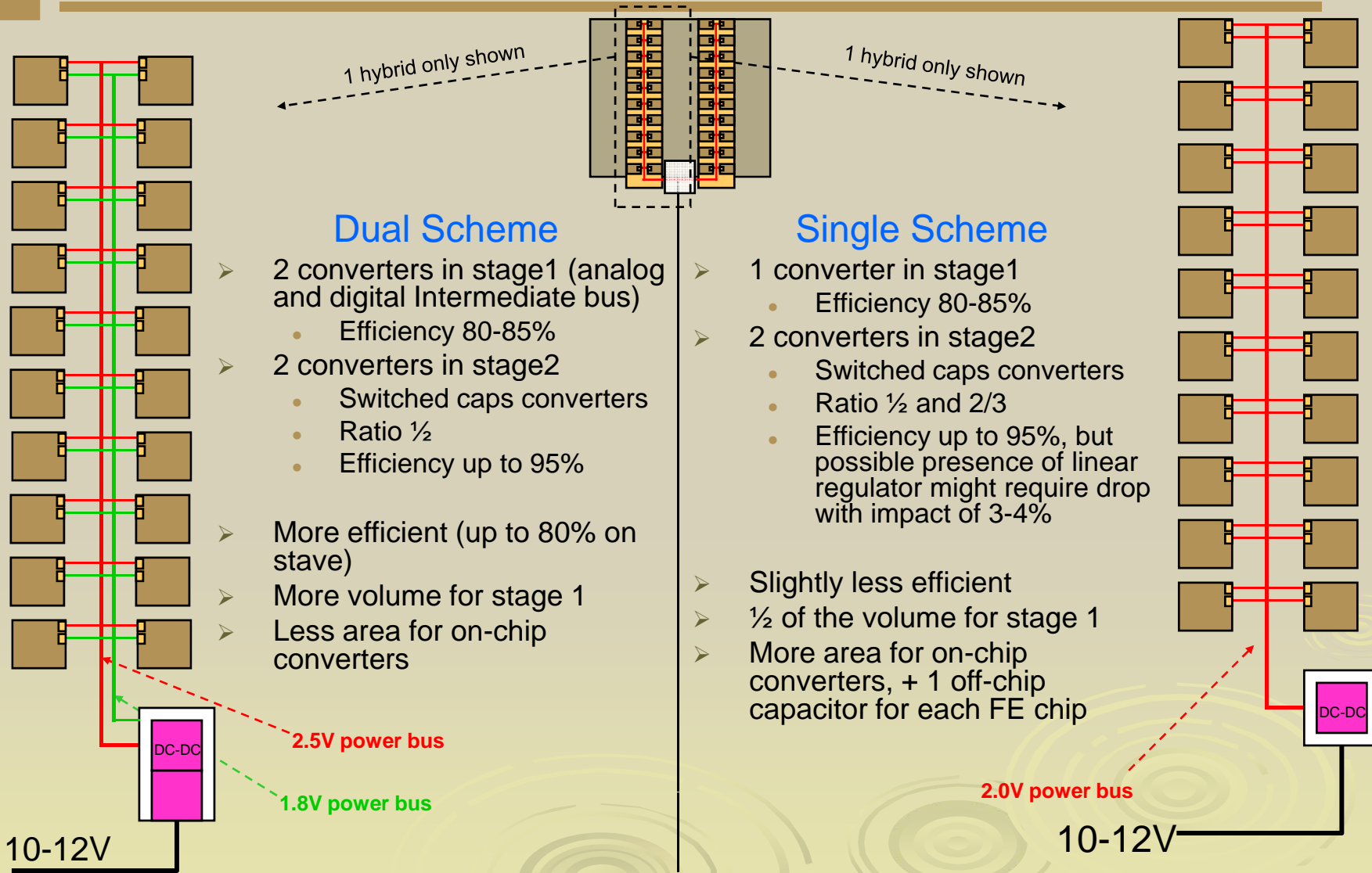
Same blocks can be combined differently to meet custom system requirements

Proposed distribution scheme (2)

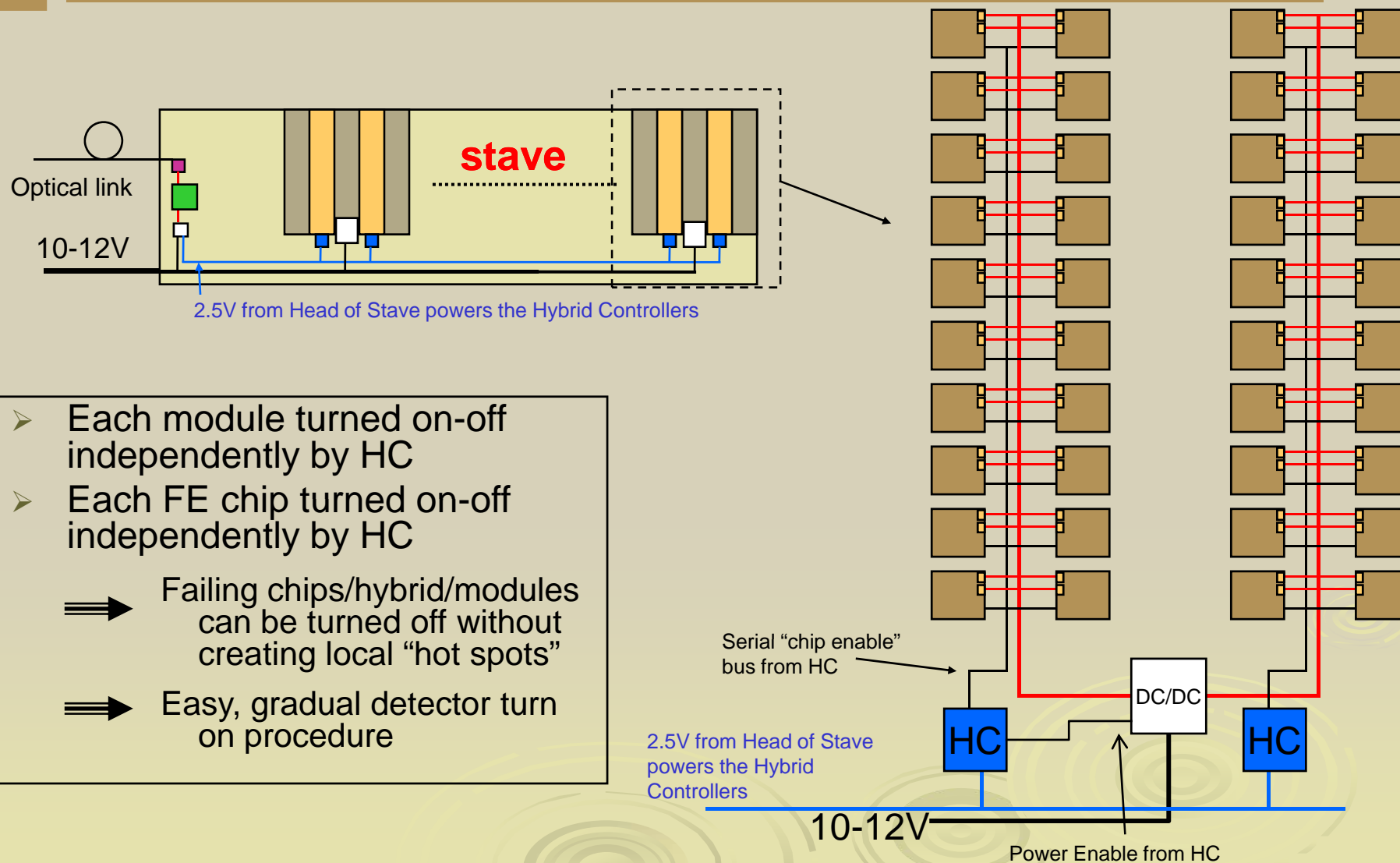
Summary of features

- Modular approach, very flexible – building blocks can be custom assembled following system requirements
- Very efficient to provide only required power to every system component, at appropriate voltage
- **Conventional grounding scheme**
- **Conventional detector powering**
- **We can build on the experience accumulated for LHC experiments (and others)**

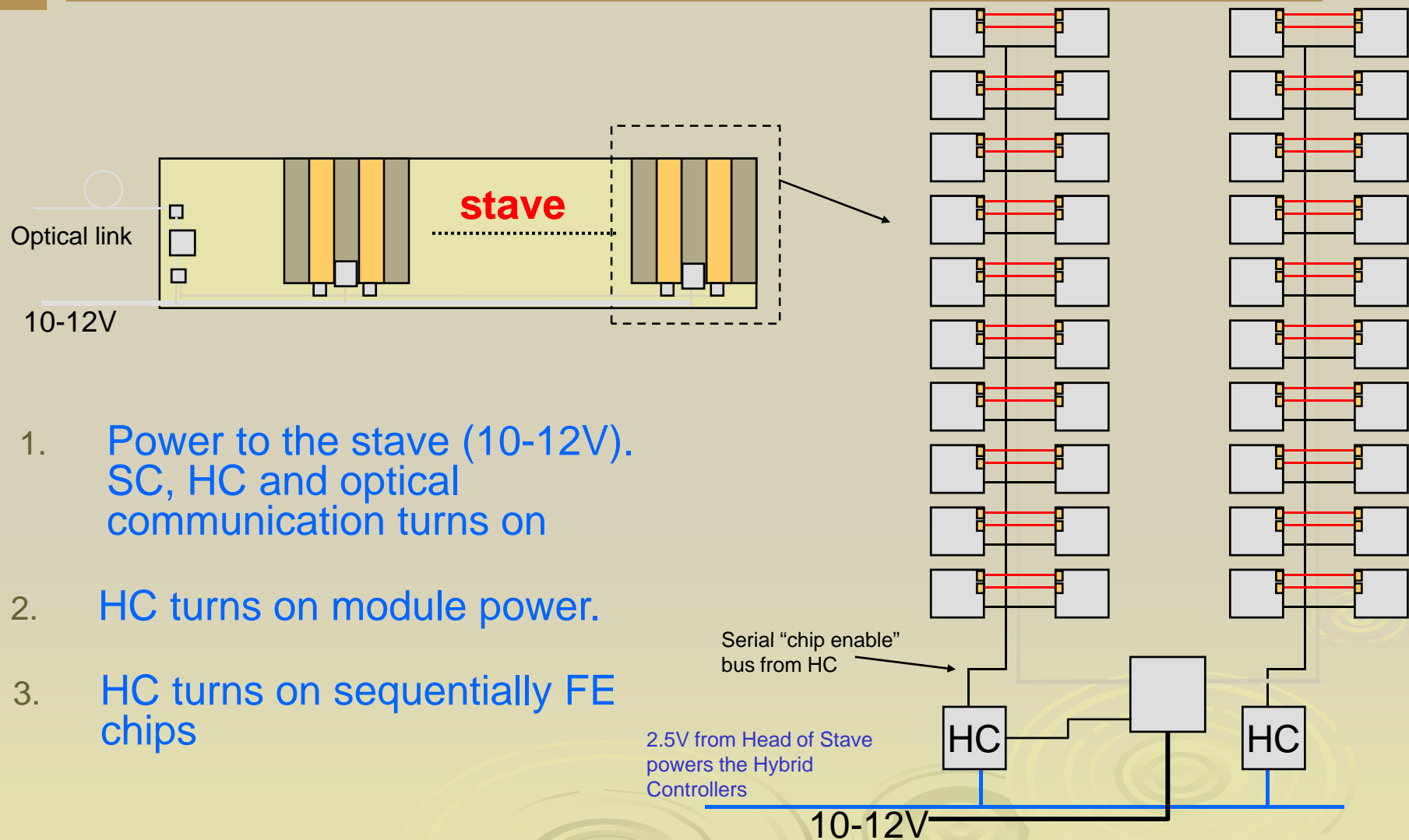
On-module distribution



Granularity and control



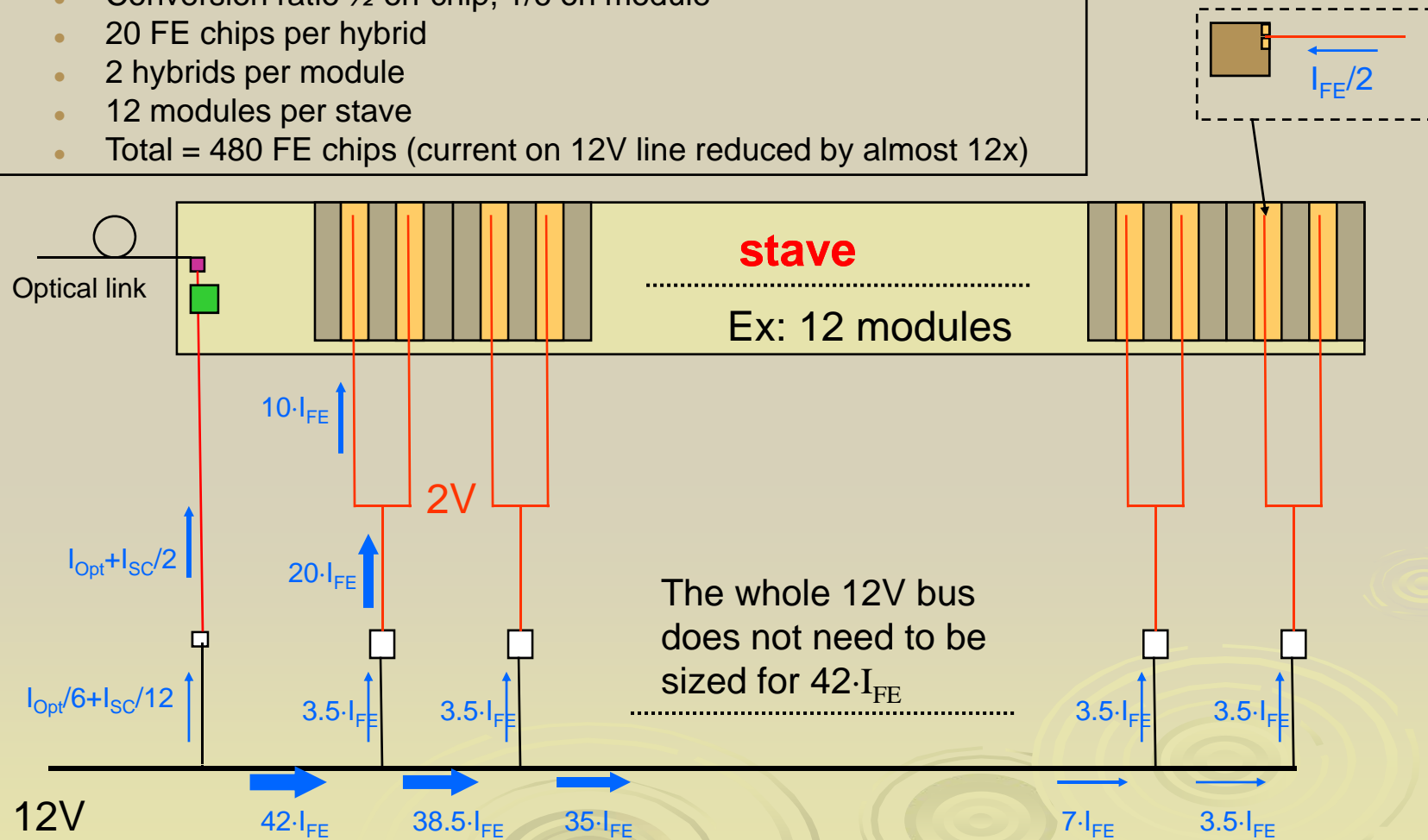
Example power-up sequence



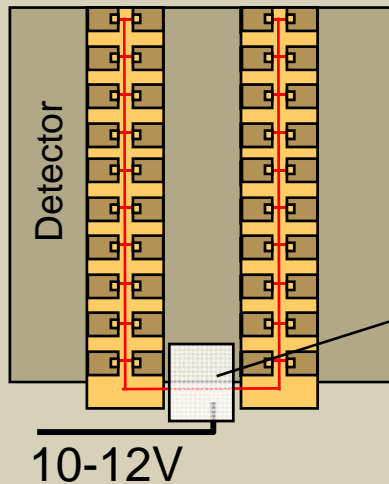
Power distribution on stave

➤ Hypothesis for this conceptual design:

- Conversion ratio $\frac{1}{2}$ on-chip, $\frac{1}{6}$ on module
- 20 FE chips per hybrid
- 2 hybrids per module
- 12 modules per stave
- Total = 480 FE chips (current on 12V line reduced by almost 12x)



Protection features



➤ Conversion stage 1 components:

- ASIC
- Coreless inductor
- SMD components

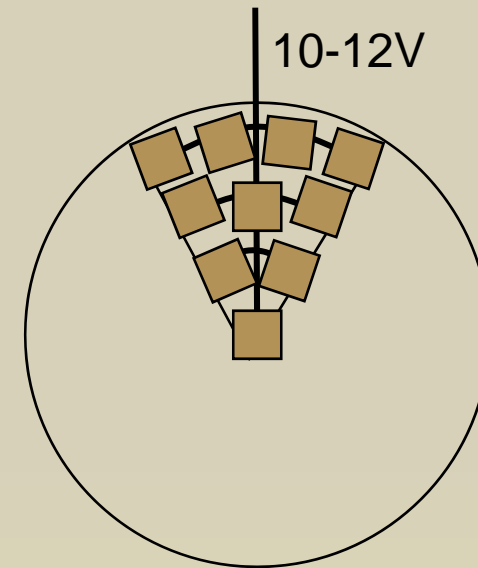
➤ **ASIC embeds soft-start and protections**

This is a routine in commercial components

- Over-current (cycle by cycle current control)
- Over-voltage
- Over-temperature (thermal shutdown protection)
- In case a problem is detected, the output is disabled and a flag is raised (power-good pin not asserted)

Distribution in end-caps

- The power distribution system described can be used in exactly the same way in the petal geometry of the end-caps (or by the way in any other geometry)

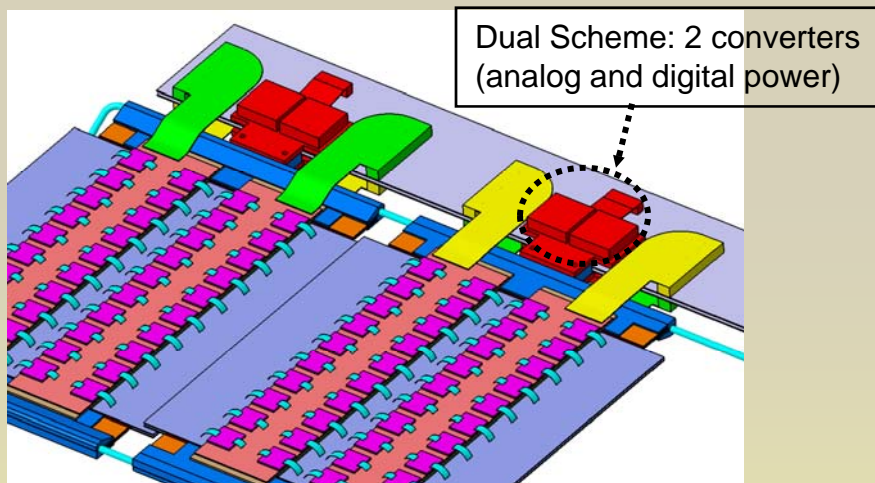
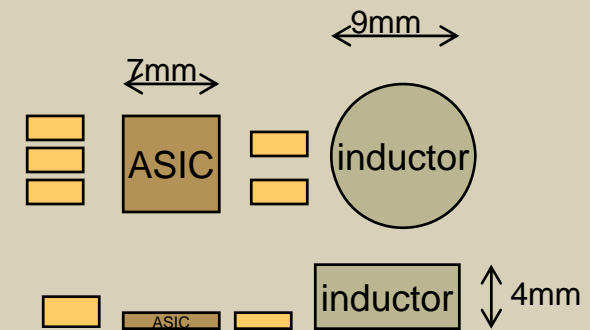


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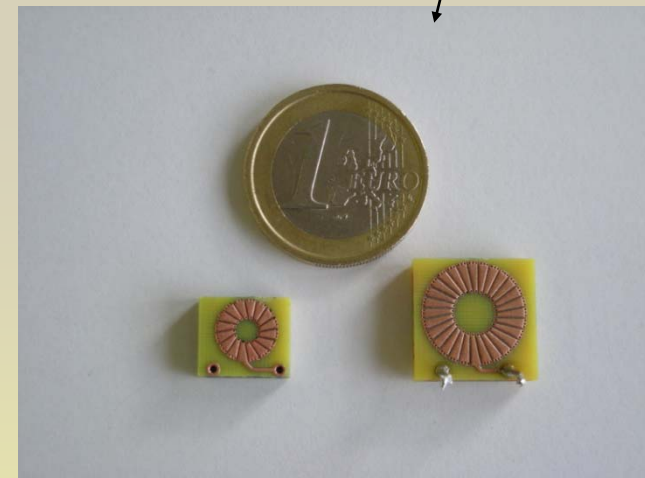
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Towards integration of stage 1

- Compact design
 - Reducing the size of the full converter
 - Components:
 - ASIC (in package 5x5 or 7x7 mm)
 - Inductor (4mm thick, 8-14mm diameter)
 - SMD components
 - Design compatible with tracker layout (evolving) in terms of area, volume, material budget, cooling



Integration in ATLAS SCT module design
From D.Ferrere - University of Geneva

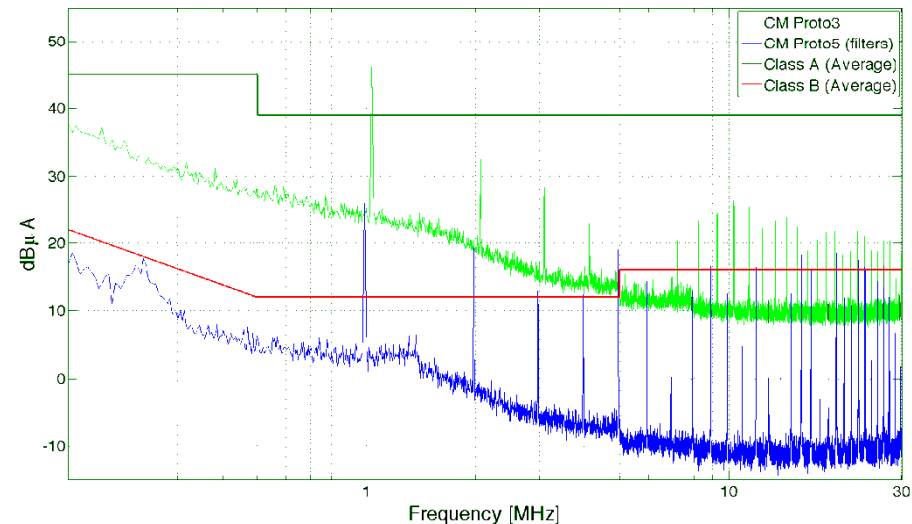
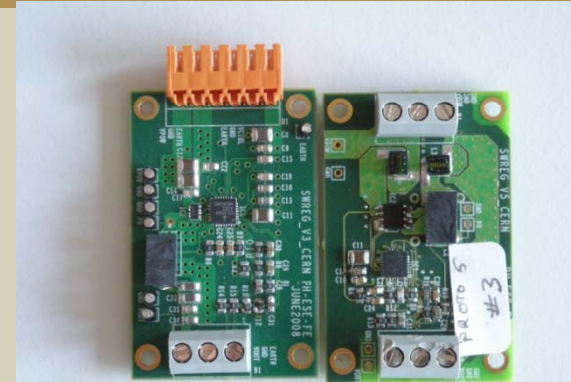


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EMC: noise issues

- 4 generations of converter prototypes using discrete commercial components developed
- Aim:
 - Understand noise sources
 - Study and verify appropriate countermeasures
 - Provide experiments with hardware for integration studies
 - Develop know-how for final integration
- Large decrease of noise observed on last prototypes
- With small pi-filters, noise level meets class-B of CISPR11



Output common mode noise (current) measured with the CERN-ESE standard test bench for prototypes 3 and 5 (difference: layout of the board, and presence of pi-filters in proto5)

Tests on the TOTEM Front-End



➔ Expose the front-end system to the DC-DC converter conducted noise (Common Mode and Differential Mode currents)

Proto#3 (discrete), Proto#4 (ASIC) supply the **2.5V DC** for both the analog and the digital circuits of the hybrid.

	Nominal noise	Proto #3 with long cables	Proto #3	Proto #4
VFAT #1	1.76	1.76	2.00	1.81
VFAT #2	1.81	1.73	2.00	1.77
VFAT #3	1.68	1.62	1.69	1.55
VFAT #4	1.56	1.59	1.93	1.67

- Measurements above a ground plane
- LISN connected at the input of the converter
- Output of the converter directly connected at the hybrid decoupling capacitors

EMC issues

- Converters emit conducted noise.
 - Can be reduced by proper layout.
- Converters emit radiated noise.
 - Inductor should be shielded.
 - Coupling strongly decreases with distance.
- Given this, front-end systems can be powered by DCDC converters close to the tracker modules.

Conclusions

- An optimal powering scheme based on DCDC converters was worked out.
- The scheme enables high granularity of the power distribution while minimizing the losses and the required material.
- The global efficiency on stave can be between 75% and 80%.
- The control of power nodes is more flexible than in LHC systems: nodes and modules can be individually powered from a control station.
- The scheme remains compatible with today's grounding and biasing of the detector.
- The technology to design converters that are compatible with B field, radiation and that emit low noise is today available.