Buck DC-DC design and implementation

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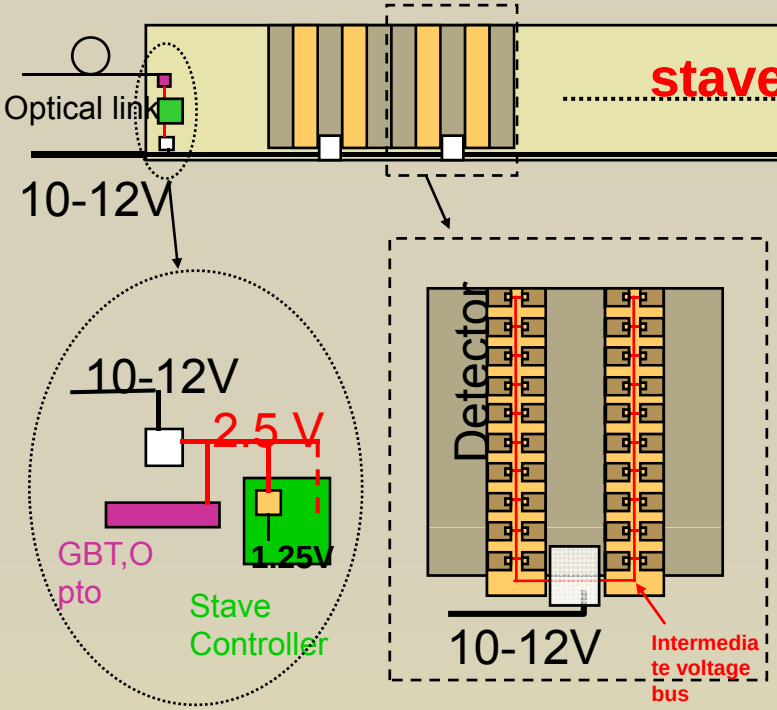
Outline

- Introduction
- Conversion stage 1
  - Semiconductor technology
  - Inductor design
  - EMC (conducted and radiated noise)
  - ASIC design
  - Integration
- Conversion stage 2 (on-chip)
  - Different conversion ratios
  - Efficiency and area
- Conclusion

Proposed distribution scheme (1)

Distribution based on 2 conversion stages



Slide taken from previous talk of G. Blanchot

Building Blocks

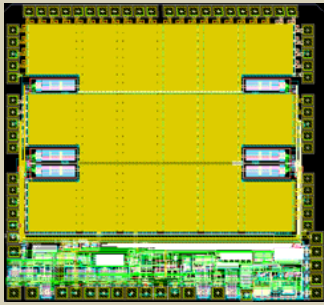
Stage1:
- Inductor-based buck → Use of air core inductor
- Vin = 10-12 V → Use of high voltage technology
- Vout = 2.5-1.8 V
- Pout = 2-4 W

Stage2:
- On-chip switched capacitor → Use front end technology
- Vin = 2.5-1.8 V
- Conversion ratio ½ or 2/3
- Iout = 20-100 mA

Issues:
- High efficiency
- Low noise

Semiconductor technology (1)

- The converter requires the use of a technology offering both low-voltage and high-voltage (15-20V) transistors
- Properties of high-voltage transistors largely determine converter's performance
  - Need for small Ron, and small gate capacitance (especially Cgd) for given Ron!
- Survey of available options covered 5 technologies
- Best results with 0.25um SGB25V GOD technology from IHP

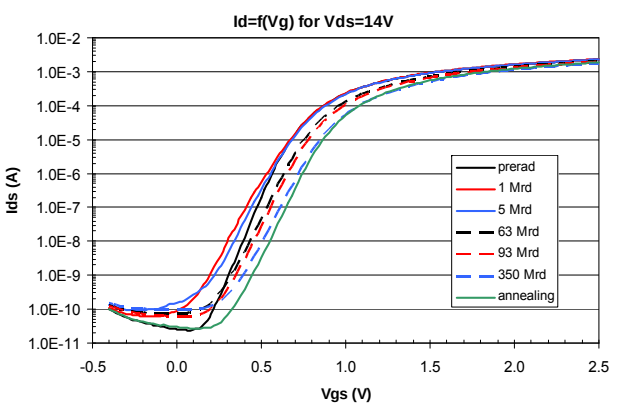


Prototype in 0.35µm

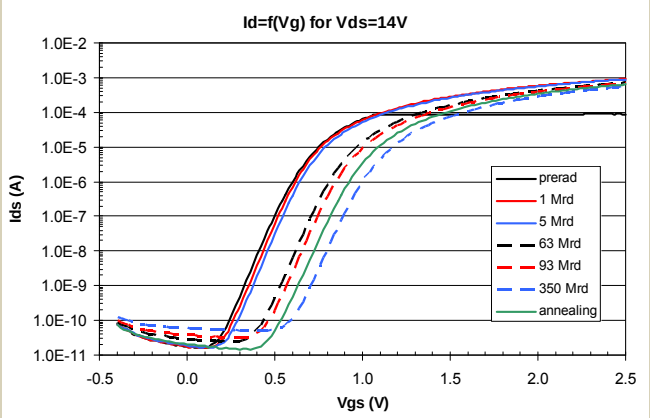
Tech Node (um)	Trans type	Max Vds (V)	Vgs (V)	Tox (nm)	Ron*um (kOhm*um)	Status
0.35	Lateral Vertical	14 80	3.5 3.5	7 7	8 33	Tested
0.18	Lateral	20	5.5	12	4.75	Tested
0.13	Lateral	20	4.8	8.5	7	Tested
0.25	Lateral	20	2.5	5	4-5	Tested
0.18	Lateral	20	1.8	4.5	9.3	First MPW April 09

Semiconductor technology (2)

X-ray irradiation (TID) up to 350Mrd



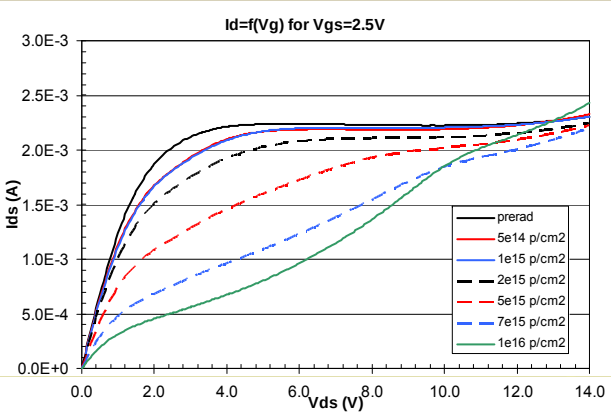
NMOS, switching bias



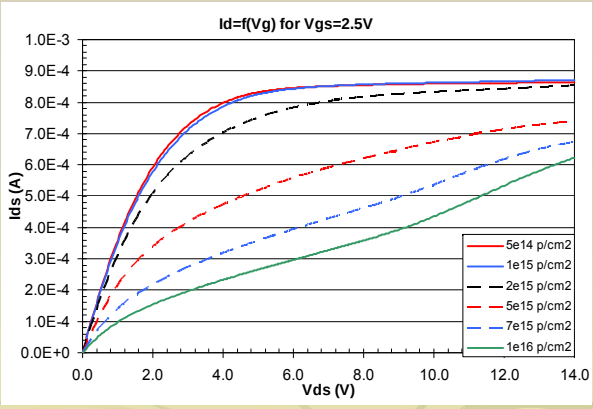
PMOS, WC bias

- Manageable Vth shift
- Small or no leakage current increase
- Ron decrease <20% (NMOS) and <40% (PMOS)

Proton irradiation (displacement) up to 10^{16} p/cm^2



NMOS, floating bias



PMOS, floating bias

- Negligible Vth shift
- No leakage current increase
- At $5 \cdot 10^{15}$ p/cm2, Ron decrease <60% (NMOS) and <80% (PMOS)

Semiconductor technology (3)

- One technology (0.25µm node) has demonstrated radiation tolerance compatible with benchmark:
  - NMOS Ron decrease below 60% for $2.5 \cdot 10^{15}$ n/cm^2 (1MeV equivalent)
  - Vth shift manageable (below 200mV for NMOS, 400mV for PMOS @ 350Mrd)
  - Negligible leakage current with TID
  - Overall, radiation could affect converter performance as small drop of efficiency (below 5%)
- One technology (0.13µm node) could satisfy requirements for installation further from collision point, where fluence is limited below $1 \cdot 10^{15}$ n/cm^2 (1MeV equivalent)
- The other 2 technologies are less performant and will not be considered further
- **Conclusion**:
  - While starting prototype work in the 0.25um technology, another 0.18µm technology will be tested in 2009 (we look for a second source with comparable radiation performance)

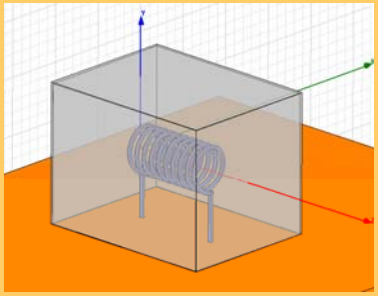
Inductor design: requirements

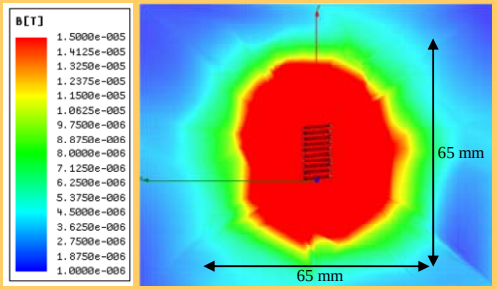
- Coreless (no ferromagnetic material)
- Value: from 150 to 700nH (this is feasible with air-core)
- Compact for high integration
- Light for low material budget
- With small ESR both in DC and AC (at the switching frequency) for high efficiency
- It needs to be shielded for low radiated noise

Air core inductors

- We simulated (Ansoft Maxwell 3D) the magnetic field from inductors of different type, and the effect of shielding

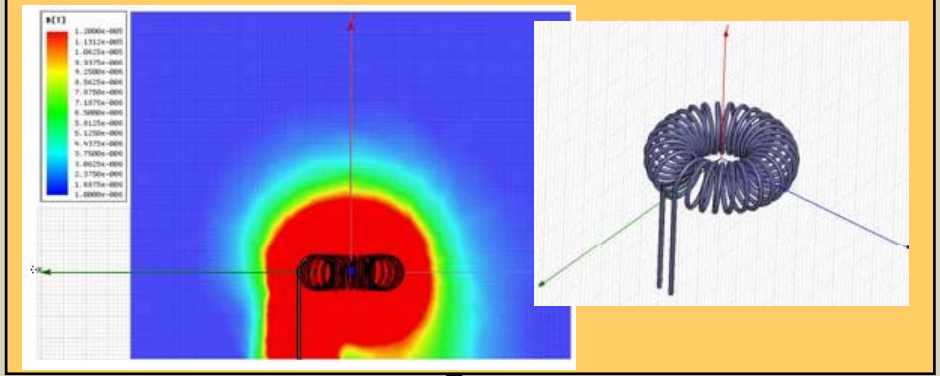
An unshielded solenoid radiates considerably the surrounding space

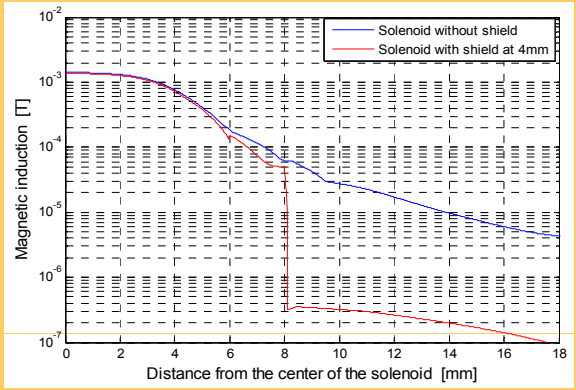




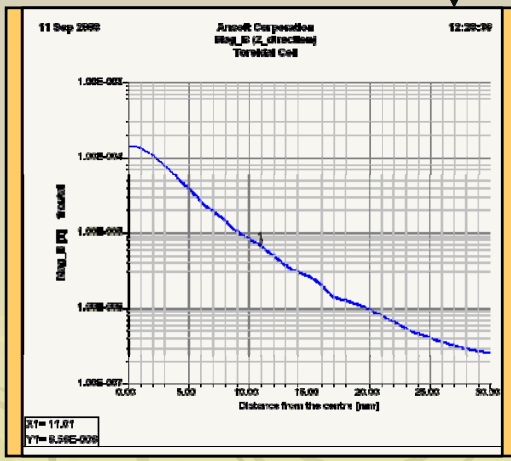
A 100µm Al shield is placed 4mm far from the solenoid not to affect the inductance value (and create losses)

➢Air-core toroid contains the main magnetic field (the one determining the inductance value)…





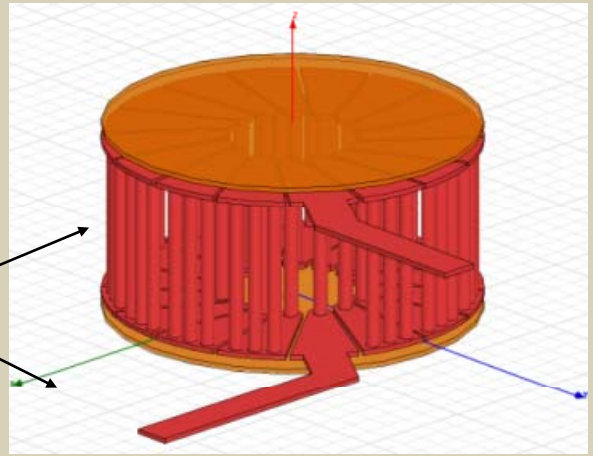
The shield is very effective in decreasing the EM radiation
But the volume is largely increased
AND this structure is mechanically unstable as it is…

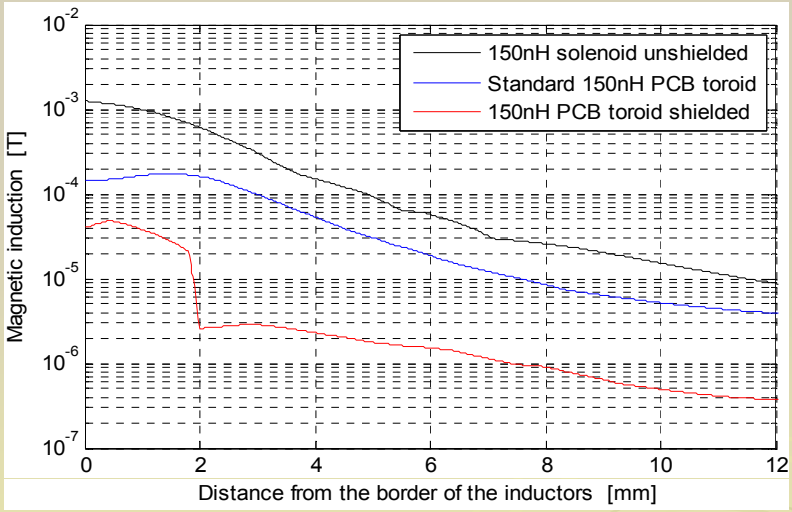


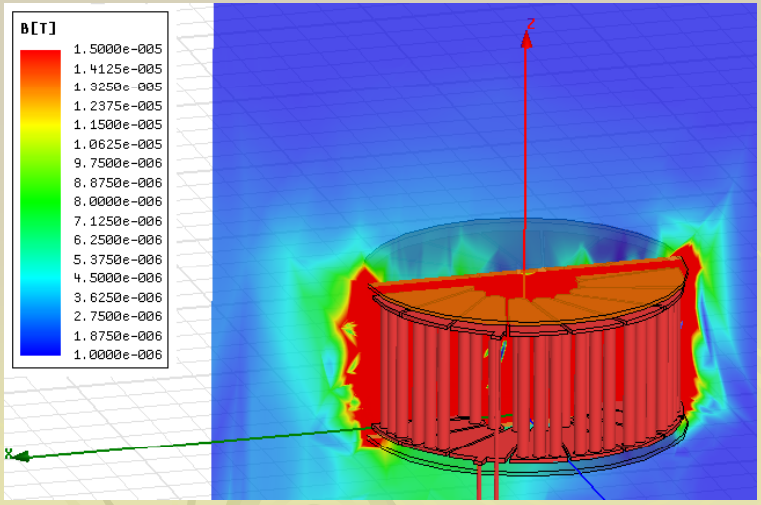
… but it still radiates because of the one-loop current path around its center
This can in principle be shielded effectively by "wrapping" the inductor in an Al layer

“Optimized” PCB toroid (1)

- Custom design exploiting PCB technology: easy to manufacture, characteristics well reproducible
- Design can be optimized for low volume, low ESR, minimum radiated noise
- With the help of simulation tools (Ansoft Maxwell 3D and Q3D Extractor), we estimated inductance, capacitance and ESR for different designs. This guided the choice of the samples to manufacture as prototypes
- The addition of two Al layers (top, bottom) shields the parasitic radiated field efficiently

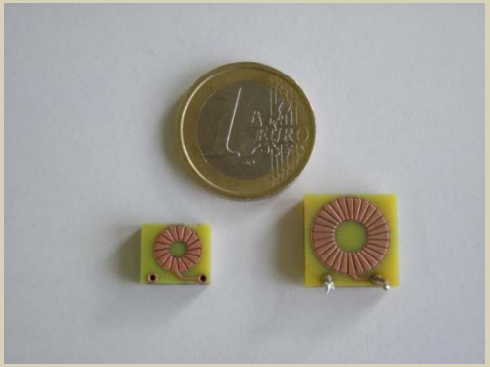


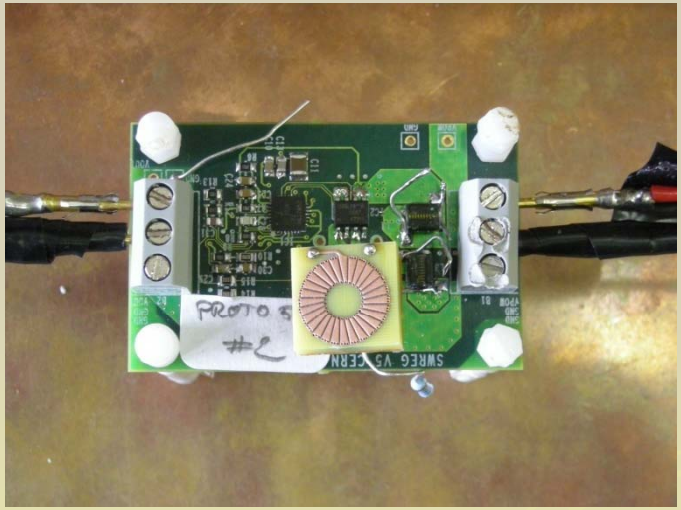


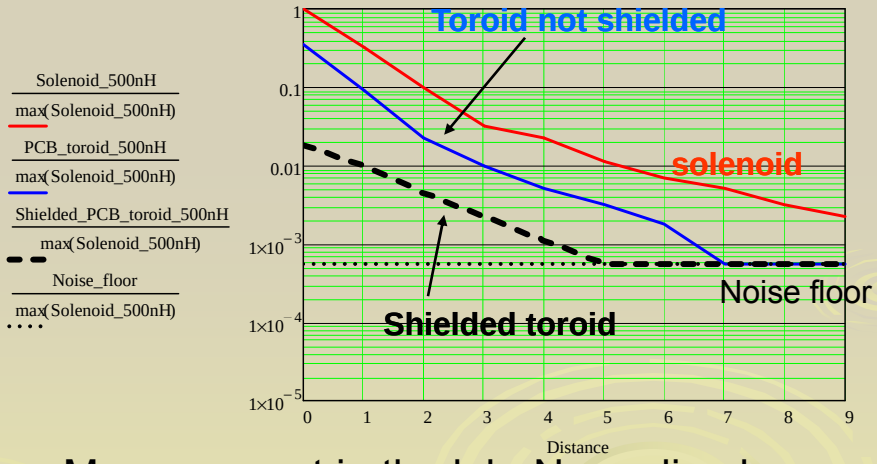


“Optimized” PCB toroid (2)

- First samples manufactured at the CERN PCB shop
- Inductance, shield efficiency, ESR in agreement with simulation
- ESR can be decreased still by 2x by “filling” the vias – this has not yet been done
- Now that the concept has been validated, we prepare for a prototype run with all the final characteristics (ESR, volume, shield material)



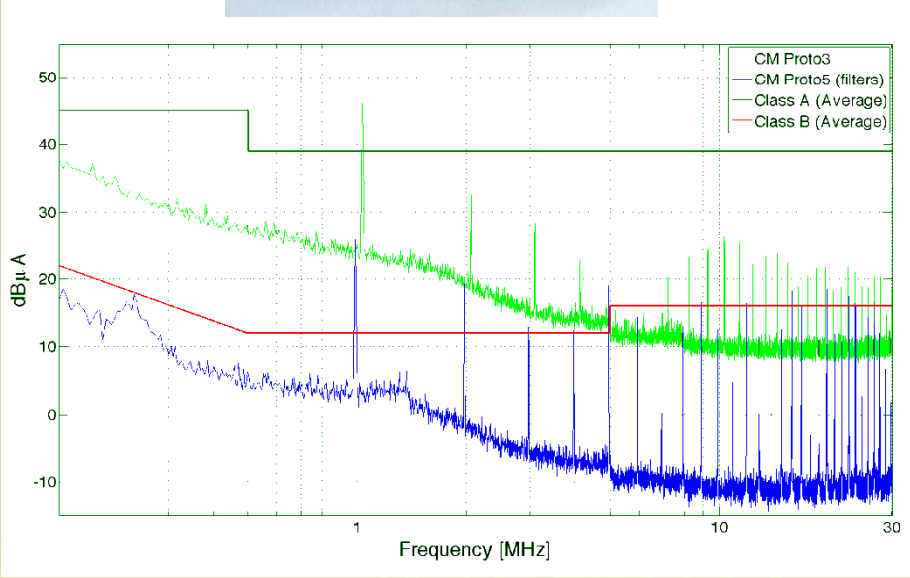




Measurement in the lab: Normalized current induced in 1 Cu loop at increasing distance from the inductor (cm)

EMC: conducted noise

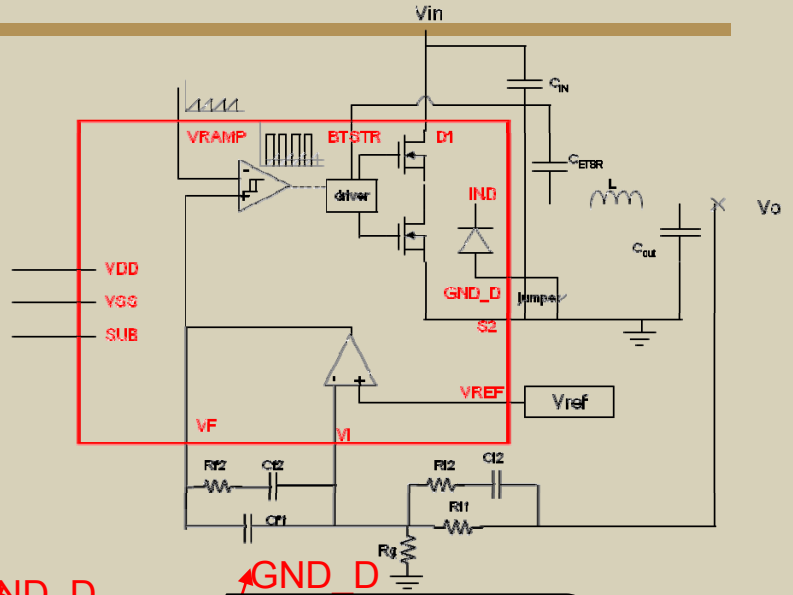
- 4 generations of converter prototypes using discrete commercial components developed
- Aim:
  - Understand noise sources
  - Study and verify appropriate countermeasures
  - Provide experiments with hardware for integration studies
  - Develop know-how for final integration
- Large decrease of noise observed
- With small pi-filters, noise level meets class-B requirements of CISPR11 (voltage on line and neutral)

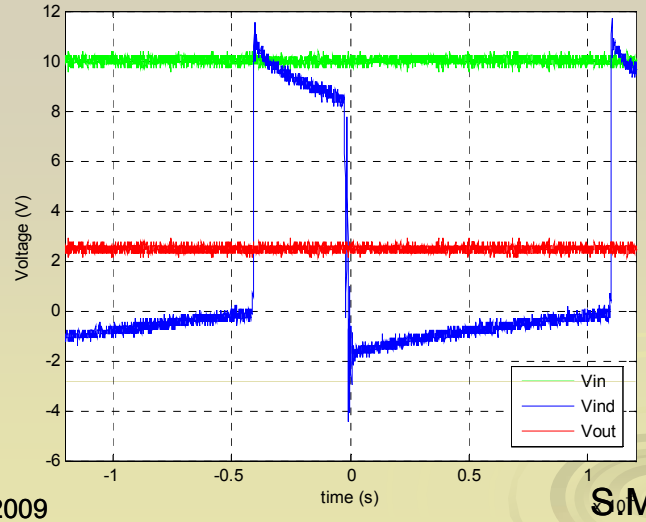


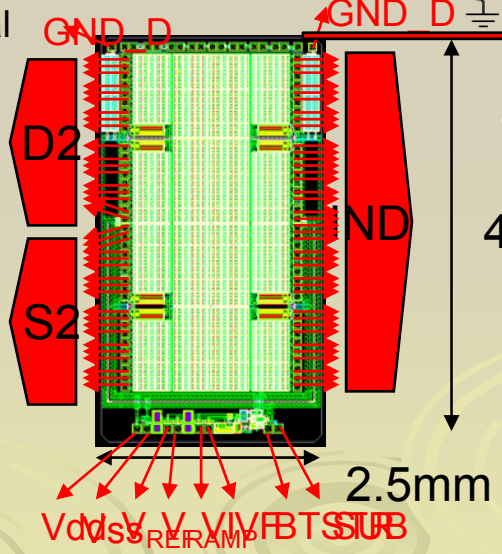
Output common mode noise (current) measured with the CERN-ESE standard test bench for prototypes 3 and 5 (difference: layout of the board, and presence of pi-filters in proto5)

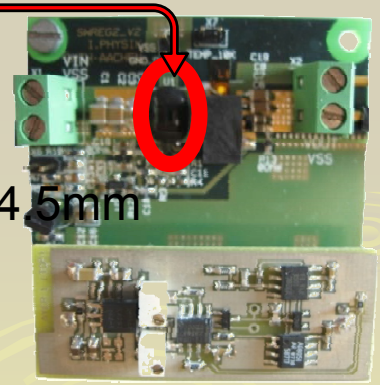
ASIC development – 1st generation

- First generation prototype (include only fundamental building blocks)
- Manufactured in AMIS 0.35µm
- Features:
  - VIN and Power Rail Operation from +3.3V to +24V
  - Fast Transient Response - 0 to 100% Duty Cycle
  - 14MHz Bandwidth Error Amplifier with 10V/µs Slew Rate
  - External oscillator Programmable from 250kHz to 3MHz
  - External voltage reference (nominally (1.2V)
- Submitted March 08
- Mounted on PCB
- Test result presented in TWEPP08
- Demonstrated working function of the fundamental building blocks







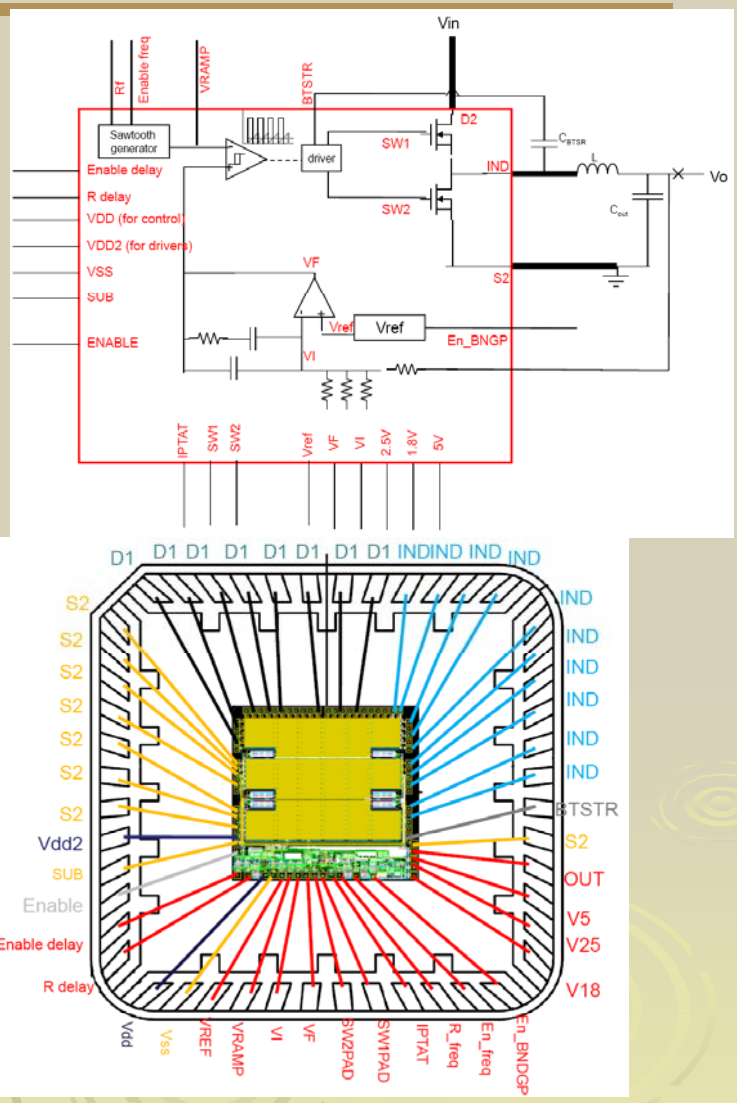


The PCB was designed, produced and assembled in RWTH, Aachen thanks to W. Karpinski and K. Klein

ASIC development – 2nd generation

- Second generation prototype
- Still manufactured in AMIS 0.35µm
- Features:
  - VIN and Power Rail Operation from +3.3V to +12V
  - Selectable output voltage (nominal 2.5V)
  - Maximum output current: 3A
  - Fast Transient Response - 0 to 100% Duty Cycle
  - 14MHz Bandwidth Error Amplifier with 10V/µs Slew Rate
  - Internal oscillator fixed at 1Mhz, programmable from 400kHz to 3MHz with external resistor
  - Internal voltage reference (nominally (1.2V)
  - Remote Voltage Sensing with Unity Gain
  - Programmable delay between gate signals
  - Integrated feedback loop with bandwidth of 20Khz
- Submitted December 08, expected back in April 09
- Mounted in 7x7mm QFN package

- Third generation will be in the IHP 0.25µm technology
- It will be a simple buck
  - Refined comparison with 2-phase interleaved with V-divider (alternative topology), using also prototypes, has indicated little advantage of this latter topology at the small load currents foreseen for a module



ASIC development – future

- Third generation will be in the IHP 0.25μm technology

  Tests shows that this technology has better performance
  - for radiation tolerance (total dose and ions)
  - for efficiency (lower on-resistance and capacitance)

- The first integration is foreseen for May 13th

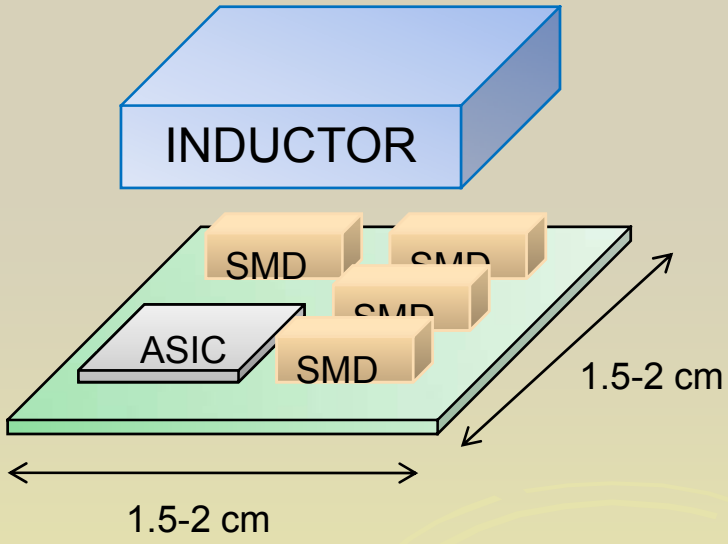
  It will be a simple buck
  - Refined comparison with 2-phase interleaved with V-divider (alternative topology), using also prototypes, has indicated little advantage of this latter topology at the small load currents foreseen for a module

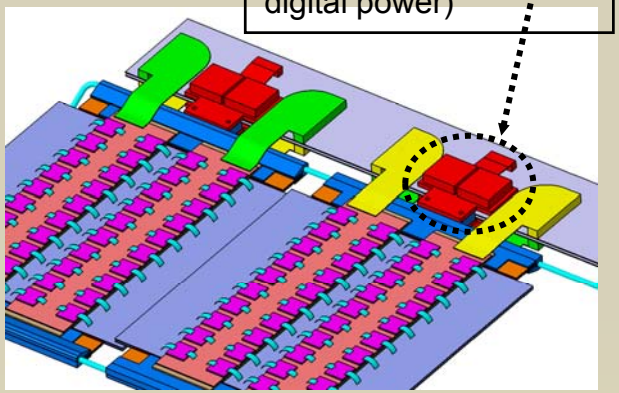
- A second integration is foreseen for November 2009

  It will be a buck including all the blocks with protections and soft start.

Towards integration

- Compact design
  - Reducing the size of the full converter
    - Components:
      - ASIC (5x5 or 7x7 mm)
      - Inductor (4mm thick, 8-14mm diameter)
      - SMD components
  - Design compatible with tracker layout (evolving) in terms of area, volume, material budget, cooling





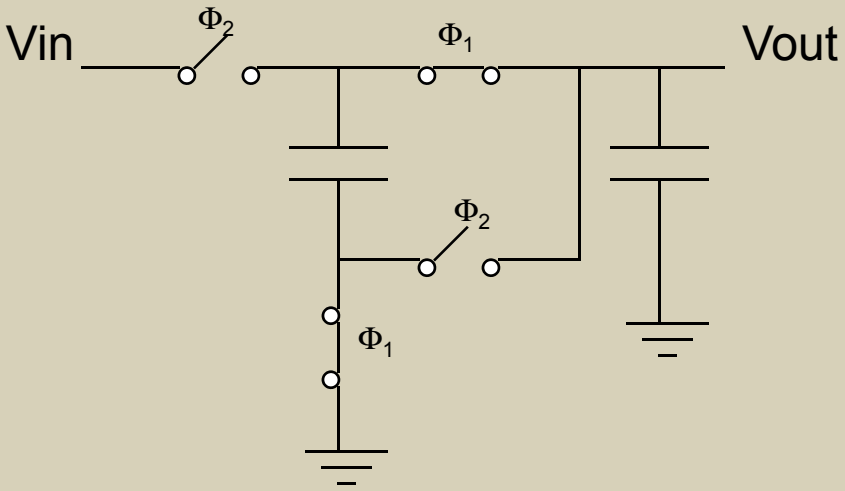
Integration in ATLAS SCT module design
From D.Ferrere
University of Geneva

Outline

- Proposed scheme using DC-DC converters
- Conversion stage 1
  - Semiconductor technology
  - Inductor design
  - EMC (conducted and radiated noise)
  - ASIC design
  - Integration
- Conversion stage 2 (on-chip)
  - Different conversion ratios
  - Efficiency and area
- Conclusion

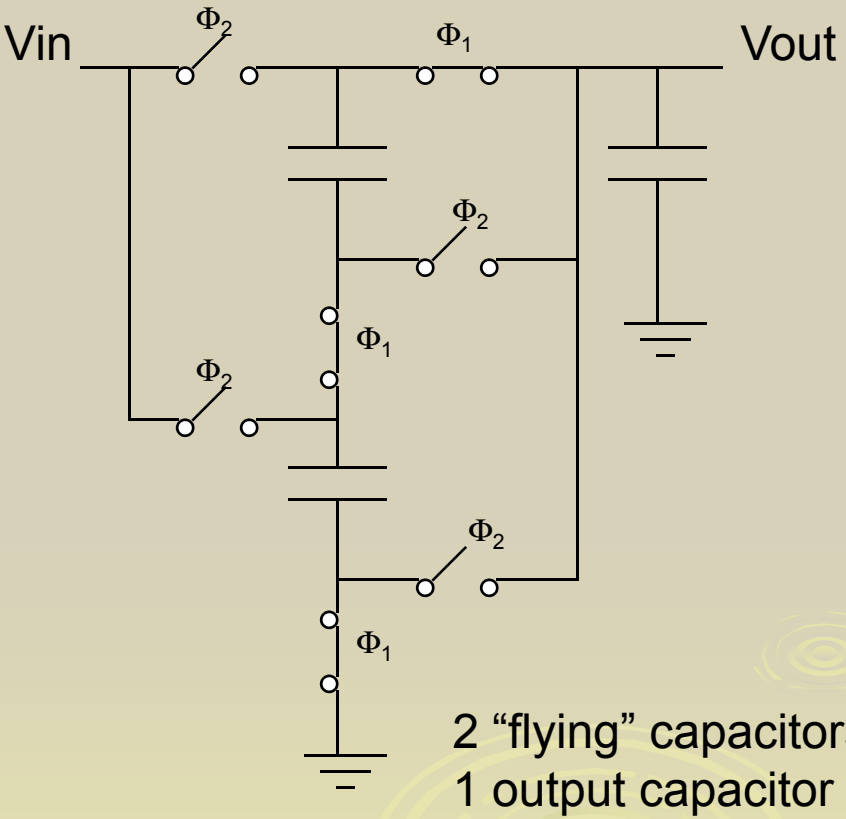
Different conversion ratios

½ Conversion



1 “flying” capacitor
1 output capacitor
4 switches

2/3 Conversion



2 “flying” capacitors
1 output capacitor
7 switches

Efficiency, area

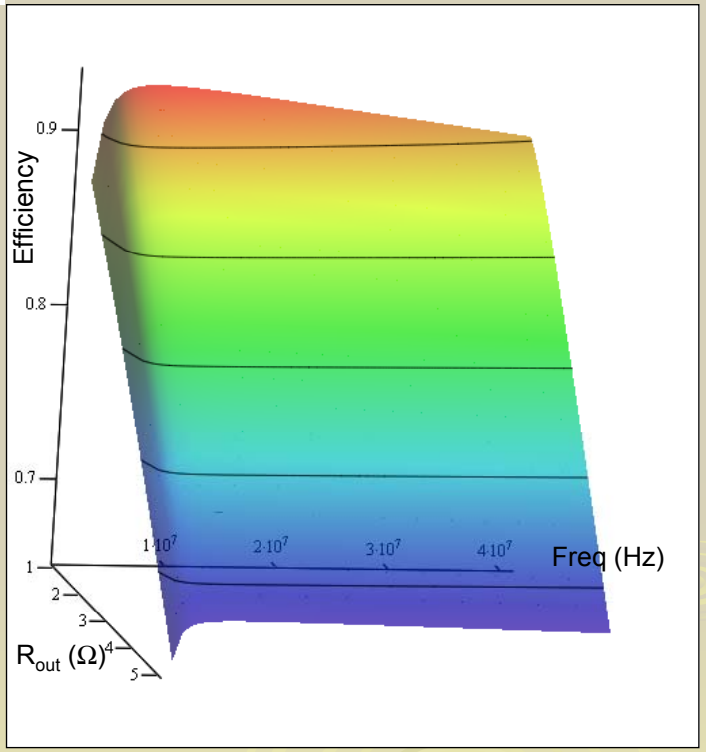
Efficiency:

- Analytical model developed and integrated in mathcad for conversion ratio ½
  - It allows for estimating efficiency vs Rout and Frequency
  - Good agreement with Spice simulation in IBM 130nm technology (using I/O transistors)
- Same work planned for conversion ratio 2/3

Area:

- Estimate of on-chip area
  - Dependent on required efficiency
  - In the IBM 130nm technology, using I/O transistors, and for an efficiency ≥90%, it can be of the order of
    - 200x100 μm for ratio ½
    - 200x200 μm for ratio 2/3
- Off-chip capacitors
  - Size around 100-200 nF looks appropriate

Example:
Efficiency for a converter ½ in IBM 130nm technology
Vin=1.9V, Vout=0.93V, Iout=60mA, C=100nF



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Conclusion

- Power distribution using DCDC converters is conventional and very flexible
  - System can be “customized” using a set of building blocks (buck converter for stage 1, switched capacitor converters on-chip, possibly even linear regulators)
- Main difficulties in the development of a custom buck converter for stage 1 are being solved
  - Semiconductor technology satisfying radiation requirements has been found
  - Inductor design has been optimized and experimentally verified
  - Techniques for ASIC design are being learnt, and first prototypes have been developed
  - Large progress in understanding noise issues has been made and verified on prototypes (meeting class B requirements)
- Main focus of our activity for 2009:
  - Design of the ASIC buck converter in the IHP 0.25μm technology
  - Integration of ASIC, PCB inductor and SMD components in compact DCDC converter boards representative of the final integration level achievable
  - Improve understanding and working tools for switched capacitor converters (especially ratio 2/3). Further involvement will depend on the activity of other groups