Serial Powering System Architecture

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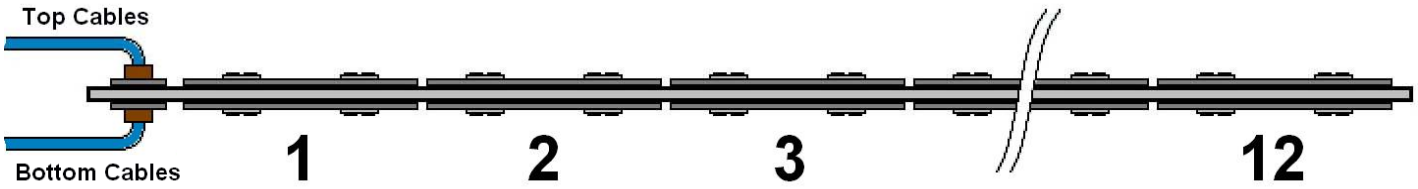
On behalf of the SP Community

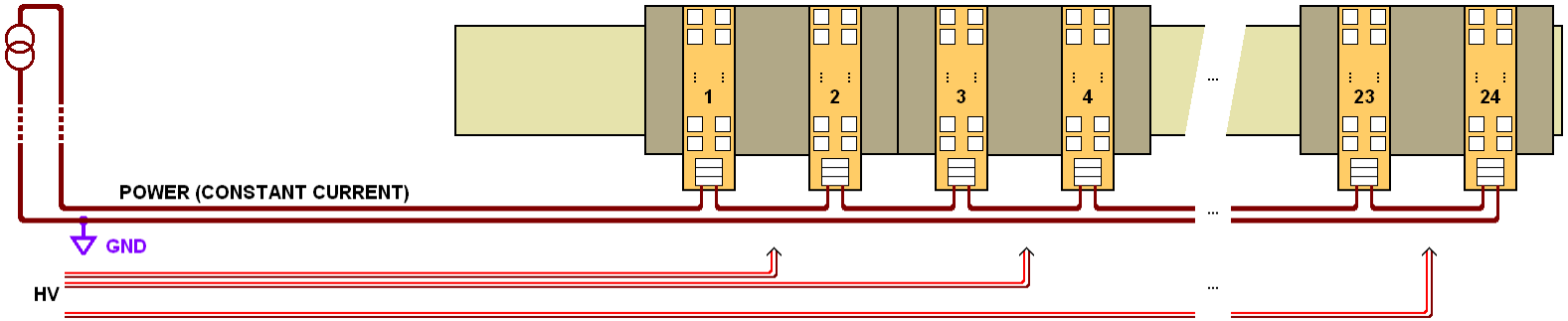
Acknowledgement: many figures prepared by Richard Holt, RAL

Outline

- SP Architecture: Modules and Staves
- System Tests
- Shunt Architectures
- Efficiency, DC-DC and 130nm
- SP and endcap geometries
- AC coupled (M)LVDS
- Serial Powering and HV
- Protection Schemes
- First Results from ABCN Integrated Shunts
- Summary and Next Steps

SP Stave Architecture





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SP Stave Architecture

For strips, the stave comprises two separate planes:

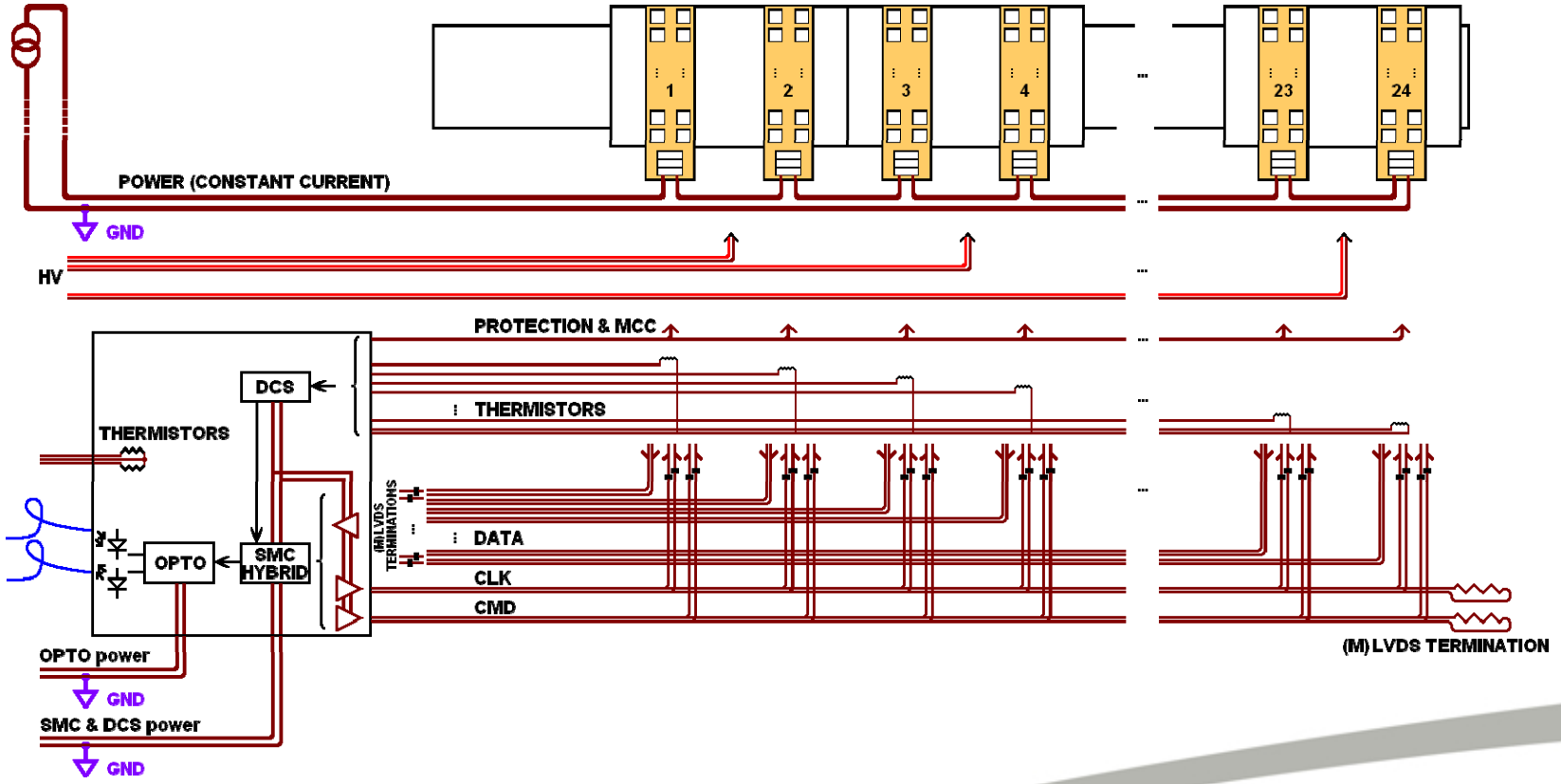
- The top and bottom faces have separate current loops
- The grounds of the two faces are connected at the stave end

Features common with pixels:

- CLK and COM are AC coupled on each hybrid
- DATA is AC coupled at the stave end
- Protection can be included such that one failed hybrid does not disturb the remainder
- DCS can monitor hybrid temperatures, the shunt current and (ideally) hybrid voltages

Depending upon design choices, the total voltage across each serial powering loop can be as low as 24 x 1V for strips, less for pixels (shorter stave)…

SP Stave Architecture



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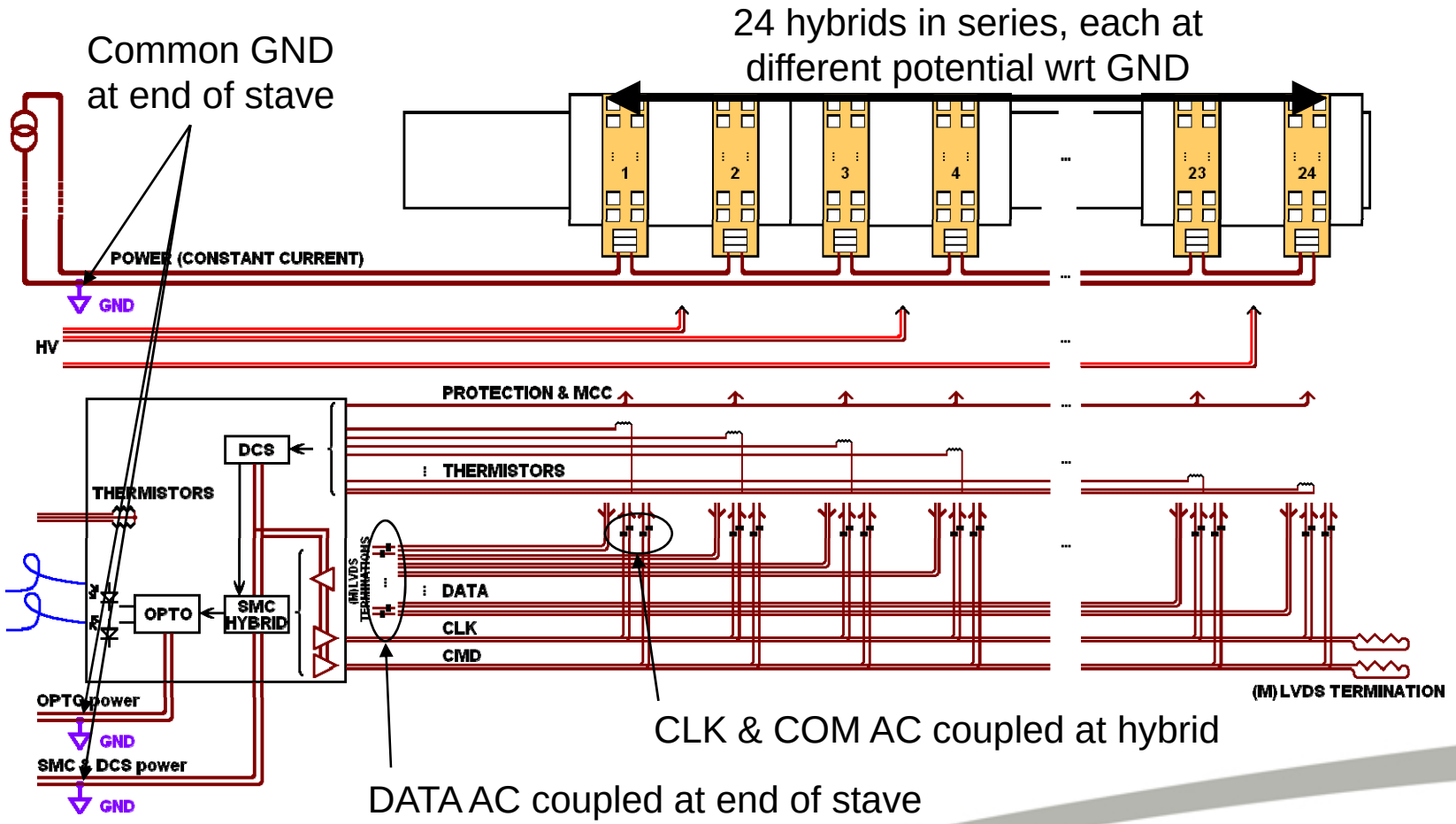
SP Stave Architecture



(DC-DC powered stave would look similar, apart from the absence of AC coupled IO)

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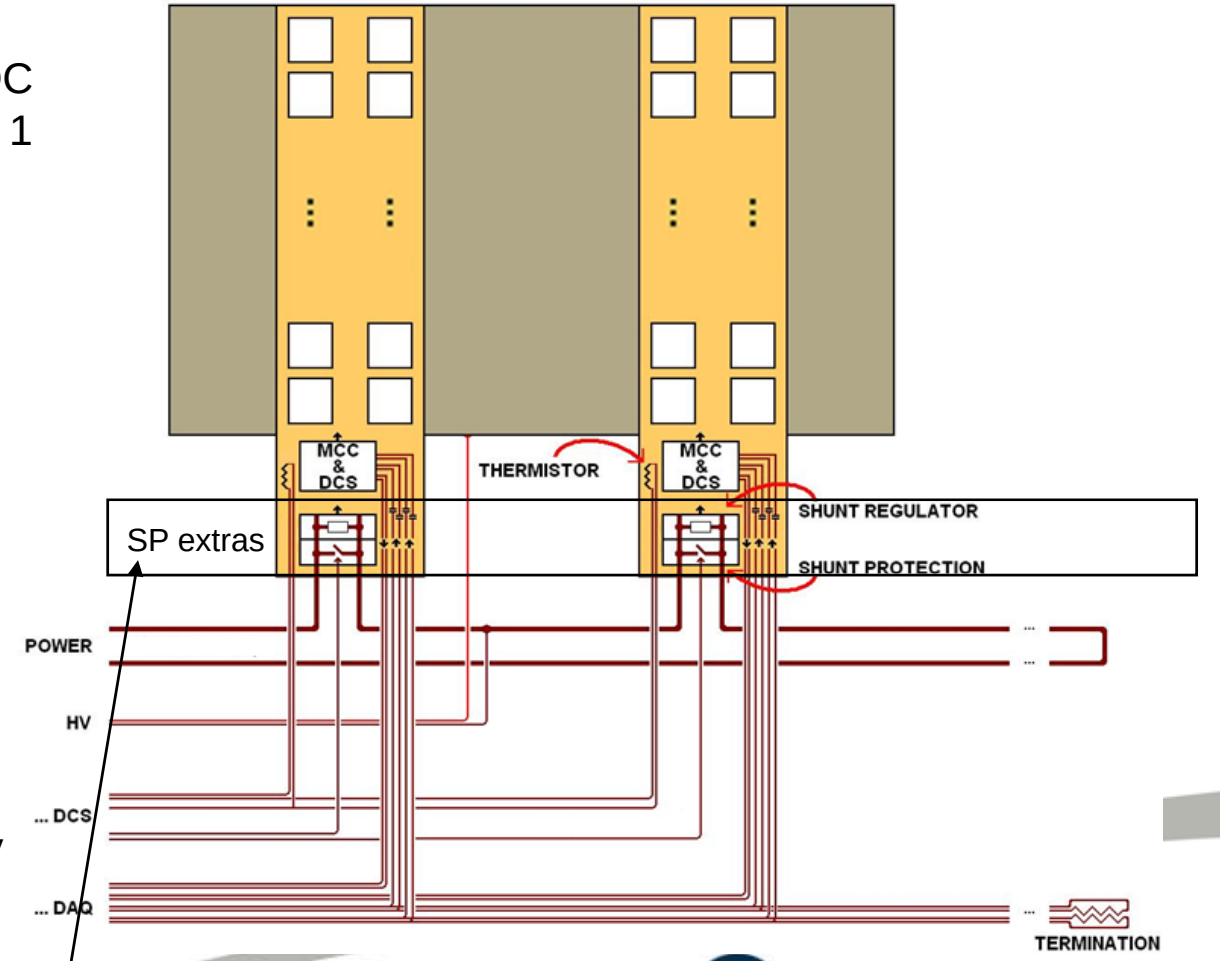
SP Module Architecture

Module Controller Chip (MCC)
- Functions common to SP & DC-DC
  - multiplexes 2 data streams into 1
  - voltage monitoring
- Additional for SP
  - powered by SP
  - AC coupling of CLK & COM
    - Requires 4 capacitors
    - Everything else on chip

Temperature
- read by (stave end) DCS
  - Monitor T before power applied

Shunt protection
- under DCS control
  - Turn on modules independently



SP requires minimal extra circuitry at the module end

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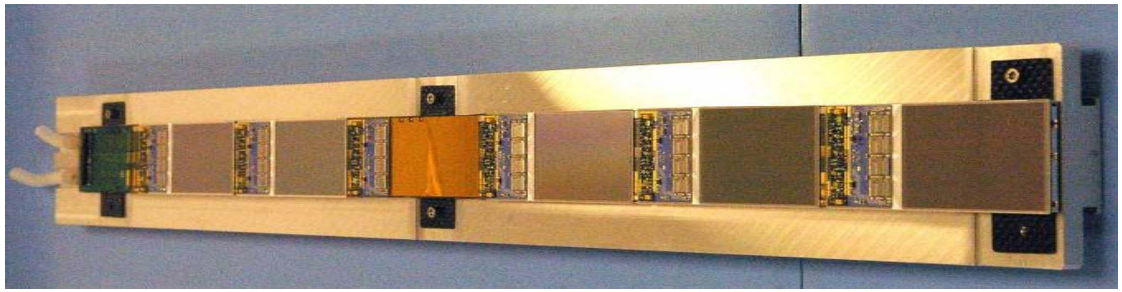
System tests of SP staves

1) Pixel stave with FE-I3 (old, published)

2) Stave06: 6 module stave with ABCD



We have verified that:

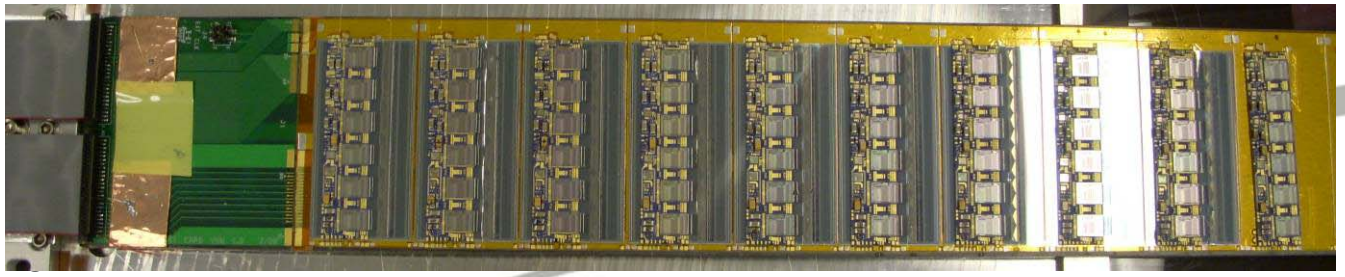
1. Noise is not an issue
2. AC coupled (M)LVDS works
3. SP uses little extra real estate
4. Can use single HV line / strip stave

All staves working well!

30 * 4V = 120V

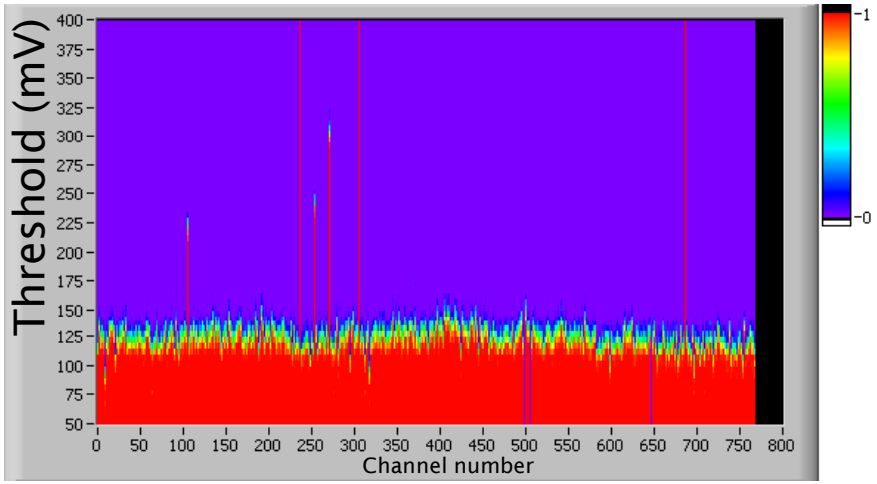
(ABCD, 800nm)

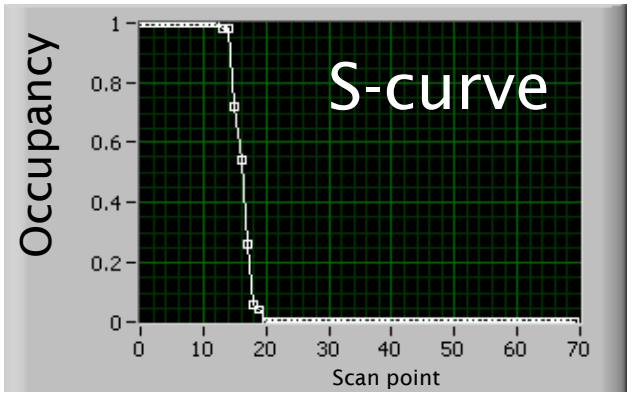
3) Stave07: 30 module stave with ABCD

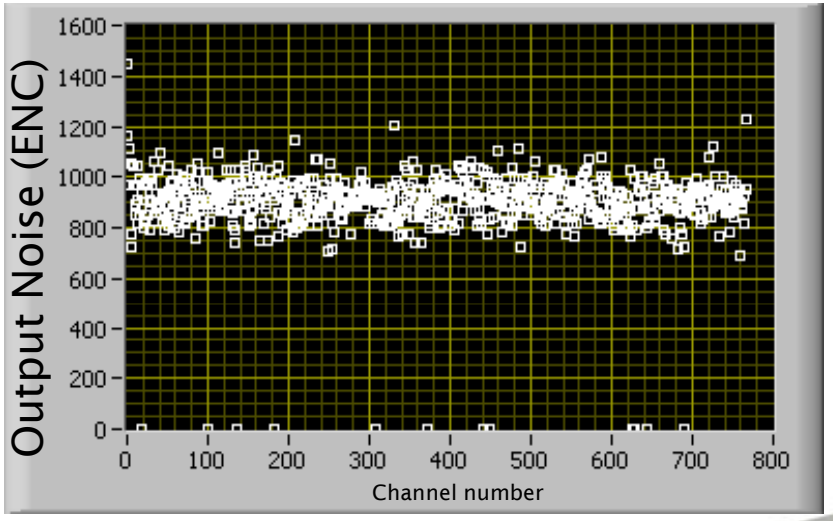


*(Future: 24 * ~1V = 24V for 130nm ABCN)*

Thirty Module Stave: Some Results





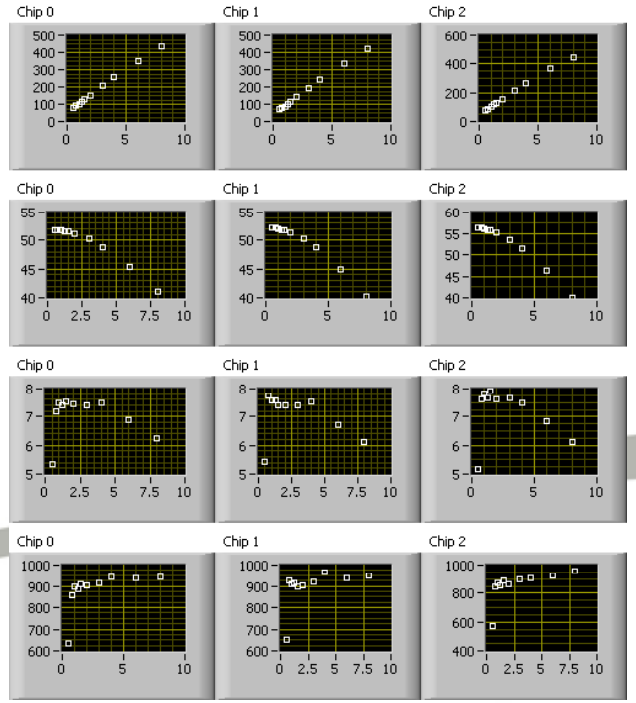


VT50 (mV)

Gain (mV/fC)

Output Noise (mV)

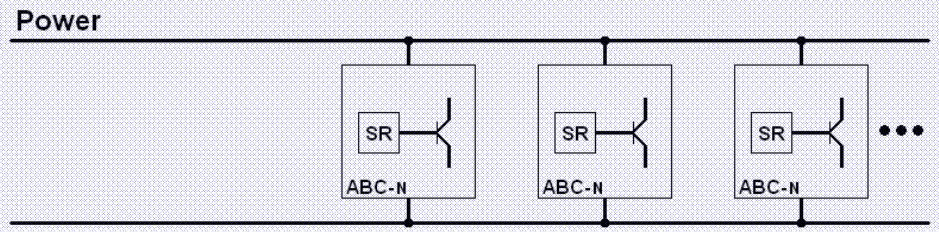
Input Noise (ENC)



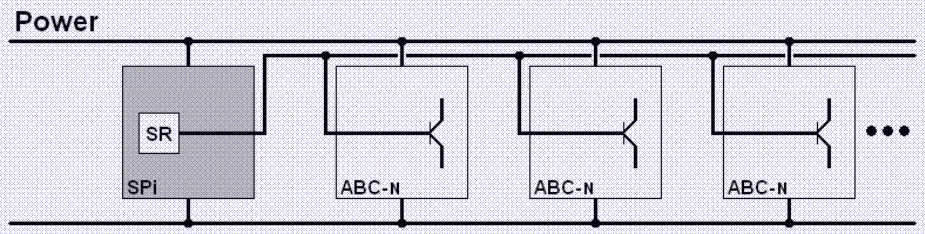
Shunt Regulator Architectures

- **Hybrid with Shunt "W"**
  - Use each ABCN's integrated shunt regulator
  - Use each ABCN's integrated shunt transistor(s)

See "Serial power circuitry in the ABC-Next and FE-I4 chips" to be given this afternoon by W. Dabrowski

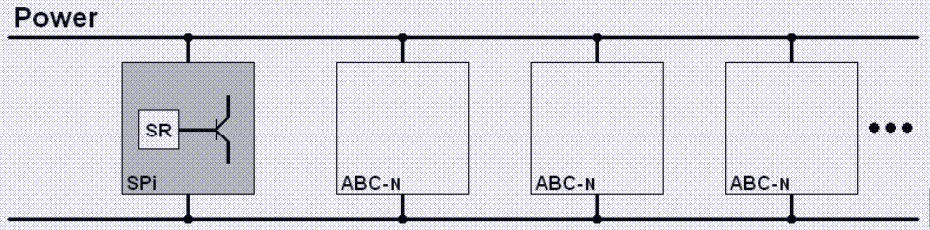


- **Hybrid with Shunt "M"**
  - Use one external shunt regulator
  - Use each ABCN's integrated shunt transistor(s)
    - Two (redundant) shunt transistors, 140mA each



- **Hybrid with SPi (or similar)**
  - Use one external shunt regulator
  - Use one external power transistor

See "The Serial Power Interface Chip", to be given this afternoon by M. Trimpl



Each option has its merits. All now available in silicon: final choice to be based upon test results.

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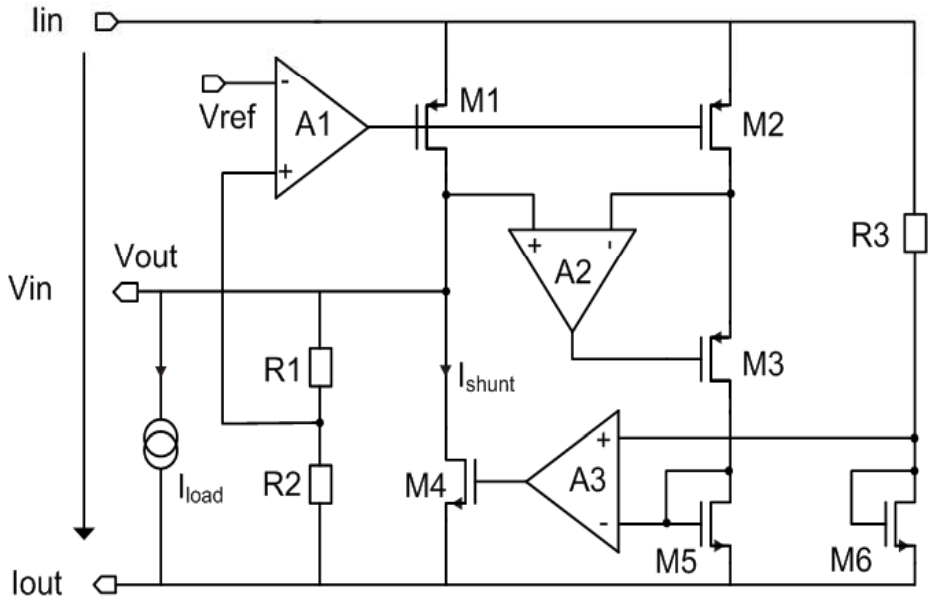
LDO Regulator with Shunt Transistor (ShuLDO)

Simplified Schematic



- Combination of LDO and shunt transistor
- M4 shunts the current not drawn by the load
- Fraction of M1 current is mirrored & drained into M5
- Amplifier A2 & M3 improve mirroring accuracy
- Ref. current defined by resistor R3 & drained into M6
- Comparison of M5 and ref. current leads to constant current flow in M1
- Ref. current depends on voltage drop V_{Iin} which again depends on supply current Iin

- „Shunt-LDO" regulators having completely different output voltages can be placed in parallel without any problem regarding mismatch & shunt current distribution
- Resistor R3 mismatch will lead to some variation of shunt current (10-20%)
- „Shunt-LDO" can cope with an increased supply current if one FE-I4 does not contribute to shunt current e.g. disconnected wirebond → ref current goes up
- Can be used as an ordinary LDO when shunt is disabled

See "Serial power circuitry in the ABC-Next and FE-I4 chips" to be given this afternoon by W. Dabrowski

Power Requirements with Modern Process Technologies

					Power per 128 channel chip	per channel
In ATLAS SCT	**ABCD** (0.8µm, biCMOS)	Digital:	4.0 volts	35 mA per chip (actual)	=> 4.0 x 35 + 3.5 x 74 = 399 mW	**3.1 mW**
		Analogue:	3.5 volts	74 mA per chip (actual)		
Present Prototype	**ABCN25** (0.25µm CMOS)	Digital:	2.5 volts	95 mA per chip (preliminary)	=> 2.5 x 95 + 2.2 x 27 = 300 mW	**2.3 mW**
		Analogue:	2.2 volts	27 mA per chip (preliminary)		
Proposed	**ABCN13** (0.13µm CMOS)	Digital:	0.9 volts	**51 mA per chip (estimate)	=> 0.9 x 51 + 1.2 x 16 = 65 mW	**0.5 mW**
		Analogue:	1.2 volts	**16 mA per chip (estimate)		

ABCN25: Vdig > Vana Idig >> Iana

If we generate Vana from Vdig using LR:

- 27mA * 0.3V = 8.1mW per chip
- 3% of chip power

ABCN13: Vana > Vdig Idig >> Iana

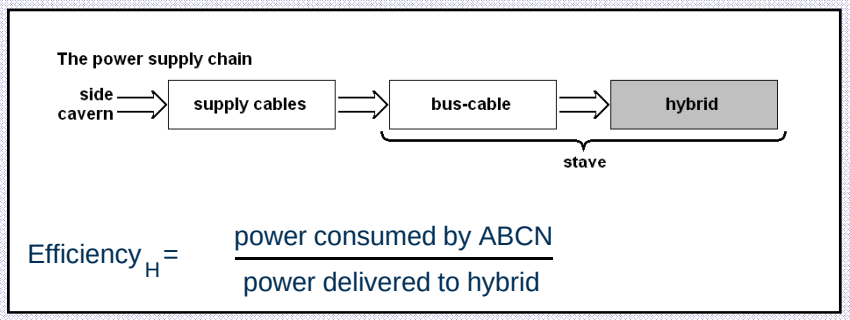
If we generate Vdig from Vana using LR:

- 95mA * 0.3V = 28.5mW per chip
- **44% of chip power**
- Can we do better than this? *Of course…*

** Power Estimates for an ABCN in 130nm Technology, Mitch Newcomer, Atlas Tracking Upgrade workshop, NIKHEF, November 2008
http://indico.cern.ch/getFile.py/access?contribId=16&sessionId=8&resId=0&materialId=slides&confId=32084

Efficiency - definitions

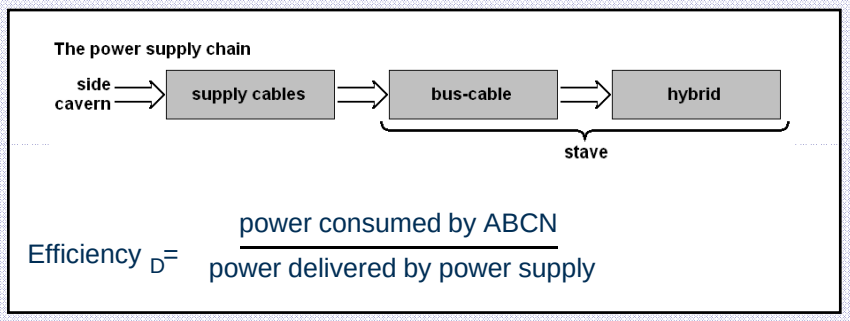
Definition – *Hybrid* (excludes stave interconnects & supply cables)



$$\text{Efficiency}_H = \frac{\text{power consumed by ABCN}}{\text{power delivered to hybrid}}$$

Efficiency$_H$

Definition – *Detector* (includes all supply cables)



$$\text{Efficiency}_D = \frac{\text{power consumed by ABCN}}{\text{power delivered by power supply}}$$

Efficiency$_D$

Some assumptions: Cable resistance 2 ohms for each line pair, SR = 85%, low current DC-DC = 90%, high current DC-DC = 85%

ABCN demand power is dependant on task. This will normally mean a shunt regulator will dissipate some power to maintain voltage under all conditions.

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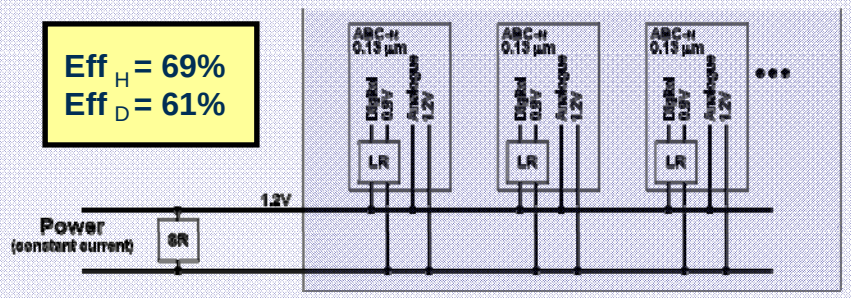
Favoured SP Options

Low Noise:

On-chip Linear Regulator for Digital only

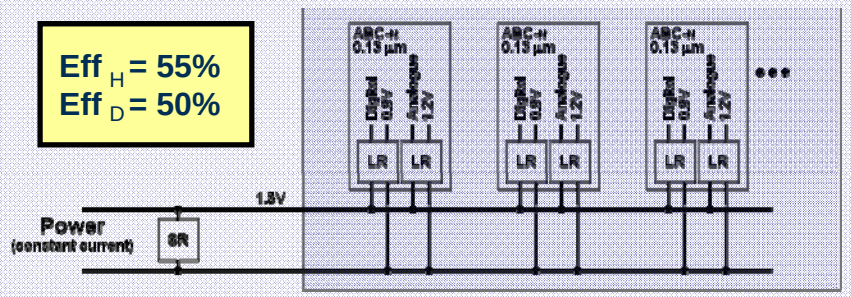
Eff $_H$ = 69%
Eff $_D$ = 61%



Very Low Noise:

On-chip Linear Regulators for both Analogue and Digital

Eff $_H$ = 55%
Eff $_D$ = 50%



For further details, see this afternoon's presentation by W. Dabrowski: "Serial power circuitry in the ABC-Next and FE-I4 chips"

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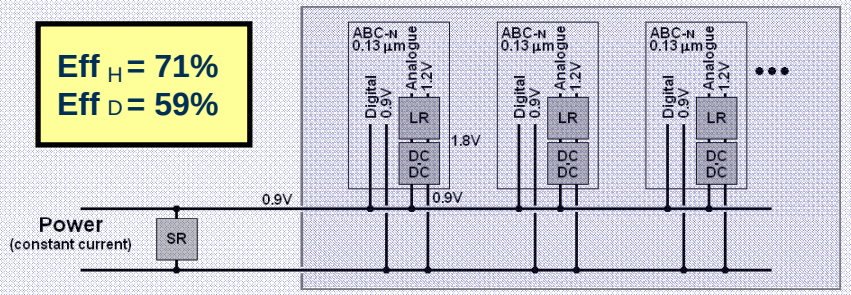
Favoured SP Options

Also Low Noise:

Analogue from on-chip DC-DC step using switched capacitors *and* linear regulator

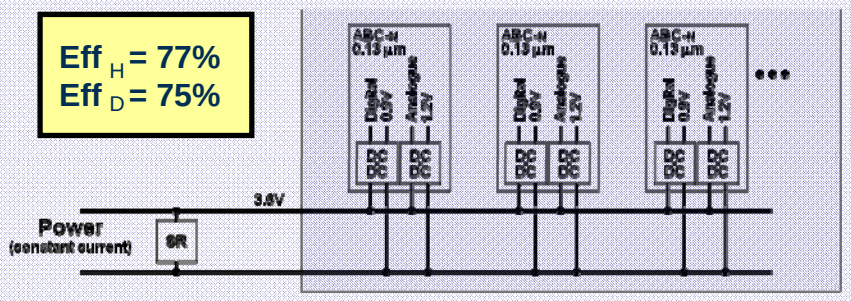
Eff $_H$ = 71%
Eff $_D$ = 59%



Highest Efficiency:

"On-chip" DC-DC conversion using switched capacitors

Eff $_H$ = 77%
Eff $_D$ = 75%



For further details, see this afternoon's presentation by W. Dabrowski: "Serial power circuitry in the ABC-Next and FE-I4 chips"

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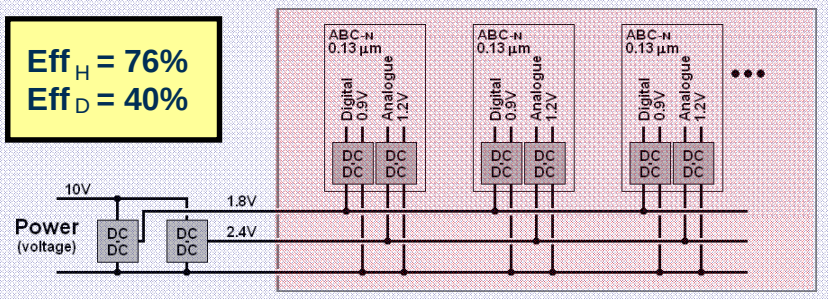
For the sake of Comparison…

Off-chip DC-DC conversion from 10V to 2.4V and 1.8V (assume 85% efficiency)

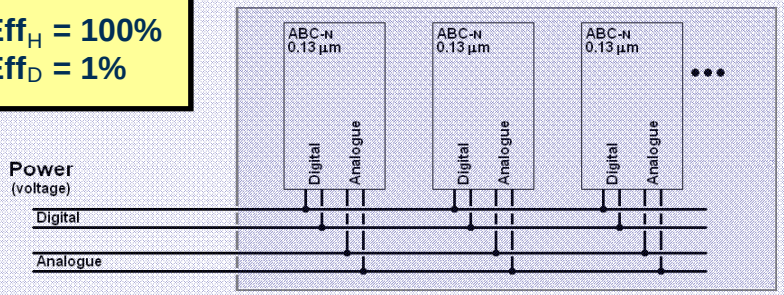
"On-chip" DC-DC conversion using switched capacitors (assume 90% efficiency)

Eff_H = 76%
Eff_D = 40%



Independent Power

Eff_H = 100%
Eff_D = 1%



With ABCN in 130 nm technology, we shall study several options to obtain the best balance between efficiency and performance…

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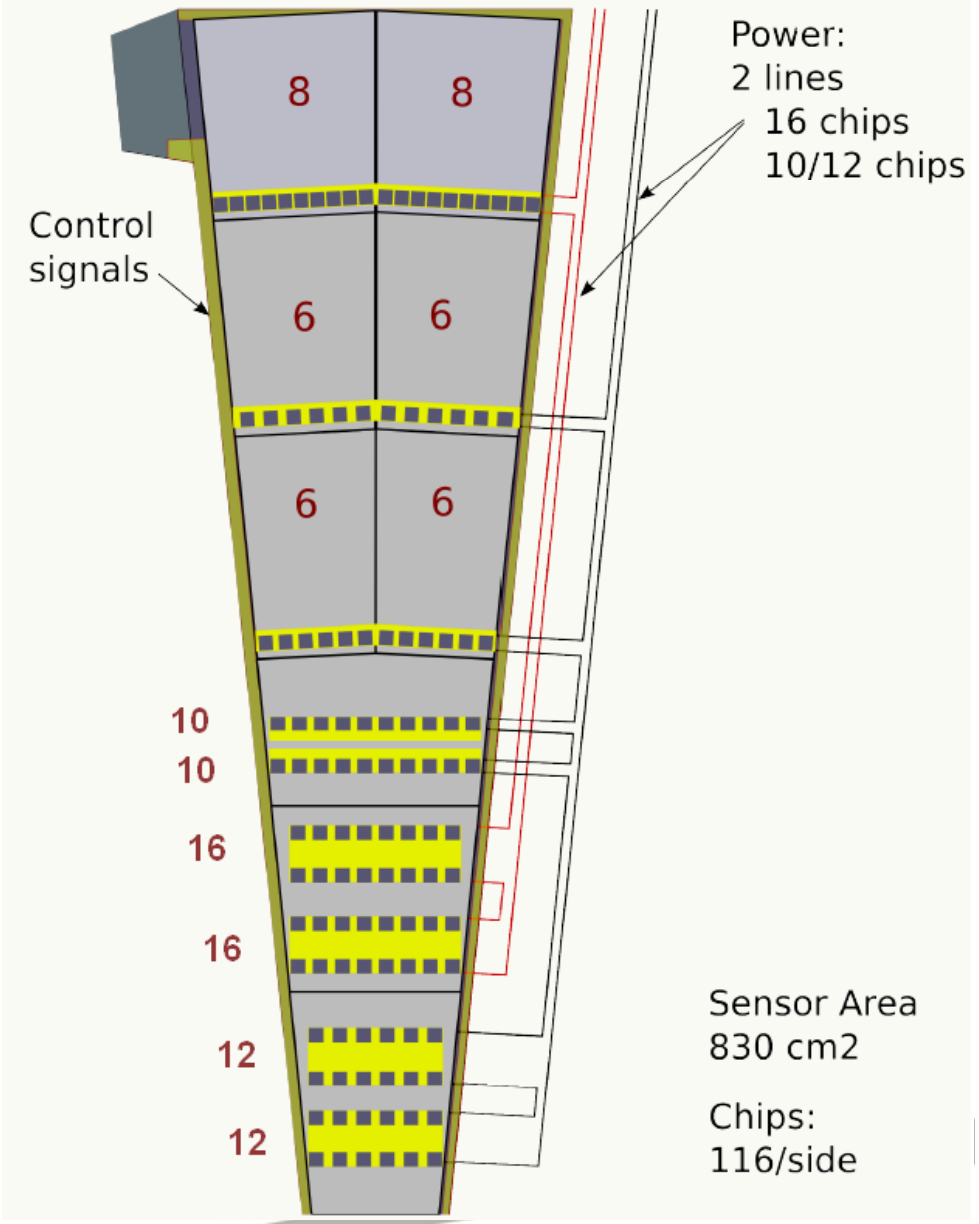
SP and Endcap Geometries

The baseline design for the endcap of an upgraded ATLAS strip detector is based around petals.

- **Not all hybrids have the same number of chips**
  - Group hybrids with *similar* numbers of chips into their own power chains
- Chain 1: (3*16) chip units
- Chain 2: (4*12)+(2*10) chip units
  - Additional current corresponding to two chips must be dissipated by the shunt(s) on each 10 chip hybrid.
- Efficiency depends upon the values of the analogue and digital voltages and the means used to generate them:
  - Example: 3 ohm cable pair, 1.5V supply, 140mA per chip and 85% shunt efficiency => **54% efficiency**
  - **GOOD ENOUGH**



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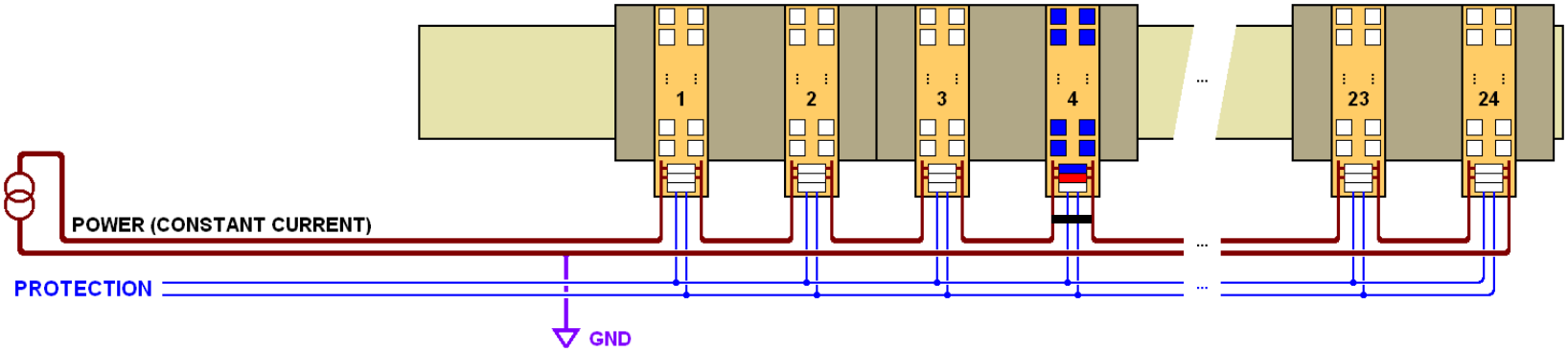
Protection



Whilst demonstration staves have generally been reliable:

- What happens if a module fails open circuit?
- What happens if a module becomes a noise generator?

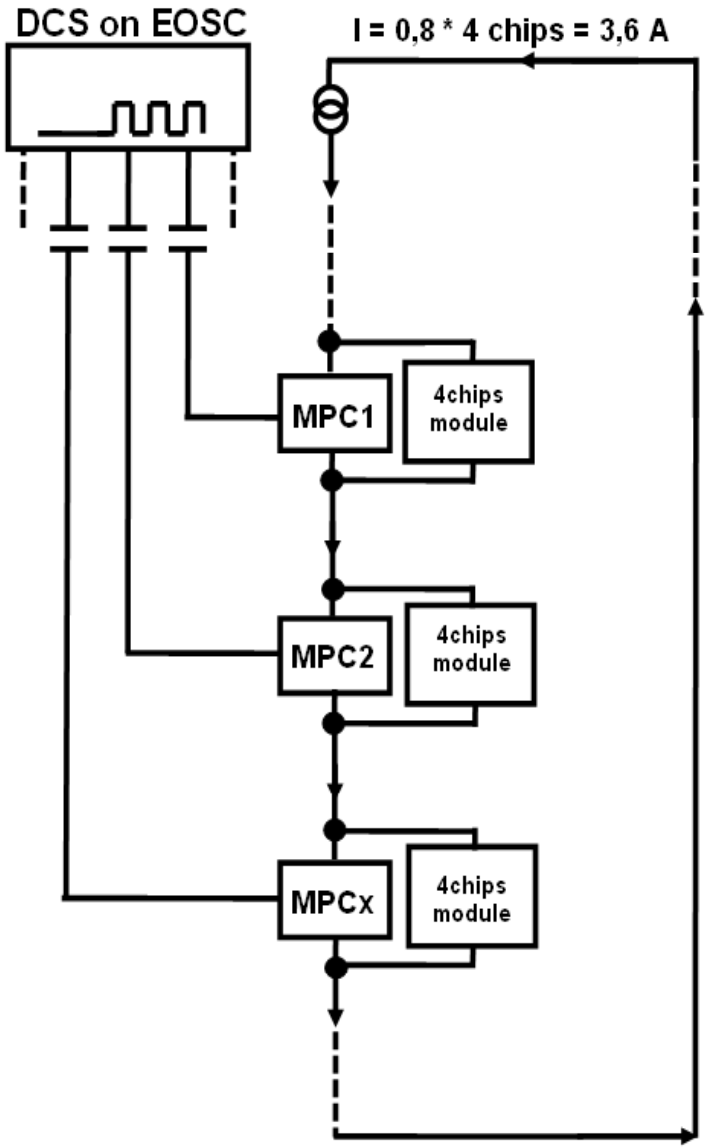
We could provide a system to “short out” each module under control of DCS

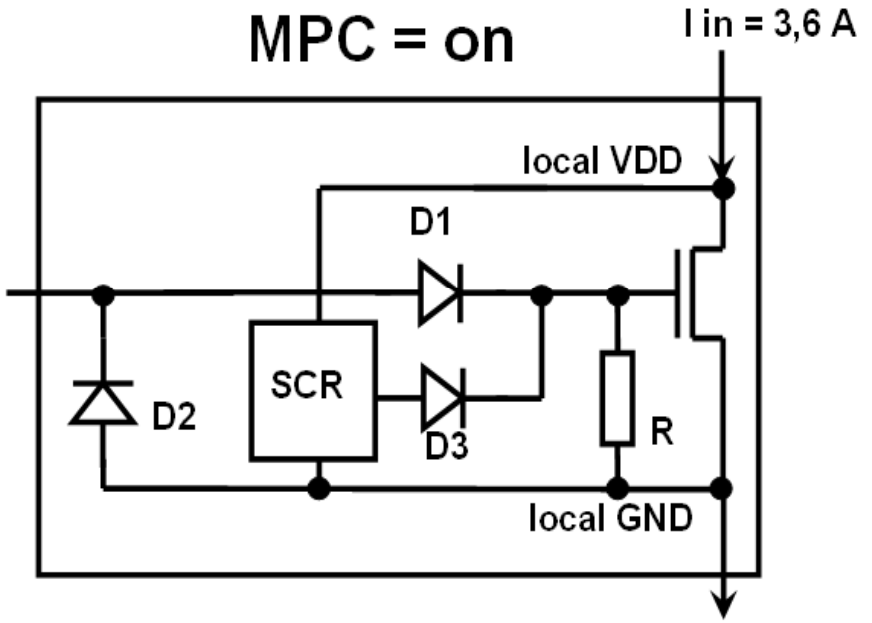
- Voltage across shorted module should be small (<100mV)
- Area of components and number of control lines must be small
- Automatic over current and over voltage protection is desirable
- Protection circuit must draw no (minimal) power when module active
- Ability to put modules into “stand by” (low power state)

See poster by Richard Holt for details of proposals by Bonn, BNL and RAL

Bonn Scheme: Module Protection Chip

"Serial Powering Protection", Andreas Eyring, ATLAS Upgrade Week, CERN, Feb 2008
http://indico.cern.ch/materialDisplay.py?contribId=4&materialId=slides&confId=52375





+ simple
+ control & monitor
+ fast auto-response

default state = OC

OC = Open Circuit (ie switch is "off", module powered)

- 1 AWG 36 line / module

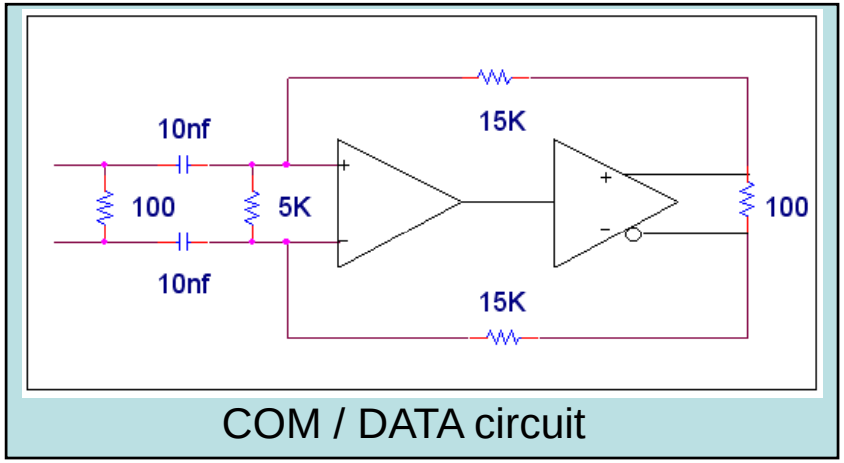
BNL and RAL are addressable schemes (fewer lines)

Silicon prototype by Summer/Autumn 2009

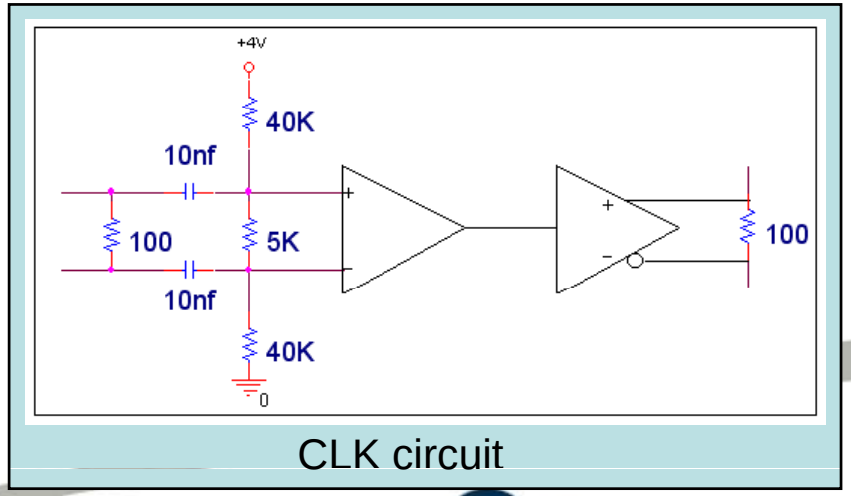
AC Coupled (M)LVDS Receivers

A viable solution!

- No need for DC balanced codes
  - COM/DATA circuit could be simplified if DC balanced codes were used (DC balanced remains the baseline for production staves)
- All components apart from the capacitors can be integrated into custom chips
  - Capacitors need to be rated to ~30V, more for present prototypes
- MLVDS drivers offers higher currents and MLVDS receivers lower thresholds (than LVDS)
  - Can help increase margins
- **Working well on STAVE07**



COM / DATA circuit



CLK circuit

See “AC Coupled LVDS drivers”, Dave Nelson, ATLAS Tracker Upgrade workshop, NIKHEF, Nov. 2008
http://indico.cern.ch/materialDisplay.py?contribId=19&sessionId=8&materialId=slides&confId=32084

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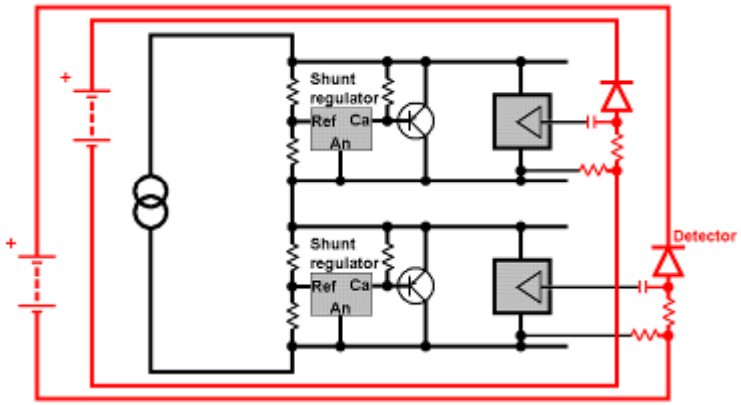
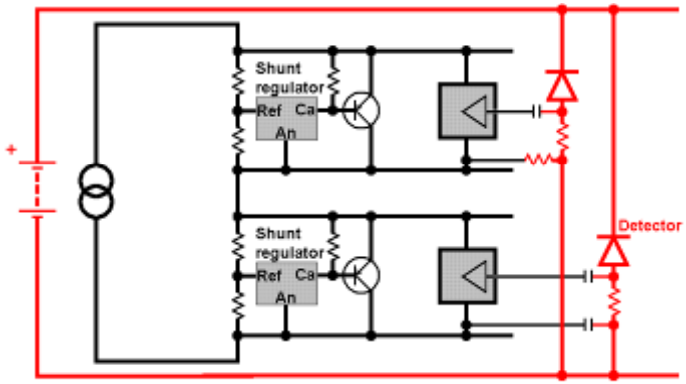
Serial Powering and HV



Standard HV powering: one HV per module



Alternative HV powering: one HV supply per M modules

- Serial Powering is compatible with the use of a single HV supply for several modules
- Each sensor is dynamically connected to current source ground through output impedances of the chain of shunt regulators
- Low shunt output impedance is crucial to achieve good ‘grounding’ and reduce noise

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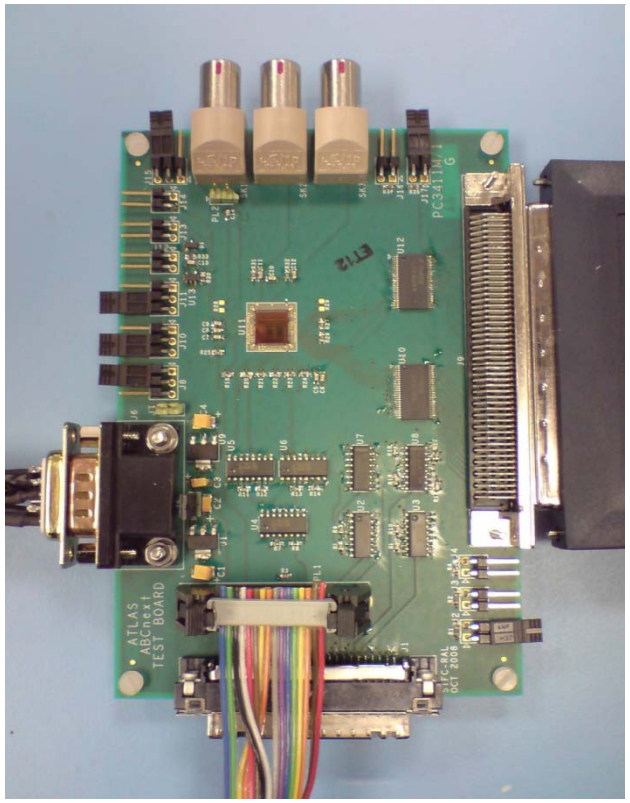
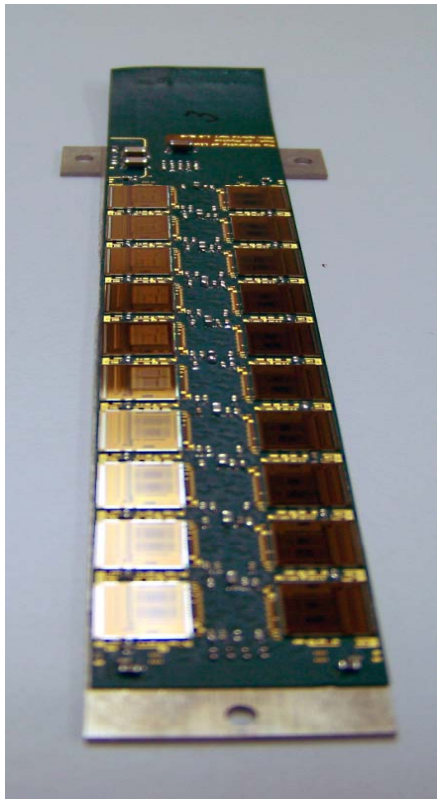
First tests of integrated shunts in ABCN: RAL single chip PCB and Liverpool Hybrid





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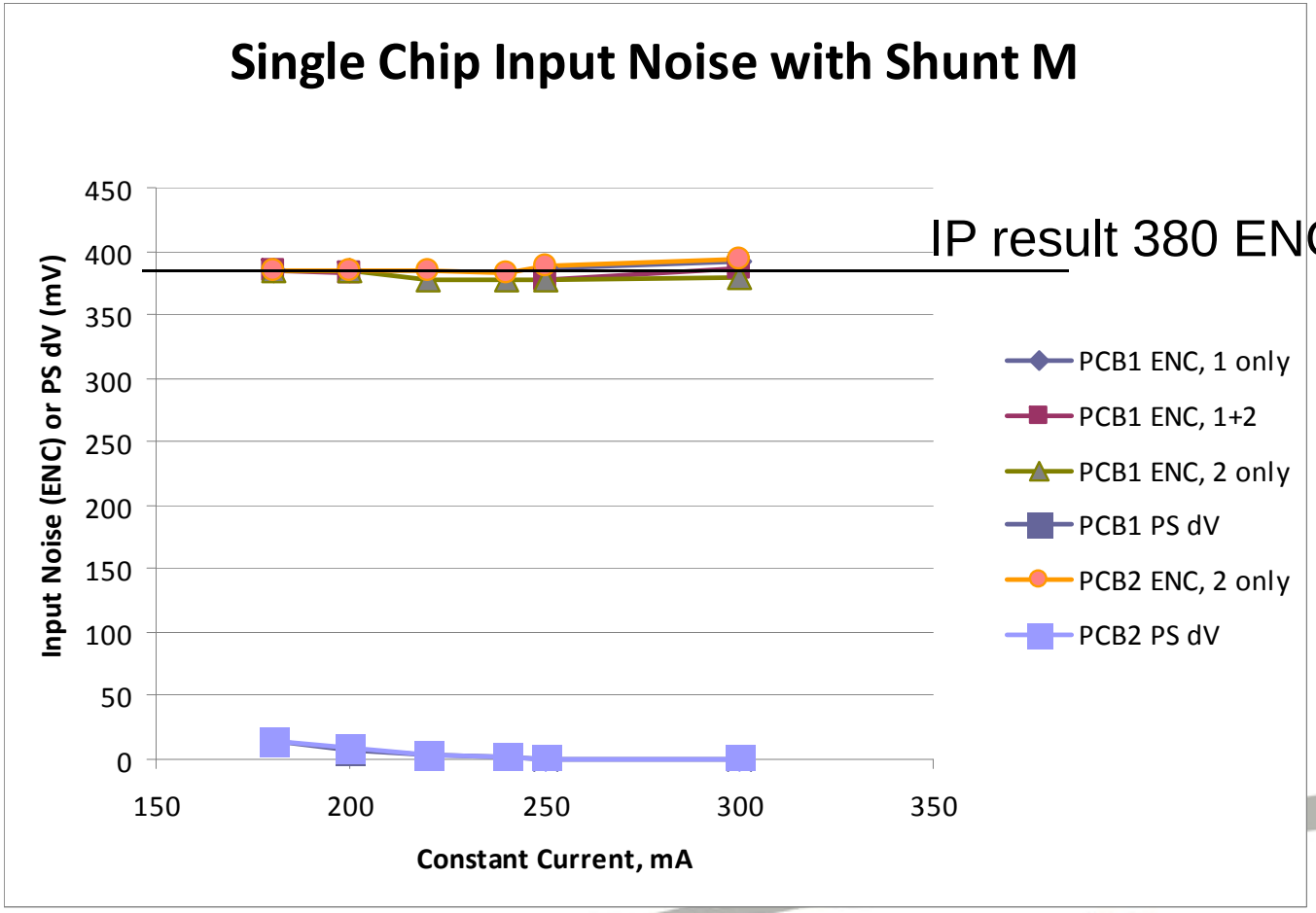
Single Chip using shunt “M”



IP result 380 ENC: SAME!

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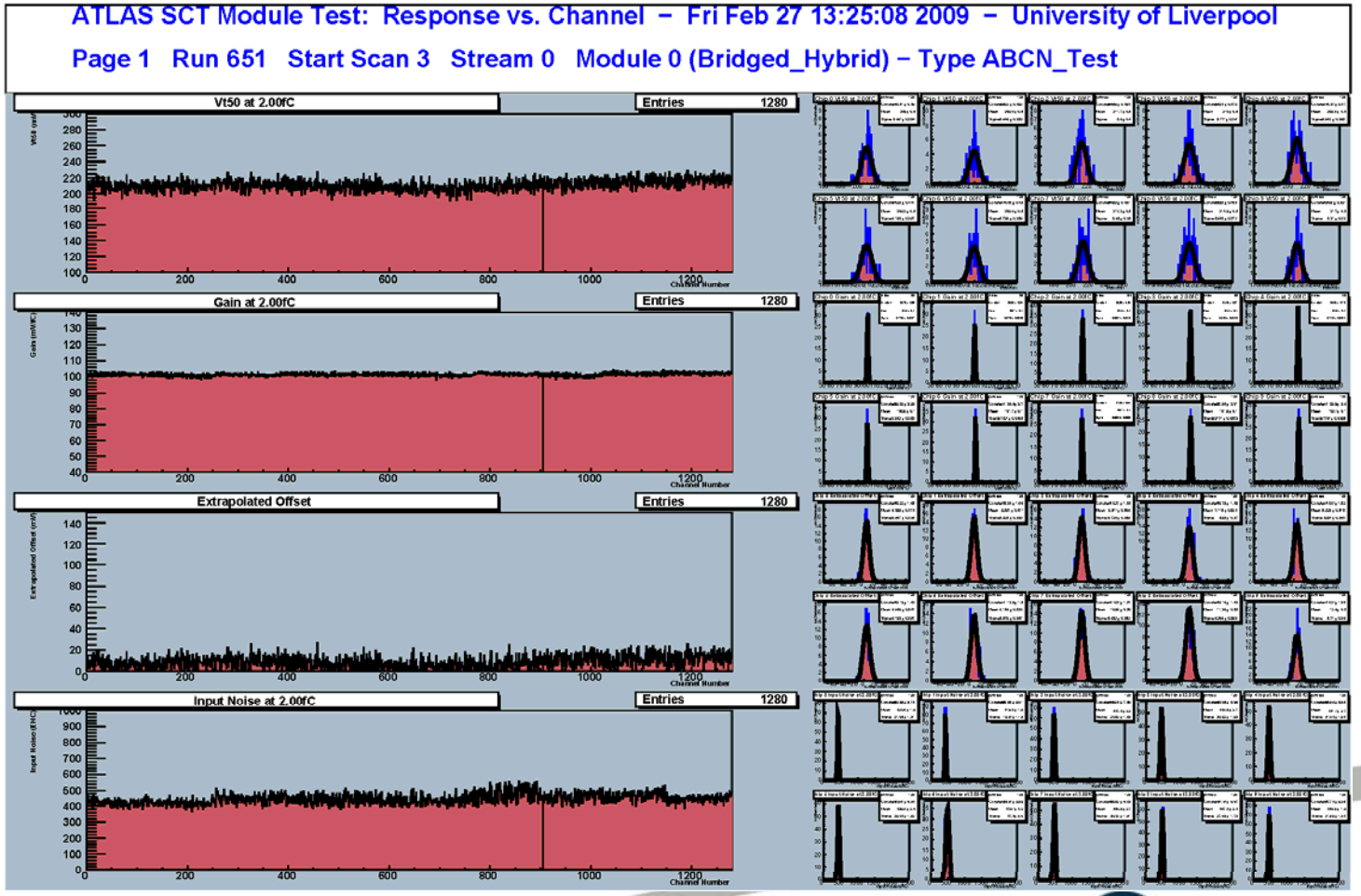
ABCN hybrid using shunt “W”

PRELIMINARY



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SP Summary and Next Steps

- We have ~2 years successful experience building and running staves with commercial SP components
- Shunt circuitry can be integrated into FE chips
  - Low requirements in terms of component area
  - First results from ABCN shunts very encouraging
- Protection can be part of SP architecture
  - Basic scheme demonstrated
- First ABCN demonstrator stave planned for this year
  - Integrated shunts + protection
- SP is an attractive option for sLHC power distribution!

Supplemental Material

Large Diameter Wire Bonds

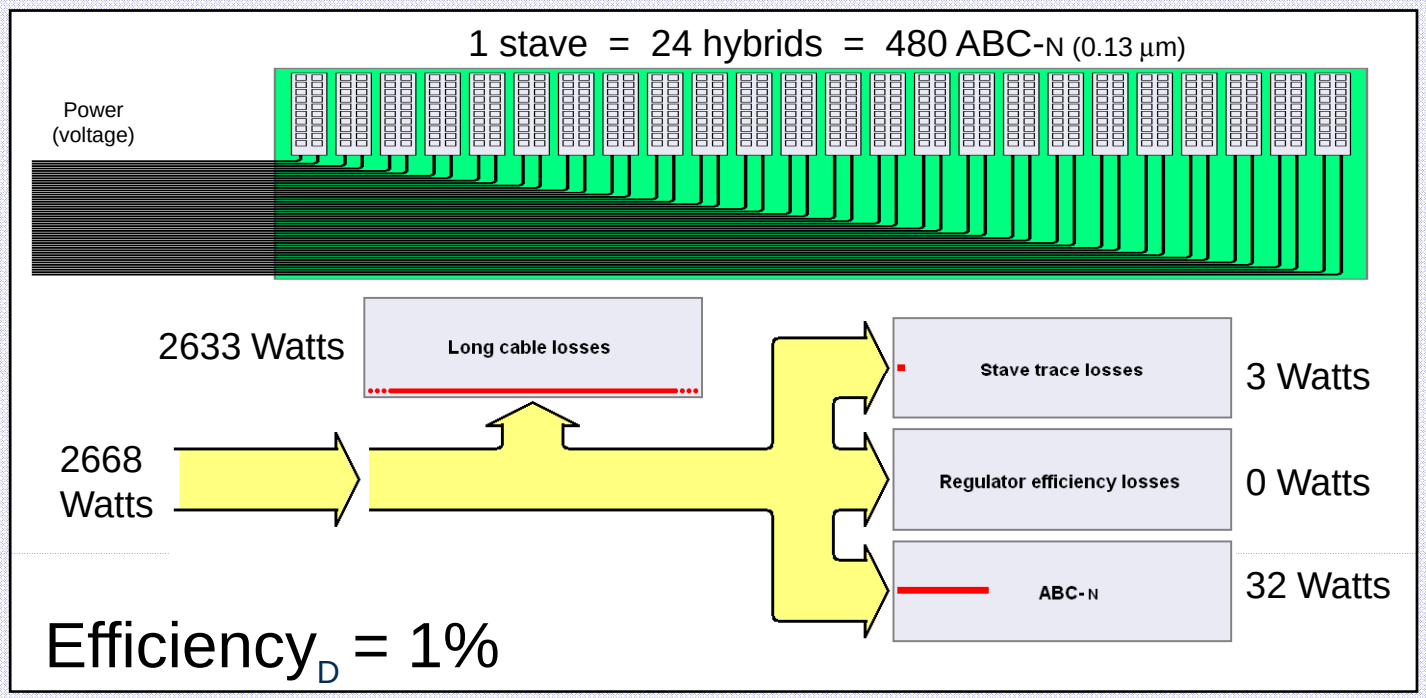
Delvotec 64/66000
100 – 600 micron wire

Hesse + Knipps Bondjet BJ920
125 – 500 micron wire

Used in harsh automotive applications, e.g. ABS
Shear strength for 250 micron bond 1000cN
250 micron bond => 15 A
Manufacturers can do test samples

Detector power efficiency

Independent powering (100% hybrid efficiency)



Independent supplies (line pairs) for digital and analogue power.
Same amount of copper => Cables are 96 ohms total for each line pair. Each line pair carries 20 x 51mA (digital) and 20 x 16mA (analogue).

Numbers rounded

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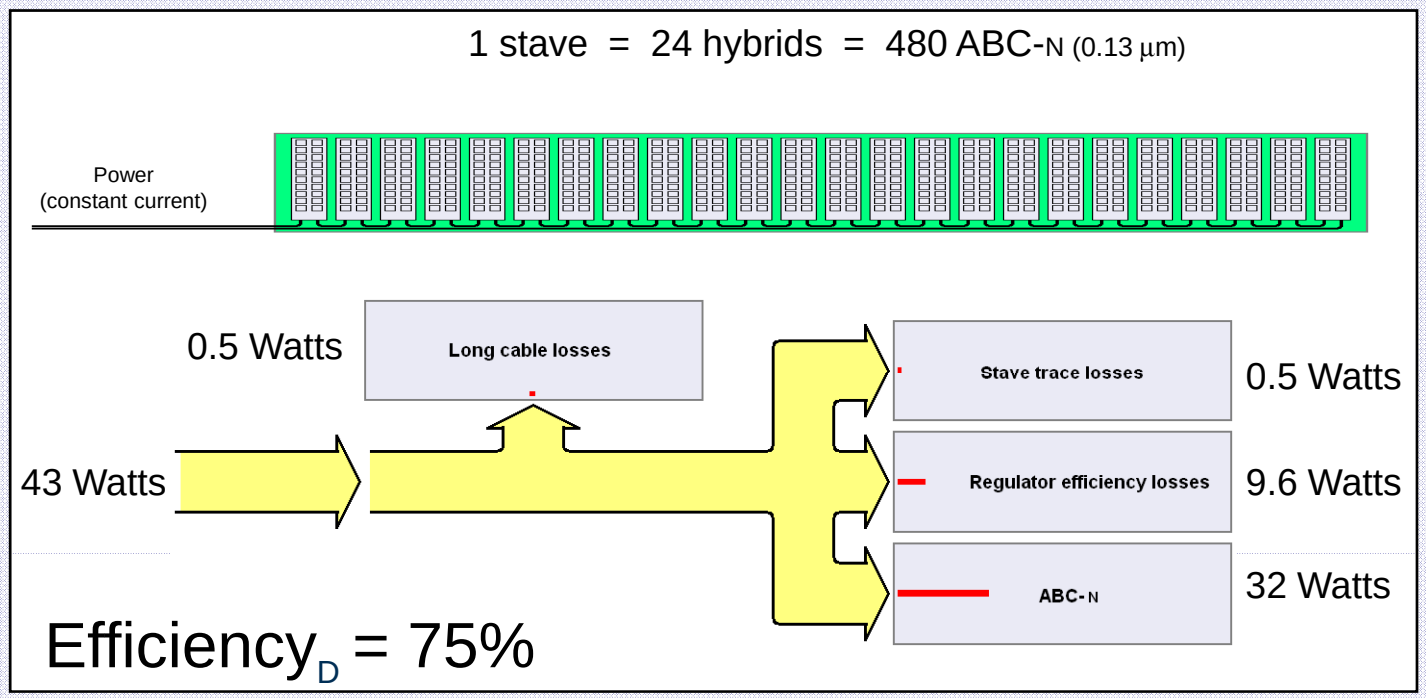
Detector power efficiency

Serial powering 3.6V, 3:1 & 4:1 DC-DC using switched capacitors



Cables assumed to be 2 ohms total for each power line pair
Regulator power = (1/eff$_H$ - 1) x ABC power
Stave supply current = (32 + 9.6 + 0.5)watts / (3.6volts x 24) = 0.49amps

Numbers rounded

Science & Technology Facilities Council