GBT Project Status

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2009/03/04 – CERN Switzerland

http://cern.ch/proj-gbt

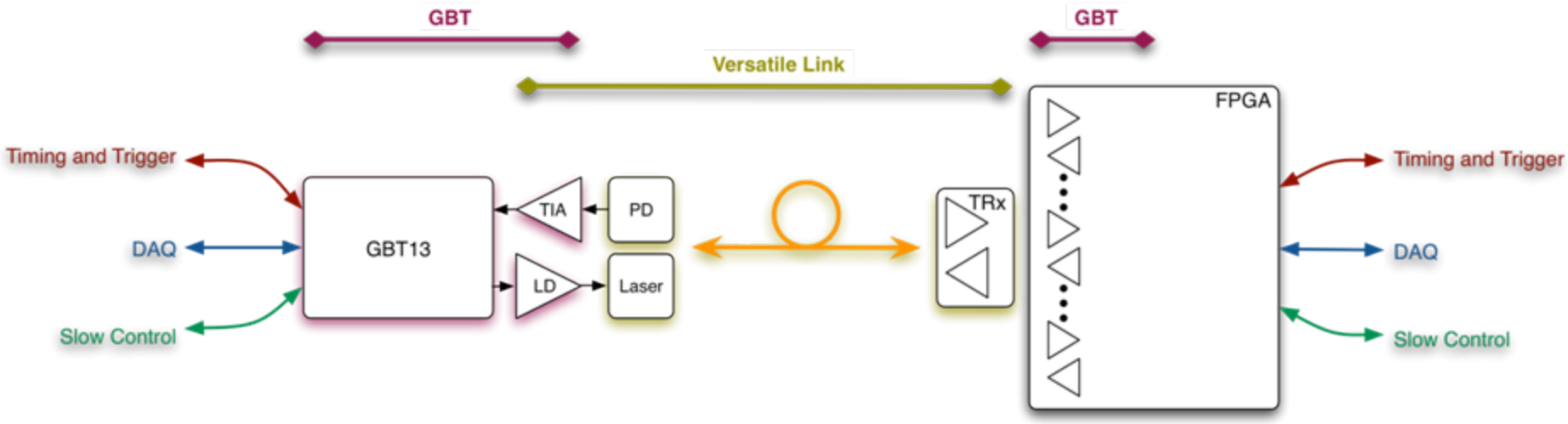
Radiation Hard Optical Link Architecture

Defined in the "DG White Paper"

- *"Work Package 3-1"*
  - Objective:
    - Development of an high speed bidirectional radiation hard optical link
  - Deliverable:
    - Tested and qualified radiation hard optical link
  - Duration:
    - 4 years (2008 – 2011)

Radiation Hard Optical Link:

- *Versatile link project:*
  - Opto-electronics
  - Radiation hardness
  - Functionality testing
  - Packaging
- *GBT project:*
  - ASIC design
  - Verification
  - Functionality testing
  - Packaging

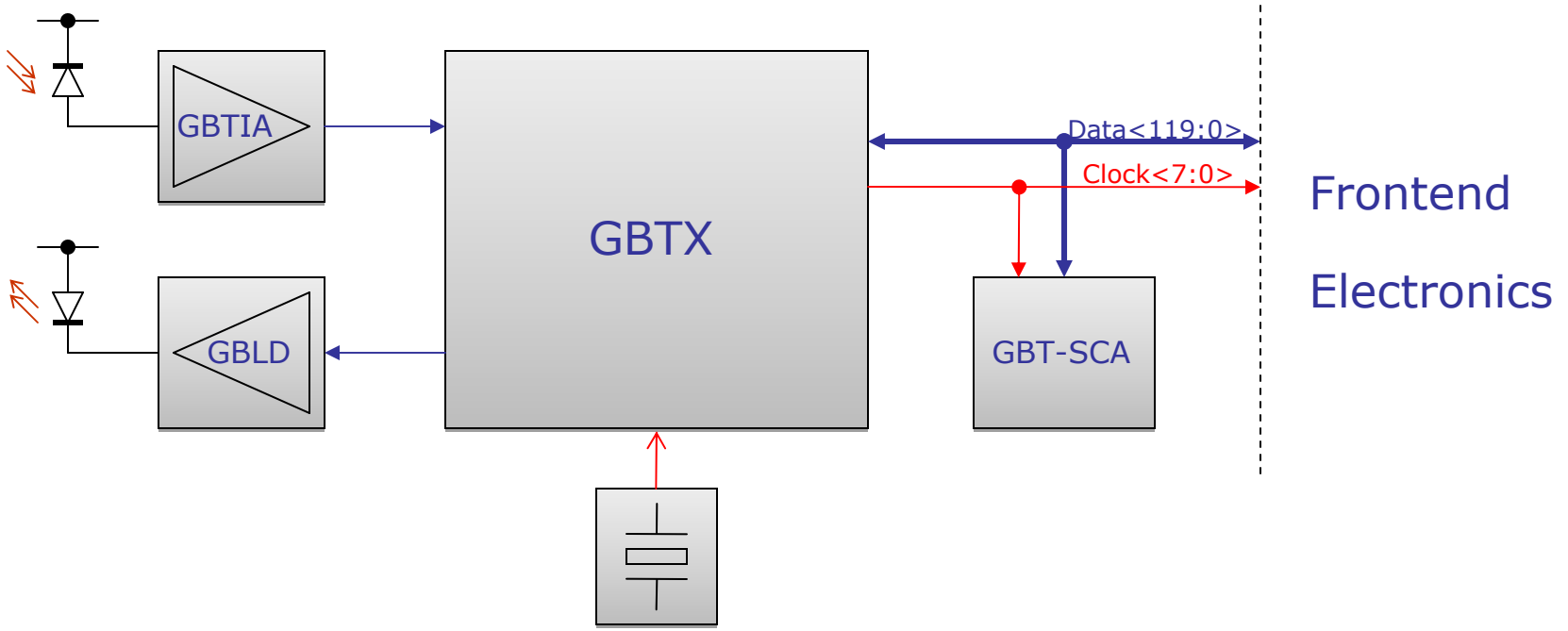


On-Detector
Custom Electronics & Packaging
Radiation Hard

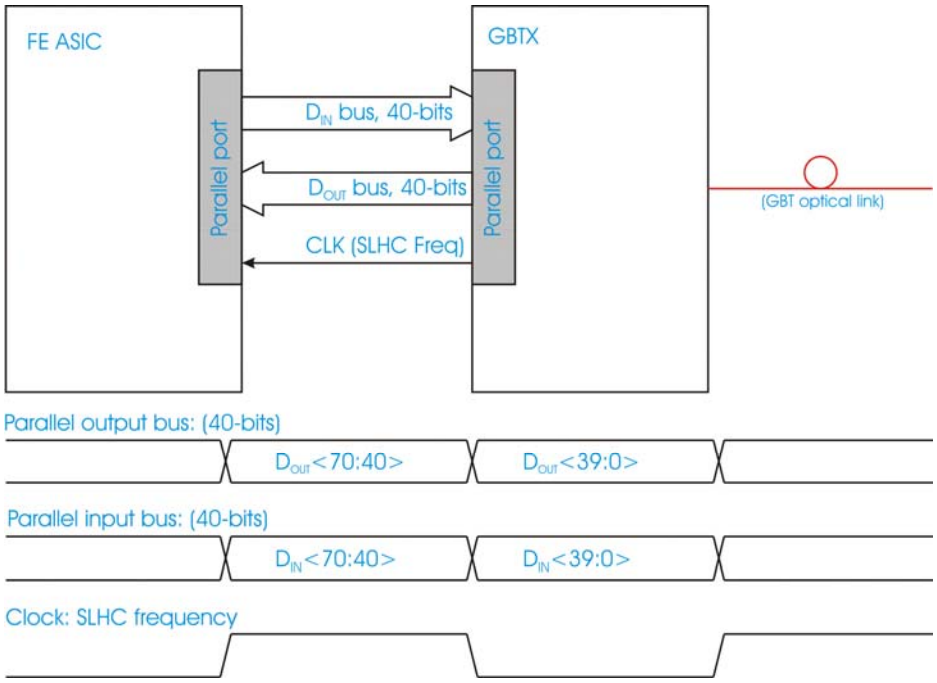
Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

GBT Chipset

- *Radiation tolerant chipset:*
  - GBTIA: Transimpedance optical receiver
  - GBLD: Laser driver
  - GBTX: Data and timing and transceiver
  - GBT-SCA: Slow control ASIC
- *Supports:*
  - Bidirectional data transmission
  - Bandwidth:
    - Line rate: 4.8 Gb/s
    - Effective: 3.36 Gb/s
- *The target applications are:*
  - Data readout
  - TTC
  - Slow control and monitoring links.
- *Radiation tolerance:*
  - Total dose
  - Single Event Upsets



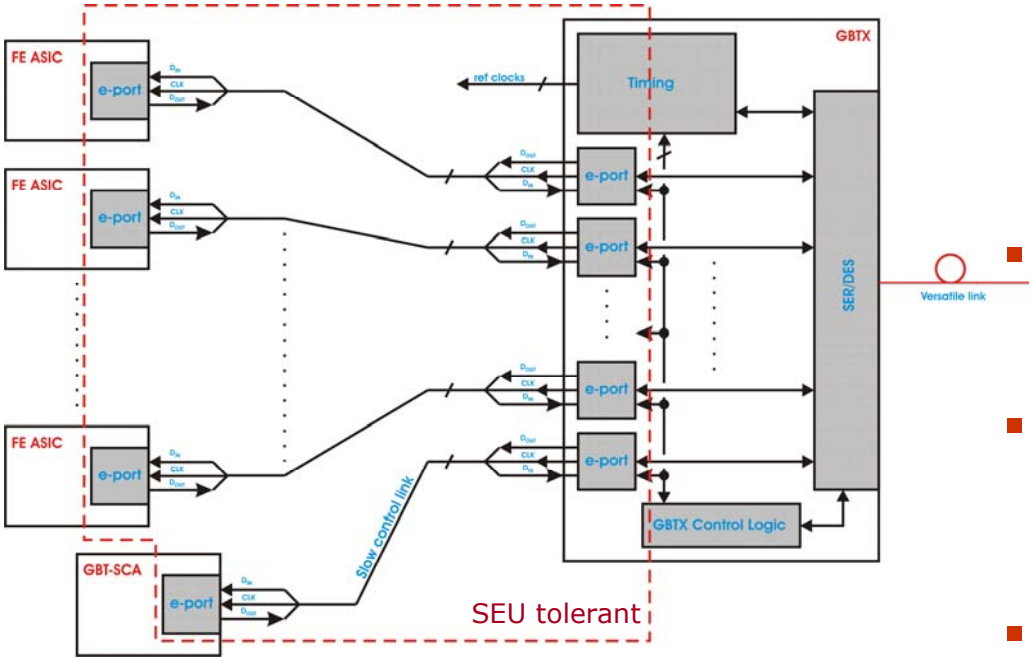
GBTX-TO-FRONTEND: Parallel Modes



- *P-Bus Mode:*
  - Simple parallel interface
  - 40-bit wide bus
  - Bidirectional
  - Double Data Rate (DDR)
- *B-Bus Mode:*
  - A byte-bus mode is also available
  - Up to five independent buses can be used simultaneously
- *Electrical levels:*
  - SLVS electrical level:
    - 100 Ω termination
    - 400 mV differential
    - 200 mV common mode
    - I_{LOAD} = ±2 mA

JEDEC standard, JESD8-13
Scalable Low-Voltage Signalling for 400 mV (SLVS-400)
http://www.jedec.org/download/search/JESD8-13.pdf

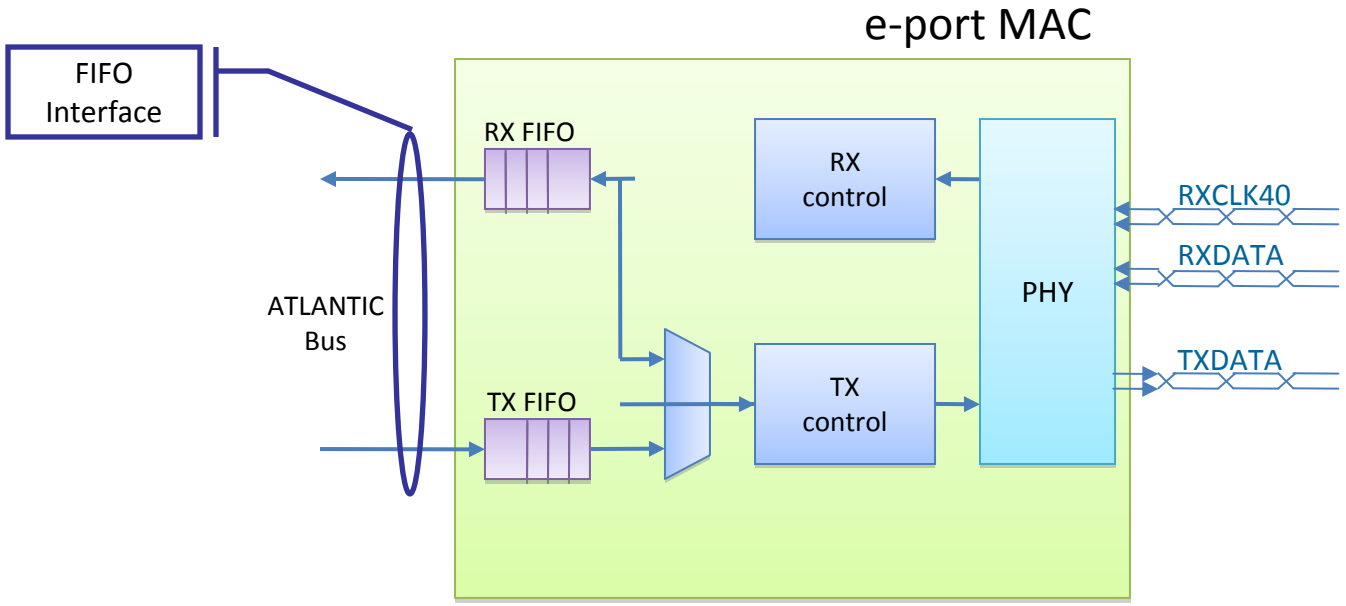
GBTX-TO-FRONTEND: E-Link Mode



Mode	Type	Data Rate	Notes
OFF	Power off	-	
B-Bus	parallel	80 MB/s	Up to 5 Bytes (DDR)
P-Bus	parallel	80 MW/s	One 40-bit word (DDR)
2 ×	serial	80 Mb/s	Up to 40 serial links
4 ×	serial	160 Mb/s	Up to 20 serial links
8 ×	serial	320 Mb/s	Up to 10 serial links
8 ×	serial-lanes	> 320 Mb/s	

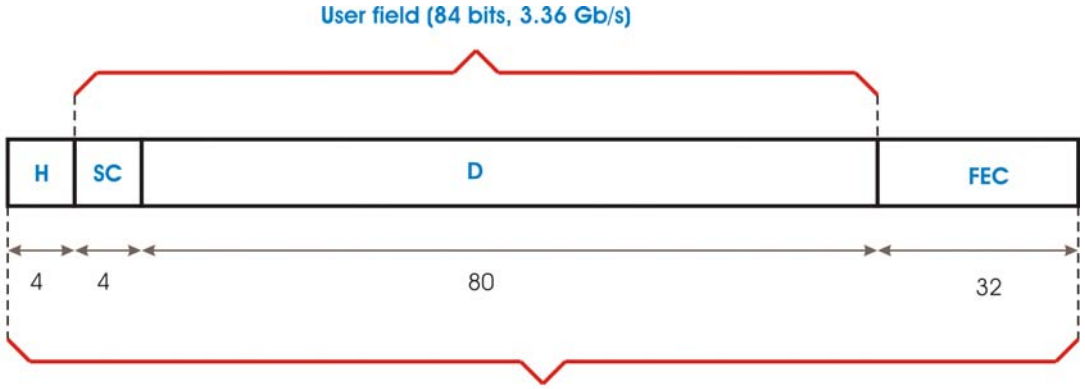
- *GBT/Frontend interface:*
  - Electrical links (e-link)
  - Serial
  - Bidirectional
  - Up to 40 links
- *Programmable data rate:*
  - Independently in five groups
  - 80 Mb/s, 160 Mb/s and 320 Mb/s
- *Lanes:*
  - To achieve > 320 Mb/s
  - Two or more e-links can be grouped forming a "lane"
- *Slow control channel:*
  - 80 Mb/s
- *E-Link:*
  - Three pairs: $D_{OUT}/D_{IN}/CLK$
  - SLVS
- *E-Links will be handled by E-ports:*
  - Electrically
  - "Protocol"

e-port Block Diagram



- *The FE interfaces with the GBTX through an e-port*
- *The e-port handles:*
  - The physical interface;
  - The multiple data rates;
  - The lanes (for bandwidth > 320 Mb/s)
  - Line coding:
    - Clock recovery (if required)
    - "AC coupling (if required)
- *The user application does not have to care about the frame formats in full detail*
  - It s done through a standard protocol:
    - Atlantic interface proposed (http://www.altera.com/products/ip/altera/t-alt-atlantic.html)
    - Fixed latency needs to be considered!
- *An E-Link Port Adaptor (EPA) "macro" will be available for integration in the front-end ASICs*

GBT Link Bandwidth

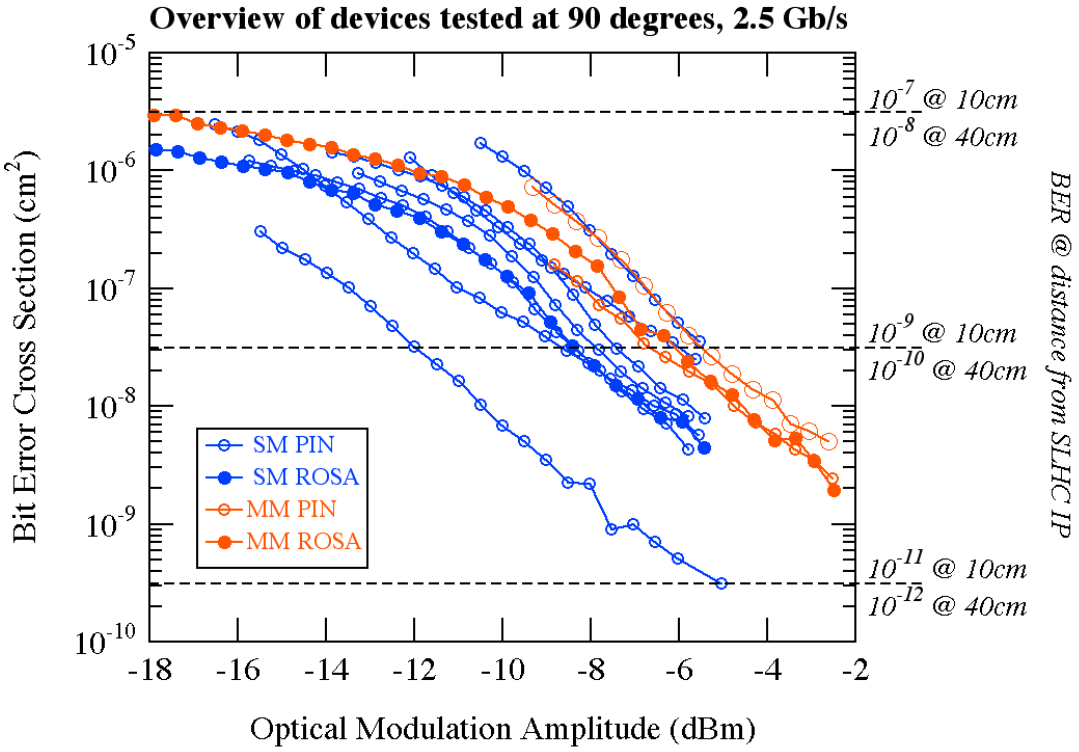


H: Header, 4 bits
SC:
GBT control, 2 bits (80 Mb/s)
Slow control port, 2bits (80 Mb/s)
D: DATA/TTC/EC - User data, 80 bits (3.2 Gb/s)
FEC: Forward Error correction, 32 bits

- *Bandwidth:*
  - User: 3.36 Gb/s
  - Line: 4.8 Gb/s
- *Dedicated channels:*
  - Link control: 80 Mb/s
  - Slow control channel: 80 Mb/s
- *DC balance:*
  - Scrambler
  - No bandwidth penalty
- *Forward Error Correction and Frame Synchronization*
  - Efficiency: 73%
  - To be compared with 8B/10B: 80% (no error correction capability)
- *Link is bidirectional*
- *Link is symmetrical:*
- *Down-link highly flexible:*
  (Will be clear later when discussing e-links)
  - Can convey unique data to each frontend device that it is serving
  - "Soft" architecture managed at the control room level
  - Other schemes would require dedicated topologies that will be difficult to accommodate on a generic ASIC like the GBTX
- *Now demonstrated to be compatible with FPGAs*

Single Event Upsets

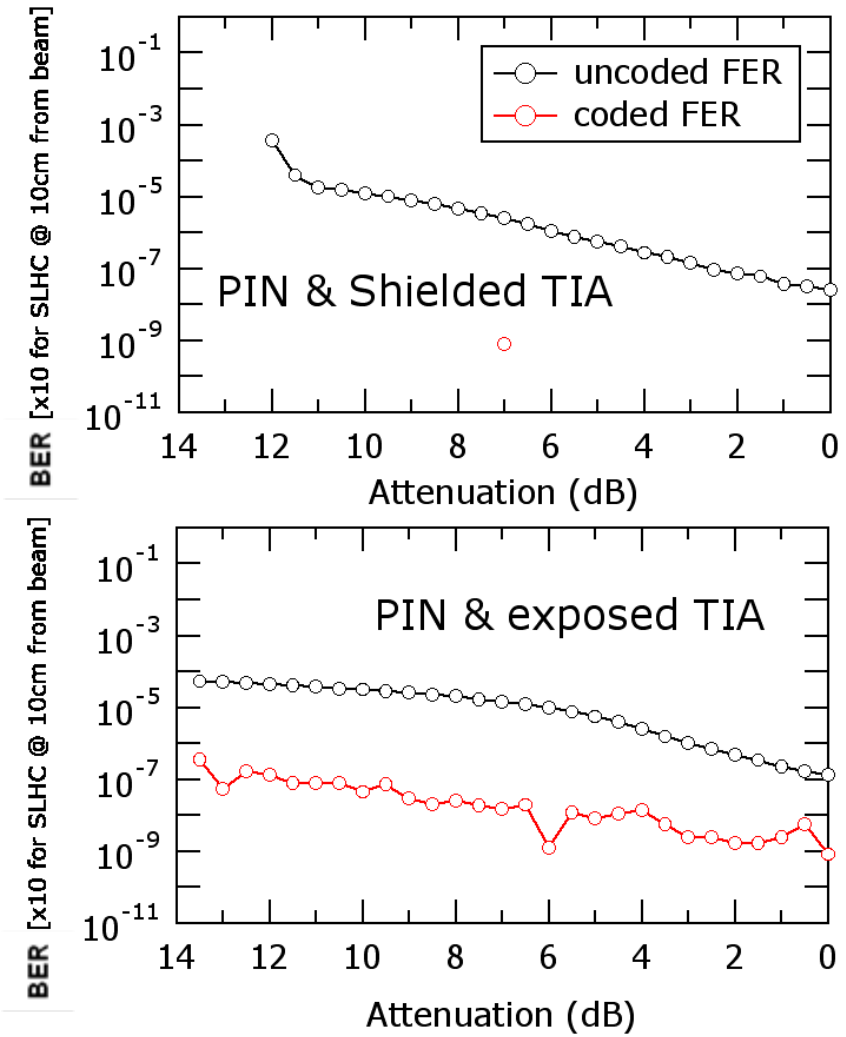
- *An issue that needs to be carefully addressed for SLHC links is the expected high rates of Single Event Upsets (SEU).*
- *Theses can be caused by:*
  - Particle "detection" by Photodiodes used in optical receivers.
  - SEUs on PIN-receivers, Laser-drivers and SERDES circuits
- *First SEU Test results on High Speed Links (1.5 - 2.5Gb/s)*
  - Carried out first survey of results in different devices in Dec.07



- 12 device types tested
  - PINs without TIA
  - ROSAs with TIA
- Confirmed that for Error-rates below 10^{-12} Error Correction is mandatory
- Measured Upsets lasting multiple bit periods for the first time

Forward Error Correction (FEC)

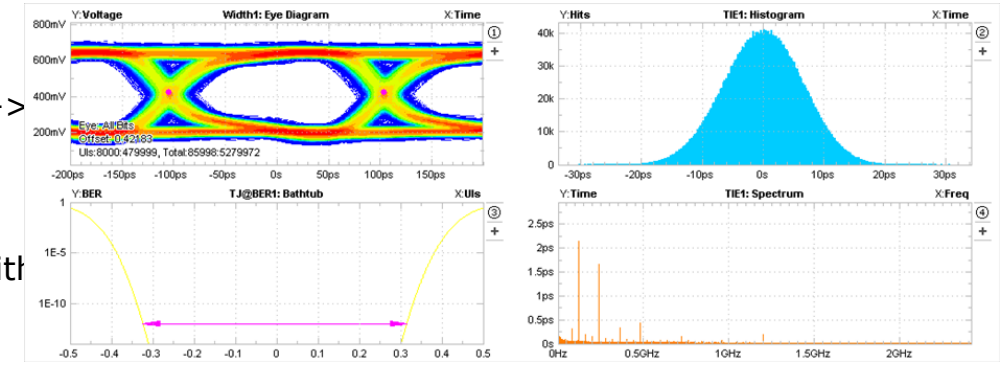
- *Objectives:*
  - Correct errors generated in the system:
    - PIN photodiode
    - Transceiver ASICs (TIA/LD)
    - Fast SERDES circuits (can't use TMR)
  - Requirements
    - Minimal latency
    - Minimal coding overhead
    - Merged with line-coding
    - Compatible with FPGA embedded SerDes
- *Proposed code:*
  - Interleaved Reed-Solomon double error correction (Similar to today's CDs)
  - 4-bit symbols (RS(15,11))
  - Interleaving: 2
  - Error correction capability:
    - **$2_{\text{Interleaving}} \times 2_{\text{RS}}$ = 4 symbols ≅ 16-bits**
  - Code efficiency: 88/120 = 73%
  - Line speed: 4.80 Gb/s
  - Coding/decoding latency: one 25 ns cycle
- *GBT frame efficiency: 70%*
  - A line code is always required for DC balance and synchronization
  - For comparison, the Gigabit Ethernet frame efficiency is 80% (at the physical level)
  - At a small penalty (10%, when compared with the Gigabit Ethernet) the GBT protocol will offer the benefits of Error Detection and Correction



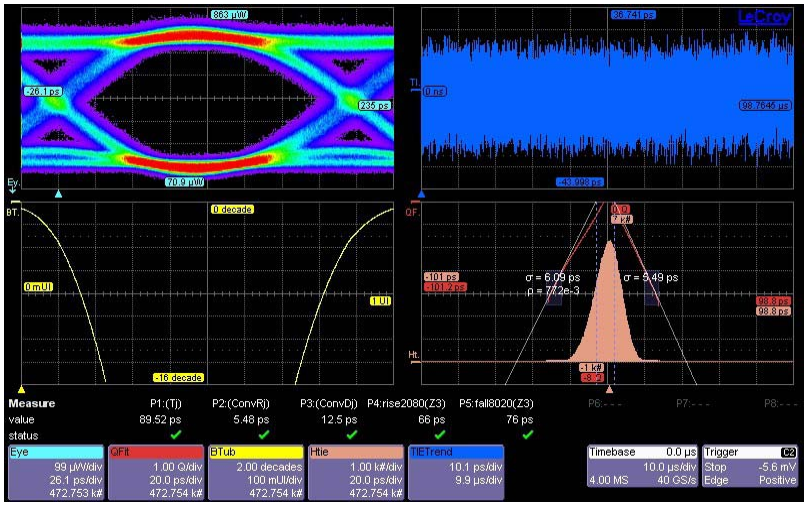
FPGA implementation of the GBT protocol

- *Full chain implemented:*
  - Scrambler -> Encoder -> Serializer -> link/cable -> Deserializer -> Decoder -> Descrambler
- *XILINX Virtex-4FX*
  - Electrical & Optical loop-back tested with commercial TRx
  - @ 4.8Gb/s: T_j = 75ps
- *ALTERA StratixII GX*
  - Encoder/decoder chain
  - Optical loop-back
  - @ 4.8 Gb/s: T_j = 89 ps
  - @ 6.4 Gb/s: T_j = 83 ps
- *To be demonstrated:*
  - Can fixed and "deterministic" latency links be implemented with FPGAs?
- *Engineers:*
  - Sophie Baron – CERN, Switzerland
  - Jean-Pierre Cachemiche – CPPM, France
  - Frederic Marin– CPPM, France
  - Csaba Soos – CERN, Switzerland

Xilinx - 4.8 Gb/s



Altera + opto TRx - 4.8 Gb/s



GBTIA

Main specs:

- Bit rate 5 Gb/s (min)
- Sensitivity: 20 µA P-P (10^{-12} BER)
- Total jitter: < 40 ps P-P
- Input overload: 1.6 mA (max)
- Dark current: 0 to 1 mA
- Supply voltage: 2.5 V
- Power consumption: 250 mW
- Die size: 0.75 mm × 1.25 mm

Engineers :

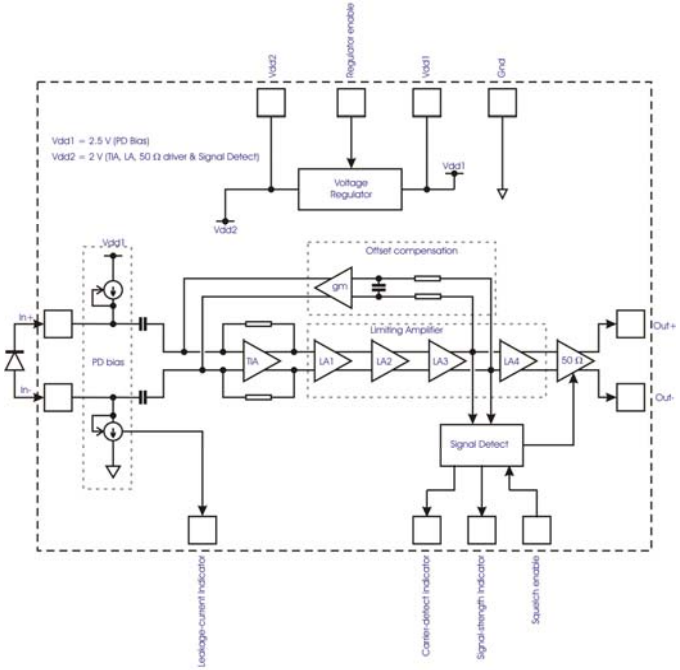
- Ping Gui – SMU, USA
- Mohsine Menouni – CPPM, France

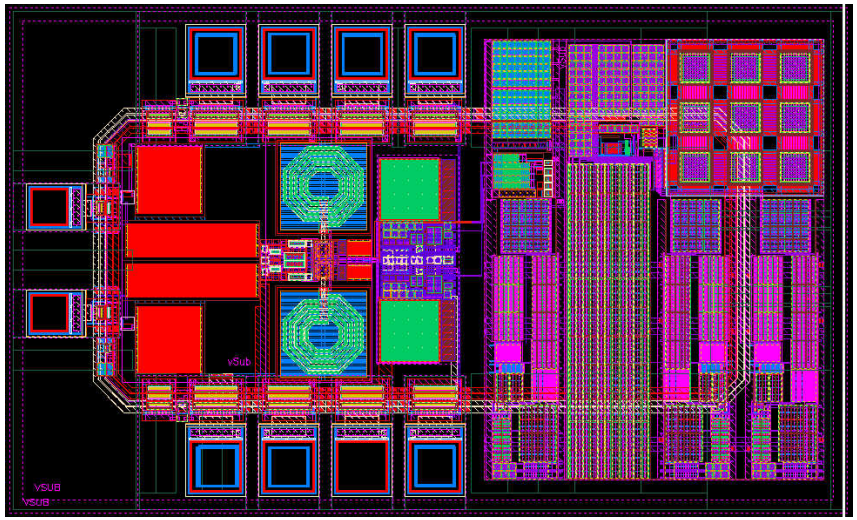
Packaging:

- Part of the versatile link project

Status:

- Chip submitted: 2008/07/12
- Received: January 2009
- Tests in preparation!

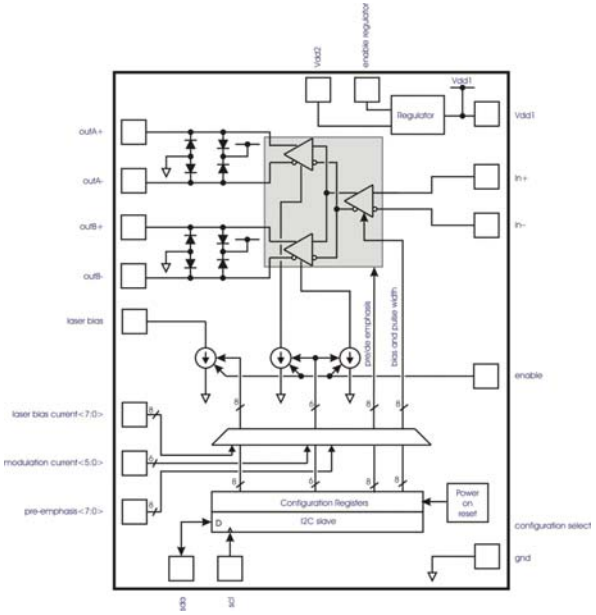




GBLD

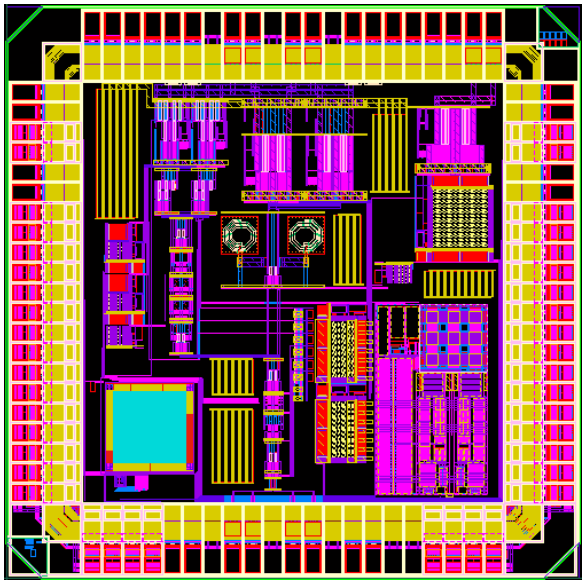
Main specs:

- Bit rate 5 Gb/s (min)
- Modulation:
  - current sink
  - Single-ended/differential
- Laser modulation current: 2 to 12 mA
- Laser bias: 2 to 43 mA
- "Equalization"
  - Pre-emphasis/de-emphasis
  - Independently programmable for rising/falling edges
- Supply voltage: 2.5 V
- Die size: 2 mm × 2 mm
- I2C programming interface



Engineers :

- Gianni Mazza – INFN, Italy
- Angelo Rivetti – INFN, Italy
- Ken Wyllie – CERN, Switzerland



Packaging:

- Part of the versatile link project

Status:

- Chip submitted: 2008/07/12
- Received: January 2009
- Tests in preparation!

e-Port

Specification work in progress

- Two "tentative" protocols already "proposed":

7B/8B

- Balanced
- Fixed latency
- Suitable for Trigger commands links
- RTL code under development

High-Level Data Link Control (HDLC)

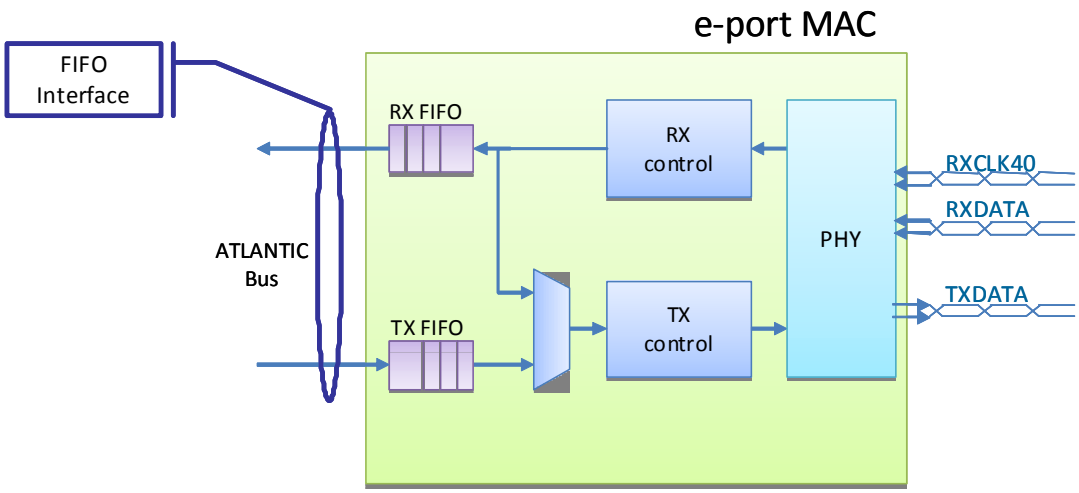
- Packet oriented data
- Bandwidth efficiency (~96%)
- Non-fixed latency
- Suitable for slow control and data links
- RTL code ready

To be specified

- Clock recovery and phase alignment
- Lanes support

Engineers:

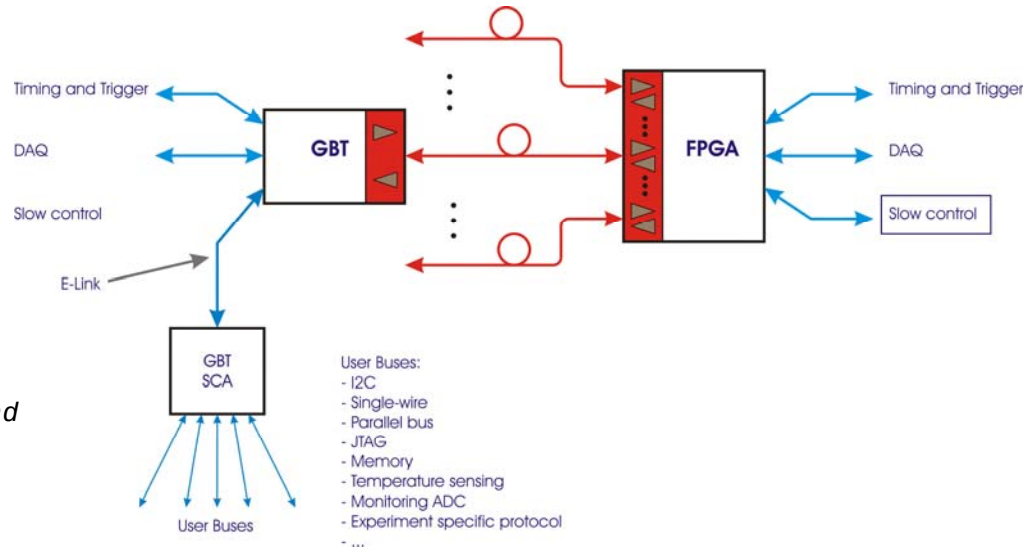
- Sandro Bonacini – CERN, Switzerland
- Kostas Kloukinas – CERN, Switzerland



Slow Control & Monitoring ASIC: GBT - SCA

GBT-SCA Main specs:

- Dedicated to slow control functions
- Interfaces with the GBTX using a dedicated E-link port
- Communicates with the control room using a protocol carried (transparently) by the GBT
- Implements multiple protocol busses and functions:
  - I2C, JTAG, Single-wire, parallel-port, etc…
- Implements environment monitoring functions:
  - Temperature sensing
  - Multi-channel ADC



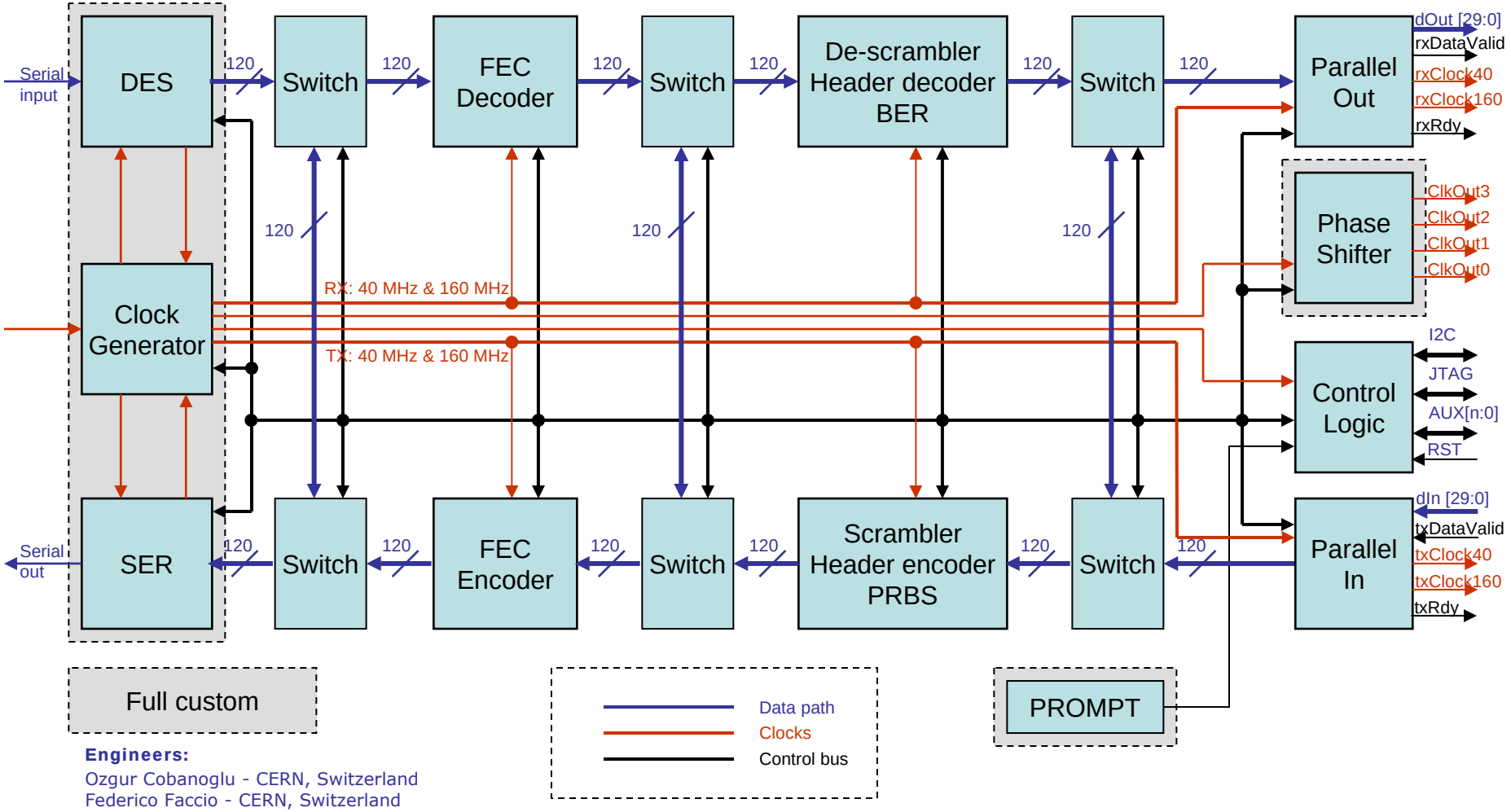
Engineers:

- *Alessandro Gabrielli – INFN, Italy*
- *Kostas Kloukinas – CERN, Switzerland*
- *Alessandro Marchioro – CERN, Switzerland*
- *Antonio Ranieri – INFN, Italy*
- *Giuseppe De Robertis – INFN, Italy*

Status

- Specification work undergoing:
- 1st Draft already available
- RTL design undergoing
- Tape-out: 4th Quarter 2009

GBTX Transceiver



Engineers:
Ozgur Cobanoglu - CERN, Switzerland
Federico Faccio - CERN, Switzerland
Rui Francisco – INESC, Portugal
Ping Gui – SMU, USA
Alessandro Marchioro - CERN, Switzerland
Paulo Moreira - CERN, Switzerland
Christian Paillard - CERN, Switzerland
Ken Wyllie - CERN, Switzerland

Project Schedule

- *2008*
  - Design and prototyping of performance critical building blocks:
    - TIA, laser driver, PLL, serializer, de-serializer, phase shifter
  - First tests of optoelectronics components
    - (e.g. to understand SEU in PIN receivers)
  - Proceed with the link specification meetings
  - General link specification

- *2009*
  - Design/prototype/test of basic serializer/de-serializer chip
  - Design/prototype/test of optoelectronics packaging
  - Detailed link specification document

- *2010*
  - Prototype of "complete" link SERDES chip
  - Full prototype of optoelectronics packaging

- *2011*
  - Extensive test and qualification of full link prototypes
  - System demonstrator(s) with use of full link
  - Schedule of the final production version is strongly dependent on the evolution of the LHC upgrade schedule

Radiation Hard Optical Link Project Collaborators

Institute	Project Management	System Design	ASIC Design	FPGA Design	Opto-Electronics	Passive Components	Radiation Testing
CERN	x	x	x	x	x	x	x
CPPM Marseille			x	x			
FERMILAB					x		
INFN Bari			x				
INFN Bologna		x	x				
INFN Torino			x				
Oxford						x	x
SMU Dallas		x	x	x			x

Additional slides

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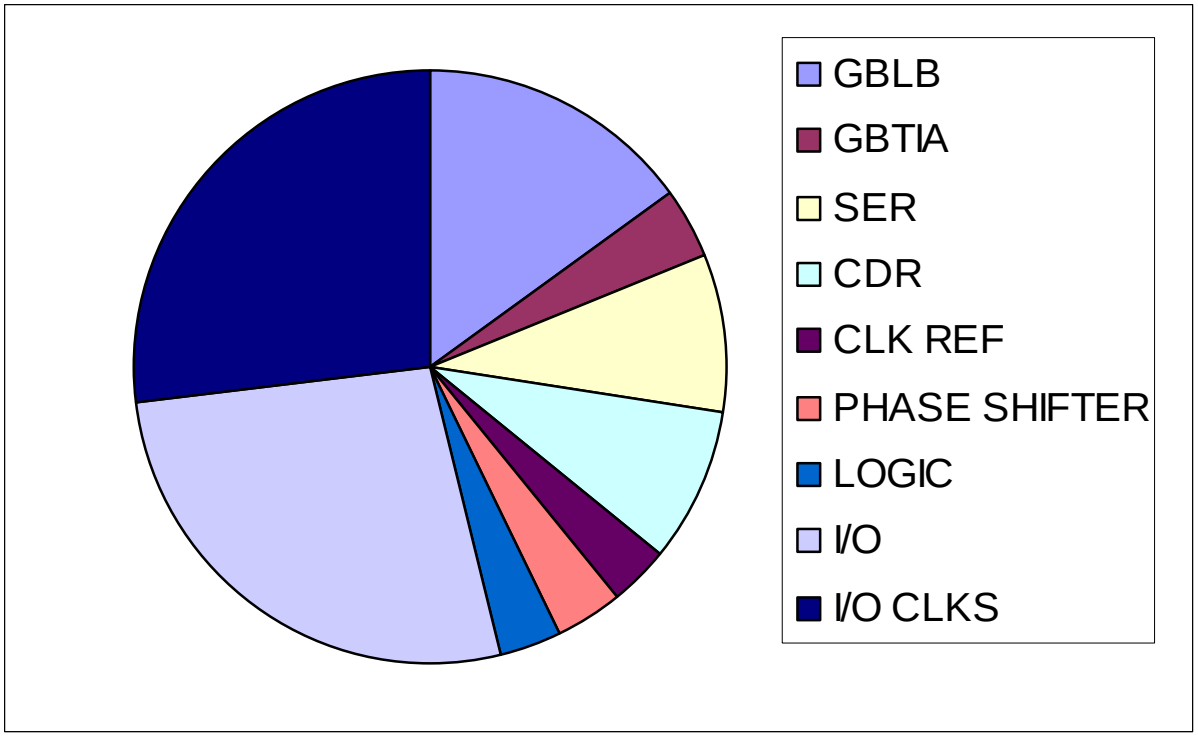
Power consumption: GBTIA + GBLD + GBTX



GBLD	450 mW
GBTIA	115 mW
SER	250 mW
CDR	250 mW
CLK REF	100 mW
PHASE SHIFTER	110 mW
LOGIC	100 mW
I/O	800 mW
I/O CLKS	800 mW
Total	2975 mW