Serial power circuitry in the ABC-Next and FE-I4 chips

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including material from ***Michael Karagounis***
on development at Bonn University

How the serial powering started

Serial powering of pixel modules

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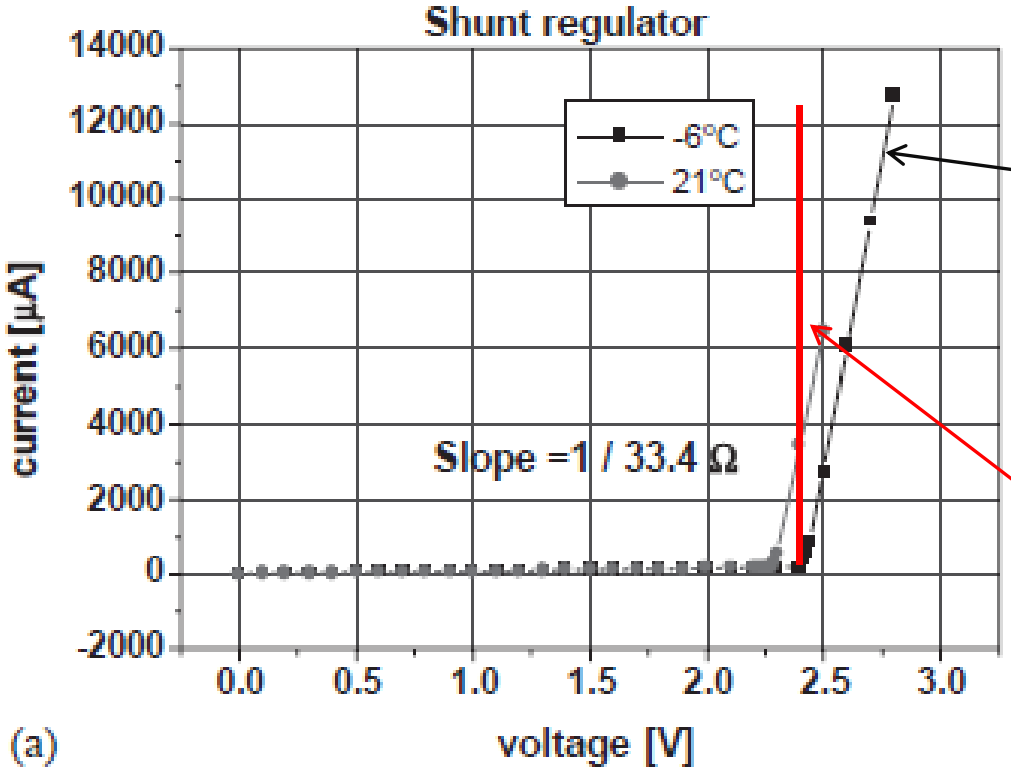


Critical problem of mismatch when connecting such devices in parallel has been overcome by making relatively large output resistance.

Ultimately we need much lower output resistance and so much better regulation of the output voltage.

Distributed shunt regulator

Power dissipated in the shunt regulators is distributed uniformly across the hybrid.

No very high current devices required.

Single point of failure reduced compared to one regulator per hybrid.

Hybrid design fully scaleable with respect to power distribution.

but ……

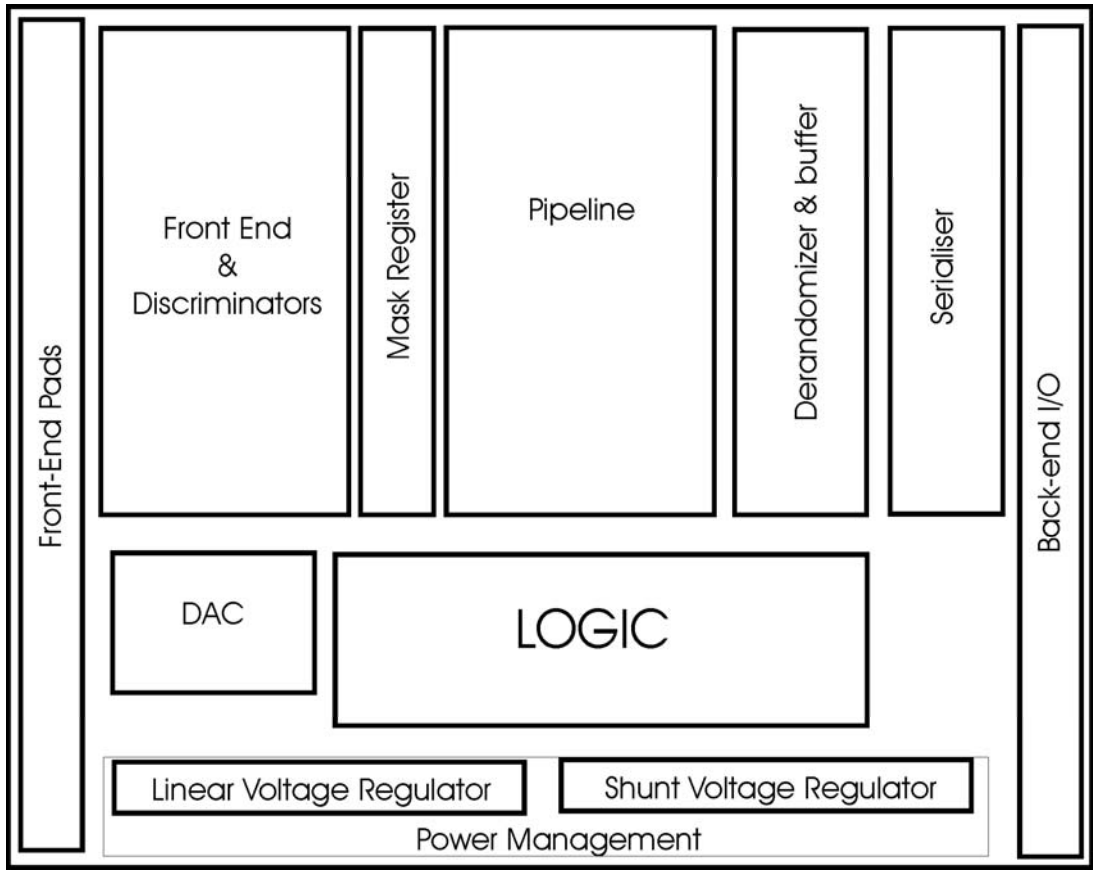
Matching becomes critical when making the shunt regulators of low output resistance.

New shunt regulator circuits suitable for integration in the readout chips have been developed independently for the strip readout and the pixel readout.

Serial powering in strip readout

Prototype chip for Si strip readout in Upgrade Inner Tracker

- **Binary readout**
- **Front-end optimised for short strips**
- **Positive or negative input charge**
- **Readout clock up to 160 Mbits/sec**
- **250 nm CMOS (IBM) technology**
- **2.5 V digital power supply (100 mA)**
- **2.2 V analogue power supply (30 mA)**
- **Compatible with serial powering scheme**



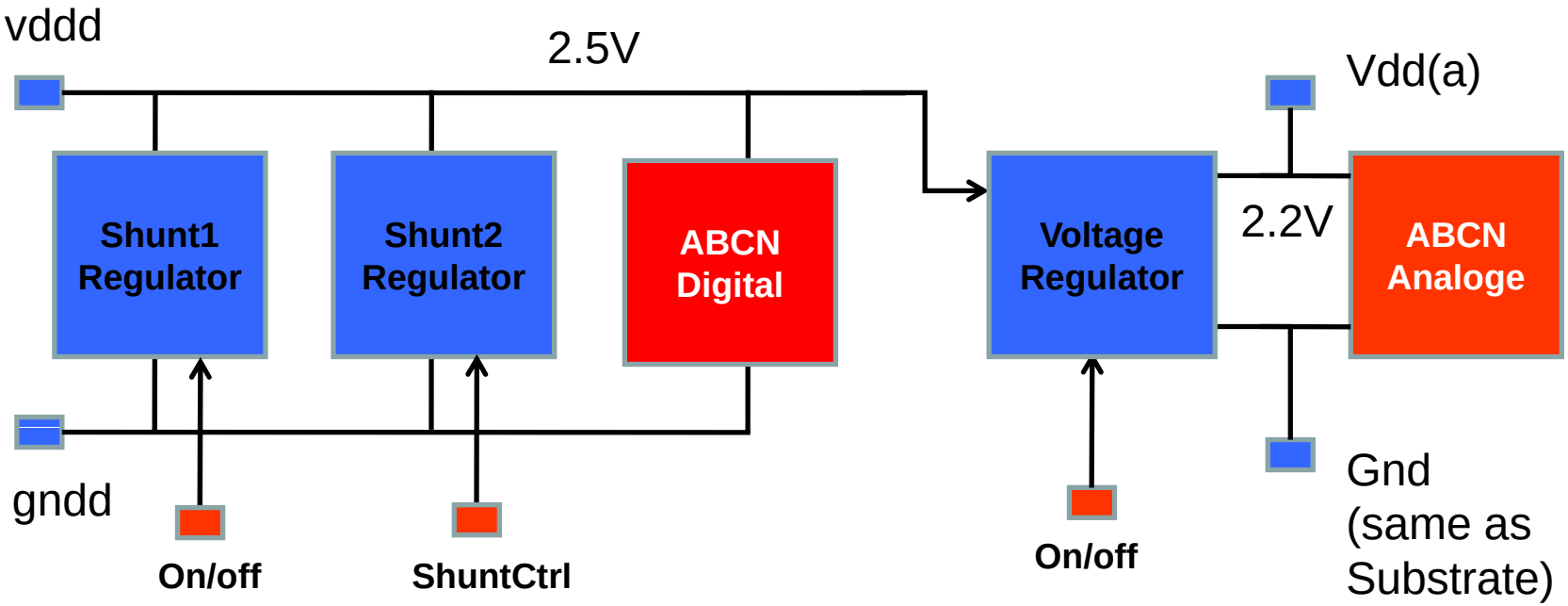
On chip power management and distribution

Two optional shunt regulators

A. Full shunt regulator in each ABCN chip

B. Shunt transistor in each ABCN and regulation circuitry external common for all chips on the moule

Serial voltage regulator (optional)



Powering-up modules

Nominal powering-up scenario

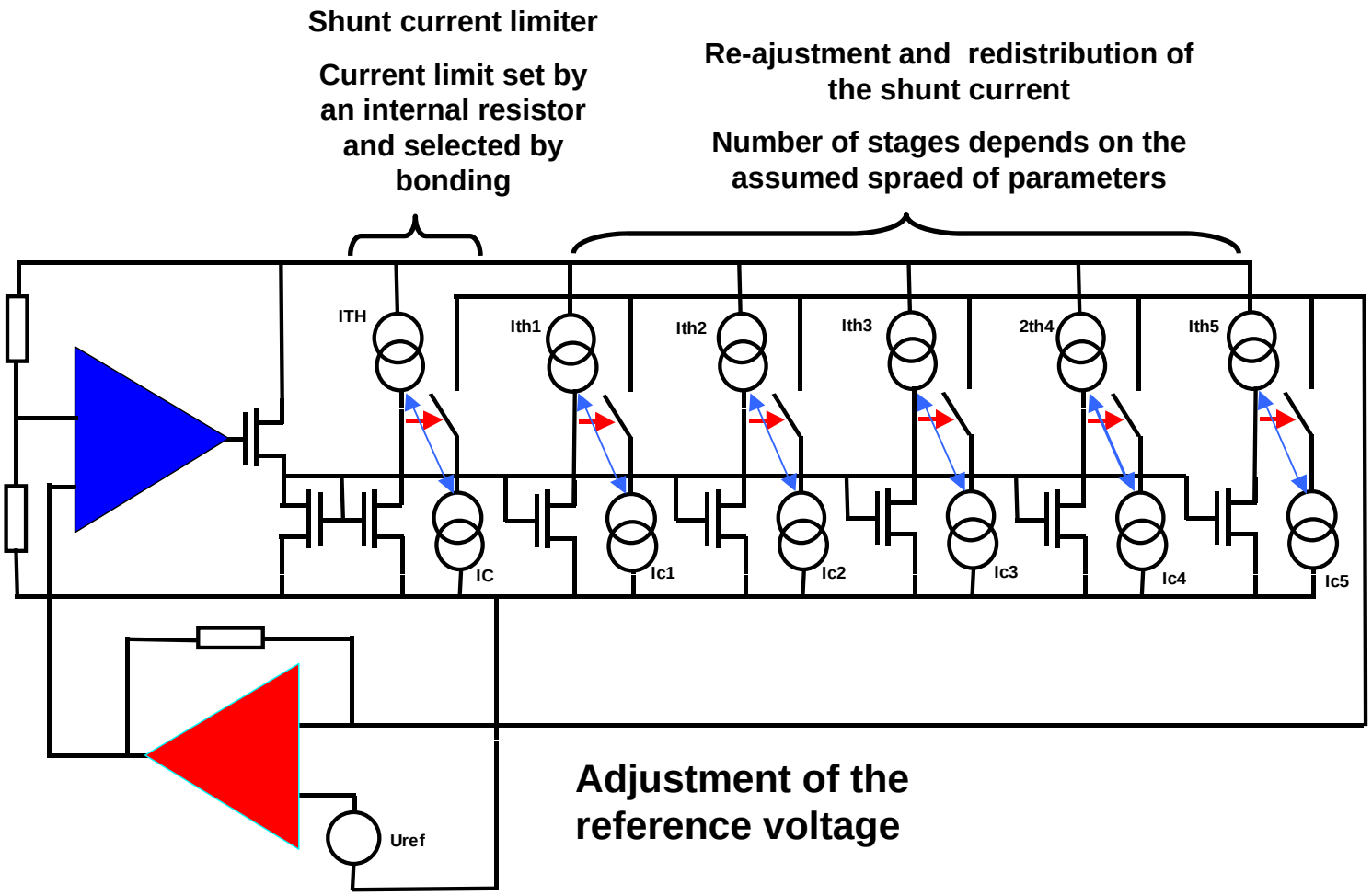
Supply current ramped up to the nominal required value with clock signal active in the digital part – digital switching current increase smoothly following the I-V characteristic of the digital load.

Critical scenarios

Clock signal is delayed with respect the power start-up – supply current forced by external current supply may temporarily go much above the ABCN current consumption.

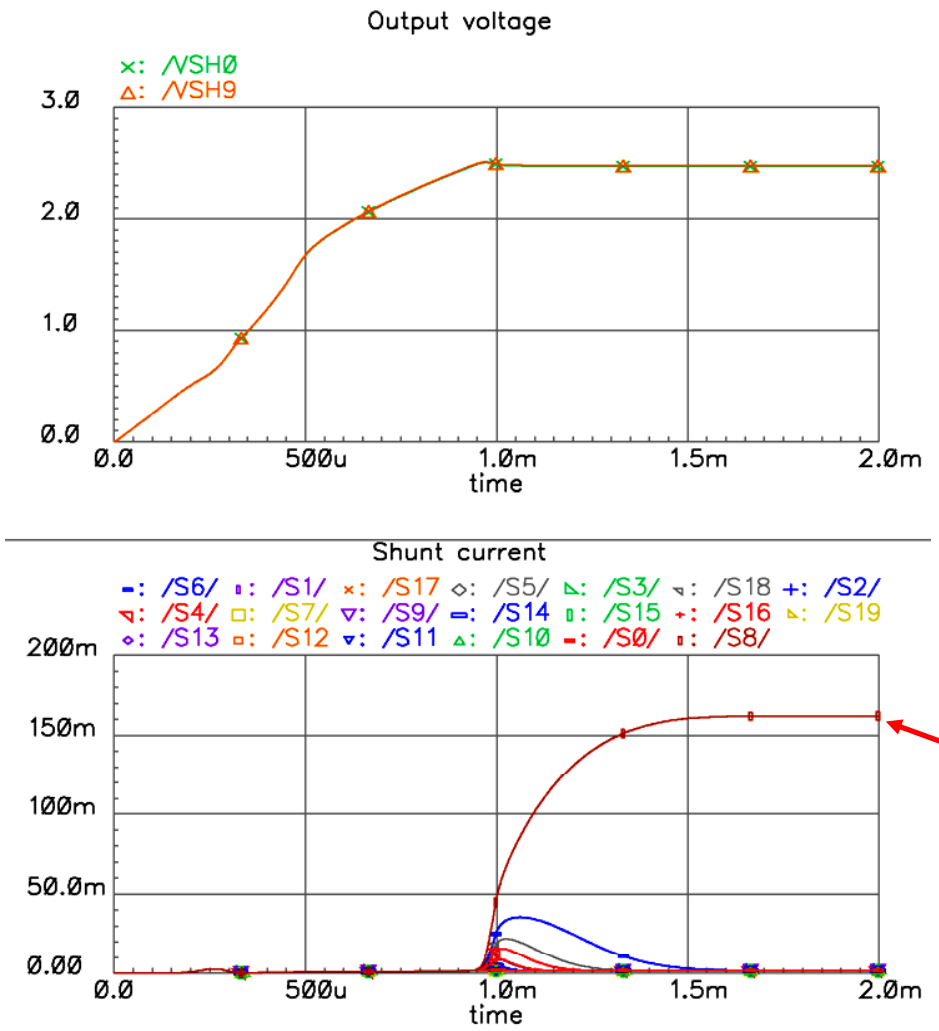
Clock signal lost suddenly during normal operation – digital current consumption suddenly reduced.

Full shunt regulator on chip - design concept



Matching problem (simulation)

Clock is ON all the time



20 ABCNs with internal shunt regulators connected in parallel.

All mismatch effects represented by mismatch of reference voltages.

Flat distribution in a range –10 mV to +10 mV assumed.

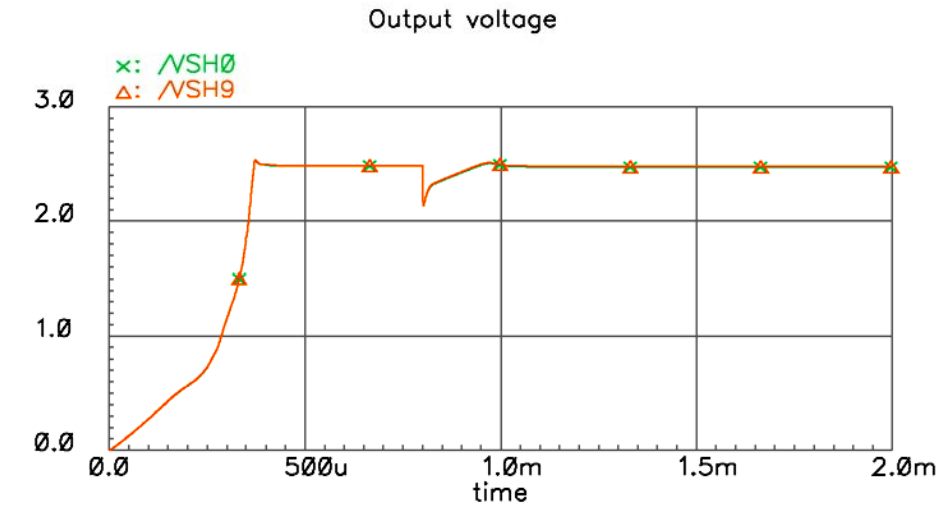
Average shunt current of 8 mA per device.

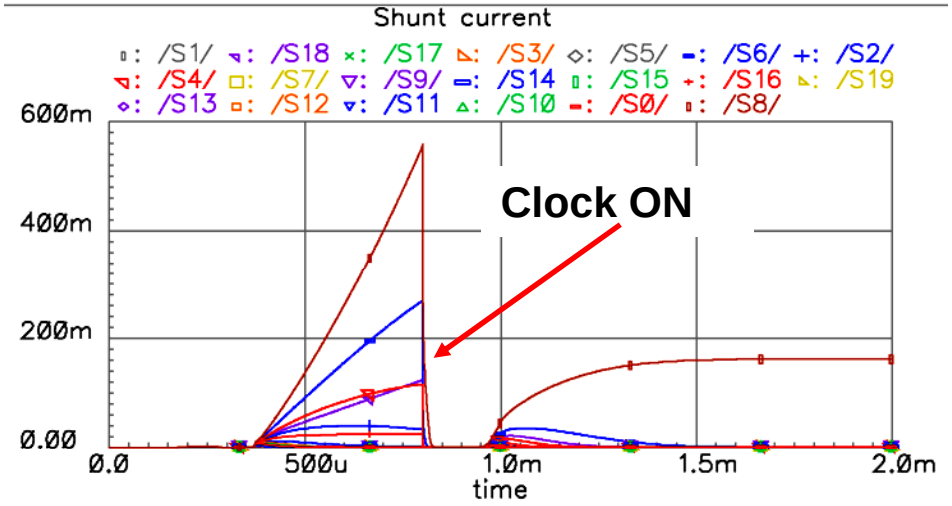
One shunt device always wins

This would happen even if we assumed perfect matching because of the voltage drops along the power busses on the hybrid.

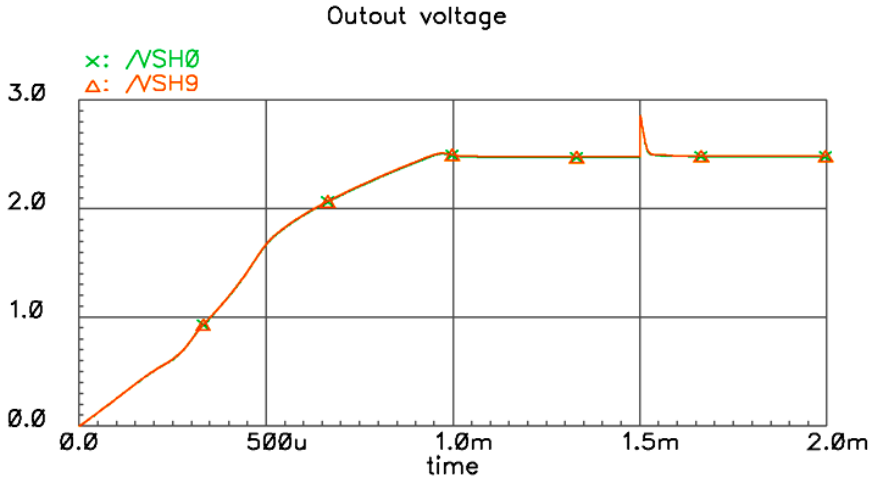
Matching problem (simulation)

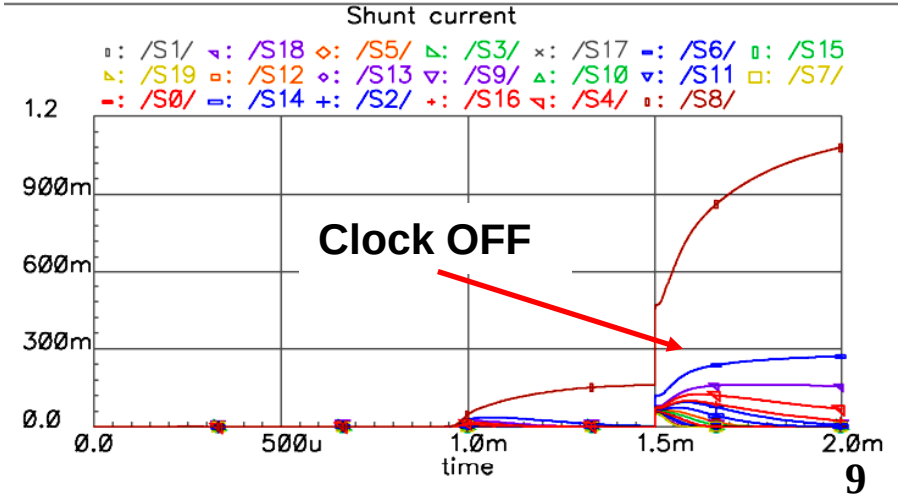
Clock delayed





Clock OFF during operation

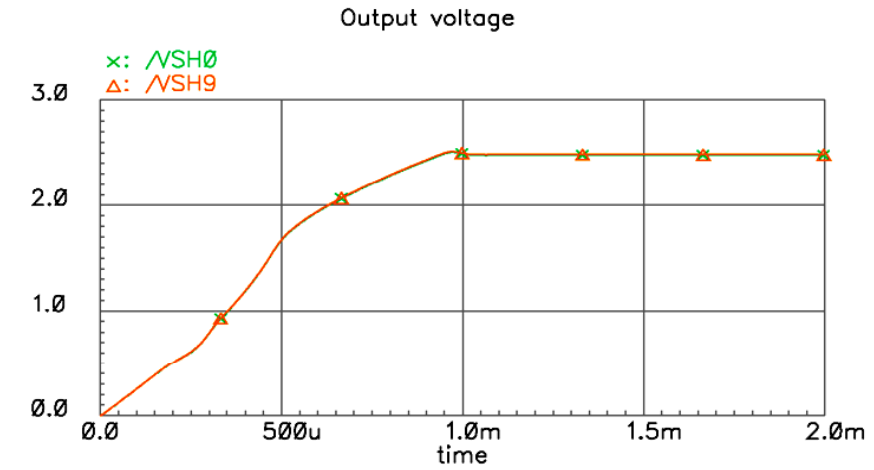


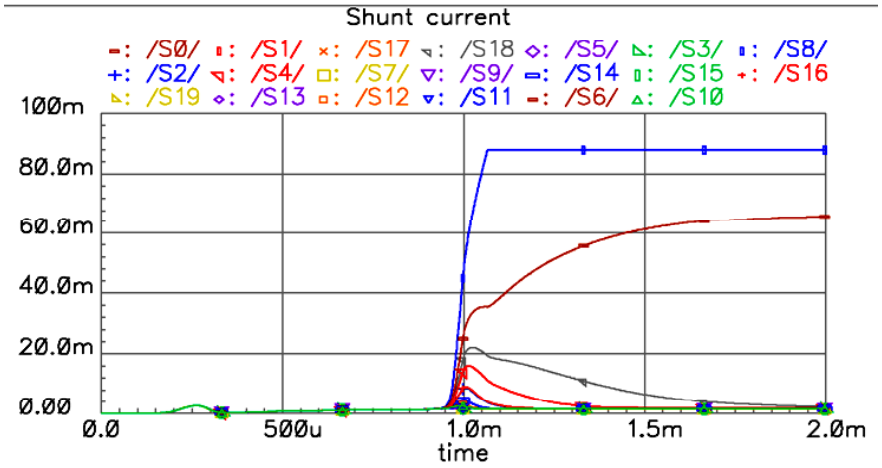


Performance of the auxiliary circuits (simulation)

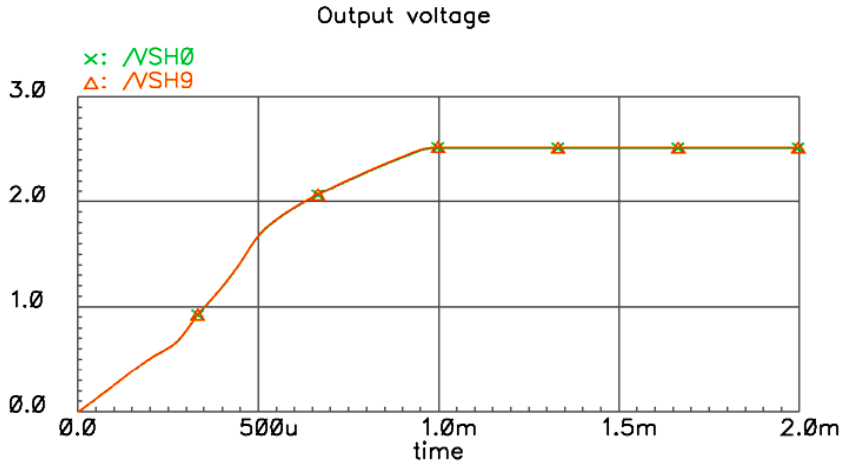
Clock is ON all the time

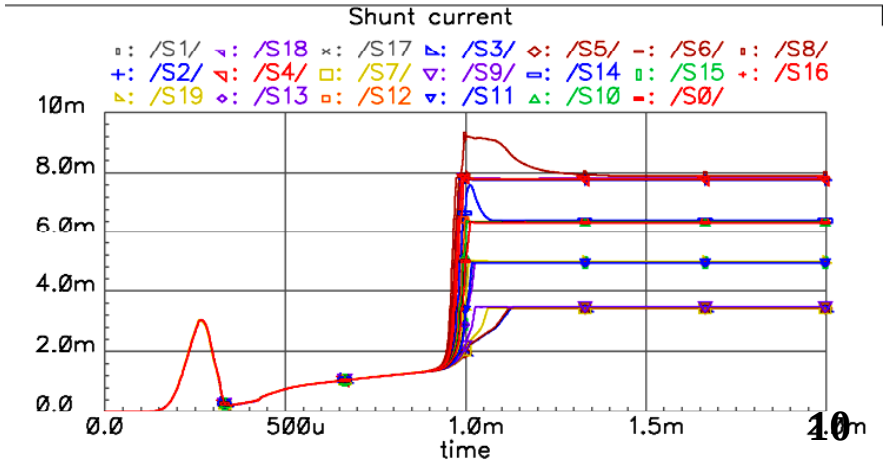
Only current limiter active





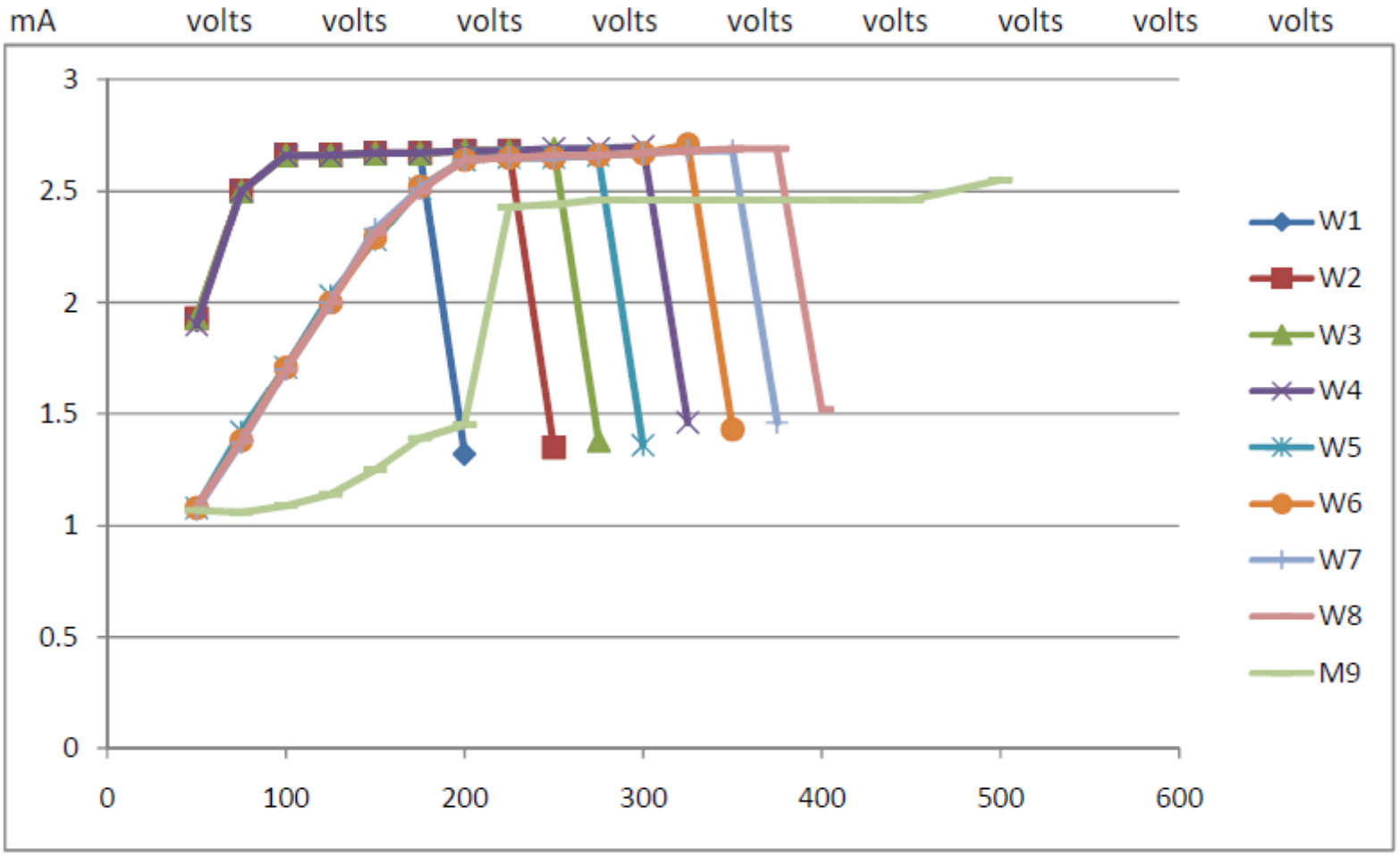
All circuitry active



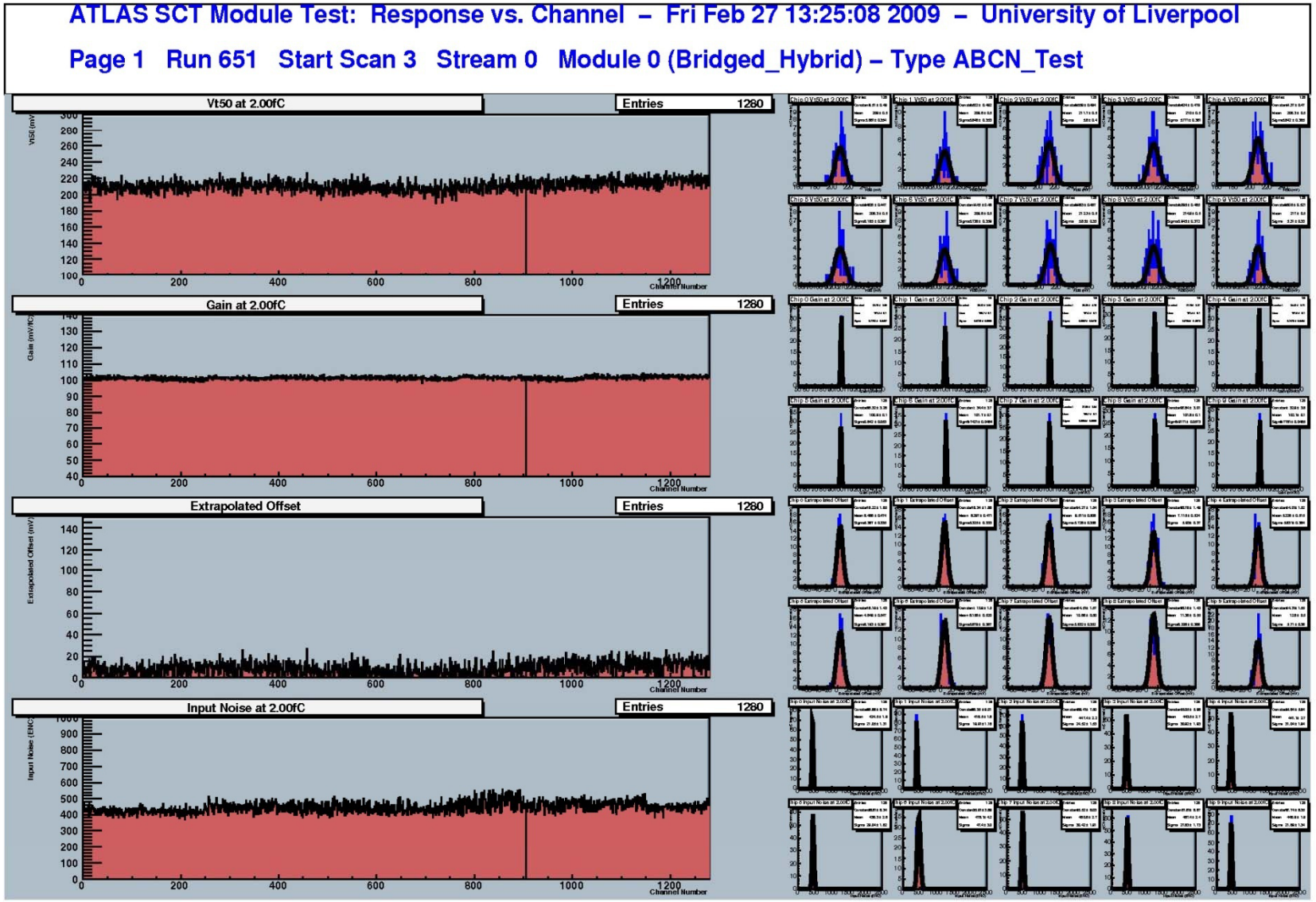


Performance of the current limiter (measurements)

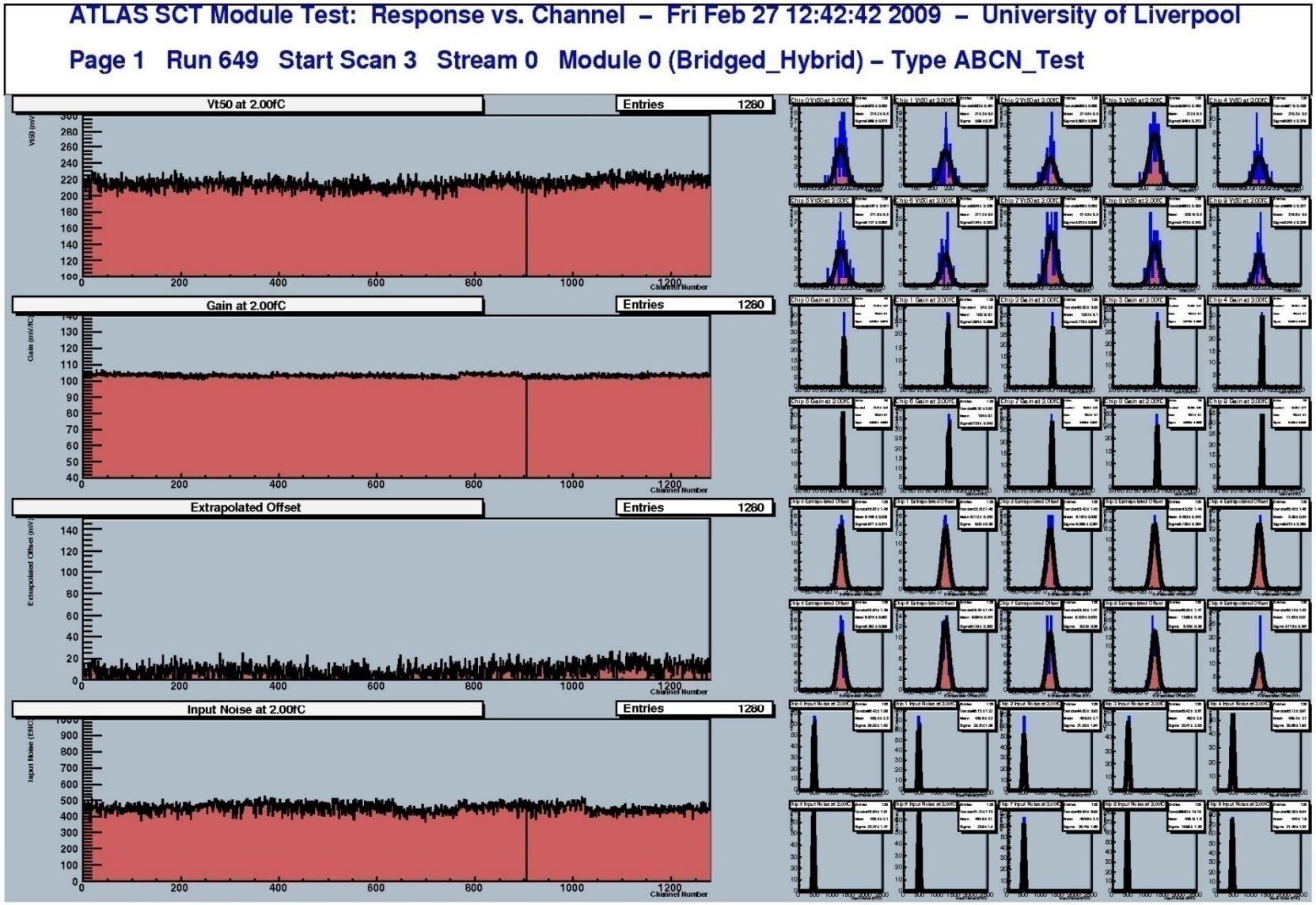
Single ABCN



20 chips hybrid – powered conventionally



20 chips hybrid – powered through internal shunts



ABCN in 130 nm

Design assumptions

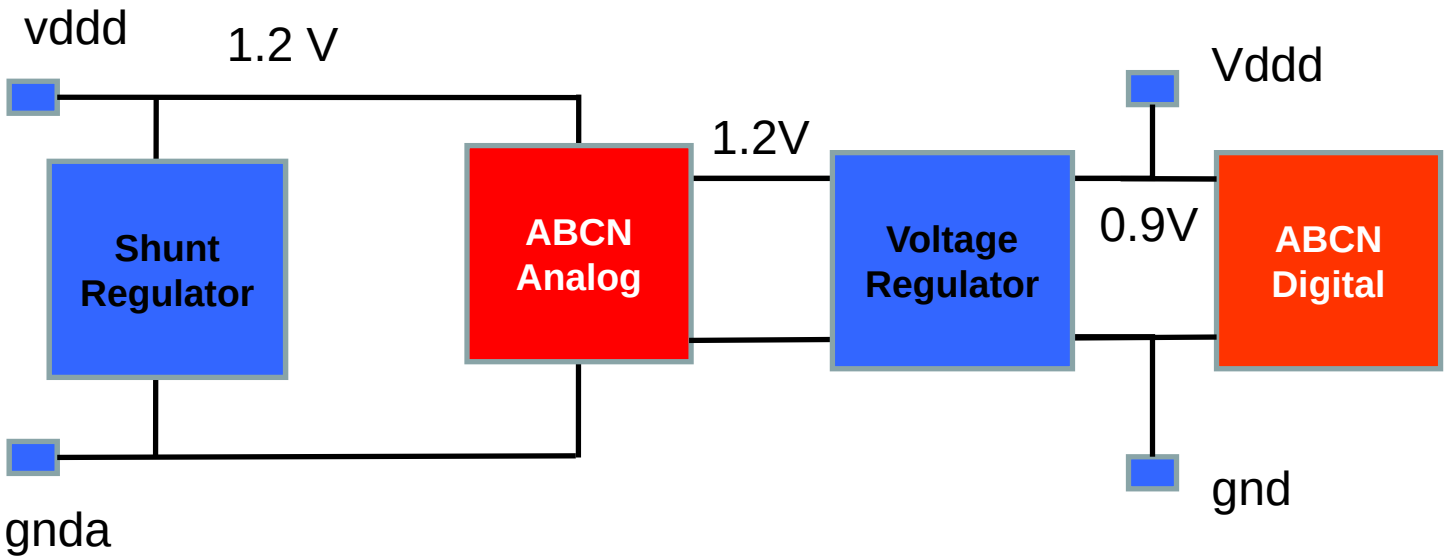
Estimate of power in ABCN130n by Mitch Newcomer

130 nm Estimate 128 Channels / chip	Supply	Short Strip Power, Current	Long Strip Power, current
Analog	VDDA @ 1.2V	20 mW, 16mA	39 mW, 32mA
Digital Supply	VDD @ 0.9V	46 mW, 51mA	46 mW, 51mA
Total Power* / Chip (ref ABCn 290mW)		66 mW	85 mW
Total Power * / 20 Chip Module		1.3 W	1.7 W

Power supply voltages are not compatible with the power management schema implemented in ABCN (250 nm) assuming serial powering.

Possible schema of power management in ABCN (130 nm)

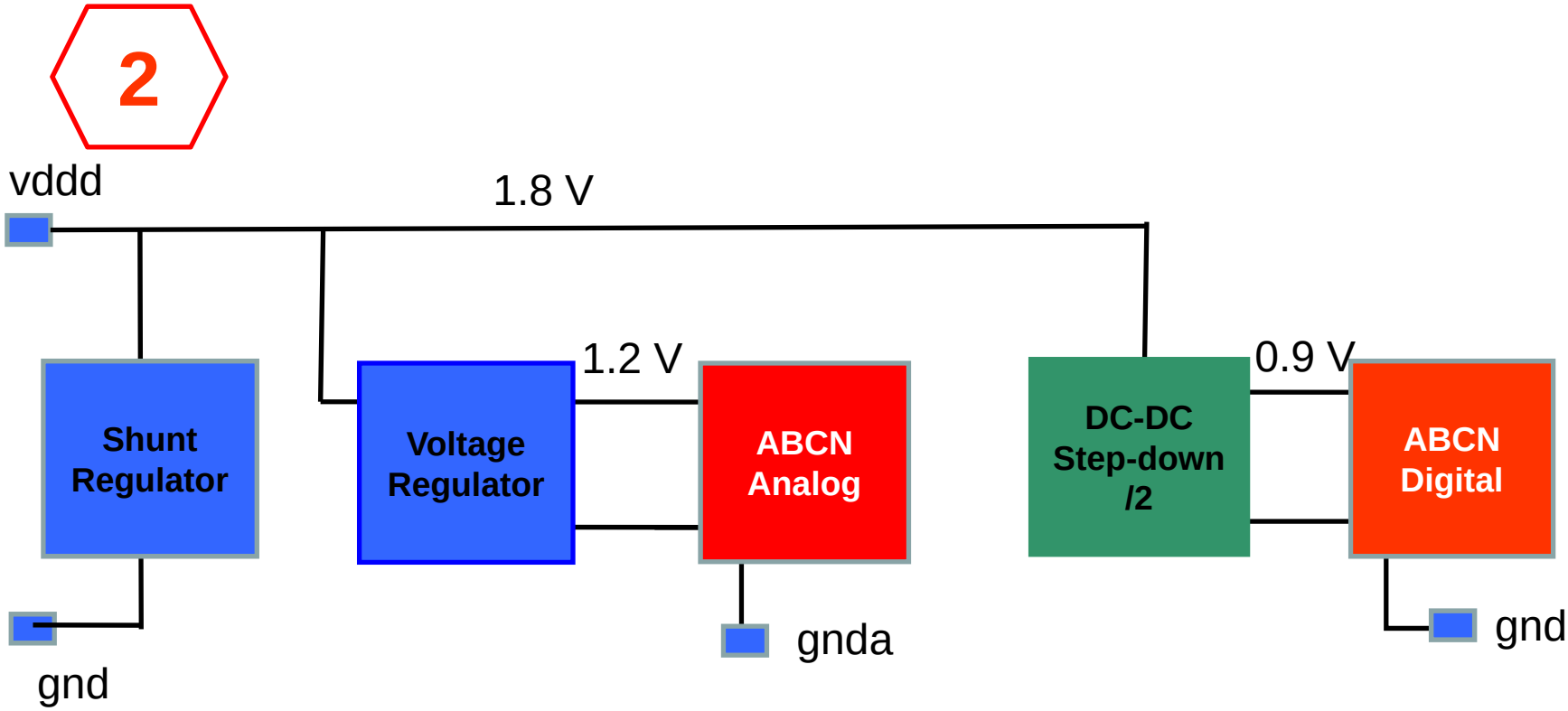
1



Quality of analogue power supply ?

Some saving of digital power due to lower voltage swing

Possible schema of power management in ABCN (130 nm)



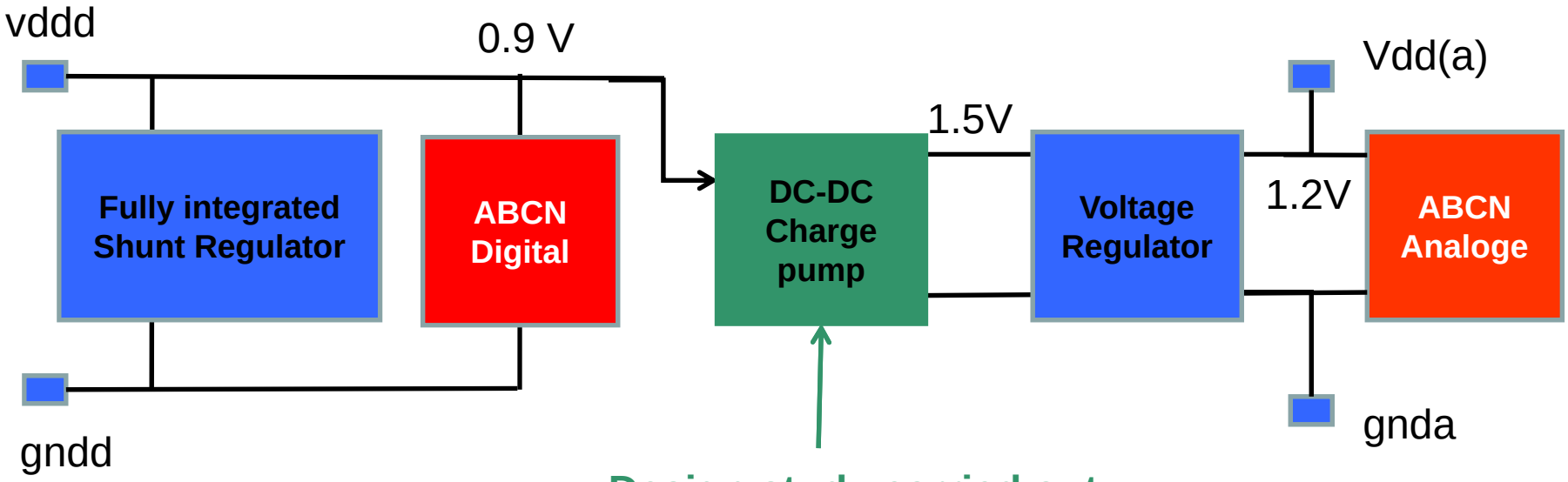
Overhead in voltage drop in the linear regulator (loss of efficiency)

No regulation on the digital power line (?)

DC-DC converter 3/2 step down may improve the efficiency

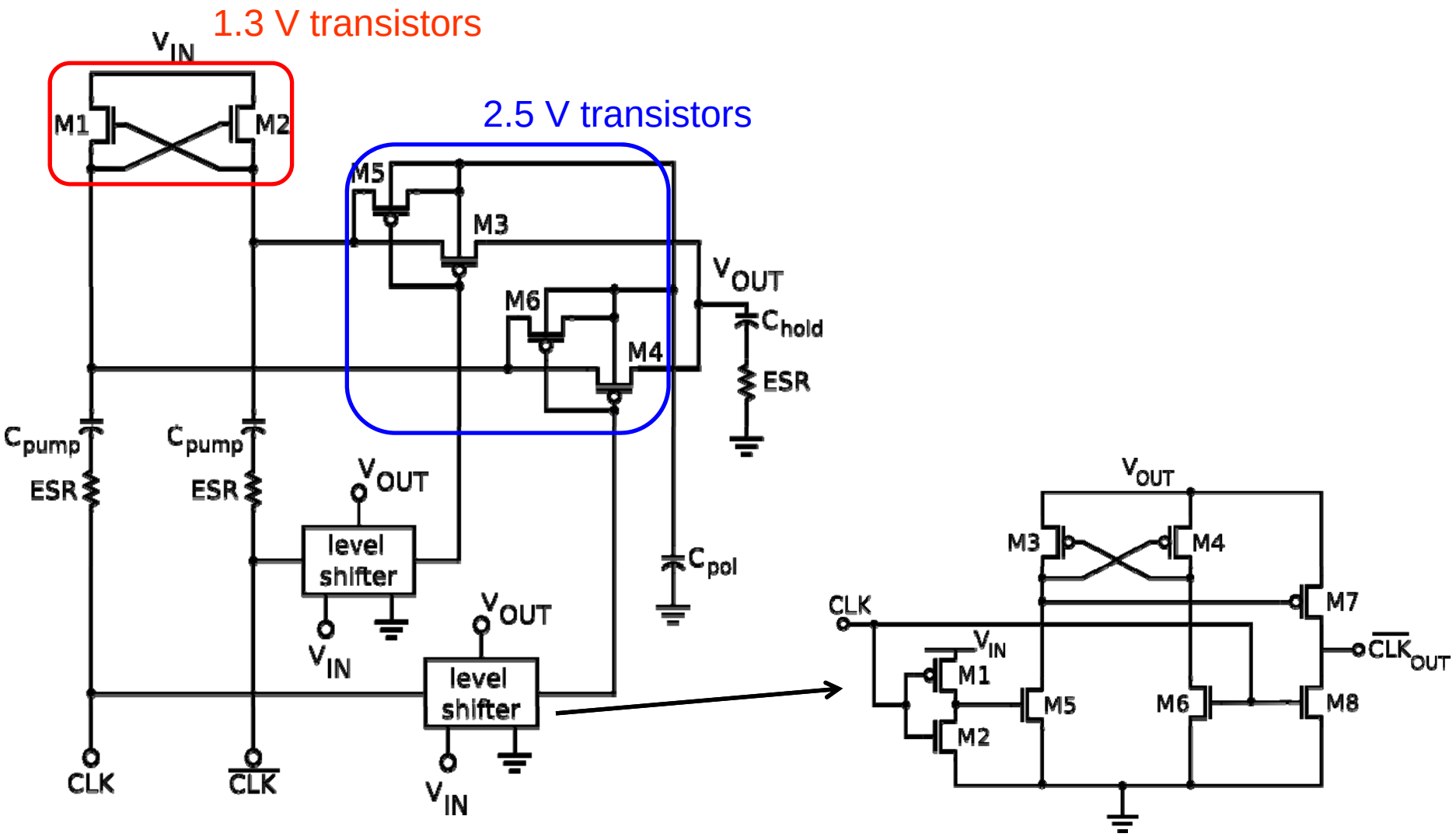
Possible schema of power management in ABCN (130 nm)

3

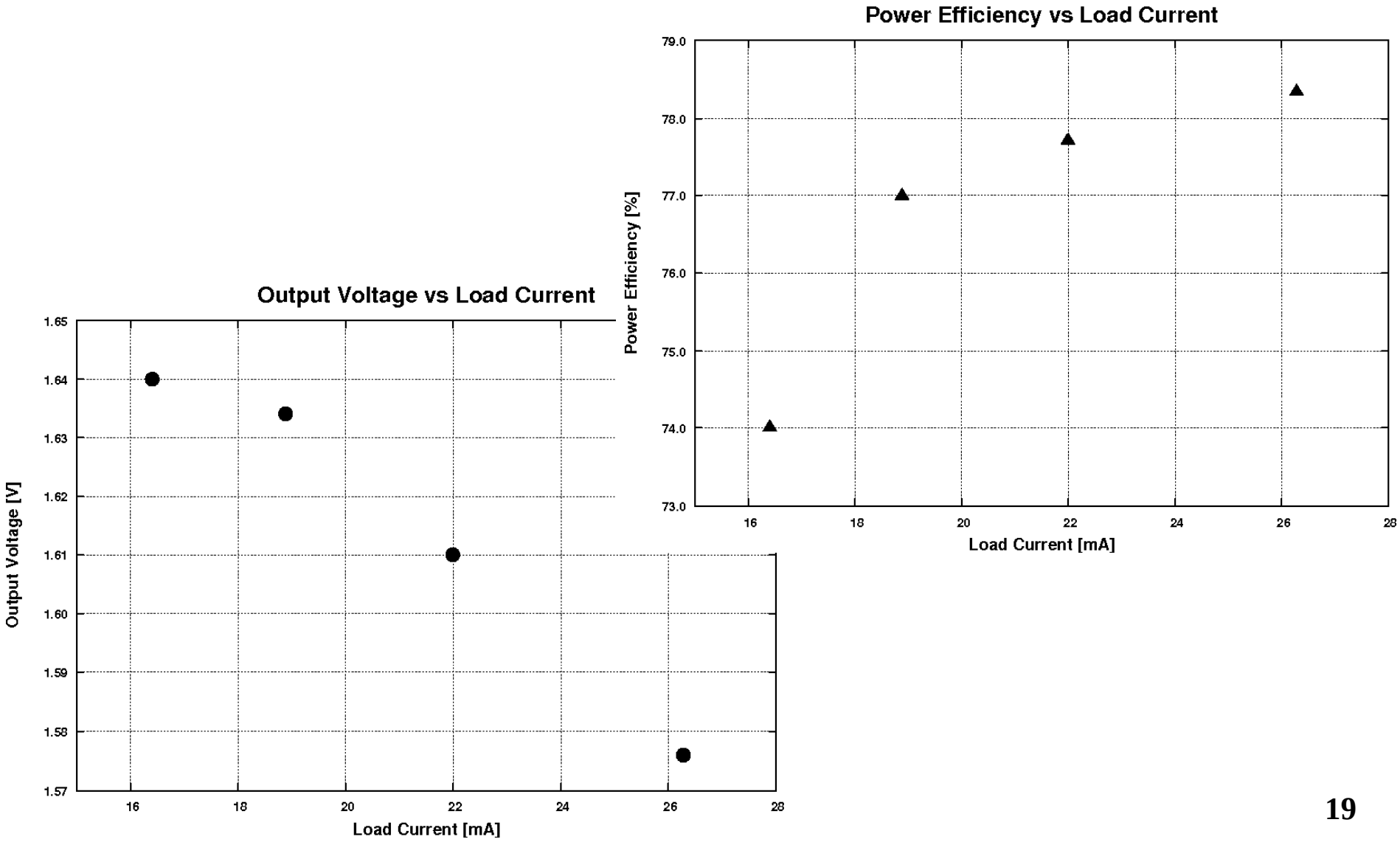


Possibly most efficient system compatible with serial powering

Charge pump – design study



Charge pump – performance (preliminary)



Power management in ABCN (130 nm) - to be done

Further optimisation of the charge pump – there is a number of details to be optimised in the design (switching transistors, buffers, level shifter ….

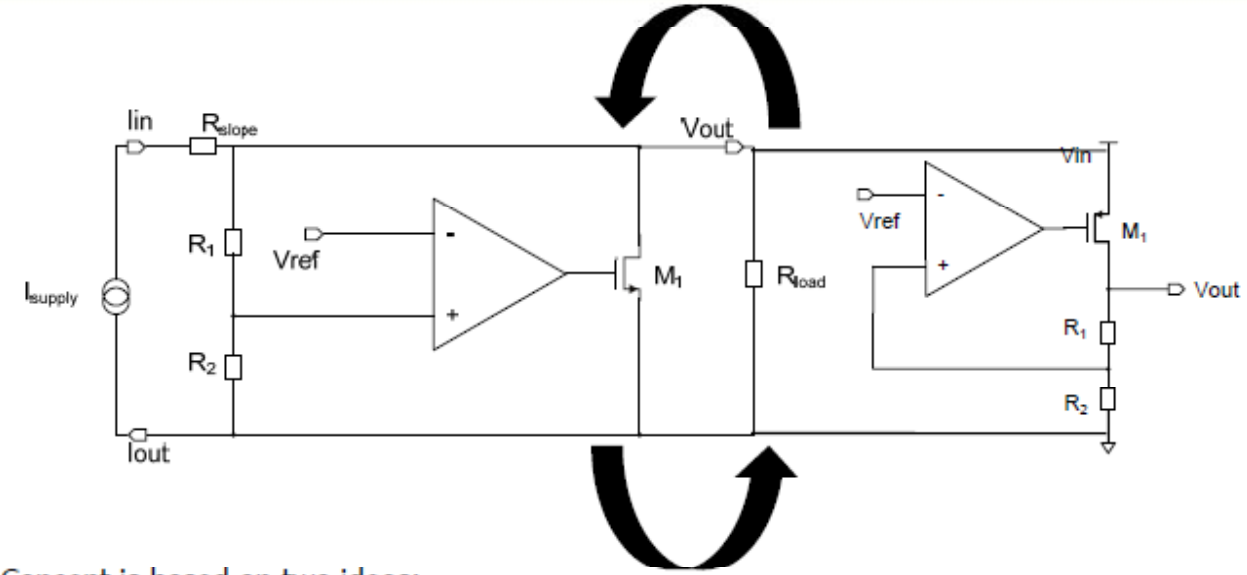
Implementation of the fully integrated shunt design from ABCN (250nm) in the 130 nm technology.

Implementation of the serial regulator in 130 nm.

Integration of a complete power management block to be included on the front-end prototype chip.

New shunt for pixel readout (ShuLDO)

New Shunt Concept Basic Ideas



New Concept is based on two ideas:

1.The added resistor Rslope does not contribute to the regulation and burns additional power
Why not replacing the added constant resistor by a regulated „resistor" of variable size

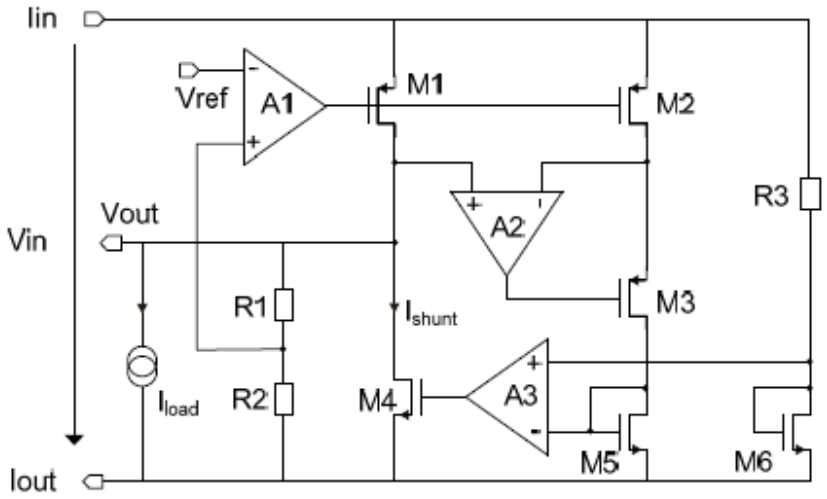
2.Very likely the shunt regulator will be used in combination with a linear regulator placed at the output of the shunt regulator
Why not changing the order and placing the LDO before the shunt regulator
The PMOS power transistor of the LDO becomes the variable regulated „resistor"
The shunt transistor becomes part of the load of the LDO

Slide 3

ShuLDO - implementation

LDO Regulator with Shunt Transistor (ShuLDO)

Simplified Schematic

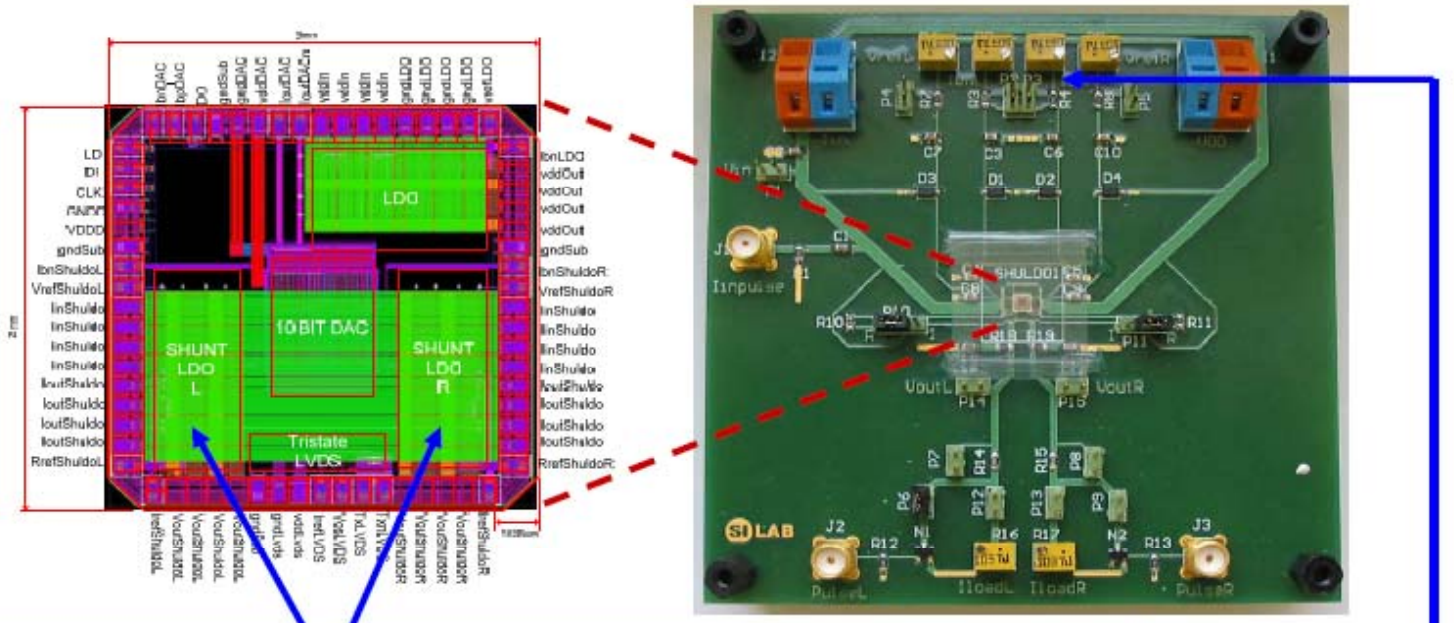


- Combination of LDO and shunt transistor
- M4 shunts the current not drawn by the load
- Fraction of M1 current is mirrored & drained into M5
- Amplifier A2 & M3 improve mirroring accuracy
- Ref. current defined by resistor R3 & drained into M6
- Comparison of M5 and ref. current leads to constant current flow in M1
- Ref. current depends on voltage drop V_{Iin} which again depends on supply current Iin

- „Shunt-LDO" regulators having completely different output voltages can be placed in parallel without any problem regarding mismatch & shunt current distribution
- Resistor R3 mismatch will lead to some variation of shunt current (10-20%)
- „Shunt-LDO" can cope with an increased supply current if one FE-I4 does not contribute to shunt current e.g. disconnected wirebond → ref current goes up
- Can be used as an ordinary LDO when shunt is disabled

ShuLDO - implementation

Setup for Test Measurements



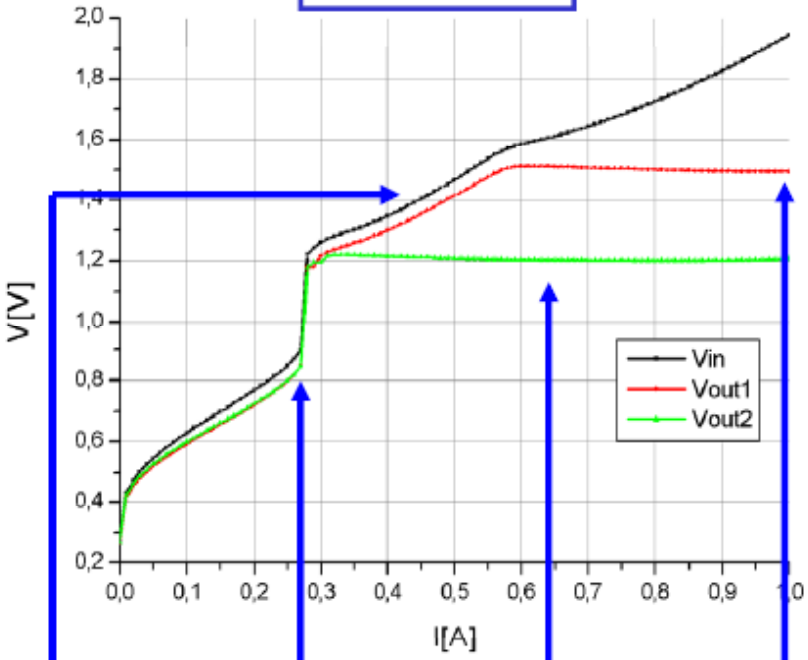
- Two Shunt – LDO regulators are connected in parallel on-chip
  → avoid influence of PCB parasitics
- biasing & reference voltage is provided externally
- input & load current is provided by programmable Keithley sourcemeter
- input & output voltages are measured automatically using a Labview based system

developed by D. Arutinov

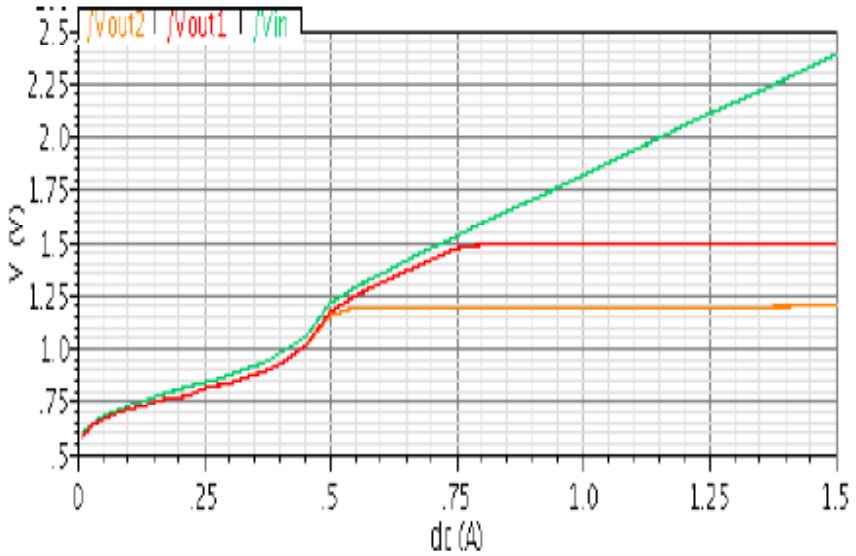
ShuLDO - test results

Two Shunt-LDO parallel connected on-chip

Measurement



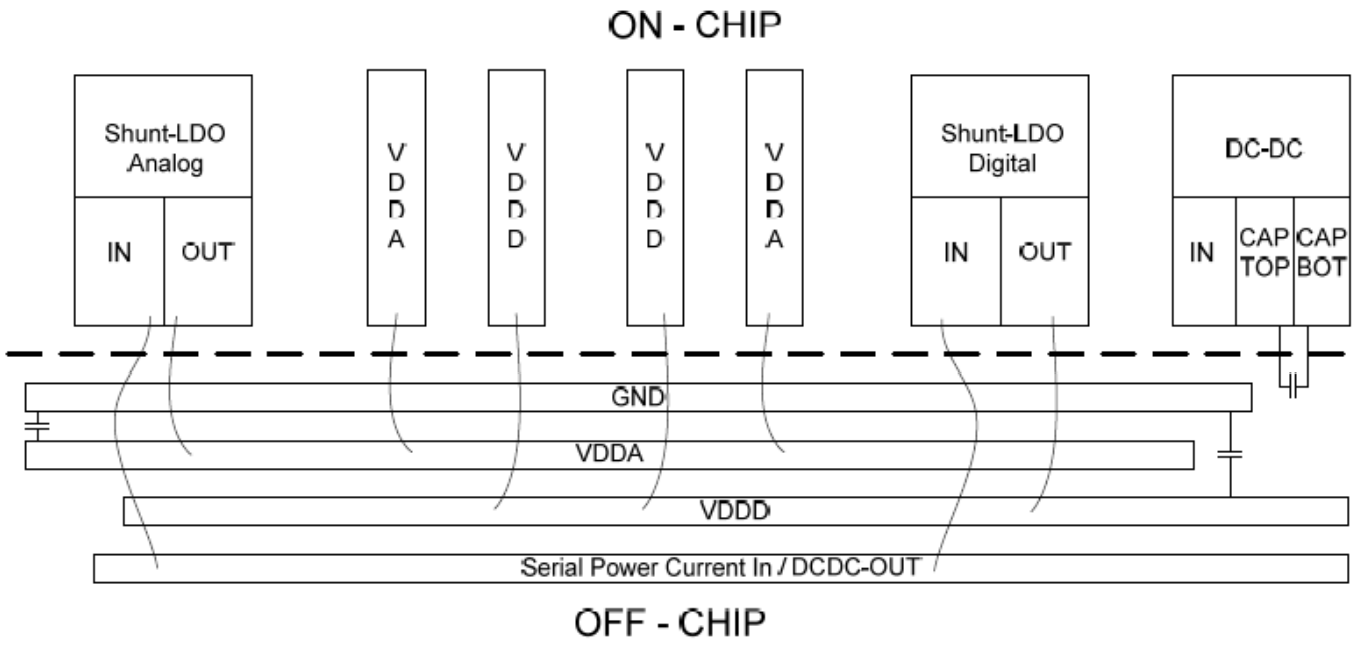
Simulation



- Saturation point is reached for smaller input currents and is more abrupt than in simulation
- Non constant slope of Vin
- Vout1 and Vout2 slightly decrease with rising input current
→ IR drop on ground rail leads to smaller effective reference voltage

Serial powering in pixel readout – development plan

Powering Scheme



flexible powering scheme → defined by bonding & external wiring

- Serial Powering: constant current fed into two ShuLDOs
- DCDC Powering: DCDC output voltage fed either directly or via LDO regulators to the core

02.03.2009

Summary

Much progress has been made on understanding and development of the serial powering for both, the strip readout and the pixel readout.

Fully integrated shunt regulator has been implemented in the ABC Next (250 nm) – it will allow building a large scale demonstrattor object with serial powering.

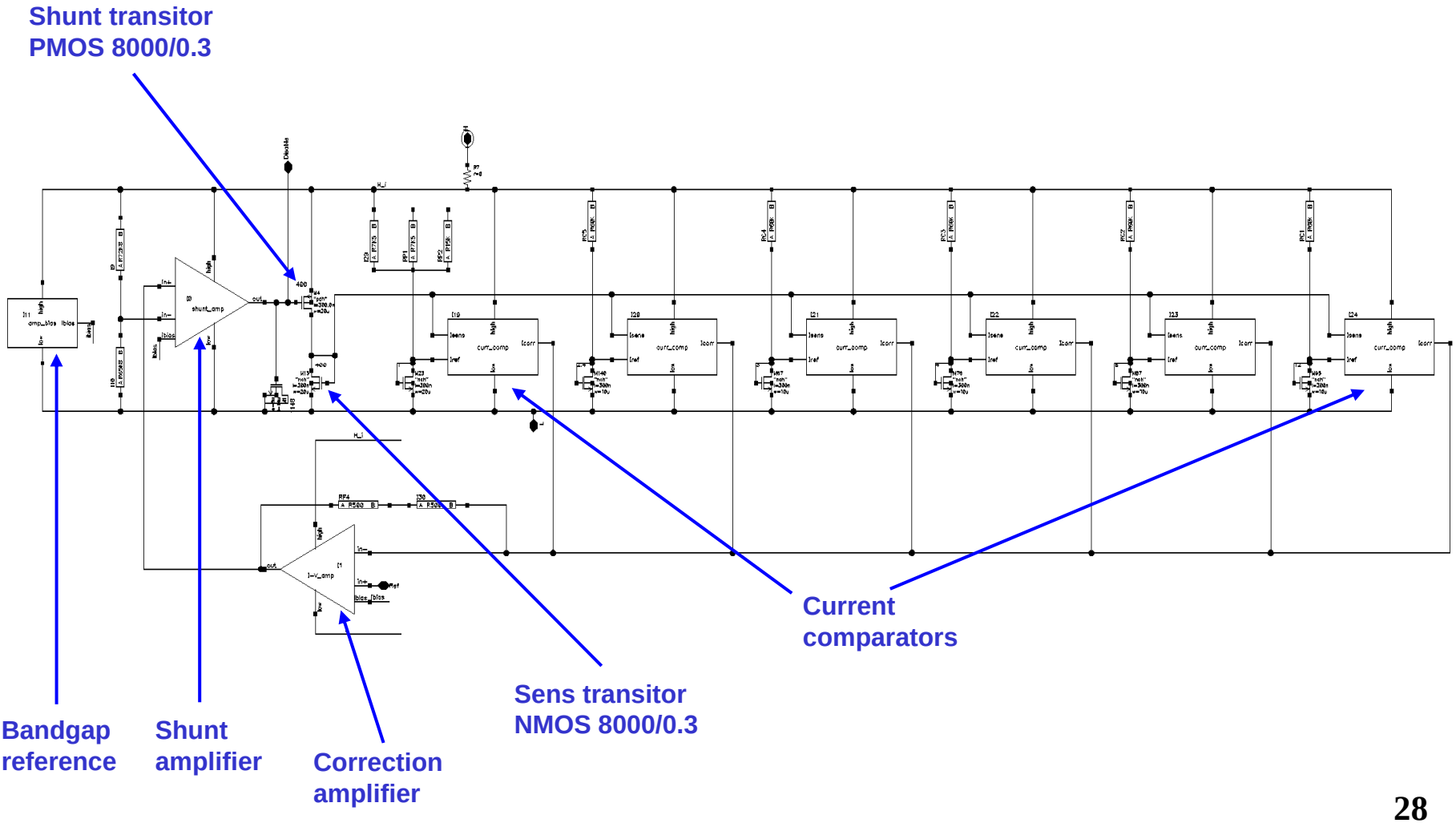
A new shunt regulator design has been proposed and prototype sucessfully for the pixel readout.

Optimising power efficiency may require combining serial powering with DC-DC on-chip conversion.

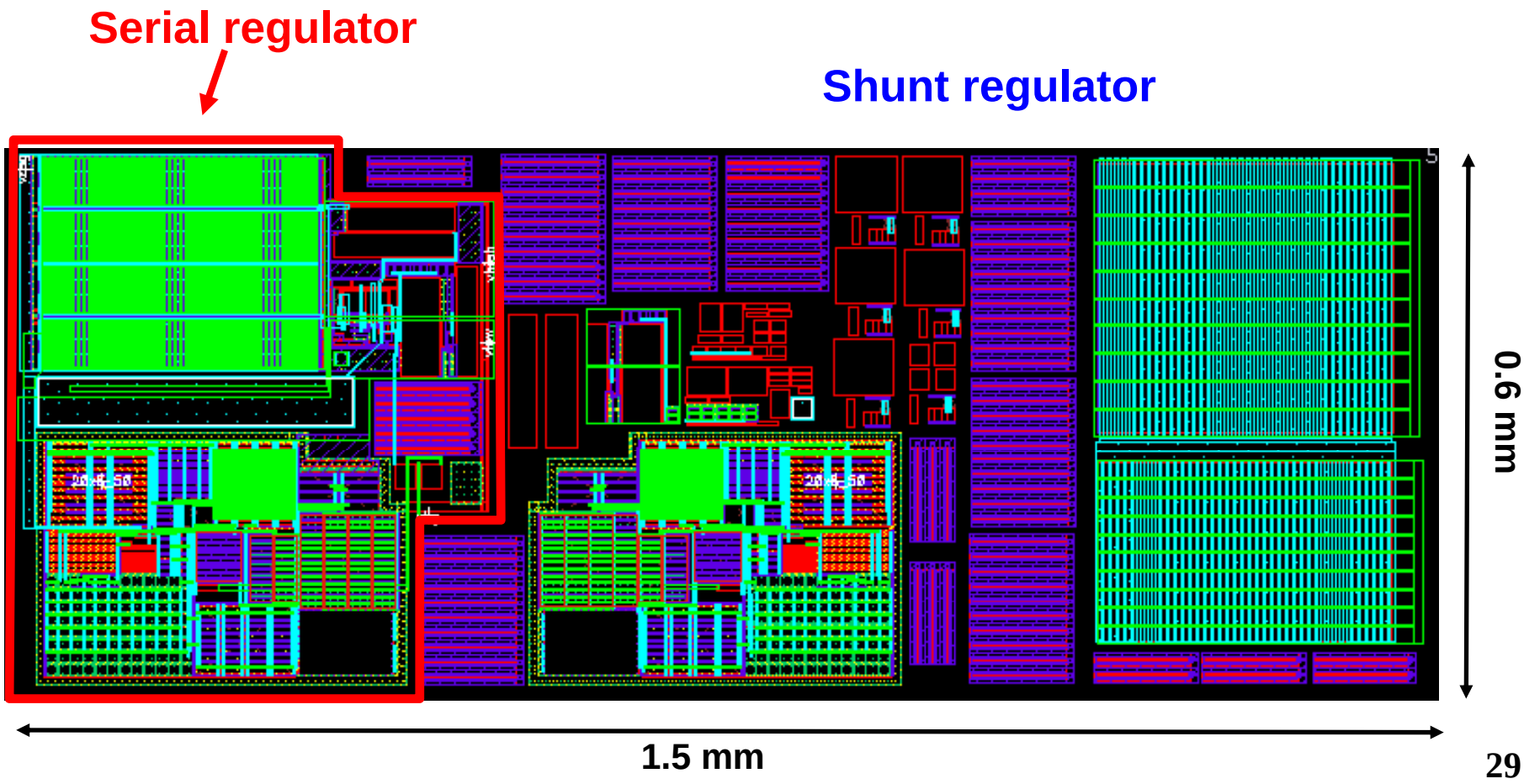
Implementation of serial powering must be readout architecture and technology specific.

Back-up slides

Implementation

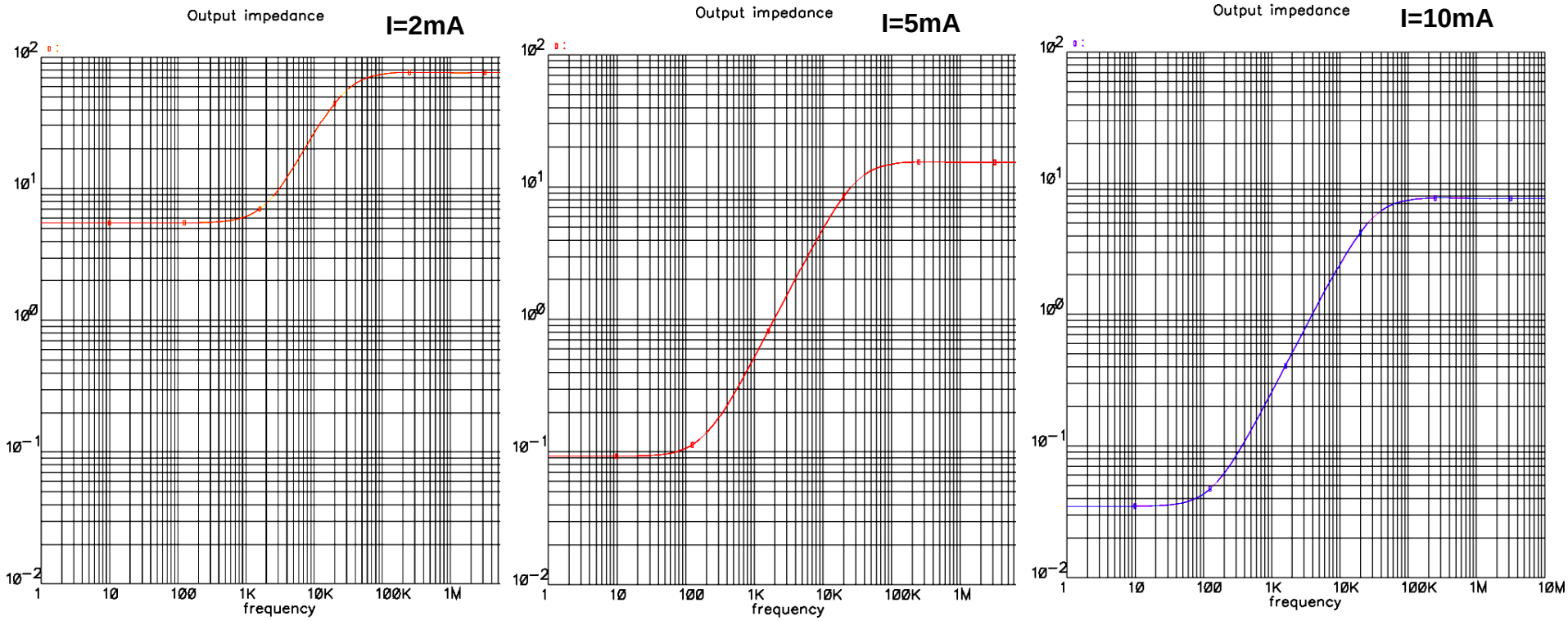


Implementation - layout



Ouput impedance - single shunt regulator

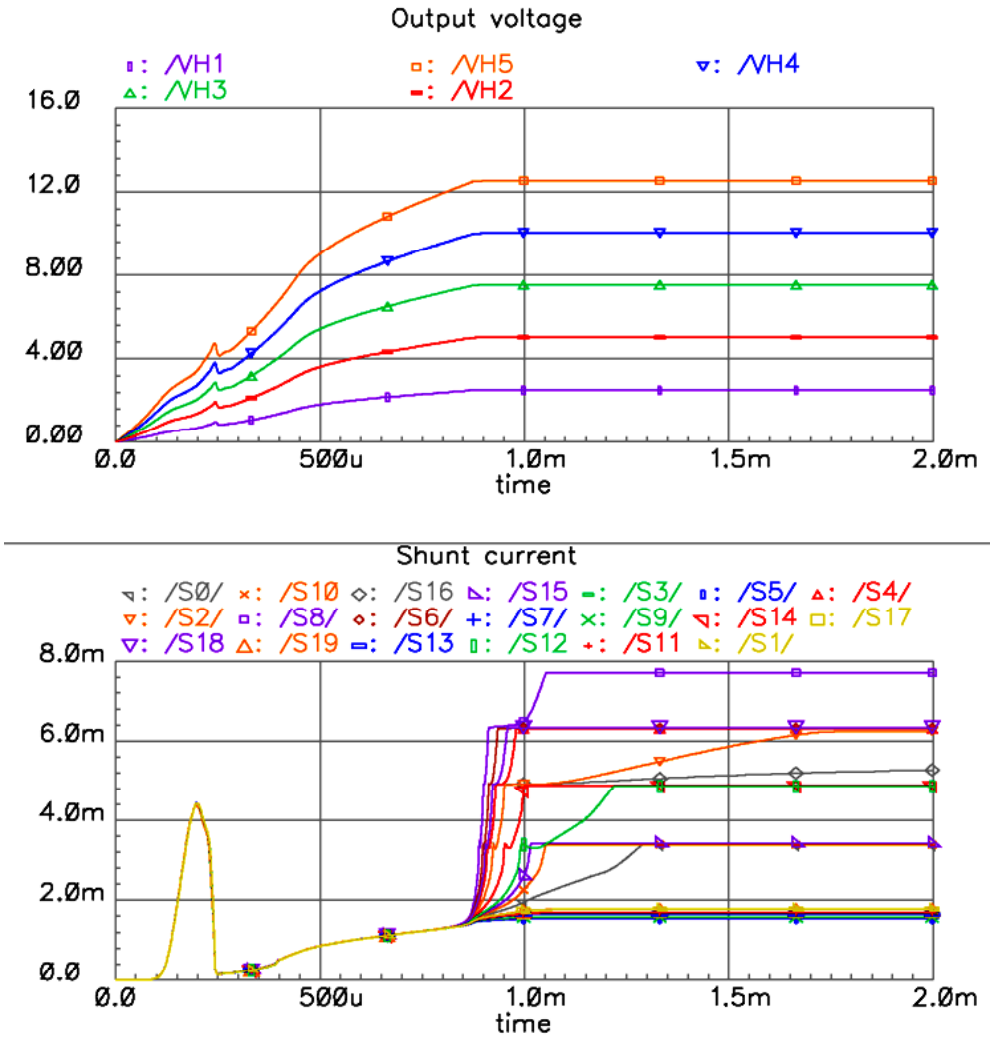
Shunt curent of 5 to 10 mA will be required



For a hybrid with 20 ABCNs the effective output impedance will be about 20 times smaller

Current setting and control

5 modules (20 ABCNs each) in series



How do we set and control the supply current?

The digital current may vary substantially with occupancy (noise scan) and process variation

An ”ideal” solution: the supply current of a super module is controlled based on the voltage sensing and voltage regulation at the super module input only, e.g. for 5 modules: 5×2.5V

Implications for the overll powering system needs to be understood better