Embedded switched capacitors DC-DC-Converter

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Motivation

4 Layer CMS Pixel Detector for Phase 1 Upgrade

- power loss in cabeling 60% because of higher current (P_{cable} goes with I^2)
- existing CAEN power supplies at the limit

Solution: Power Converter (lower I at higher V)

- DC-DC buck converter with **air coil** inductor (unusual)
- Charge Pump (switched capacitor converter): no inductor needed (only capacitors)

Configurations

- Charge Pump on ROC 24 mA (I_{ANALOG})

  on Module (TBM): 400 mA (16 ROCs)

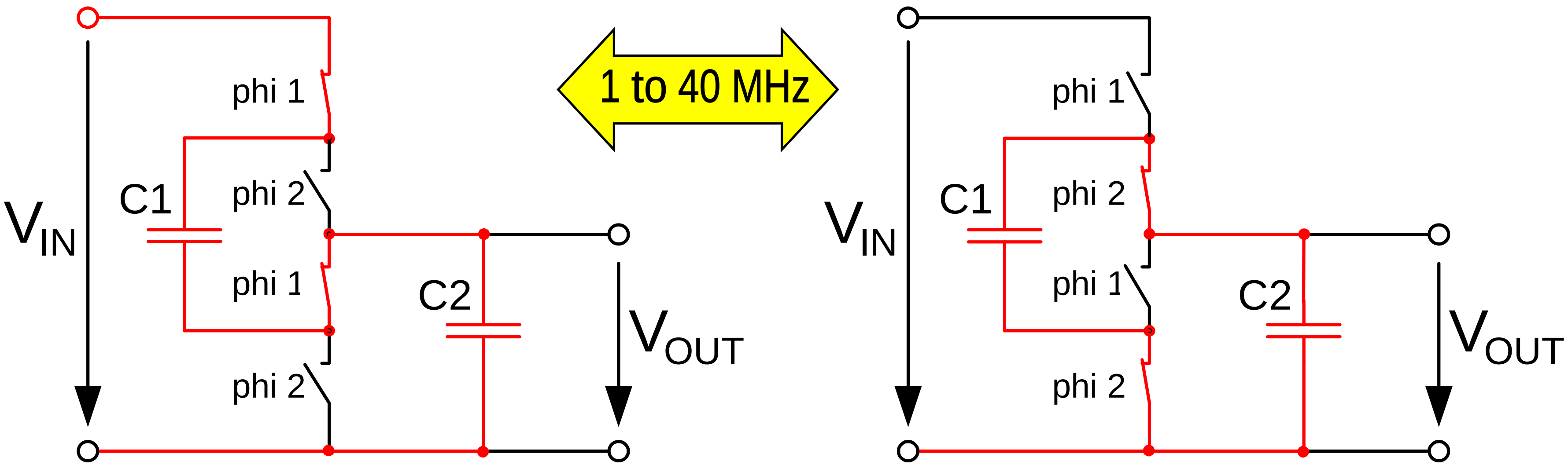
  on Supply Tube: 8A (20 Modules)

- DC-DC buck converter with air coil on **Supply Tube** (8A)

  not possible to place on the module in the tracker area (material budget)

Implementation (April 2008)

- Voltage divider by 2 (simple design)
- Implementation in 250nm CMOS radiation hardness design (same as Pixel ROC)
- Capable for powering of only one CMS Pixel ROC (24mA)
- to learn something about switched capacitor DC-DC converter (area on chip, …)
- switching frequency higher than sensitive frequency range of the ROC (> 10 MHz)



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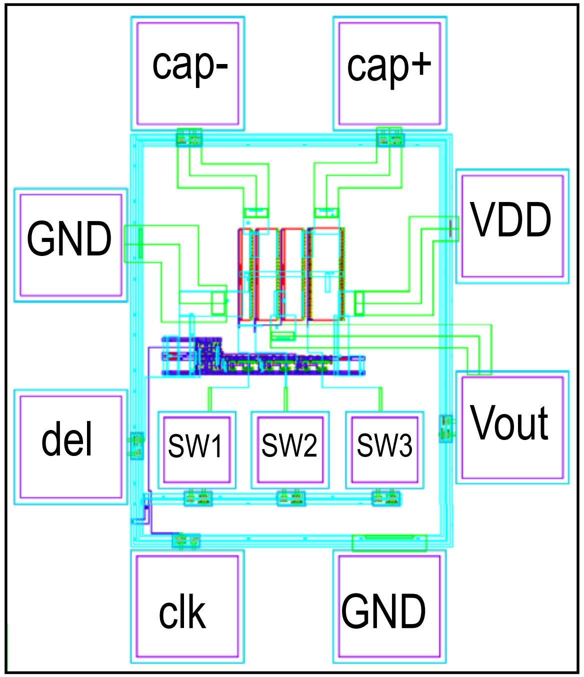
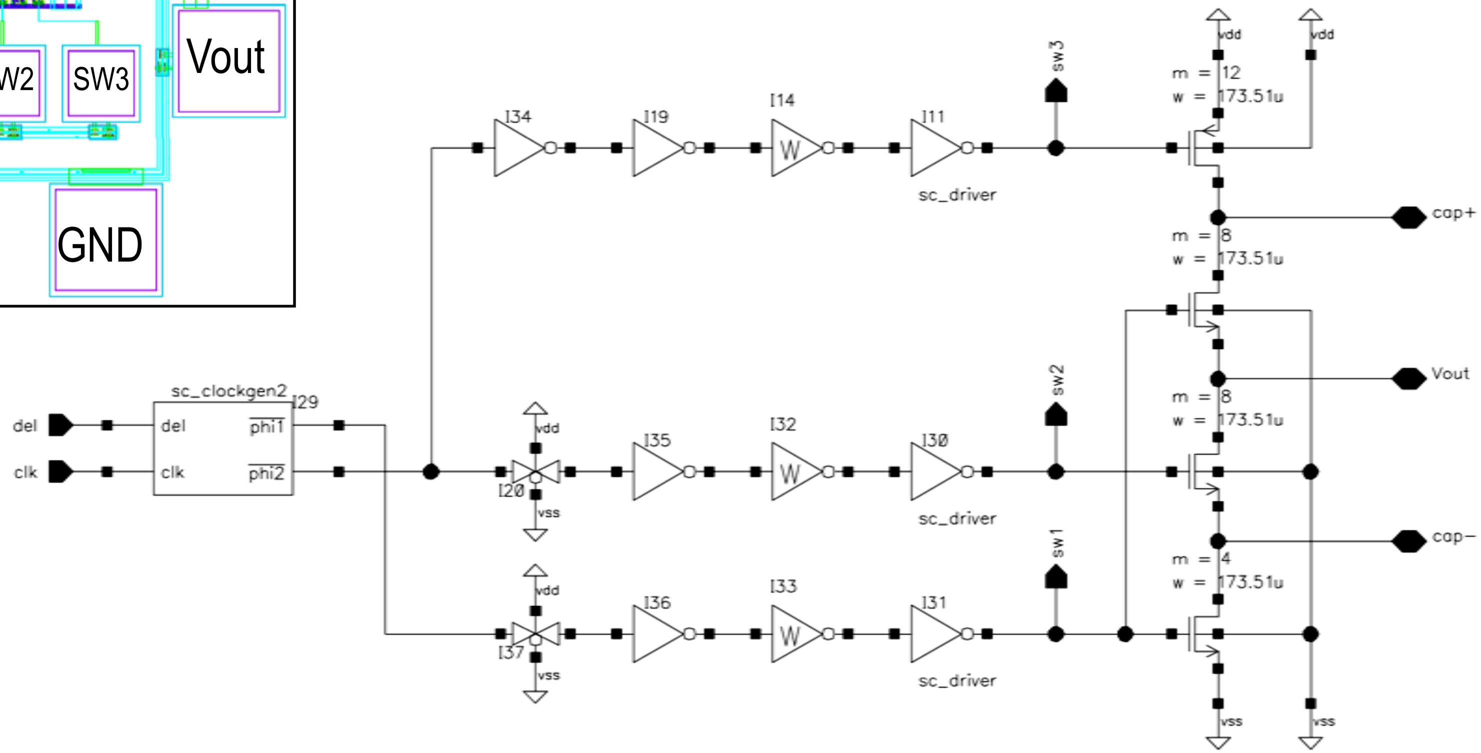
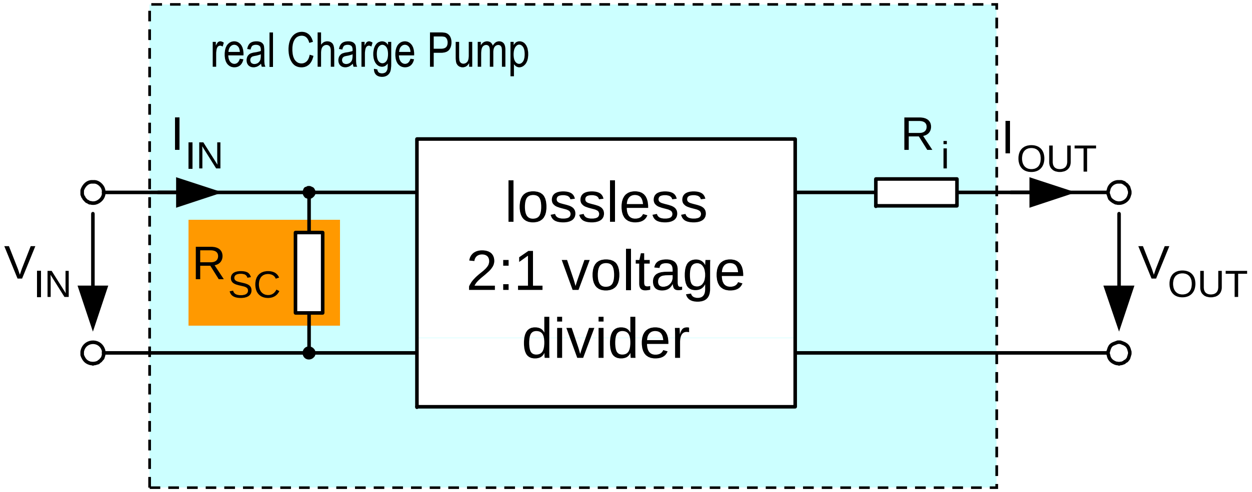
Schematic and Layout



- Size 560um x 650um, part of other test structures
- on chip: four switches, two phase generator, drivers
- external oscillator (fraction of 40 MHz LHC clock)
- external capacitors (10 … 100 nF)



Equivalent Circuit



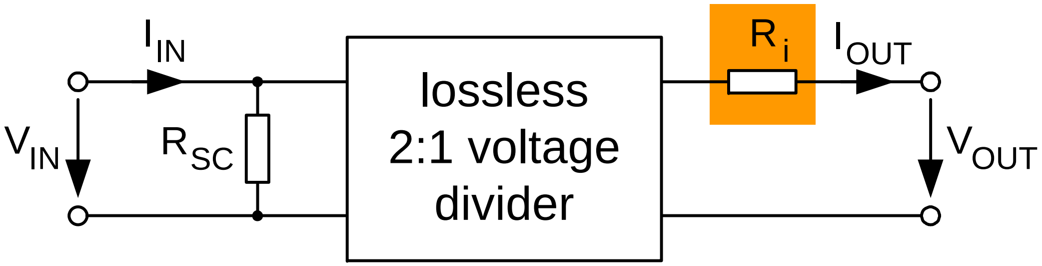
Ideal 2:1 converter ($V_{out}=V_{in}/2$, $I_{out}=2*I_{in}$) with shunt resistor and output resistor

Power Consumption (Gating Loss)

Power consumption: $$P_{SC} = \frac{V_{IN}^2}{R_{SC}} = f\,C_{SC}\,V_{IN}^2$$

(Shunt resistor)

Output Resistance



Source resistance: $$R_i = \frac{1}{4} \cdot \frac{1}{f\,C} \cdot \frac{\left[1 - \exp\left(-d_1 \frac{T}{\tau}\right)\right] \cdot \left[1 - \exp\left(-d_2 \frac{T}{\tau}\right)\right]}{1 - \exp\left(-(d_1 + d_2)\frac{T}{\tau}\right)}$$

configuration factor — SC-filter — incomplete charge transfer

$d_1\,T$ phase 1 switch duty cycle

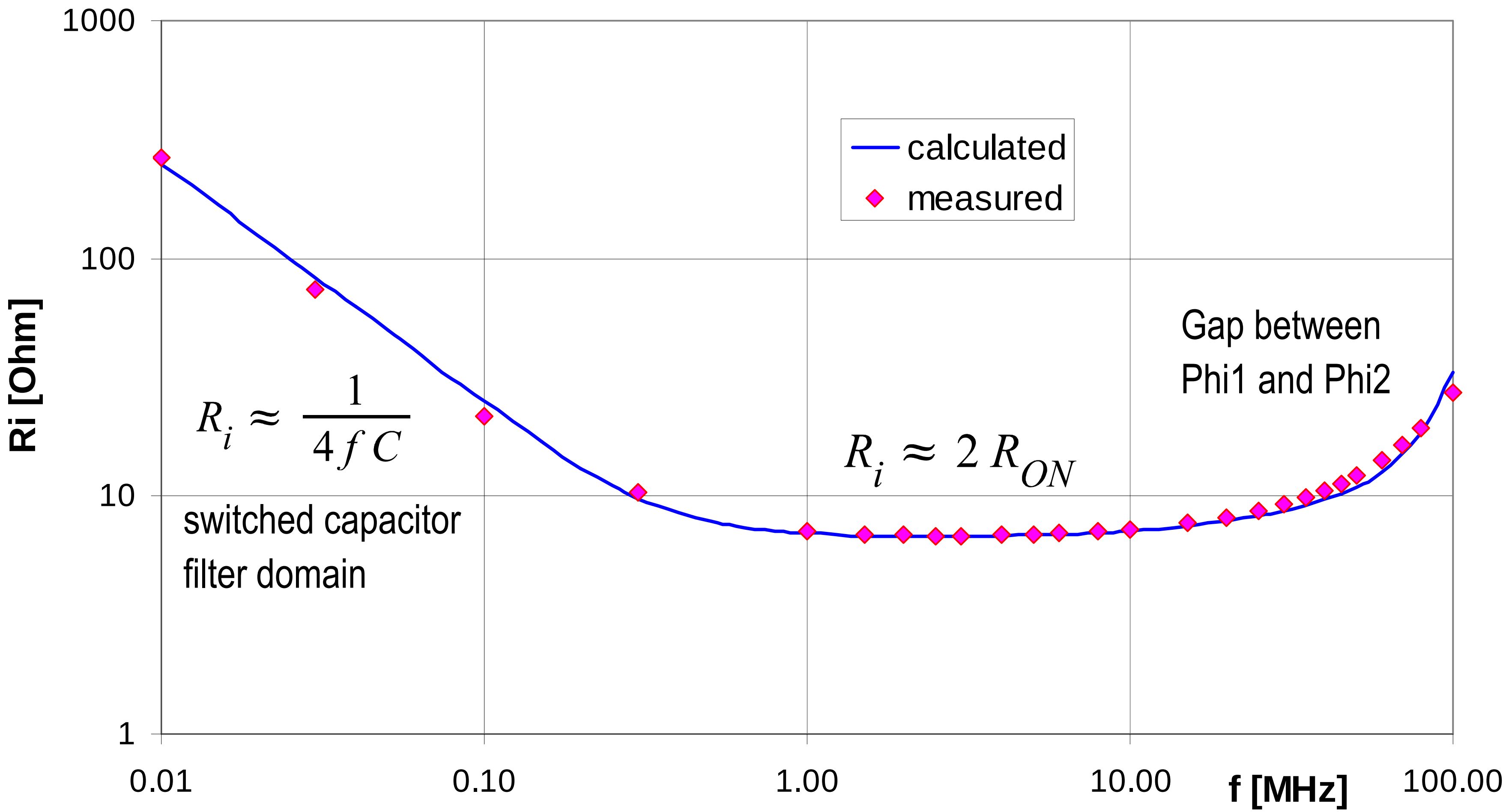
$d_2\,T$ phase 2 switch duty cycle

$$\tau = 2\,R_{ON}\;C$$

low frequency approximation (SC-filters): $R_i \approx \dfrac{1}{4\,f\,C}; \quad 2\,\tau << T$

high frequency approximation (charge pumps): $R_i \approx 2\,R_{ON}; \quad 2\,\tau >> T$

Output Resistance



Vin = 2.5V

C = 100 nF

Iout = 24 mA

Ron = 3.3 Ohm

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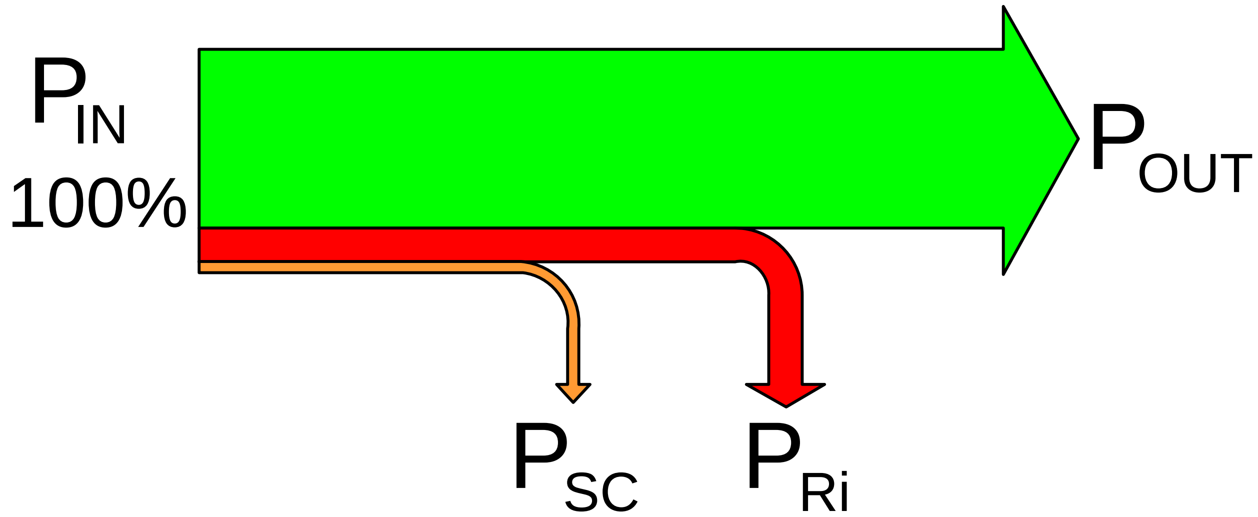
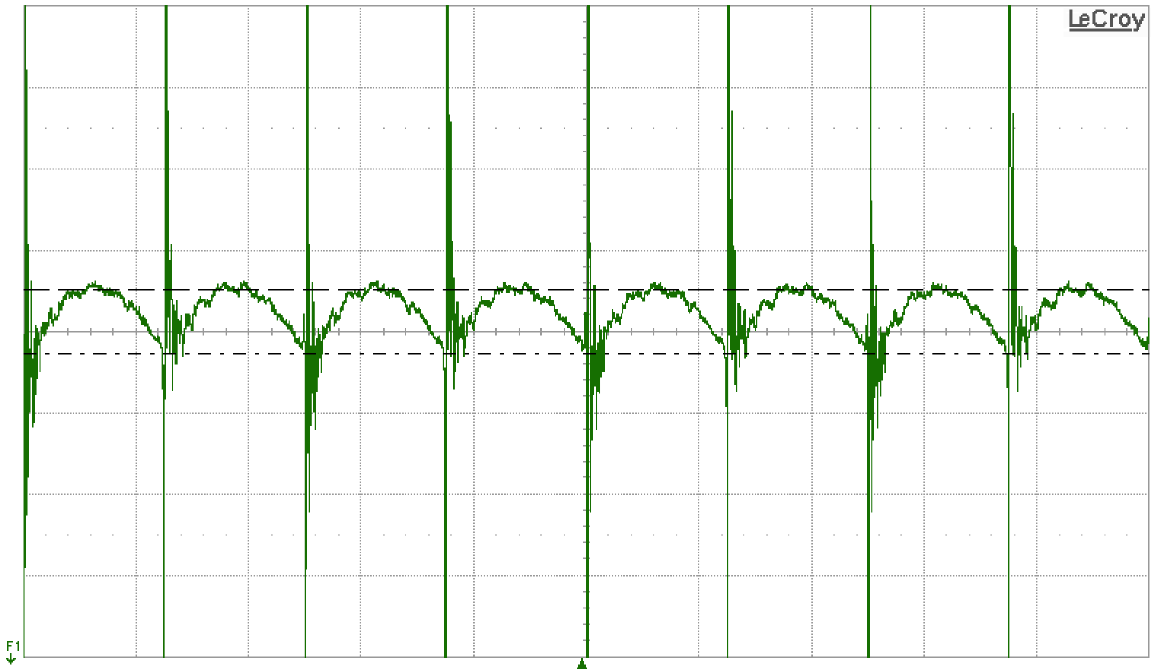
Power Budget (at 24 mA)



f [MHz]	P_SC	P_Ri	Pout
10	2 %	14 %	84 %
20	4 %	15 %	81 %
40	8 %	18 %	74 %

Ripple



Output Voltage

200 ns/div

5 mV/div

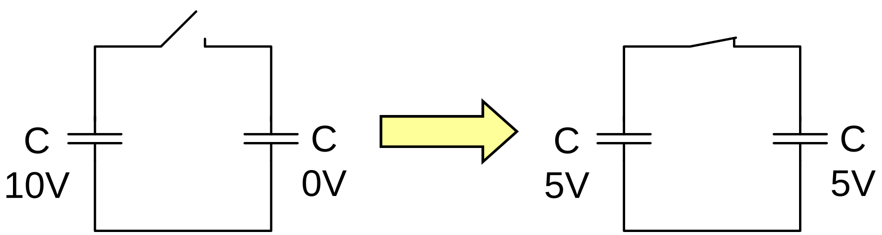
f = 4 MHz; C = 10 nF; Iout = 24 mA; Ripple: 4 mVpp (smaller at higher freq)

→ripple is not a problem

spikes ? frequency outside the sensitive frequency range

Conclusion

- over 80% efficiency at 20 MHz switching frequency
- better efficiency with lower Ron → bigger FETs
- area on chip: 10'000 μm^2 (100 μm x 100 μm)
- output voltage to small (Vout = 1.1V @ Vin=2.5V and Iout = 24 mA)
- not adjustable, no voltage regulation (additional linear regulator needed)
- No power reduction in BPIX but less cable loss



- charge conservation
- no electrical energy conservation, 50% loss

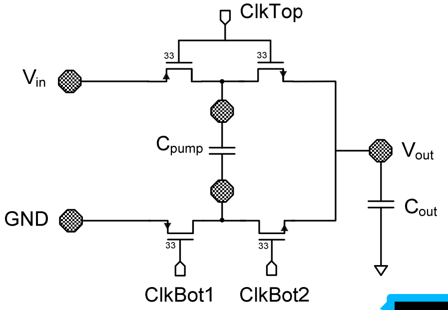
in general:
energy efficiency $u \rightarrow u + \Delta u$

$$\eta < \frac{u + \frac{\Delta u}{2}}{u + \Delta u} \approx 1 - \frac{1}{2} \cdot \frac{\Delta u}{u}$$

(for small Δu)

DC-DC Charge Pump for ATLAS FE-I4

Maurice Garcia-Sciveres and Dario Gnani (designer) Lawrence Berkeley National Lab



- Prototype in June 2008 in FE-I4 Chip
- 0.6A at 1.5V
- lower voltage compared with CMS pixel ROC (2.5V dig)
- no increased noise