

# The SPI (Serial Powering Interface) chip

- first results -

**M.Trimpl, Fermilab**

- SP Schemes / SPI Motivation
- Chip Architecture and Features
- SPi 001 Test Results (Shunt, ADC, current alarm, power down)
- Summary and Outlook

on behalf of:

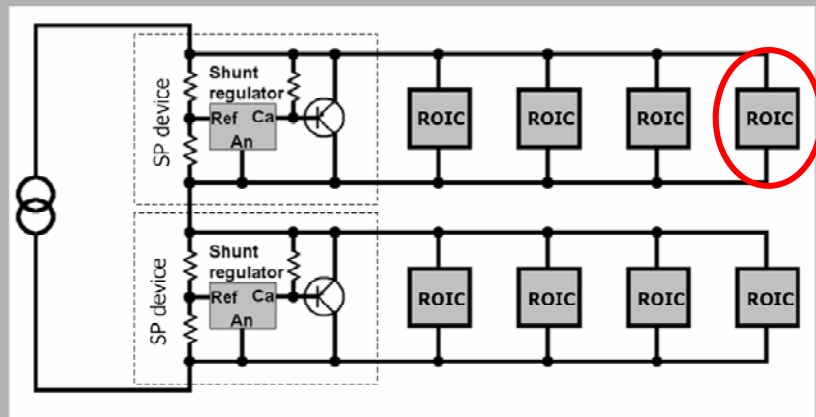
A.Dyer, G.Deptuch, C.Gingu, J.Hoff, R.Lipton, A.Shenai, M.Trimpl, R.Yarema, T.Zimmerman – FNAL

R. Holt, G.Villani, M.Weber - RAL

N.Dressnandt , M.Newcomer - UPenn

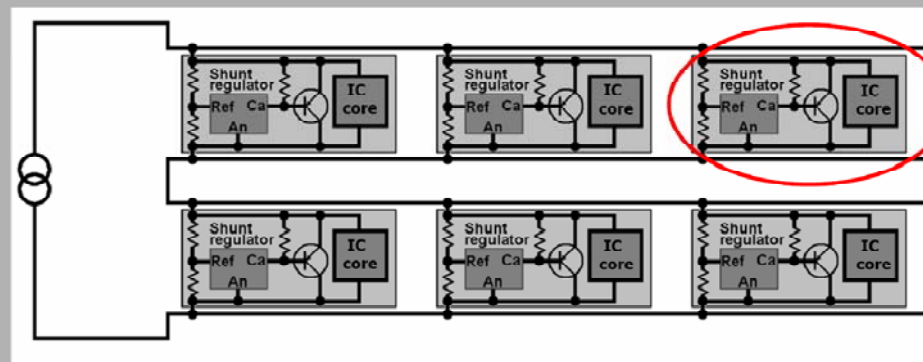
# Serial Powering Schemes

## 1) External shunt regulator + transistor



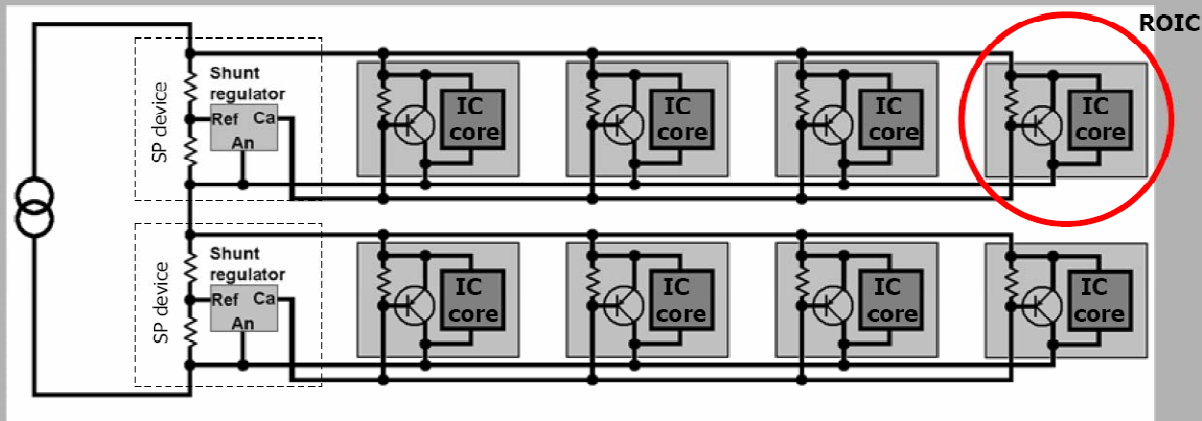
Good approach, but implies a **high current shunt**  
 -> limited experience in HEP-IC community  
 SP device enables to operate non SP-ROIC in SP mode

## 2) Internal shunt regulator + transistor in each ROIC



Disadvantage: many power supplies in parallel  
**Matching issue** can cause hot spots and potentially kill chips

## 3) External SR + parallel shunt transistor in ROIC

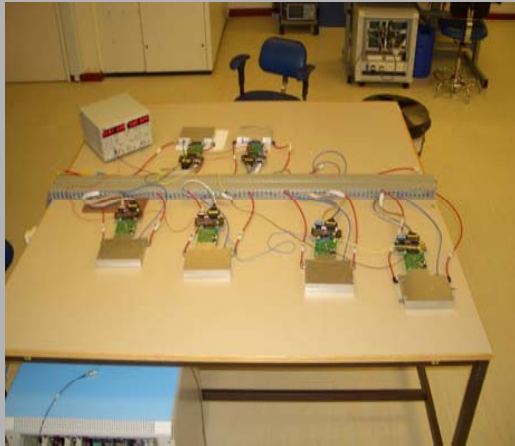


**feedback** however **more challenging** and depends on implementation

- choice of architecture **not obvious**, detailed studies anticipated by RAL/LBNL (M.Weber, C.Haber)
- scheme (2) can be realized by any ROIC standalone
- **SPI chip covers scheme (1) and (3)**

# Present setups and SPI Motivation

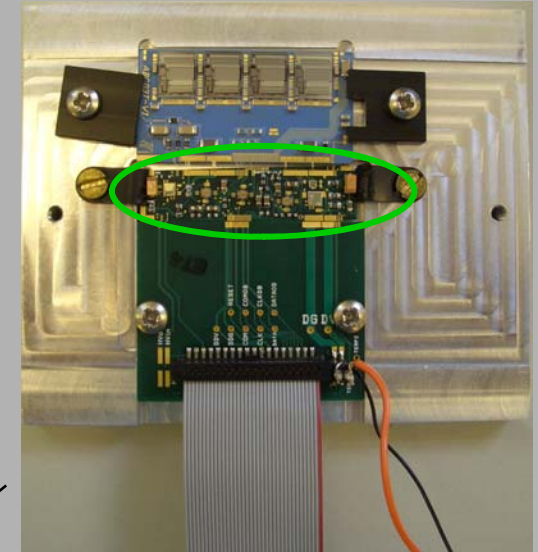
Setups using discrete components explored SP feasibility and new features ( current monitoring and overcurrent protection )



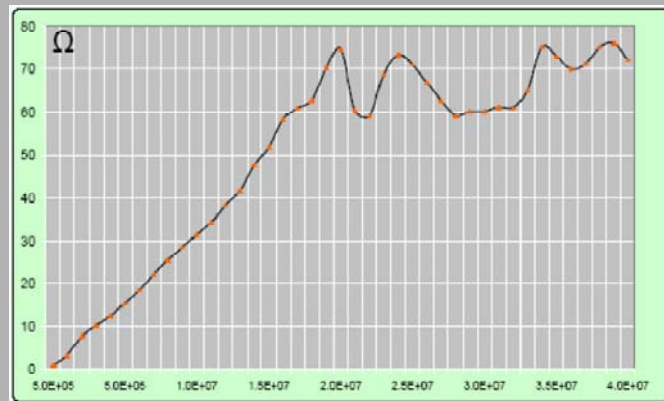
## Downsides of discrete setups

- Standard Shunts typ. current limited (less 4A)
- Power transistors not rad. tolerant
- esp. 4A for module is challenging
- **spacious** setup
- **limited performance** (e.g. dyn. impedance)

-> **integrated / customized solution**

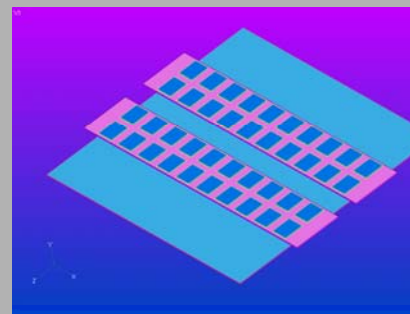


ATLAS SCT setup at RAL (similar setup at LBNL, Atlas pixel setup at Bonn U.)



**~1Ω at 1MHz, >50Ω for >10MHz**

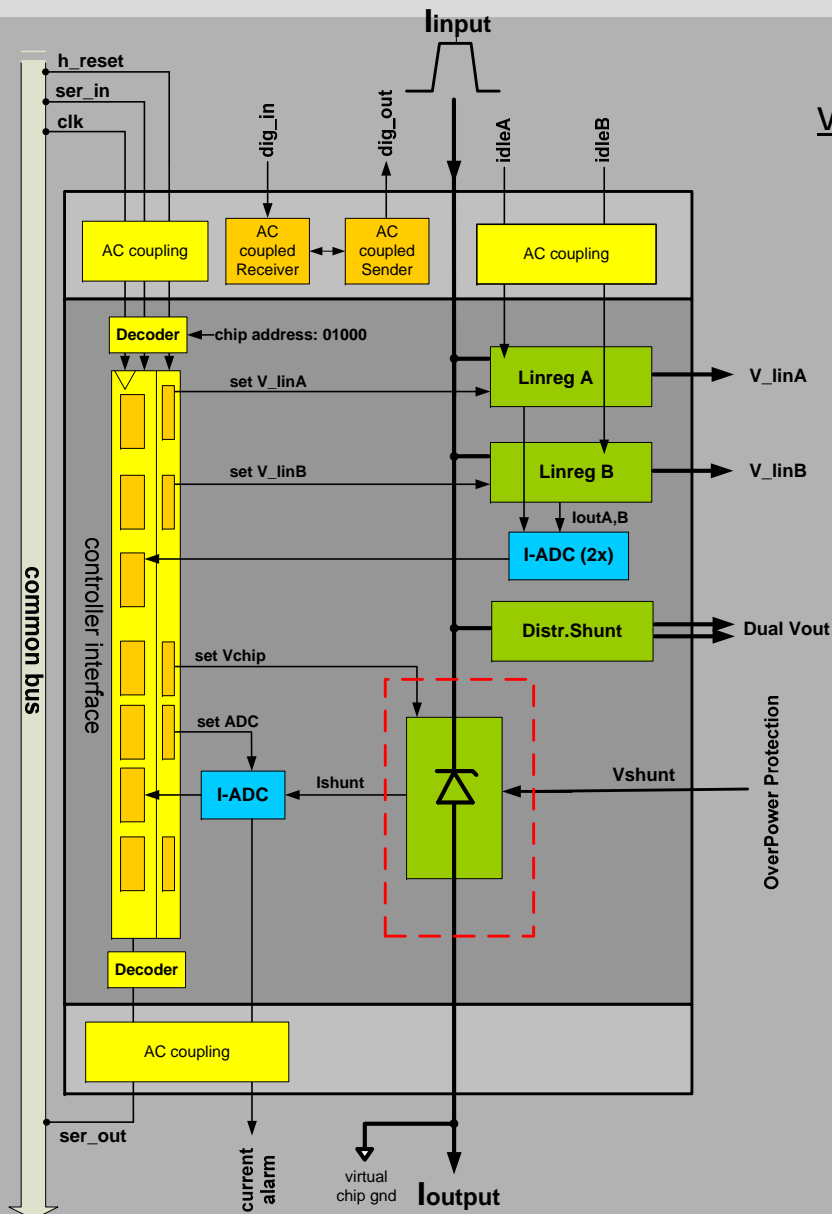
abc-n module approach:



[C.Haber, LBNL]

2x10 ROIC on a module  
20 modules in a row  
(clearly needs integrated solution)

# SPI - Architecture Overview



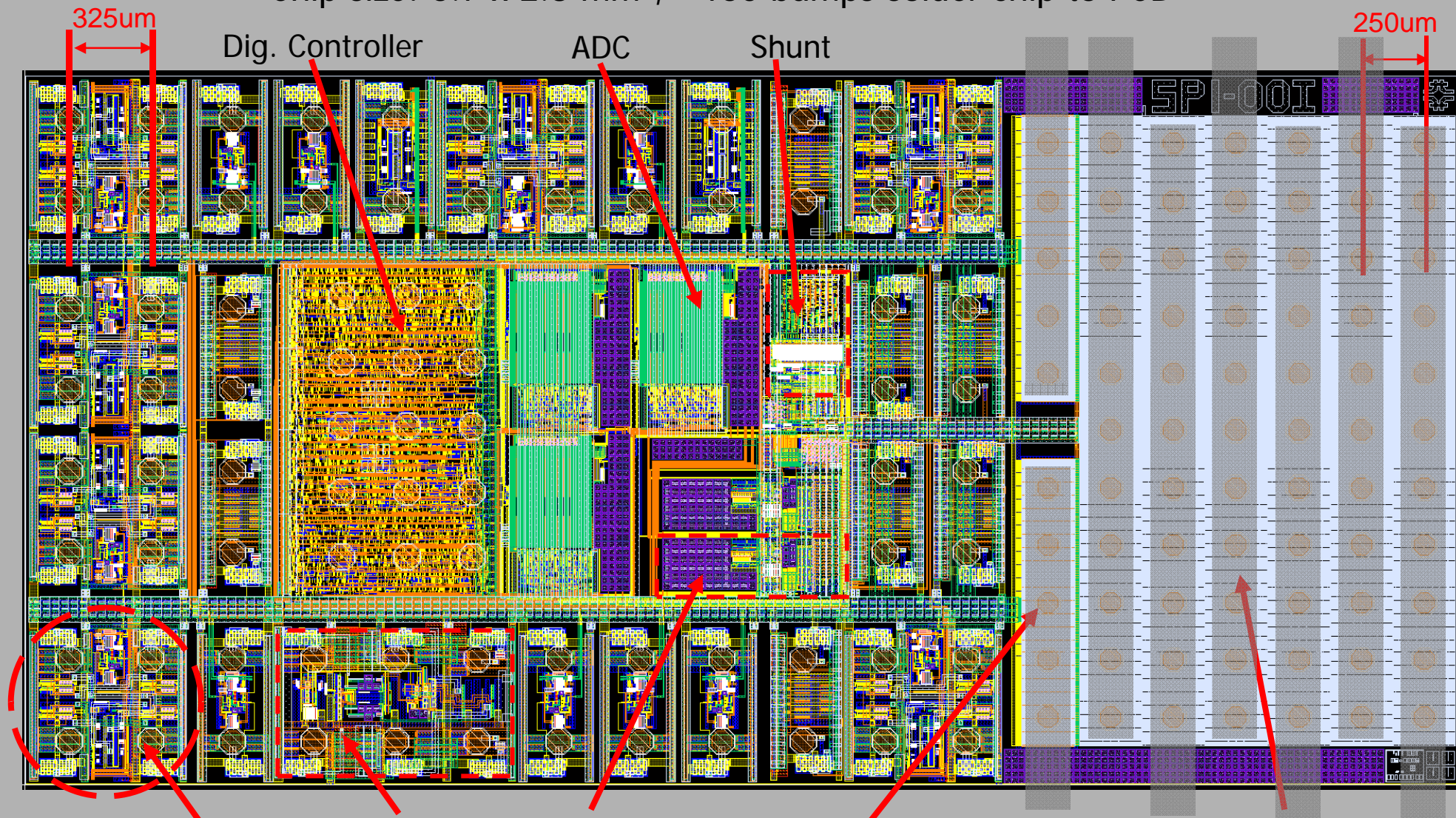
versatile SP chip - list of basic features:

- **shunt** creates Vchip (scheme1) , distr. shunt (scheme3)
- communication via **multi drop** bus (each SPI chip has 5bit address) reduces number of str.-lines for SPI to minimum of 2 (3)
- spare AC coupled interfaces (**comports**)
- **ADCs** to monitor shunt and LR current
- **2x LinReg**: separate analog / digital supply to hook up some chips (1-3) for tests  
Not proposed as a scaleable solution for a whole module (linregs should be part of ROIC, as e.g. in the ABCn)
- **OverPower** protection (avoids detector hot spots) (chip feature, needs external control)
- **radtol. design** techniques, TSMC 025MM process



# Layout / Floorplan

Chip size: 5.7 x 2.8 mm<sup>2</sup>, ~150 bumps solder chip to PCB



one (of 7) comports

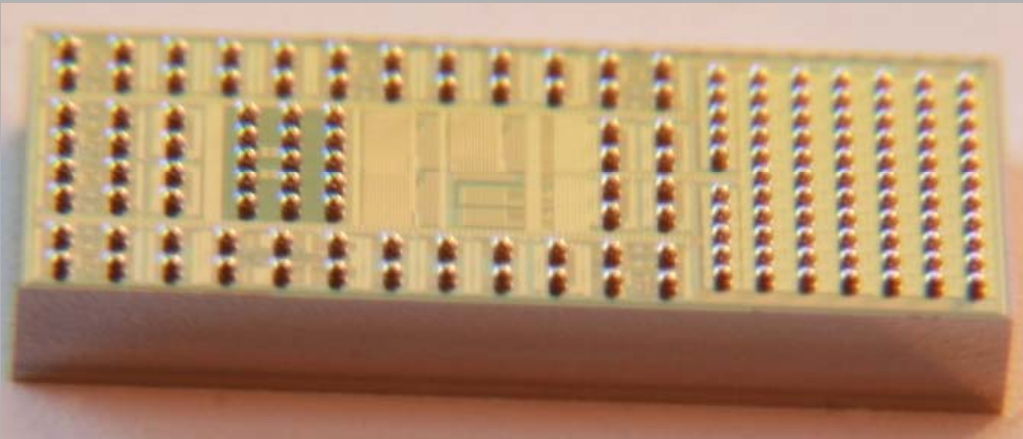
Distr.Shunt

Lin.Reg

Linreg Vout (2x)

Fanout (finger) for shuntmos

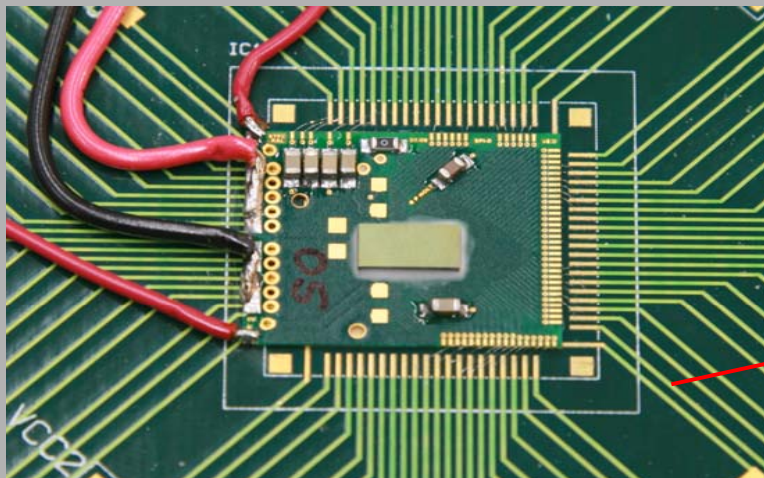
# test setup / assembly



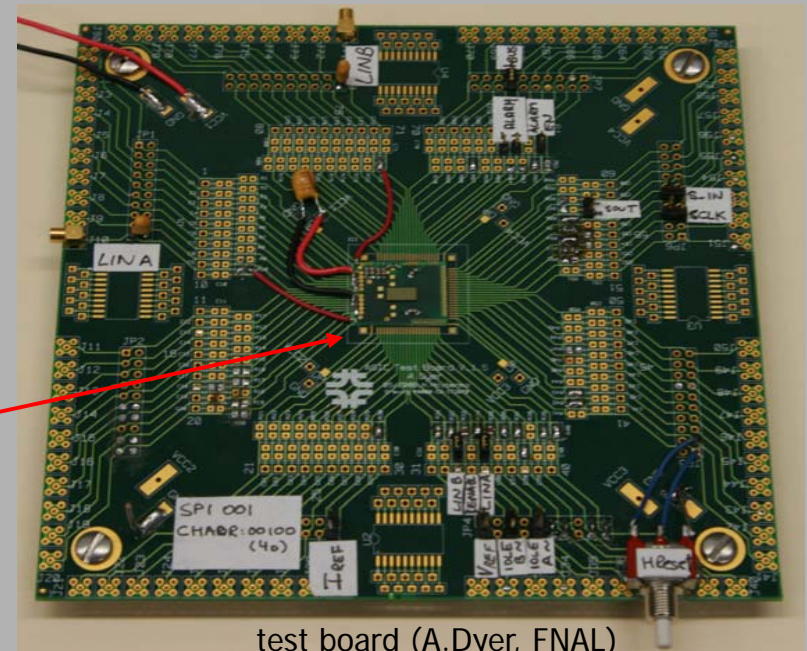
SPI001 (back since Nov2008), solder bumps placed by TSMC

## Advantages of bumps bonds (for the SPI chip)

- **better routing flexibility** (high currents)
- more robust and shorter (100um vs 5mm) as wire bonds
- **reliable connection is essential in SP scheme**
- better scale ability (if higher currents are needed)
- chip backside fully accessible for cooling / temp.monitor



- daughter board (R.Holt, RAL)
- FCOB assembly done at SiDet (E.Skup, FNAL)



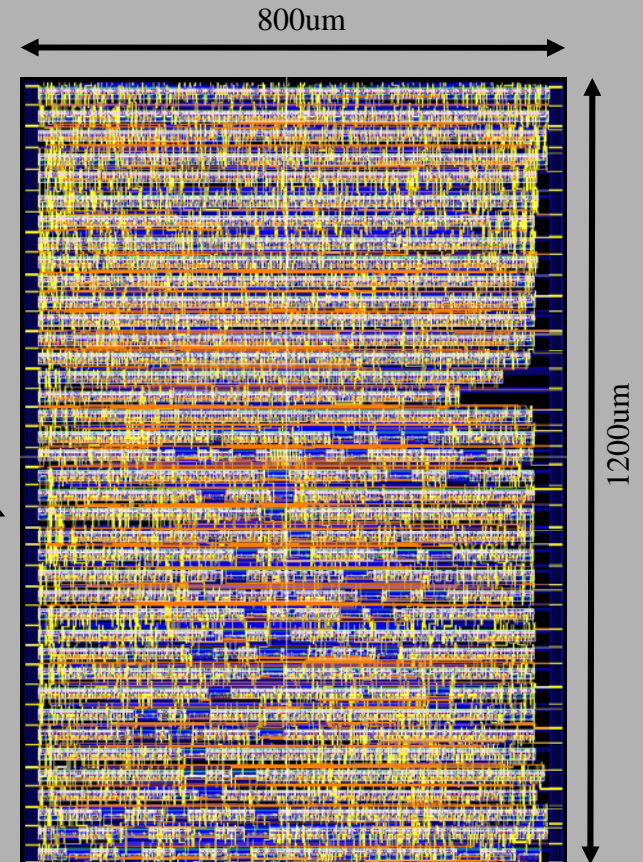
test board (A.Dyer, FNAL)

# interface controller

```

Verilog description
then auto place and route
using CERN raddtol lib.
    
```

Verilog description  
then auto place and route  
using CERN raddtol lib.



**32 bit command word** (7bit header, 4 bit trailer)  
(internal state machine)

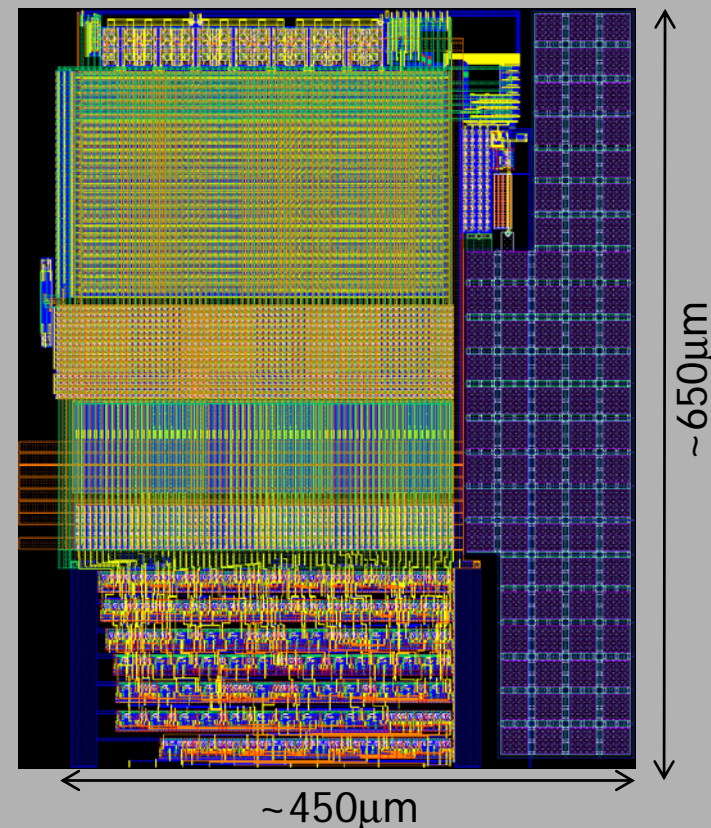
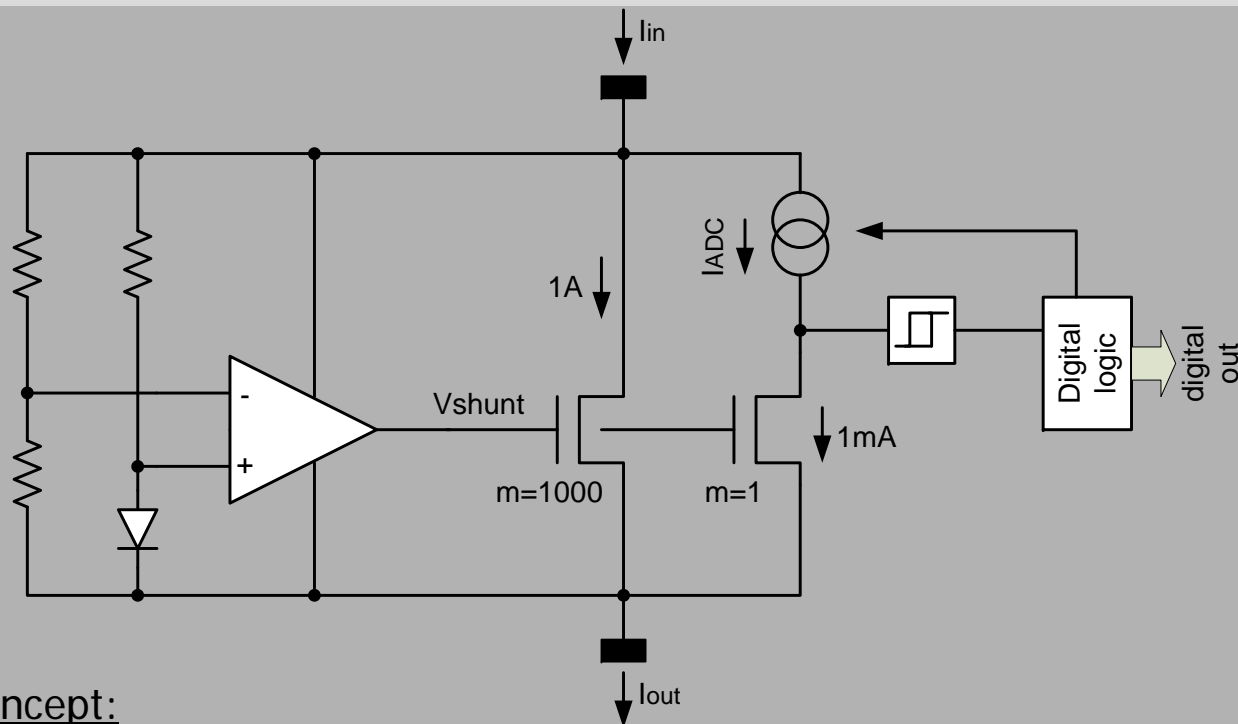
[1100111 CCCCC RRRRR III DDDDDDDD 0000]

- C: 5bit Chip Adr. (30 chips on module)
- R: Register Adr. (20 config + 3 ADC data-register)
- D: 8bit register word
- III: Instruction Code
  - Reset Register
  - Set Register
  - Default (hard coded)
  - Read ADC / Write Register

Chip and Register wildcard 10101 (21d)  
-> configure register in all chips in a setup  
-> reset all registers in all chips to default



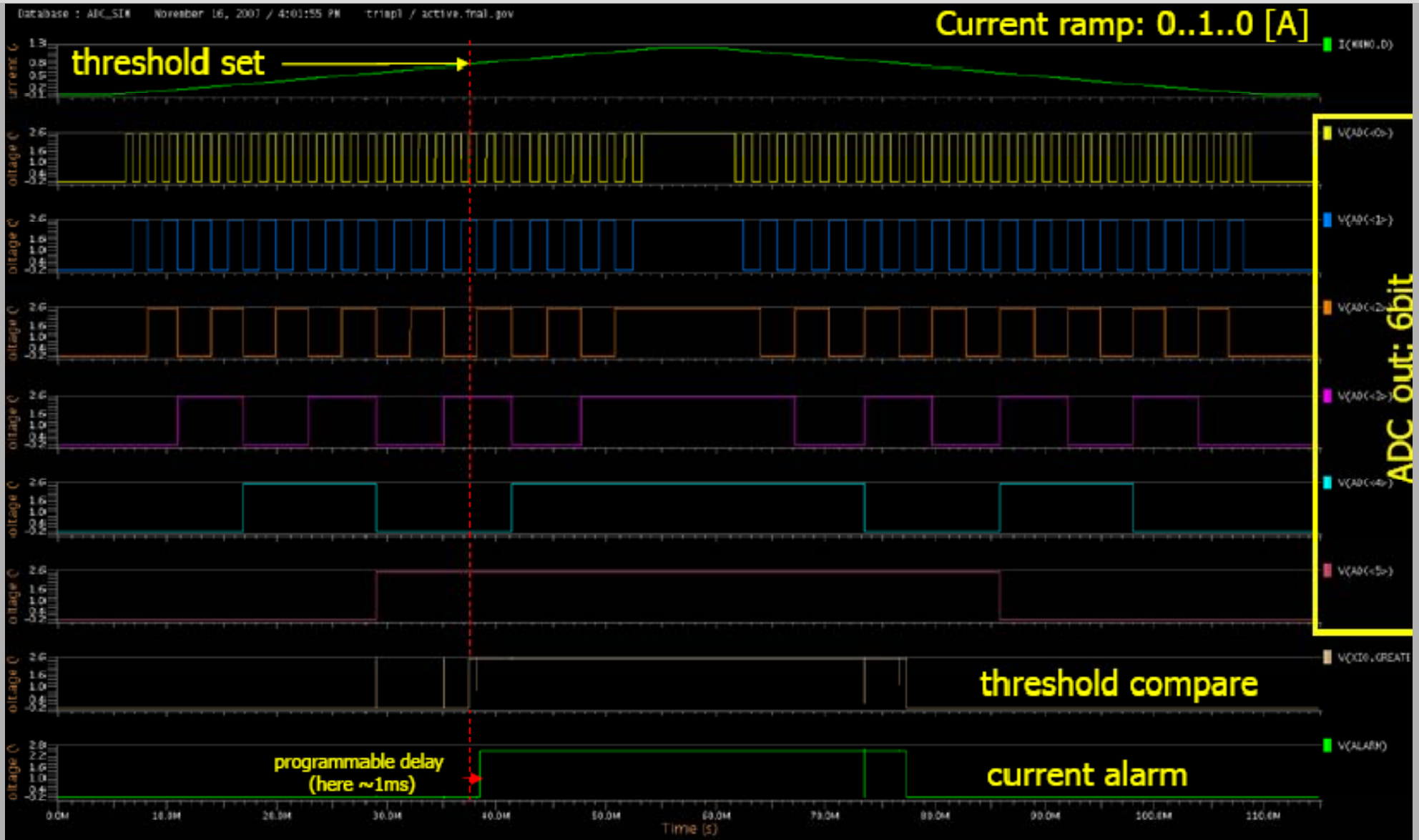
# 'shunt' ADC - principle and implementation



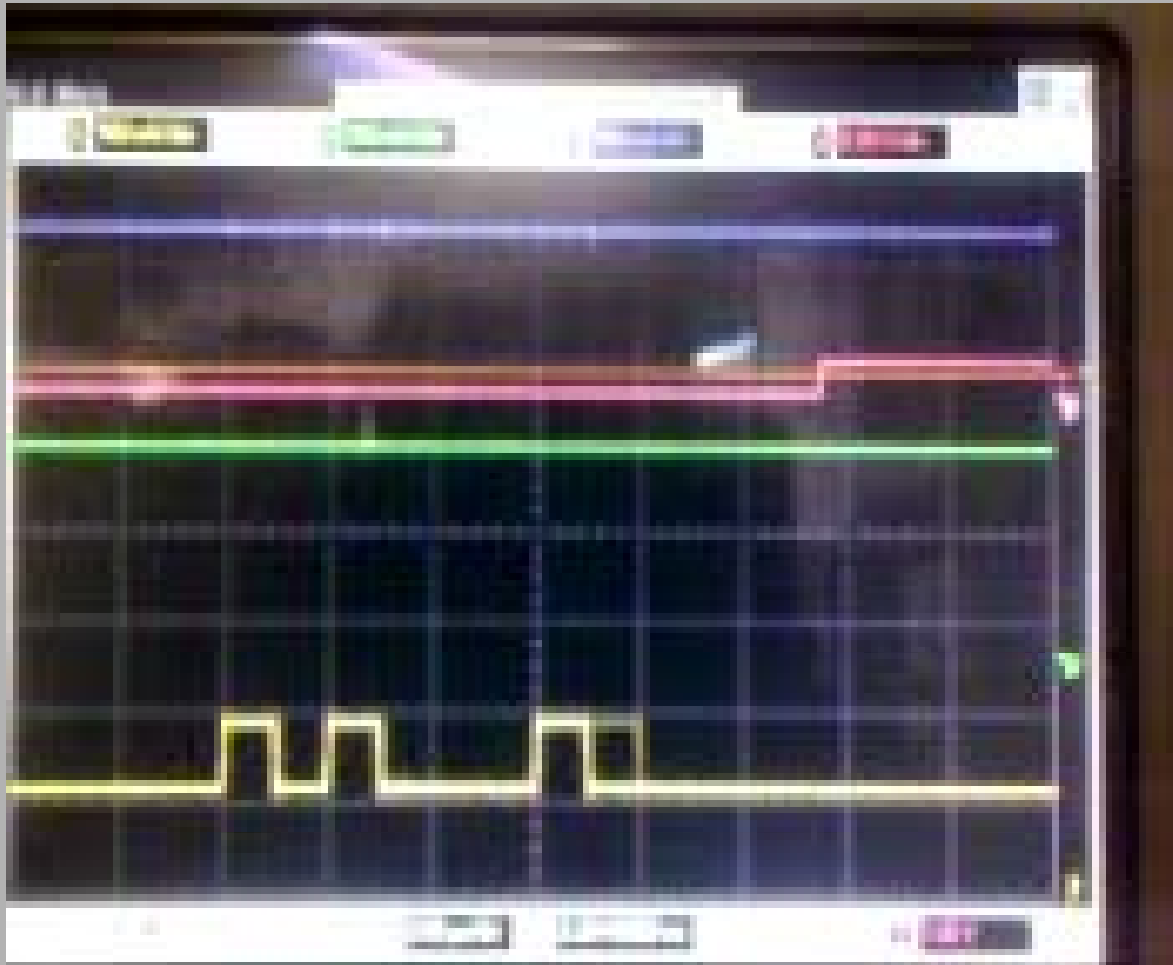
## concept:

- probing shunt current using replica mos (similar to current mirror)
- current-mode ADC  
(good approach for ultra low voltage 1.3V in a 2.5V process!!)
- implementation chosen as flash ADC: simple and fast (also faster to design ;- )
- 6bit, LSB tunable (4bit) – dyn. range  $\sim 100mA \dots \sim 2A$  (probing low current or high range)
- adjustable threshold for alarm
- 4bits to tune the alarm - delay (TOT requirement):  $\sim 150us \dots 3ms$

# single ADC (full) simulation



# results: ADC / current alarm feature



demonstrates full functionality (qualitatively) of ADC and current alarm

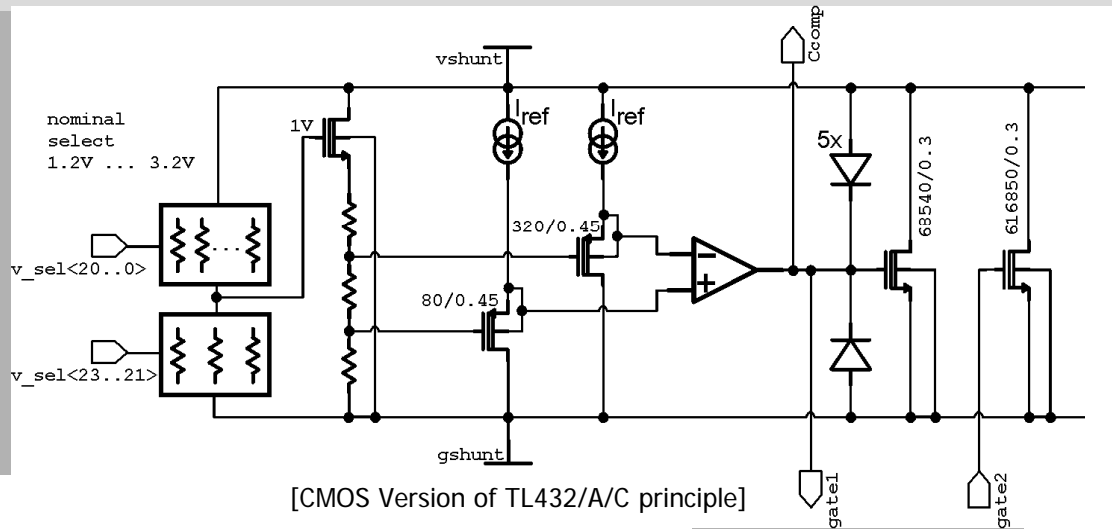
## procedure:

- shunt current (green trace eq.) is swept slowly from 50mA to 1A while ADC is read out continuously (ser\_out : yellow trace)
- the alarm threshold programmed to 011100
- blue trace is current alarm (external signal)

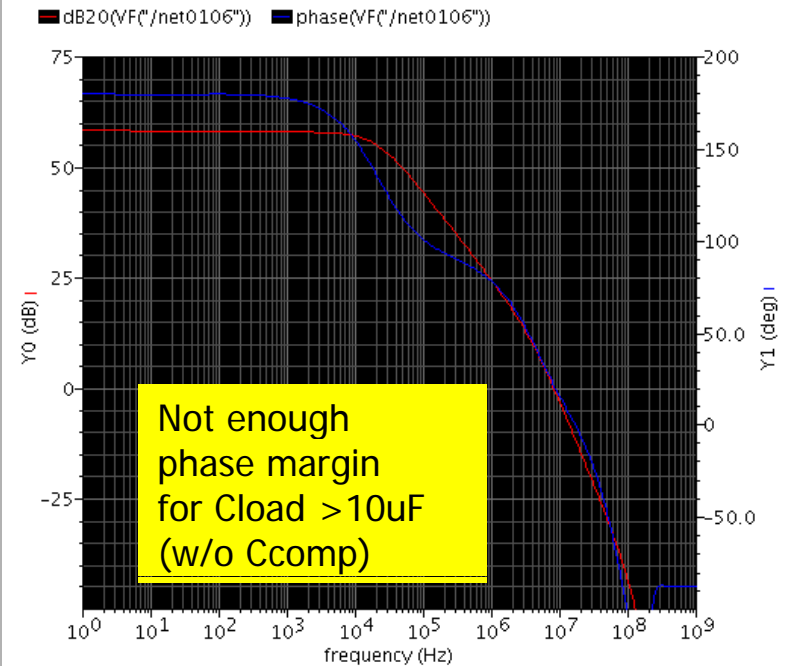
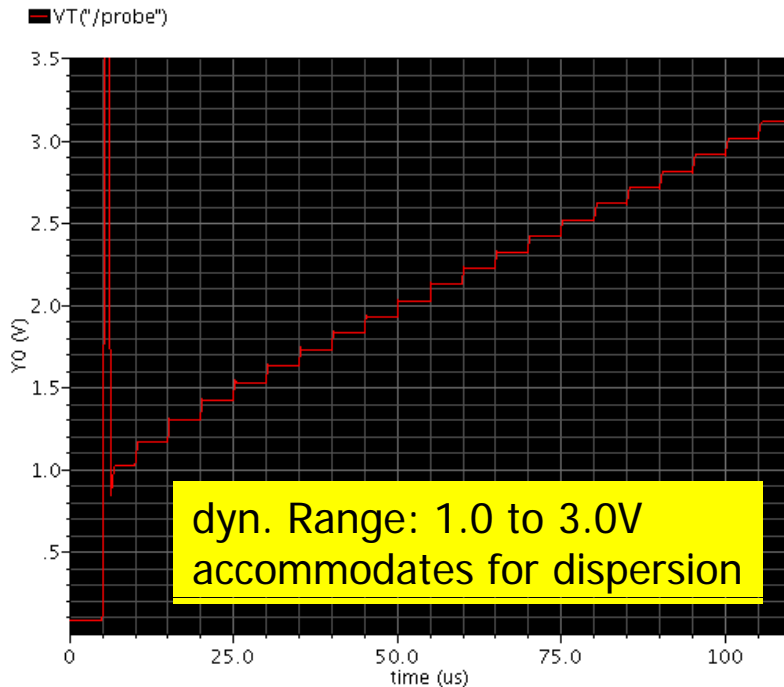
## shown in video:

- ADC bits <0:5> count / follow shunt current
- exceeding threshold triggers current alarm and sets bit<7> in the register

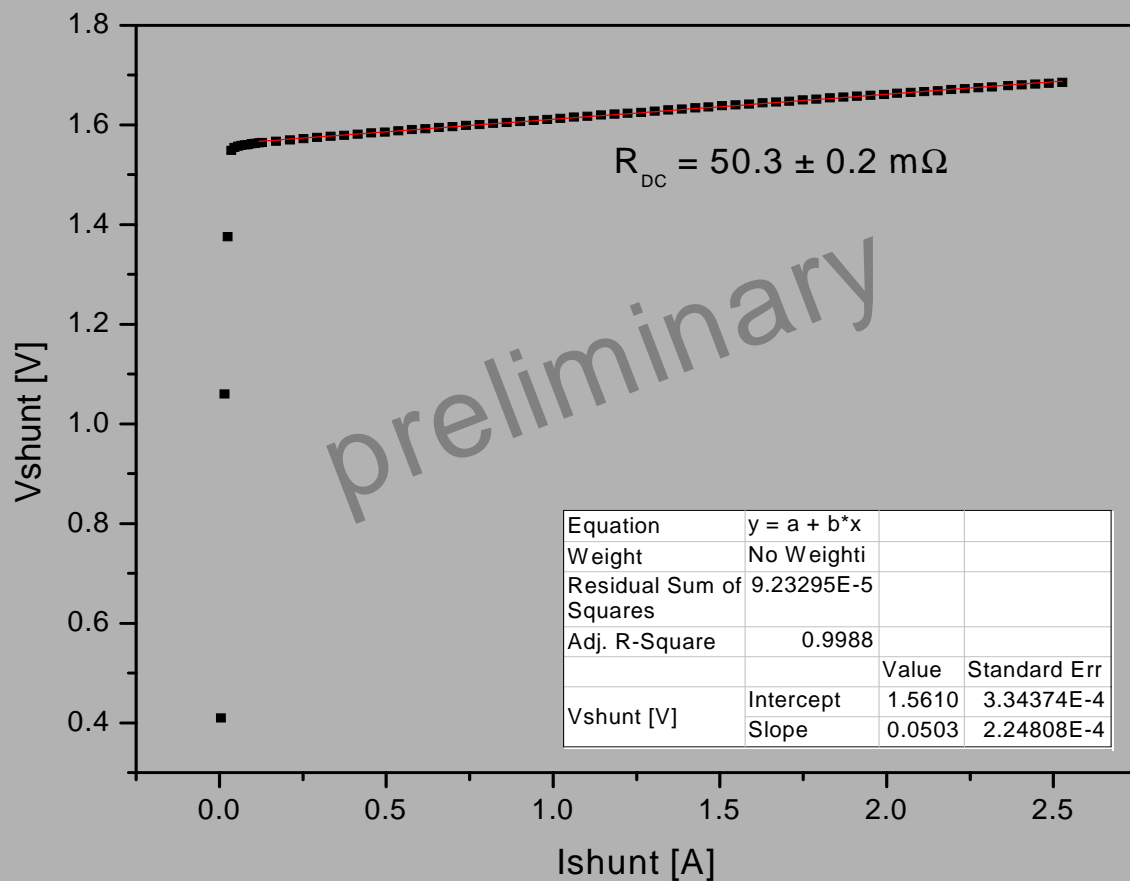
# on-chip shunt



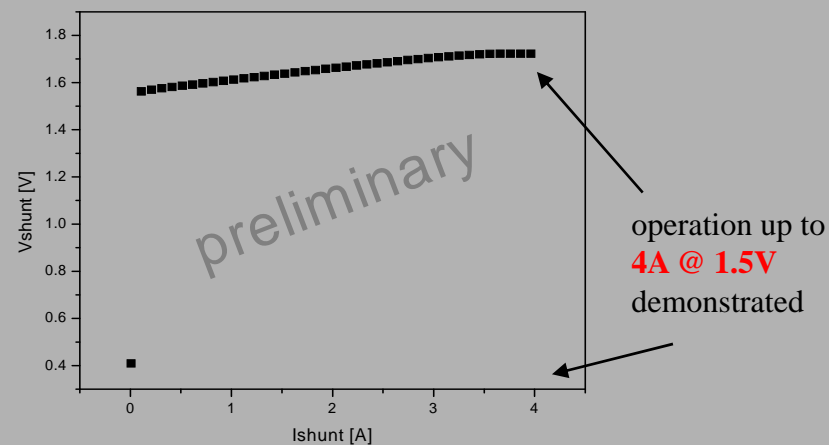
- total RMS <math>< 100\mu\text{V}</math>
- No internal compensation, but external Ccomp pad
- Two shunt transistors with 1/10 aspect ratio



# results: DC shunt characteristic

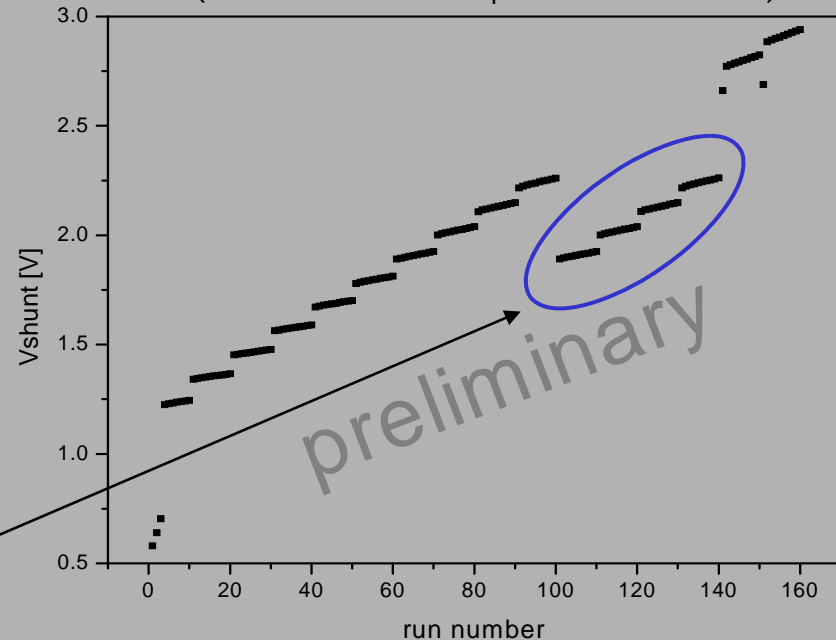


**operation from ~1.2 to ~3V possible**  
trouble with one bit in digital interface in present setup  
(may just be synchronization or bad chip -> more detailed studies )



different Vshunt settings:

(each show current sweep from 50mA to 500mA)



# first AC behavior / linear regulator

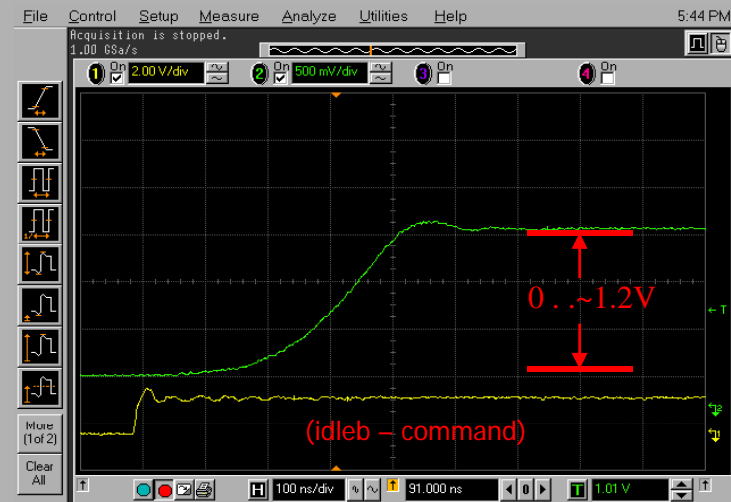


Ishunt (50mA ... 1.2A)  
(bandwidth of current source limited to 10kHz)

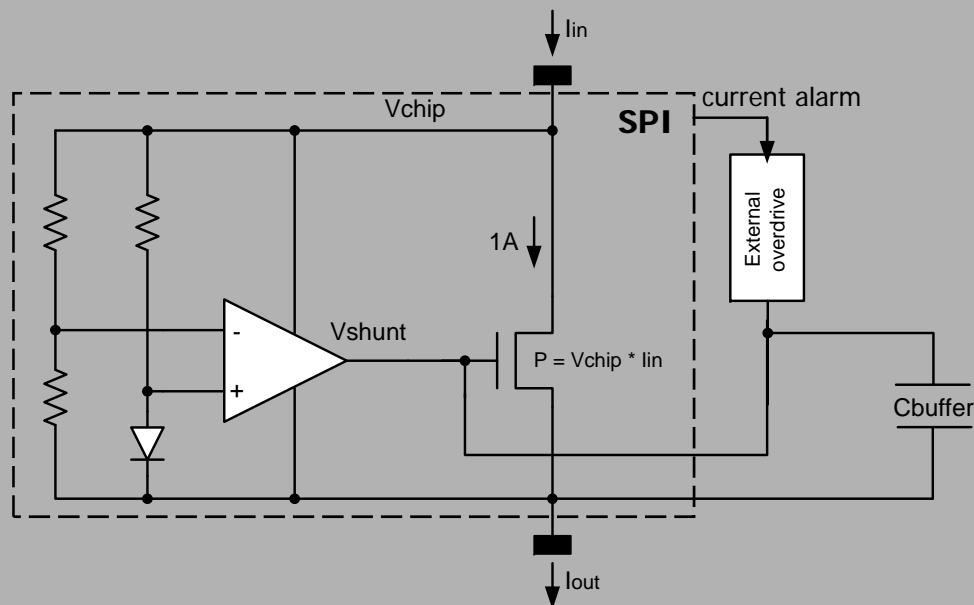
Vshunt (around 50mV)

idle feature (Linreg)

-> Impedance:  $\sim 40 \text{ m}\Omega$   
(more frequency studies needed)



# OverPower Protection (option)



1. OverPower is **NOT** OverCurrent  
-> current should stay the same  
in SP scheme!

2. Power reduction by  
**collapsing the chip voltage**

3. Goal: reduce Vchip to minimum

e.g. 100mV and 4A -> **P ~ 400mW**

- in the order of nominal operation

- comparable to ROIC on module

**-> no hot spot!**

Sounds crazy, but serial powering is already!

## Procedure (Option) for SPI:

1. ADC reports **current alarm**

2. Vshunt overwritten by external source (vdd)

-> forces shunt-mos in lin.region & **reduces Vchip** ( $R_{on} * I$ )

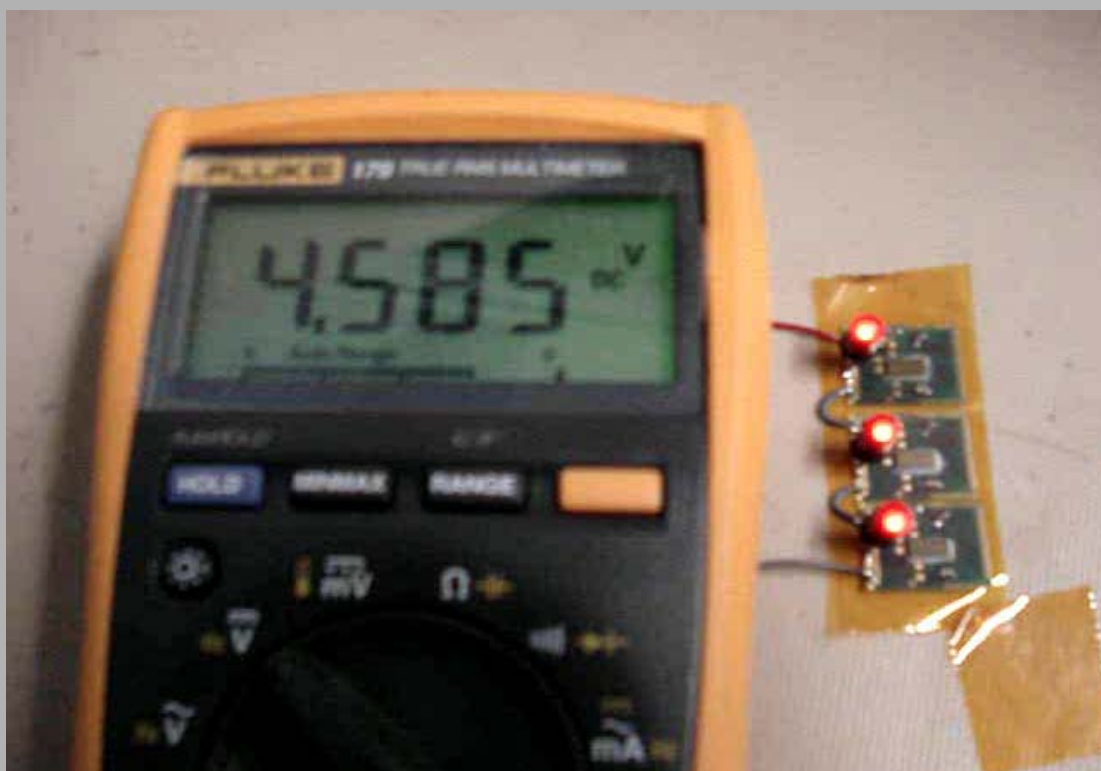
-> whole chip collapses, only shunt maintains operation

Future challenge on PCB side: voltage conserving techniques (module RnD: G.Villani)

Upon successful demonstration: integration of most promising approach in SPI

# magic christmas tree (power down)

Demonstrates power down capability of chip with external signal



**voltage levels (at chip) @ 100mA I<sub>shunt</sub>:**

<u>normal operation</u>	<u>power down (central module)</u>
----- 4.62 V ----- ( $\Delta=1.55$ V)	----- 3.11 V ----- ( $\Delta=1.55$ V)
----- <b>3.07 V</b> ----- ( $\Delta=1.51$ V)	----- <b>1.562 V</b> ----- ( $\Delta \sim 3$ mV)
----- <b>1.56 V</b> ----- ( $\Delta=1.55$ V)	----- <b>1.559 V</b> ----- ( $\Delta=1.55$ V)
----- 0.01 V -----	----- 0.01 V -----

R<sub>on</sub> < 30m $\Omega$  (corresponds to previous parasitic simulation)  
extrapolation to 4A (long time tests needed!):  
-> **P ~ 480 mW (no hot spot)**

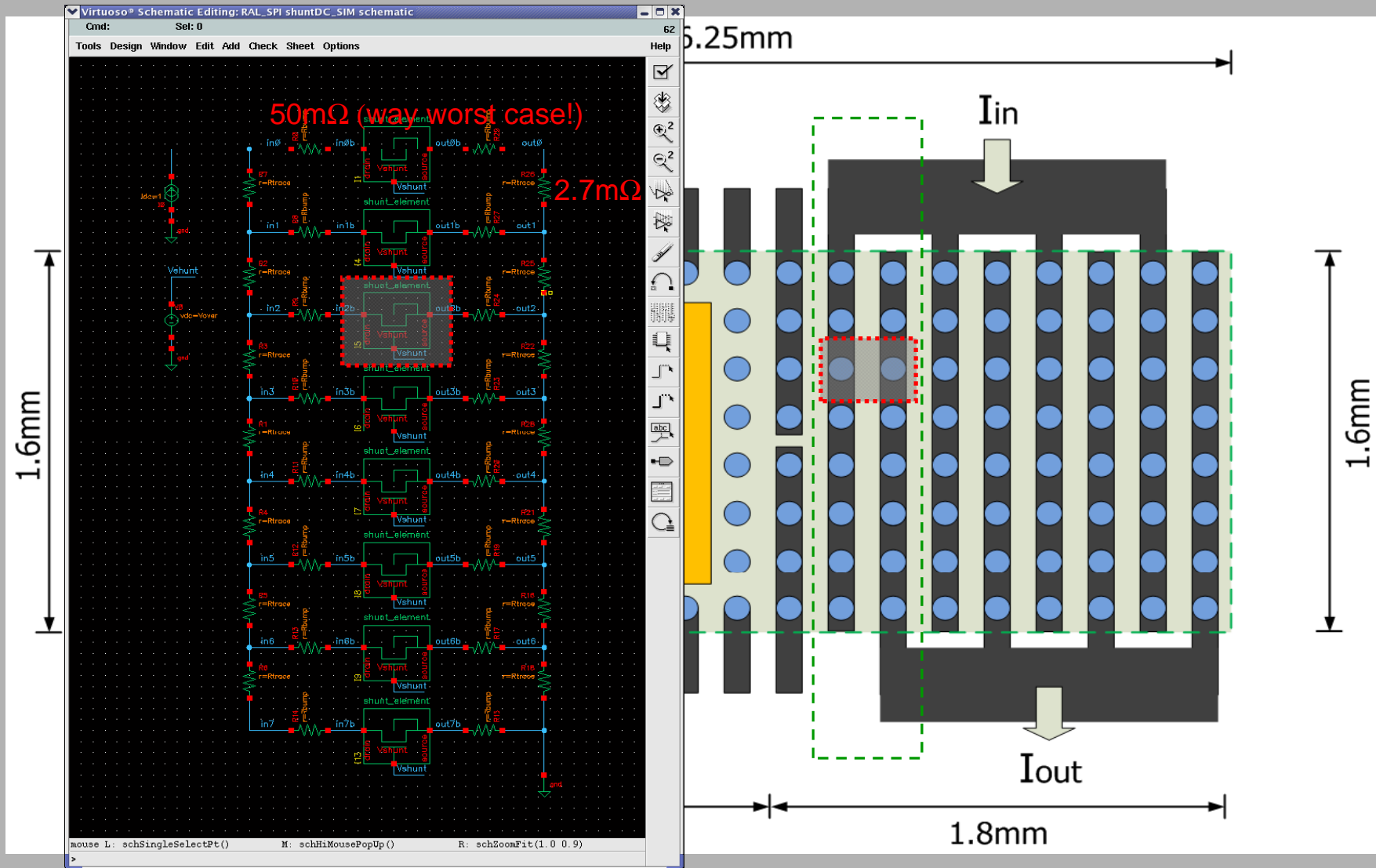


# Summary / Outlook

- **Discrete SP setups went through many iterations, limitations reached** (features vs size vs performance)
- **SPI – Serial Powering Interface**: generic chip to explore SP schemes
- TSMC025MM, radiation tolerant design (except distr. shunt), High current shunt (1A+), distributed shunt, AC coupled comports, 2 Linregs, monitoring ADCs, over power protection options
- **SPI 0.01 fabricated** (120 chips) **and FCOB successful**
- first tests -> chip tested fully functional, measurements very promising
- stand alone chip characterization (datasheet) in progress at Fermi (C.Gingu)
- operation with ABCn / AC coupling in preparation at RAL (M.Weber et al.)

# Power shunt (DC)

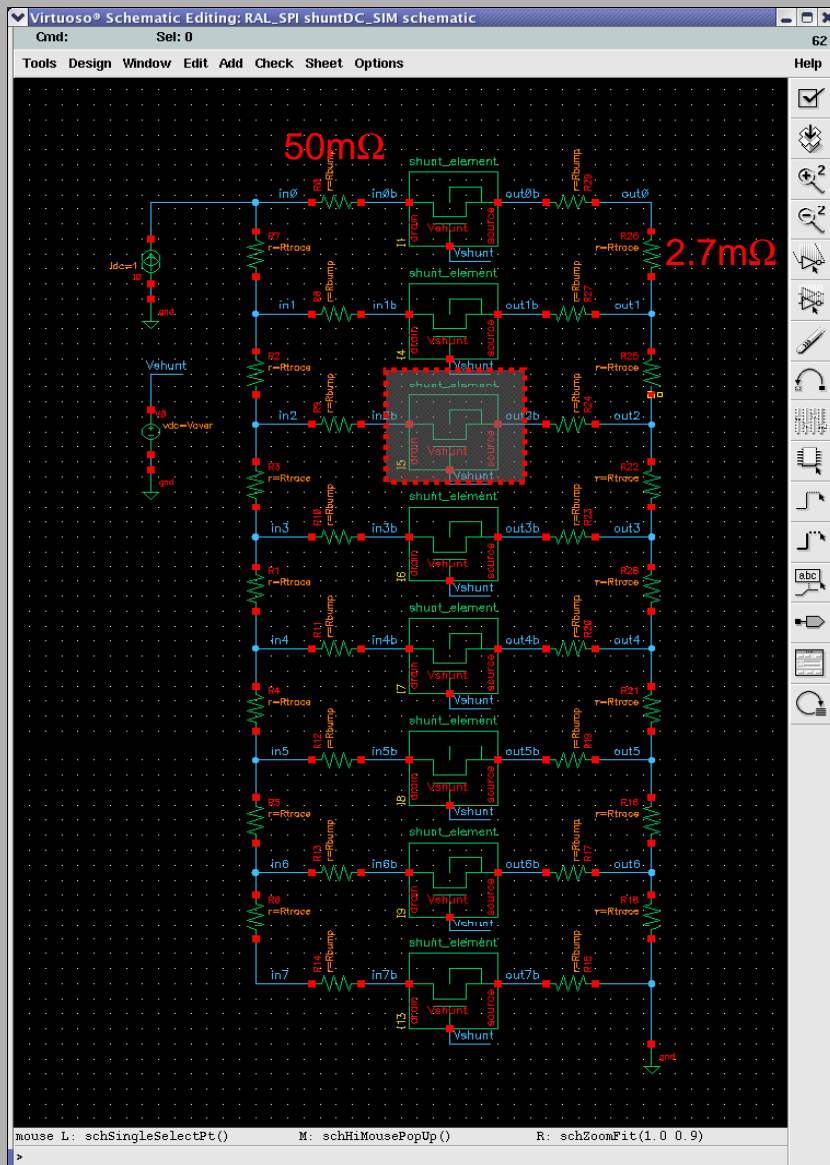
benchmark for power down



Note, 4 finger pairs assumed (old), actual design uses 3 finger but more bumps  
 -> similar or better performance expected

postlayout to include parasitics

# Power shunt (DC)



Spice-Simulation with **1A per finger pair @120C**,  
Vshunt=1.5V (worst case overpower-protection scenario)  
-> average current per bump: ~100mA, max rating 240mA

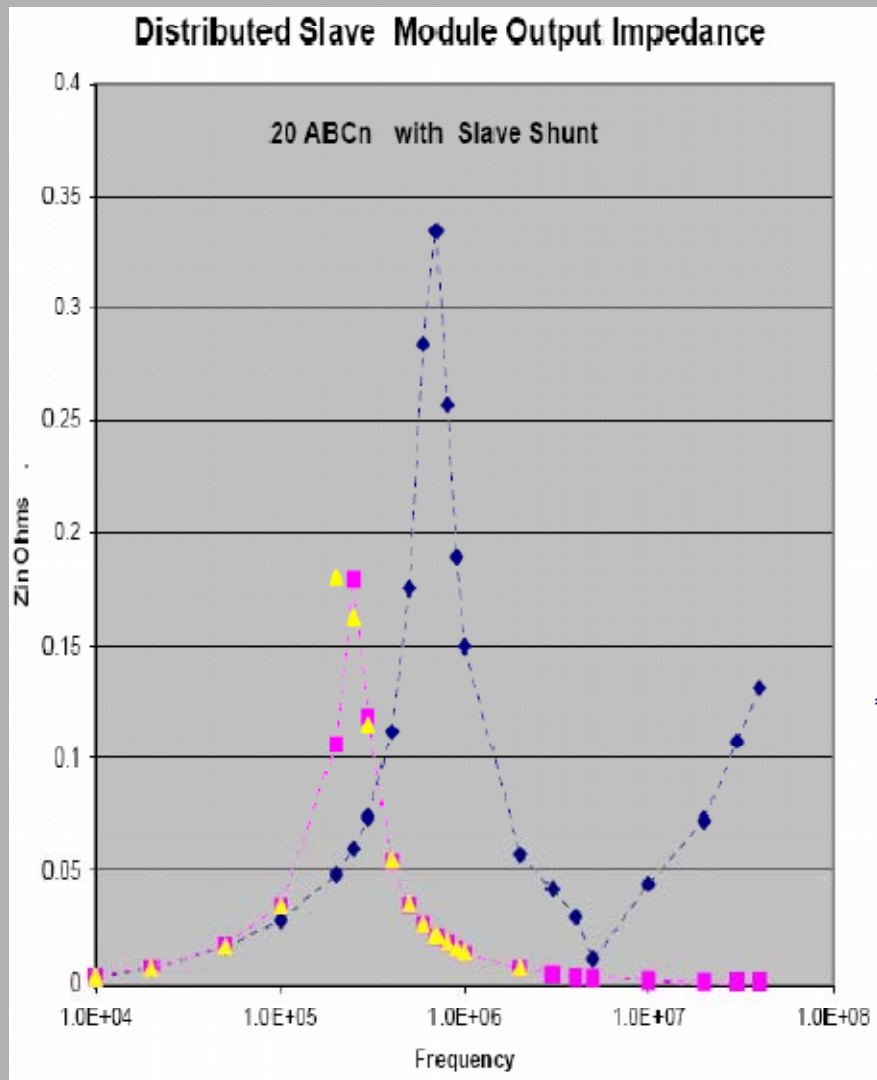
Voltage drops:

- 20mV from pure MOS model (Ron)
  - 5mV from on chip routing** (bump bond approach helps here a lot!)
  - 25mV from 'Off chip' routing: Rbump, Rtrace
- Vdrop,total ~ 50mV**

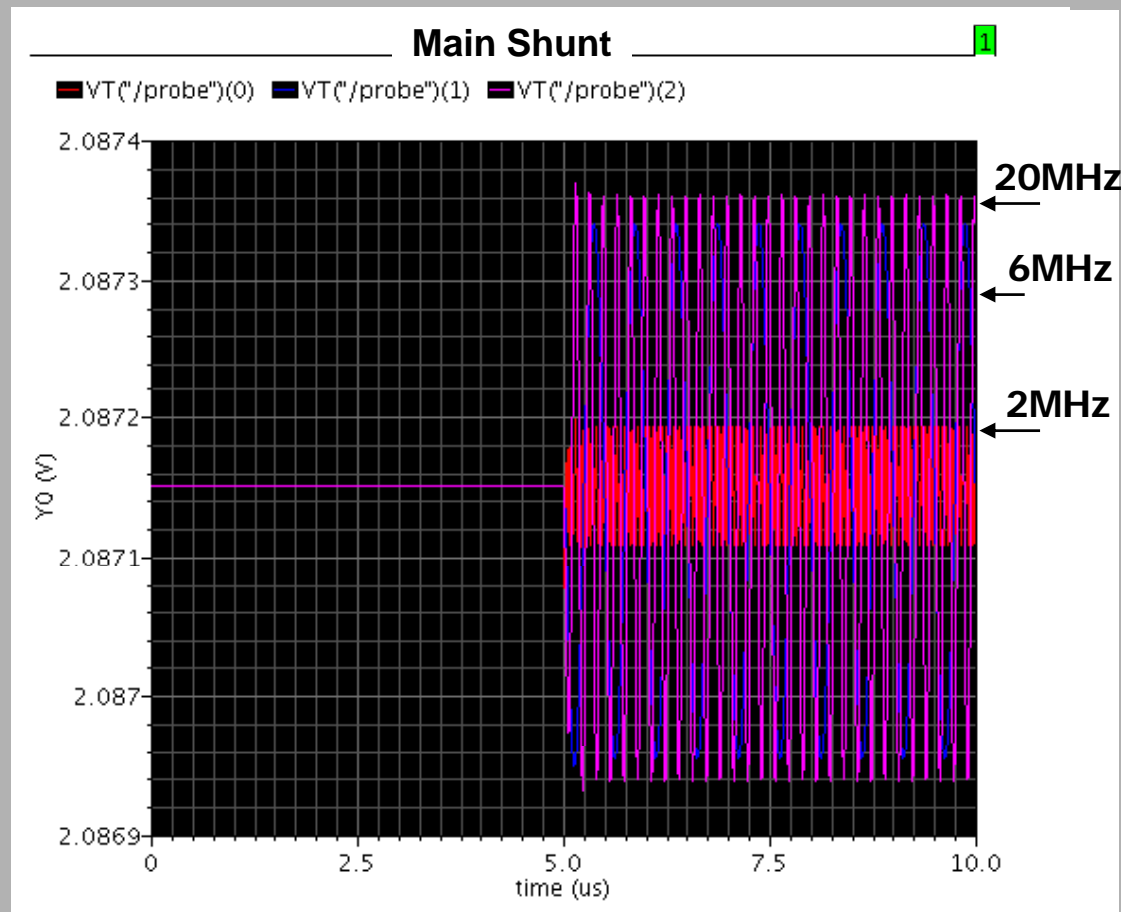
Conclusion:

- **Take these numbers with a grain of salt!**
- However, they give good indication for feasibility e.g. a different routing topology which didn't look too bad at first resulted in ~500mV drop
- **For 1A total current we should be on a safe side** (note, this simulation uses 1A per finger (4 of them!))

# Shunt performance (simulation)



- ◆--- No Module Level Cap Filter 100mA
- 10uF cap on module supply 100mA
- ▲--- 10uF cap on module supply 500mA



$I_{shunt} = 100\text{mA}$  ( $I_{sin} = 10\text{mA}$ ),  $C_{Load} = 1\mu\text{F}$

$$Z < 0.5\text{mV}/10\text{mA} = 50\text{m}\Omega$$

**Compared to 1 .. 50Ω for discrete components setup**