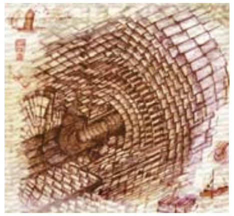
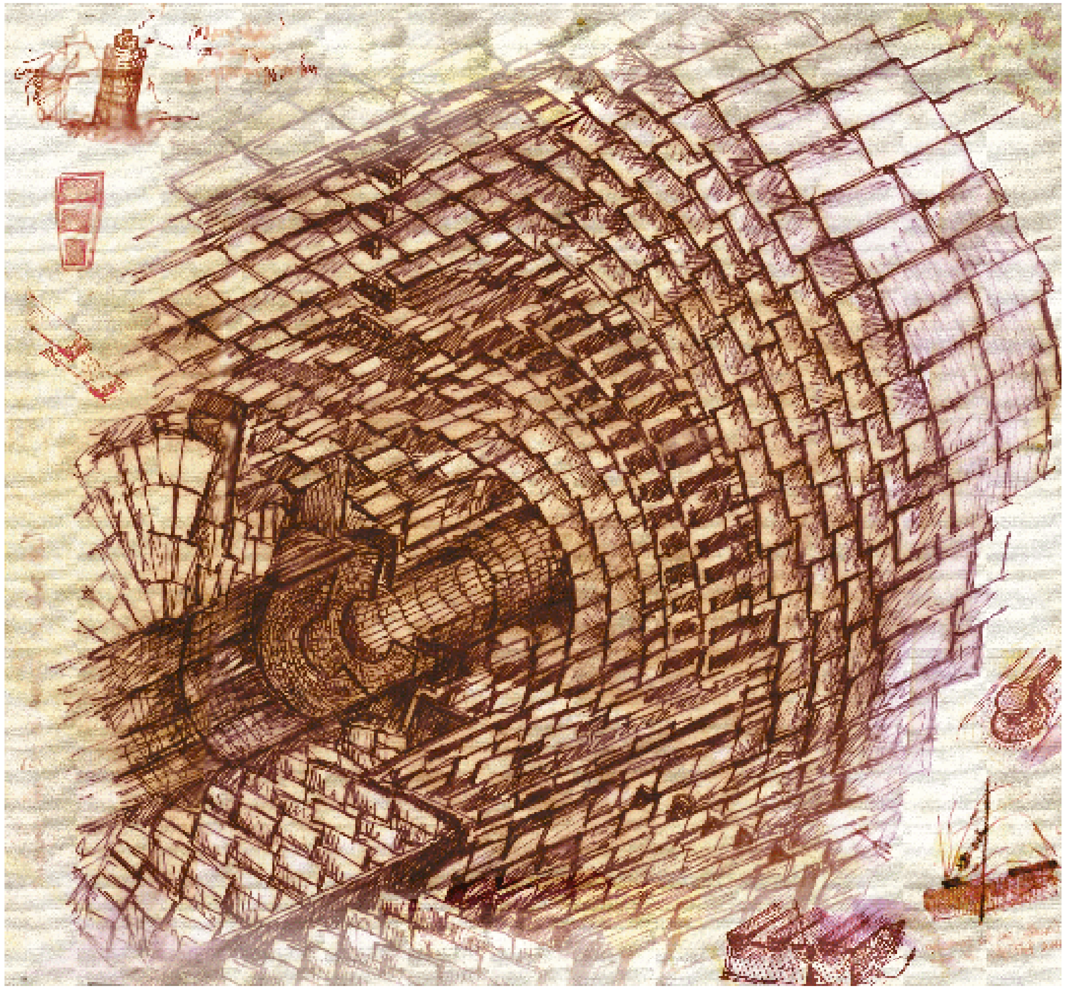
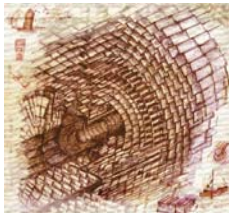


CMS Tracking Trigger
Straw men





Scope of this Discussion: Phase II Outer Tracker

- **The region of the inner-most Pixel Layers is fundamentally challenging at the SLHC, especially for the Sensor Technology**
  - **One may speculate as to the most promising way forward**
  - **B-tagging, e/γ discrimination remain Very Important**

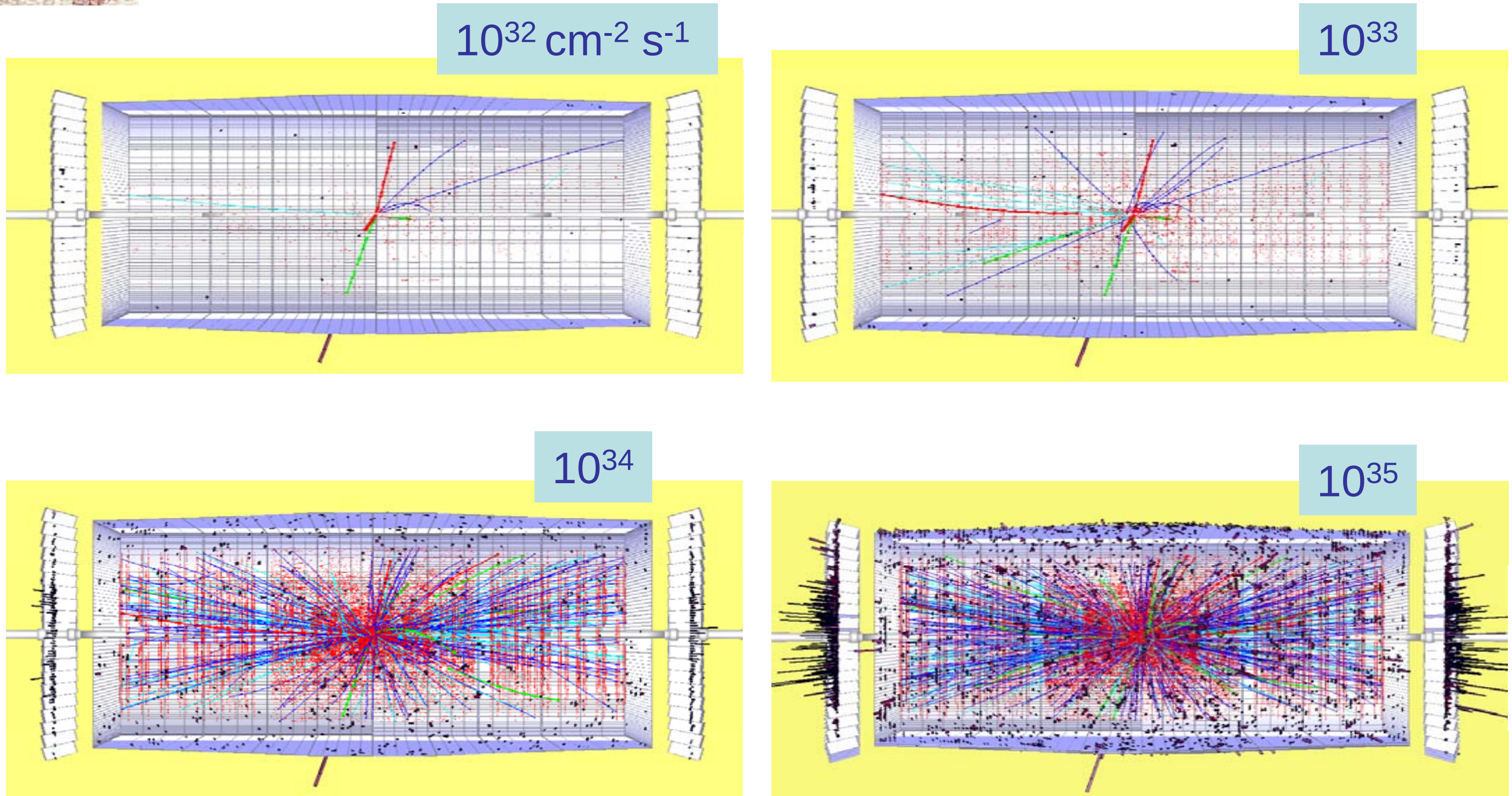
- **Here focus on Phase II Outer Tracker**

- **Assume 4 ~ 5 Inner Layers of Fine-Pitch Pixels**

- **Assume boundary between inner Pixel Layers and Outer Tracker is somewhere between 20 ~ 40cm**

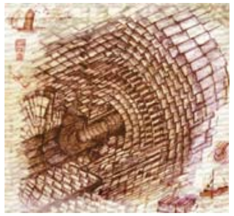
- **In any future baseline layout, Outer Tracker and inner-most Pixel Layers will have to make a coherent Tracking System**

CMS from LHC to SLHC



I. Osborne

At SLHC CMS faces new challenges, in particular for both Tracking and Triggering



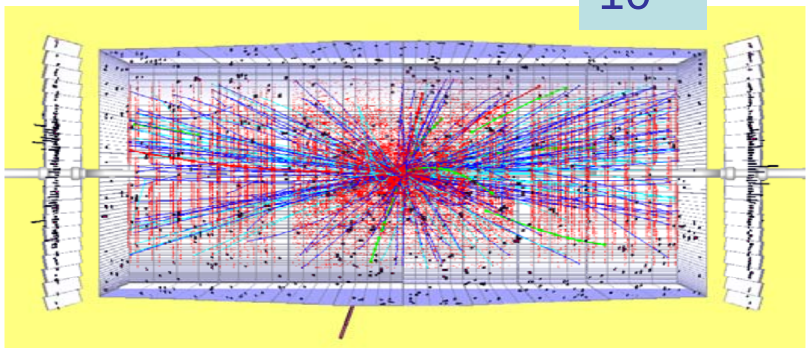
CMS from LHC to SLHC

10^{32} cm^{-2} s^{-1}

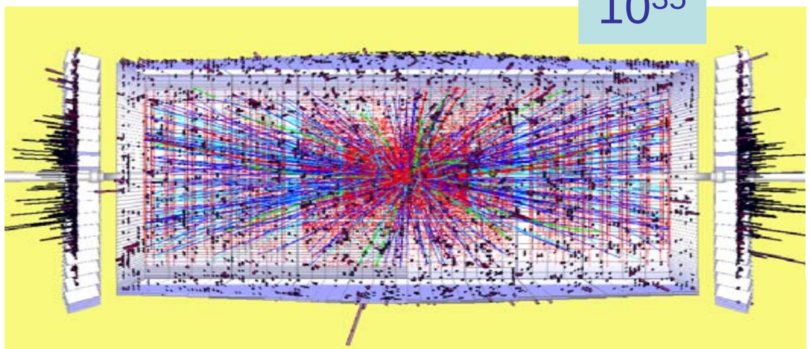
10^{33}

For CMS, even after upgrading the Trigger System to use the full granularity and resolution of the Calorimeter & Muon Systems, "an L1 Track Trigger at SLHC is Not an Elective Project"

10^{34}



10^{35}



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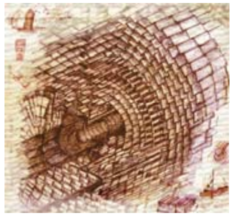
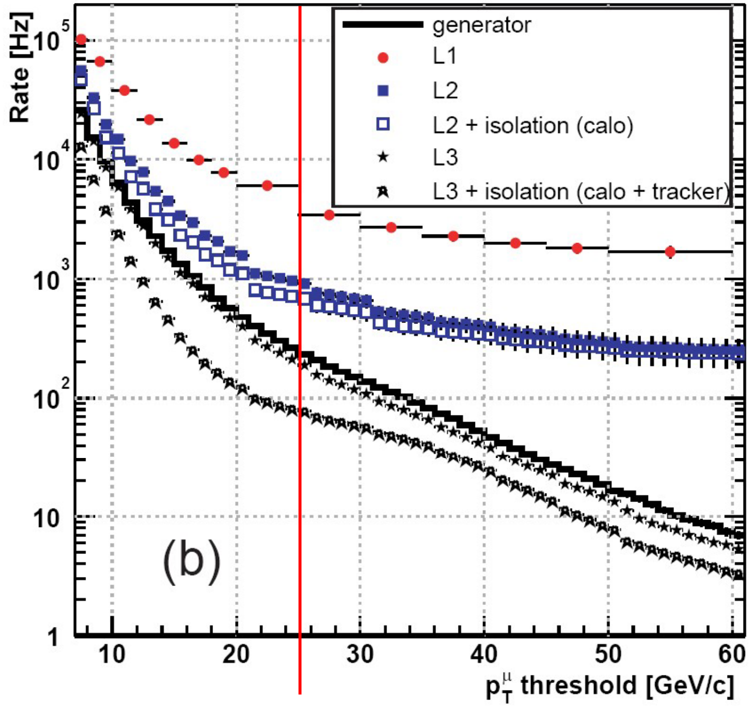


Required Functionality
L1 Trigger

- **Confirmation of Isolated High-pt μ Candidates**
  - **Fast, Efficient & Clean Tracking**
  - **Excellent Pt resolution**
  - **Isolation**
- **Increased Rejection of fake e/γ Candidates**
  - **Match with high Pt Track (nb conversions…)**
  - **Isolation**
- **Tau Jet trigger**
  - **Low Multiplicity**
  - **Isolation**
- **MET ?**
  - **Clean up High Pile-up environment**
- **Rejection of Uncorrelated Combinations, from different primary vertex ?**
  - **Match with Tracks at Vertex ?**
- **…**

Pile-up effects at 10^{35} not included in L1 μ Pt threshold curve !



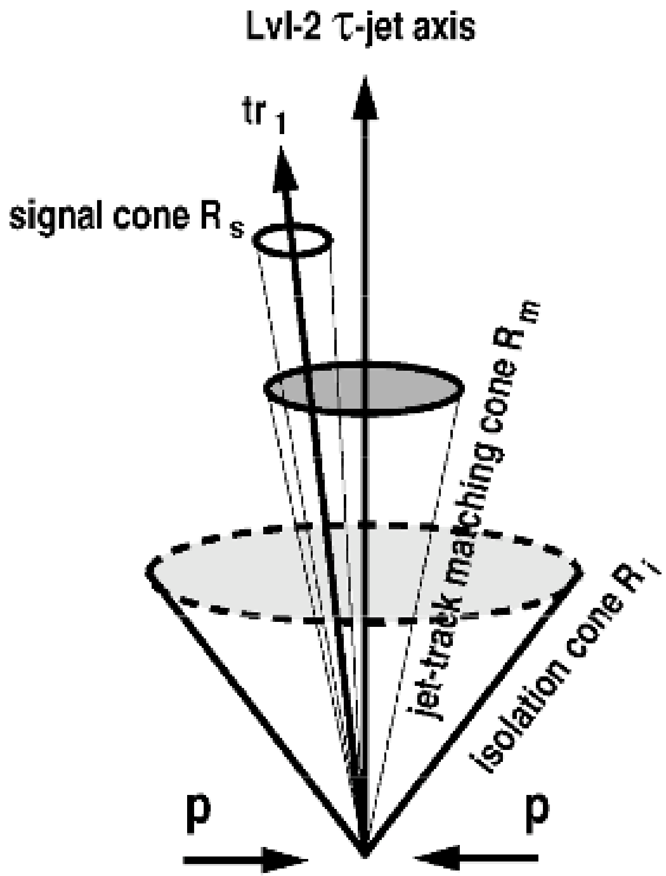
Tracker + Isolation @ HLT:
Factor ~ 100 reduction
For same nominal Pt threshold

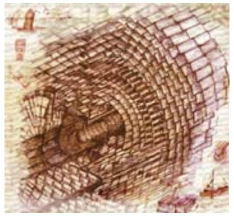
Required Functionality
L1 Trigger

- **Confirmation of High Pt Track Candidates**
  - Tracks with Pt above 15 ~ 25 GeV
  - Excellent Efficiency
  - Good Pt resolution

- **Isolation**
  - Tracks with Pt above ~ 2 GeV
  - Good Efficiency
  - Longitudinal Vertex association
    - Avoid fake vetoes in high pile-up!

- **Longitudinal Vertex association**
  - Tracks with Pt above ~ 2 GeV
  - Good Z Vertex resolution

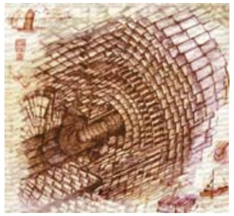




Some Numbers

- **Basic Input: Occupancy at 10^{35} at R ~ 35cm (TIB L2 Radius)**
  - **Typical ~ 2 hits / cm^2 / 35ns   Maximum < 10 * 2 = 20 hits / cm^2 / 35ns**
    - **Strip Occupancy ~ 120MHz / cm^2 at R = 25cm**
    - **Strip Occupancy ~ 80MHz / cm^2 at R = 34cm**
    - **Strip Occupancy ~ 40MHz / cm^2 at R = 50cm   1/2**
    - **Strip Occupancy ~ 20MHz / cm^2 at R = 60cm   1/2**

    (Geoff Hall, compilation of full simulation results from Ian Tomalin)
  - **Nb these occupancy are for 320um~500um thick sensors: 2 ~ 4 hits/cluster**
- **Assume Reduction Factor ~ 2 from thinner sensors & clustering**
  - **To be verified**
- **Cannot possibly transfer all Tracker data at 40MHz !**



Local Occupancy Reduction

- **Crossing Frequency / Event Read-Out ~ 40MHz / 100kHz ~ 1 / 400**
  - L1 Data reduction by a factor of 100 ~ 200 is a reasonable target

- **For L1 Trigger propose to transfer only hits from tracks with**
  Pt > ~ 2 GeV
  - The aim is to provide useful Isolation information
  - Tracks with Pt > ~ 2 Gev are less than 1% of the Tracks inside acceptance
  - This corresponds to the maximum plausibly manageable L1 data rate

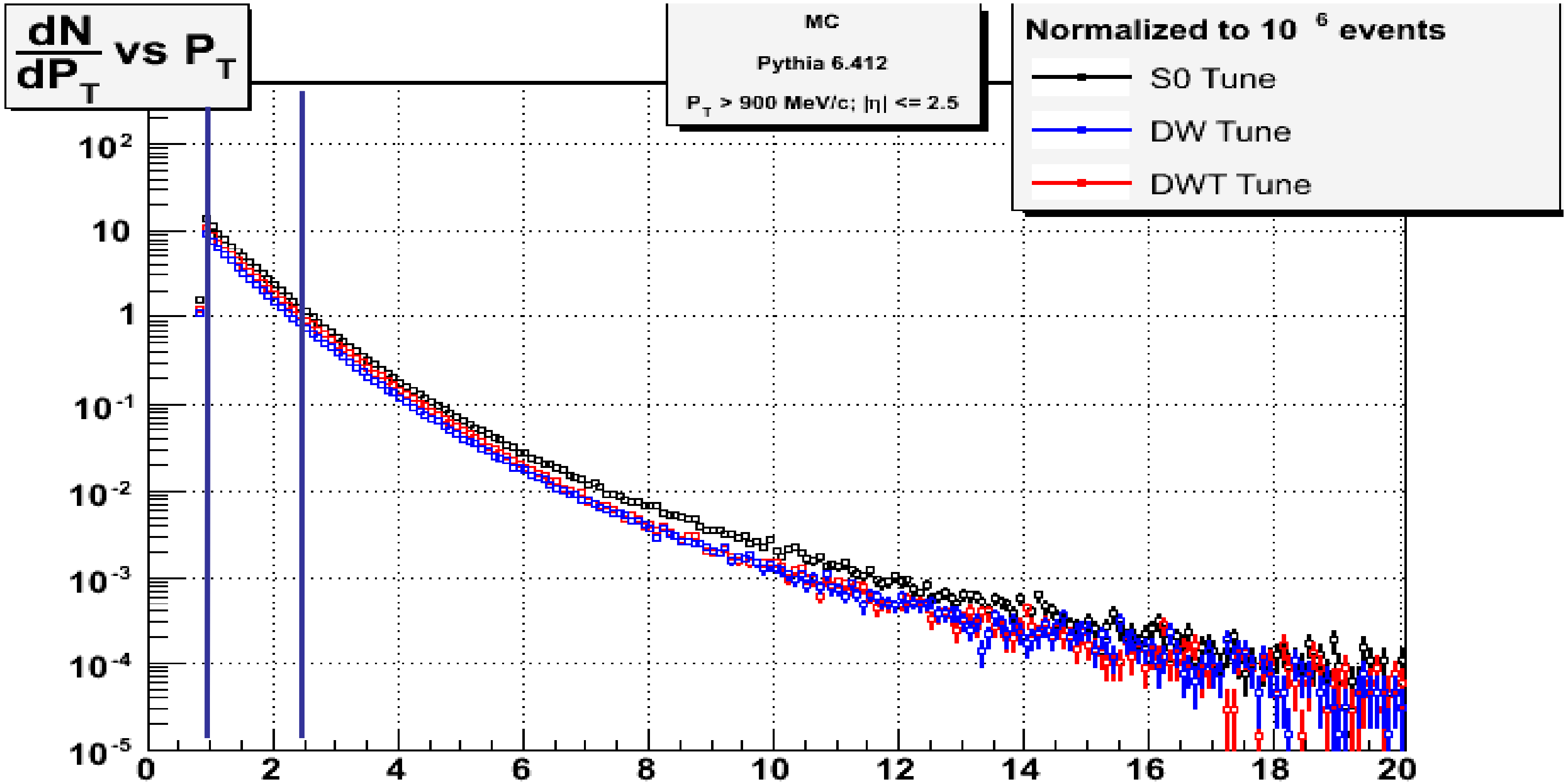
- **In addition, Tracker L1 Trigger Primitives must rapid & reliable identification of high Pt (isolated) tracks (Pt > 15 ~ 25 GeV)**

- **Good Z vertex resolution is required for Isolation and Primary Vertex Association of L1 Tracking Trigger Primitives: need 1 ~ 2mm long pixels**

Local Occupancy Reduction

Tracks with Pt > 1 GeV
< 10% of Tracks in acceptance

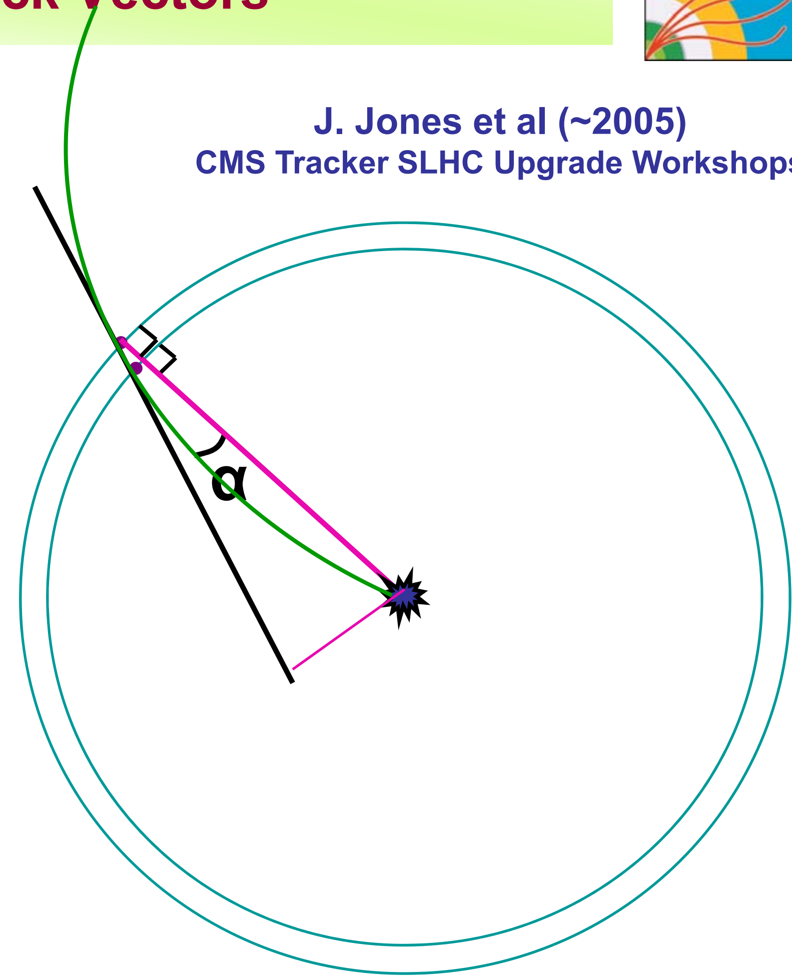
Tracks with Pt > 2.5 GeV
< 10% of the remaining Tracks



Local Occupancy Reduction with Local Track Vectors

J. Jones et al (~2005)
CMS Tracker SLHC Upgrade Workshops

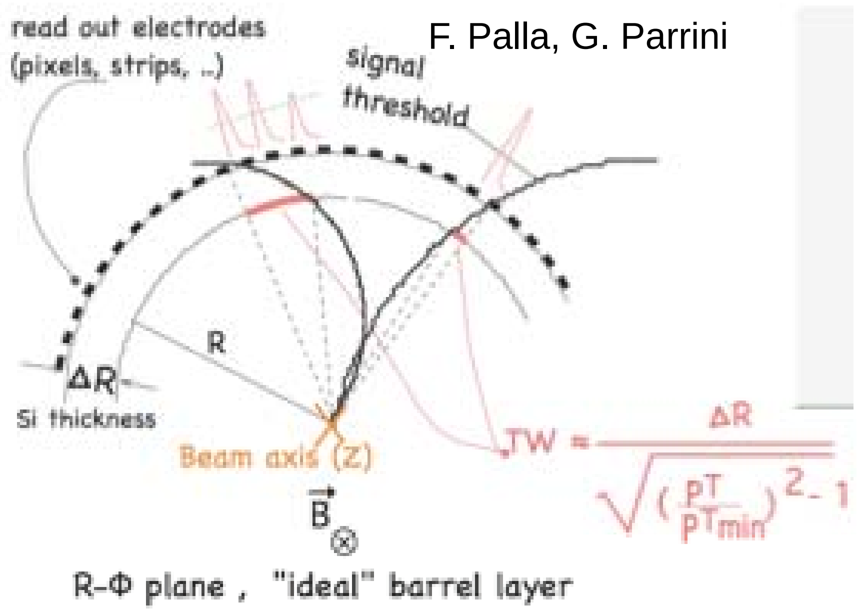
- Pairs of Sensor Planes, for local Pt measurement
- High Pt tracks point towards the origin, low Pt tracks point away from the origin
- Use a Pair of Sensor Planes, at ~ mm distance
  - Pairs of Hits provide Vector, that measure angle of track with respect to the origin
  - Note: angle proportional to hit pair radius
- Keep only Vectors corresponding to Tracks with Pt above a given threshold



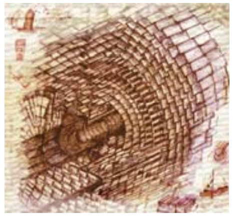
Local Occupancy Reduction with Cluster Width

- **Fine Pitch sensors, for local Clusters Width discrimination**
- **High Pt tracks point towards the origin, low Pt tracks point away from the origin**
- **Use Single Sensor Planes, with fine pitch**
  - Cluster width provides a measure of the angle of track with respect to the origin
  - Note: angle proportional to hit pair radius
- **Keep only Vectors corresponding to Tracks with Pt above a given threshold**

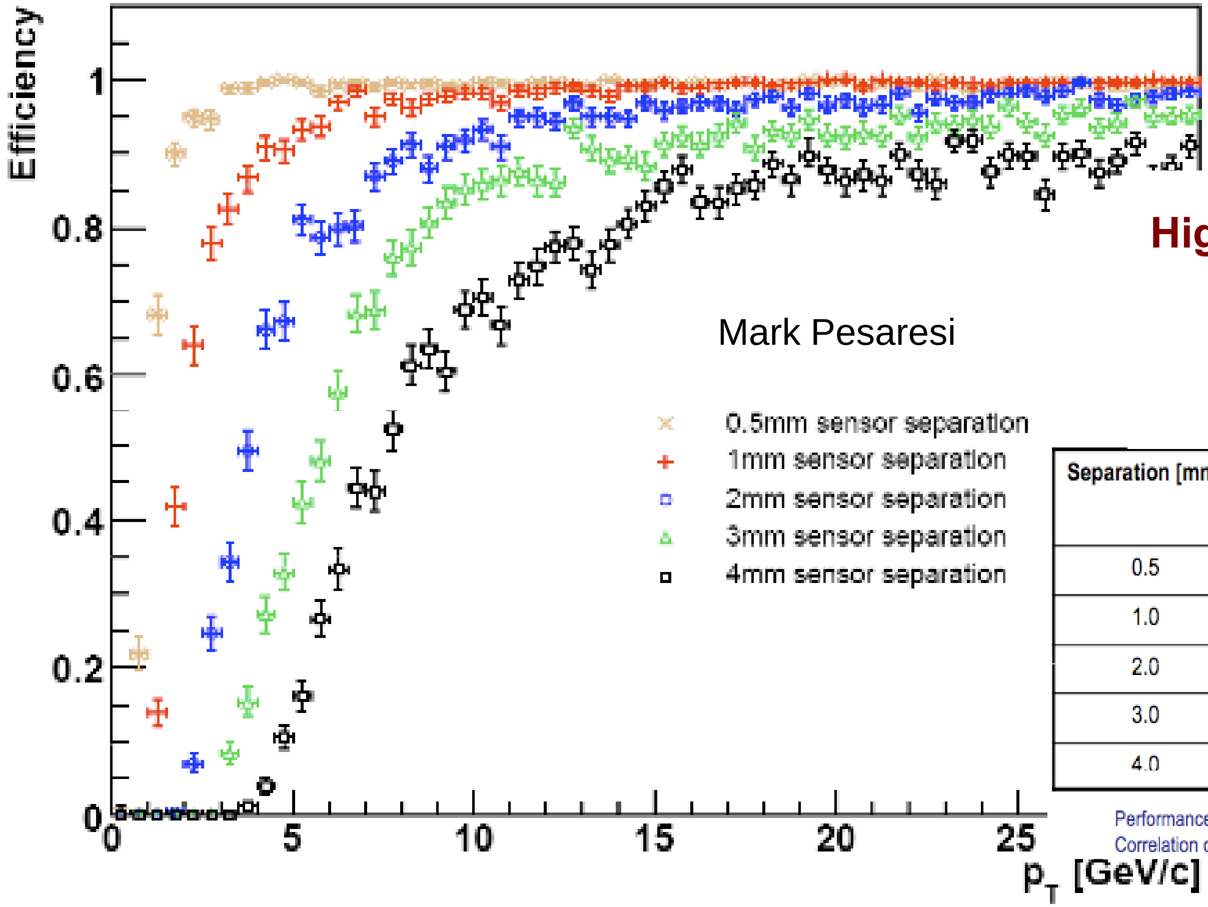
F. Palla, G. Parrini



If not as stand-alone, may at least be used for complementary data reduction in Stacked Module



Recent results for a Stack of closely spaced sensors: pitch ~ 100um*2.4mm (M. Pesaresi)



p_T discriminating performance of a stacked layer at r=25cm for various sensor separations using 10,000 di-muon events with smearing

High rejection factors possible

Much Sharper Threshold For Low Threshold Value

Separation [mm]	Max Efficiency [%]	Fake [%] (or average number/event)	Reduction Factor
0.5	99.05	0.73 (12.22)	8.04
1.0	99.35	4.14 (25.58)	22.26
2.0	97.745	17.83 (18.74)	95.99
3.0	96.00	39.08 (23.76)	210.28
4.0	92.95	47.27 (32.39)	254.35

Performance of a detector stack at r=25cm for sensors with pitch 100μmx2.37mm. Correlation cuts optimised for high efficiency

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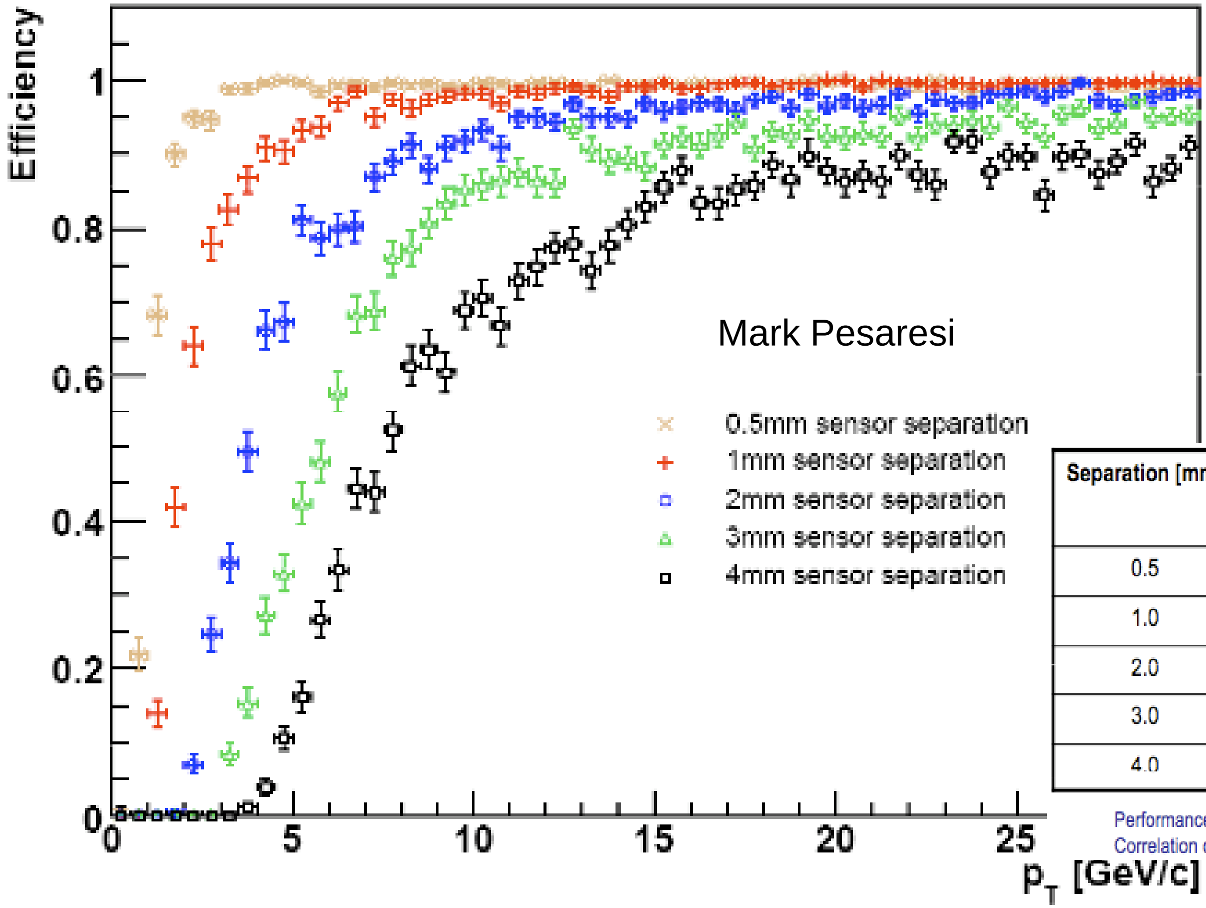

p_T discriminating performance of a stacked layer at r=25cm for various sensor separations using 10,000 di-muon events with smearing

No useful discrimination at Pt ~ 20 GeV

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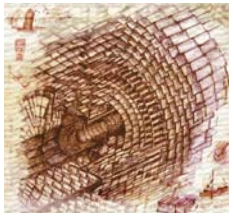
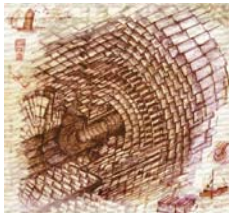


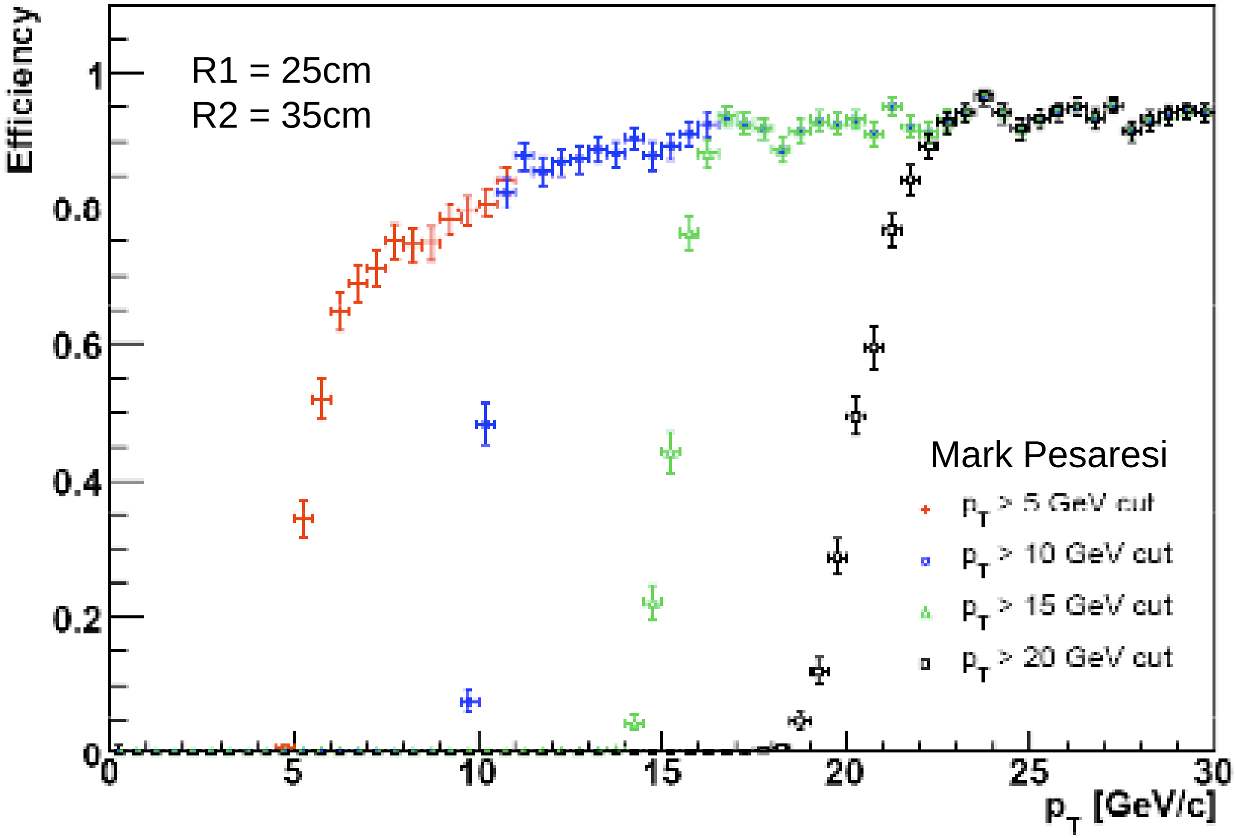
Local Occupancy Reduction
a Hierarchical scheme with Double Stacks

Local Information Gathering, and Processing Hierarchy

- **Within a Stacked-Sensor Module**
  - Collect Hits from each Sensor
  - Match into Hit Pairs & Reject Hit Pairs from Very low Pt Tracks: Pt < ~ 2GeV
- **Within a Double Stack**
  - Collect Hit Pairs from each Sensor Doublet Module
  - Match into Track Vectors of sufficient resolution for high Pt discrimination
  - Reject Track Vectors with Pt < 2GeV as required to further reduce rate
- **Transmit to USC for High Pt & Isolation L1 Track Trigger Primitives**



Recent results for two Stacked Layers spaced ~ 10cm apart (M. Pesaresi)



p_T discriminating performance using double stacks for 10,000 0-30GeV di-muon events with smearing

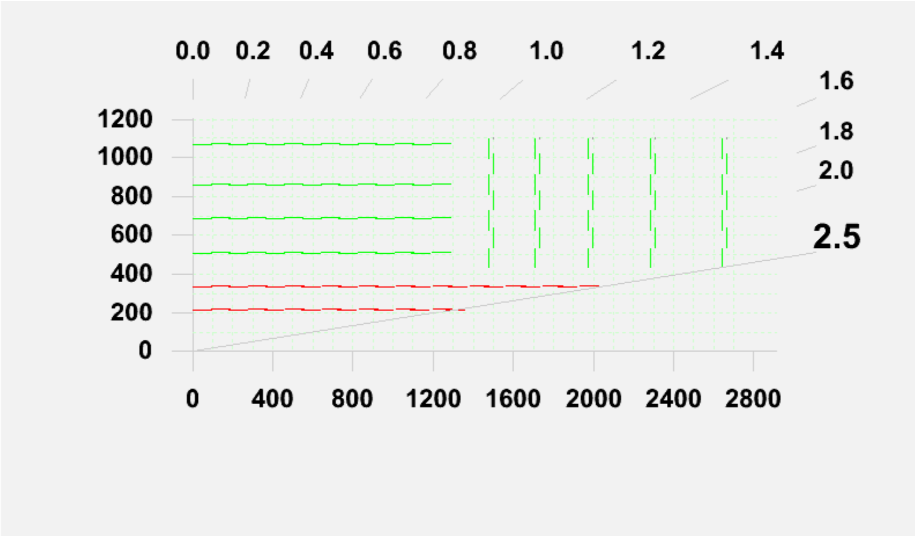
Good
Track Vector discrimination up to Pt ~ 20 GeV

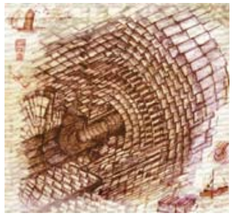
Provides high resolution Tracking Trigger Primitives

Pt thresholds improve With larger radii

Tracking Trigger Layers: Friend or Foe?

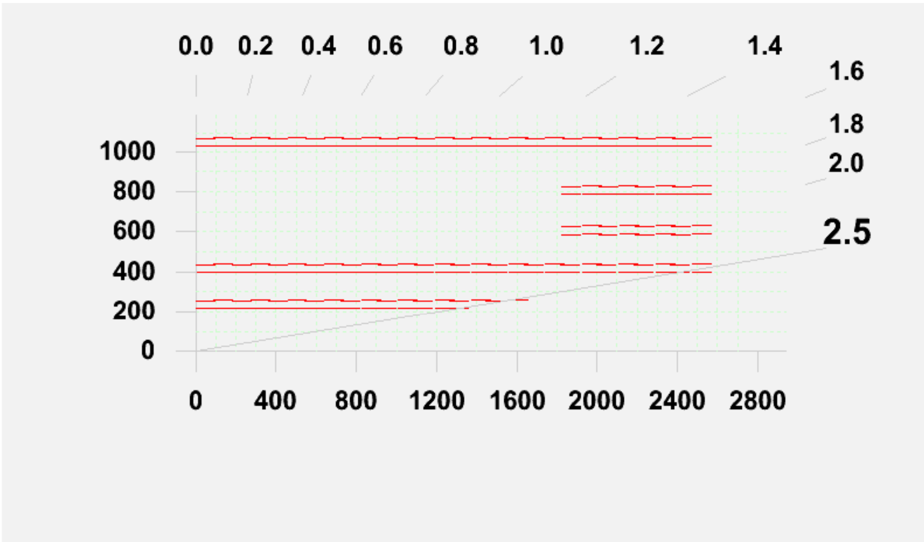
- **Tracking Trigger Layers may adversely affect Tracking Performance**
  - For example, they may be very power hungry and massive
- **May be very expensive, can we afford more than the strict minimum?**
- **Straw Man A: "Conventional" Tracker + minimal Tracking Trigger layers**
  - Ensure good Tracking
  - Identify minimal potentially viable Tracking Trigger configuration

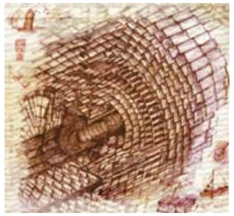




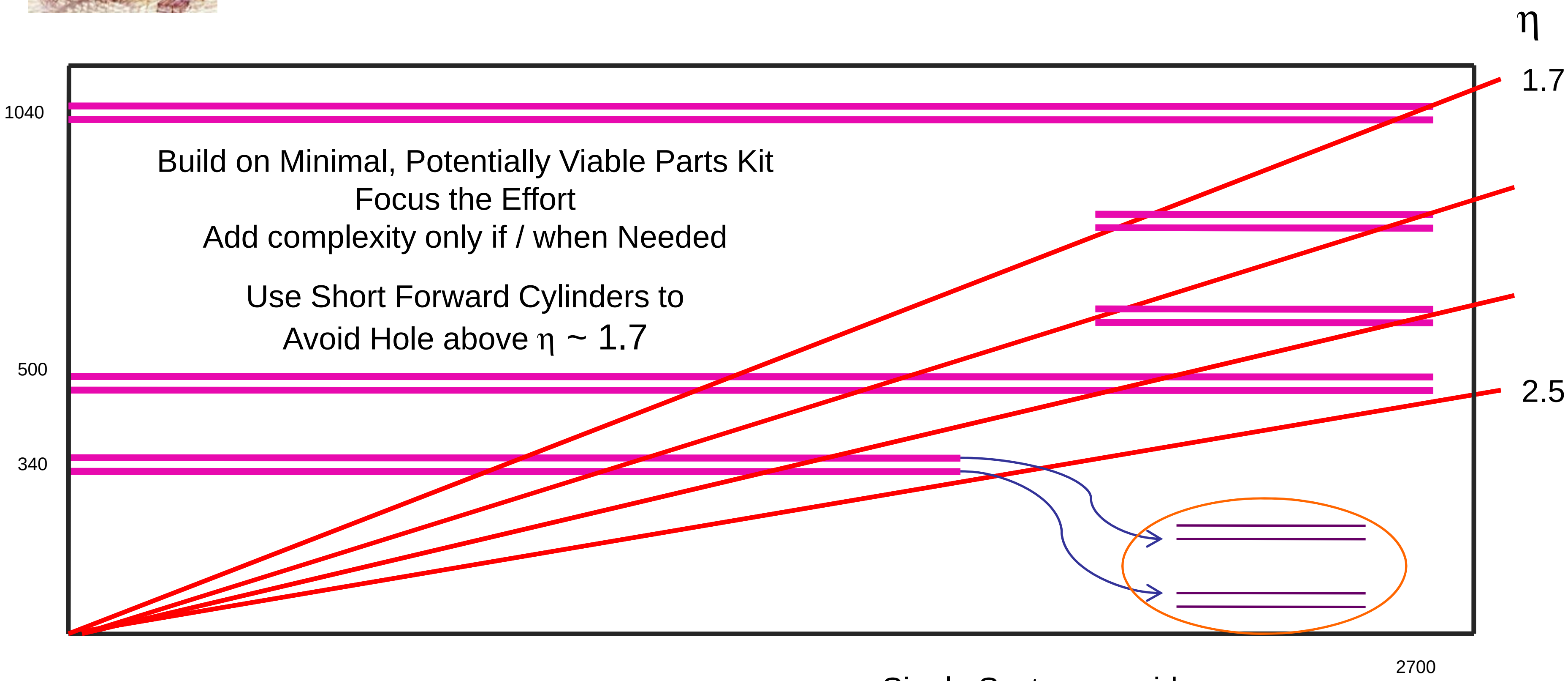
Tracking Trigger Layers: Friend or Foe?

- **Robustness is Crucial: redundancy difficult with minimal system…**
- **Can a scheme be devised, which optimally integrates BOTH Tracking Trigger & Tracking functions?**
  - **Power is important but its material budget that counts: can it be kept low?**
  - **Higher cost may be justified by improved robustness & performance?**
- **Straw Man B: a Fully Integrated Tracking Trigger Tracker**
  - **Single Concept for simultaneously optimizing Tracking Trigger & Tracking Performance?**



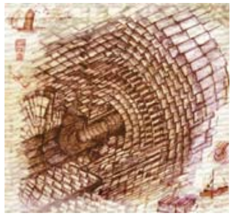


Straw Man B Layout: 3 Double Stack Layers + Short FWD Barrels



3 Double Stack L1 & Tracking Layers,
with full acceptance up to η ~ 2.1:
Each Layer provides 2 * 2 = 4 hits
3 Layers = 12 hits

Single System provides
Full L1 & Tracking functionality
Short FWD Cylinders close acceptance
Total Silicon Surface ~ 375m^2
Present Tracker ~ 210m^2

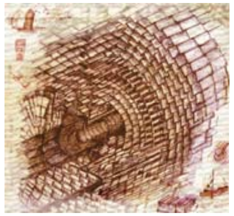


Tracking Trigger Layers: Friend or Foe?

- **A comparative study of both Straw Man A and Straw Man B is underway**
  - **This will help guide the way forward**

- **In what follows, focus on Straw Man B in order to**
  - **Highlight the novel ideas in the CMS SLHC Tracking Trigger approach**
  - **Illustrate potential implications on the Tracker Architecture**

- **Much of what follows is in any relevant also to Straw Man A**

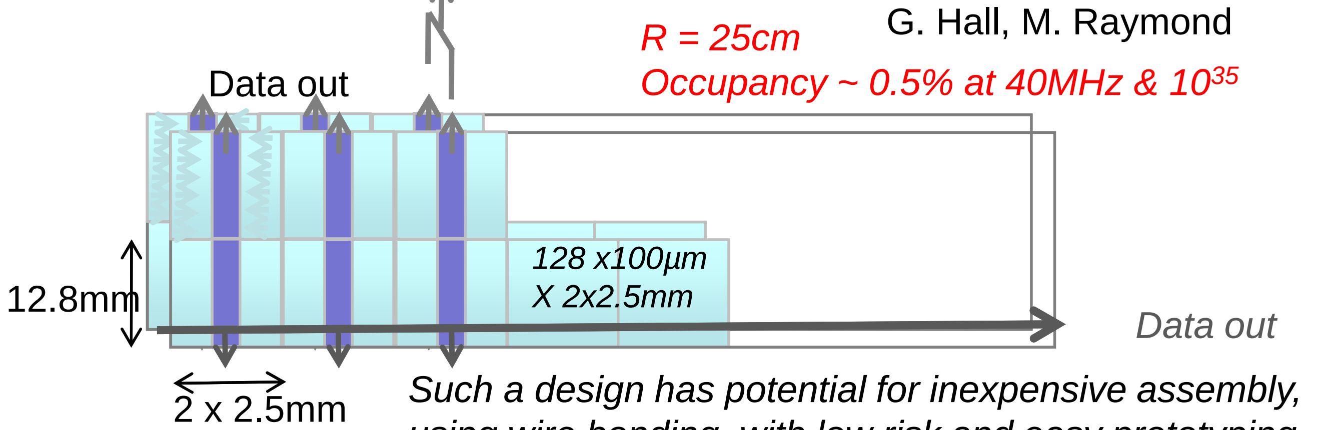


Options for the Stacked Module: ~ Conventional Module Layout

- **Example of ~ Conventionally laid out Hybrid Module (~ 24 * 94mm^2)**
  - **~ Conventional packaging**
    - **Could use either wire-bond or bump-bond**
  - **Signals are brought to module periphery for correlations**
  - **Module width = 2 * chip size ~ 24mm**
  - **Power Penalty for data transmission to module periphery?**
  - **Penalty for Narrow Modules?**

Example PT module

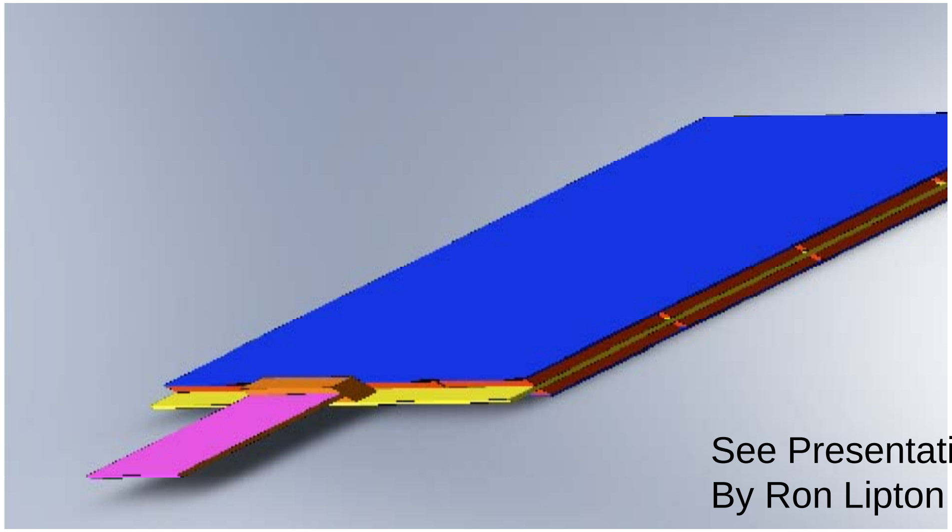
G. Hall, M. Raymond



Such a design has potential for inexpensive assembly, using wire bonding, with low risk and easy prototyping

Straw Man Sensor Doublet Module: Vertically Integrated Hybrid Module

- **Example of Vertically Integrated Hybrid Module (~ 94 * 94mm^2)**
  - **Chips are bonded both to sensor and to to central (Si) pcb**
  - **Direct Vertical Chip-to-Chip transmission: minimizes Power**
    - **Analogue connection of top sensor to bottom chips also under study**
  - **Most elegant solution relies on Chip Through-Silicon-Via (3D) technology**



See Presentation on 3D Technology
By Ron Lipton

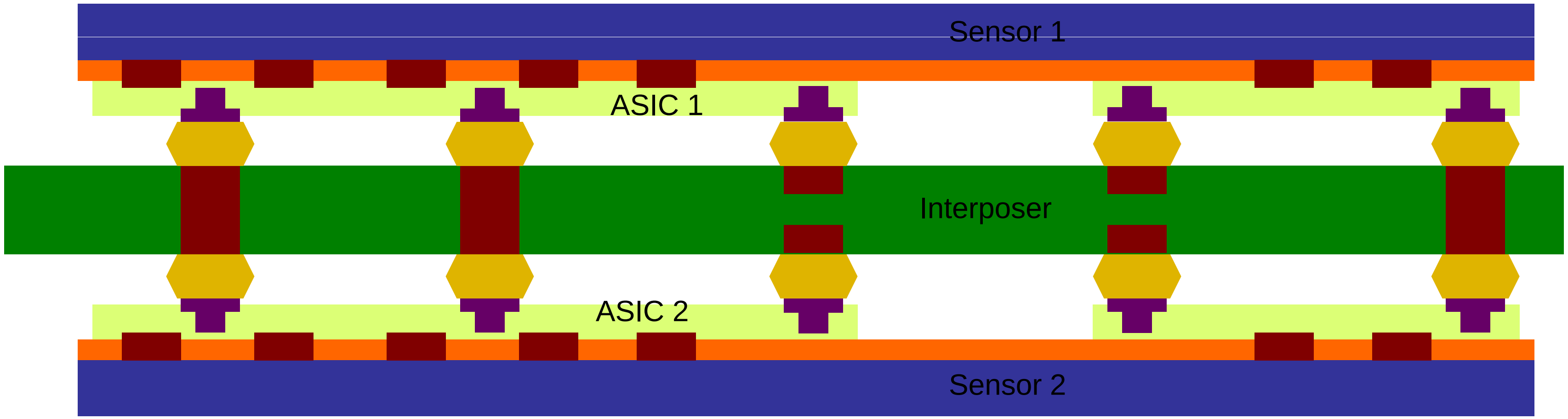
Options for The Stacked Module: 3D Vertically Integrated Module V1

See Presentation on 3D Technology
By Ron Lipton

- **Large Module Possible**
- **Very Short Data Path through Interposer: Power advantage**
- **Information available regionally, close to where needed**

Challenges:

- **Requires Chip Through-Silicon-Vias (3D)**
- **Requires Direct Oxide Bonding to Large Area device**
- **High rate data transmission without disturbing analogue performance**

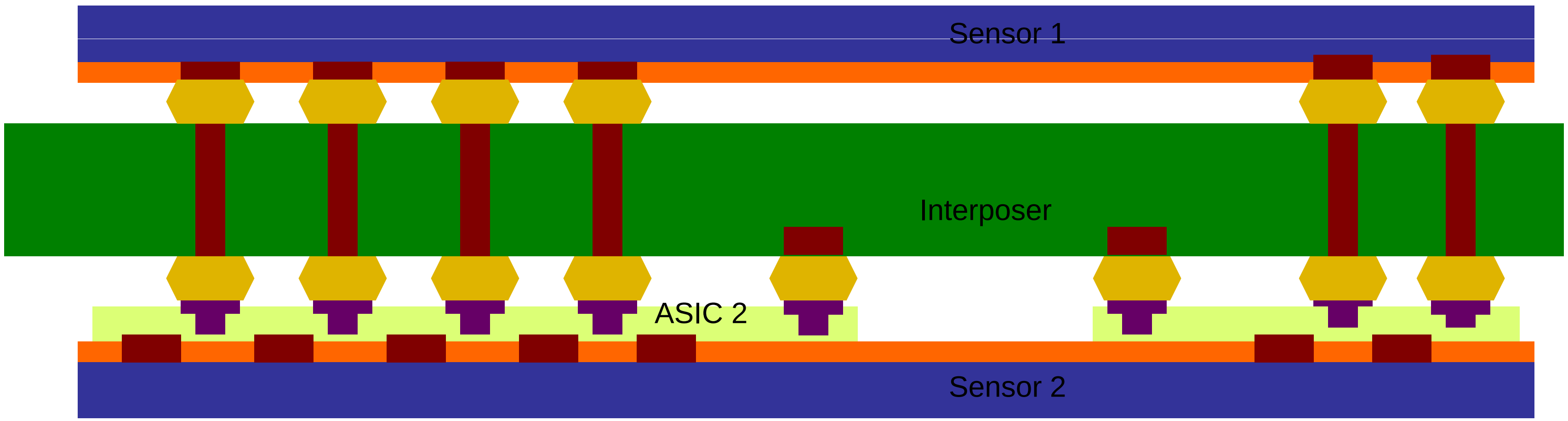


Options for The Stacked Module: 3D Vertically Integrated Module V2

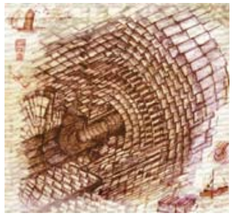
- **Only one chip layer, not two**
- **Signals brought directly where needed, at the Pixel level**
  - **Lowest power data transmission, simplest coincidence logic**

Challenges:

- **Requires Chip Through-Silicon-Vias (3D)**
- **Requires Direct Oxide Bonding to Large Area device**
- **Increased input capacitance? Shielding & cross-talk to sensor ?**



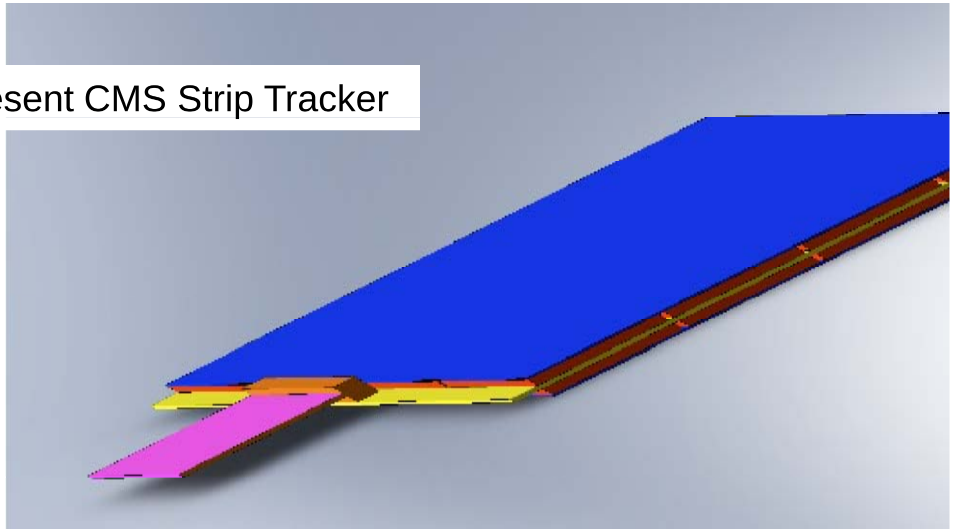
Marcello Mannelli
CERN ACES Workshop

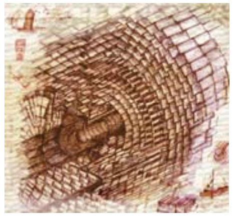


Straw Man Sensor Doublet Module: Vertically Integrated Hybrid Module

- **Example of Vertically Integrated Hybrid Module (~ 94 * 94mm^2)**
- **Assume Pixels ~ 100um * 1.5mm**
- **Estimate Module Power ~ 7W at R ~ 30cm, and ~ 3W for R > 50cm**
  - **Includes Data Transmission off-module**
  - **Estimate additional ~ 25% Power loss for DC-DC & Cables**
  - **Estimate 4 ~ 8 twisted pair cables for power (DC-DC close to module)**
  - **Estimate ~ 24 twisted pair cables each @ 1Gbps for data (L1 + Read-Out)**

Module Power 1.5 ~ 3 present CMS Strip Tracker





Making a computational challenge Manageable

- **Assembling Trigger Primitives from Tracks Stubs generated in Stacked Modules in different Tracker Layers is a potentially daunting task**
- **For L1 Trigger must take decisions at 40MHz, and satisfy stringent latency requirements**

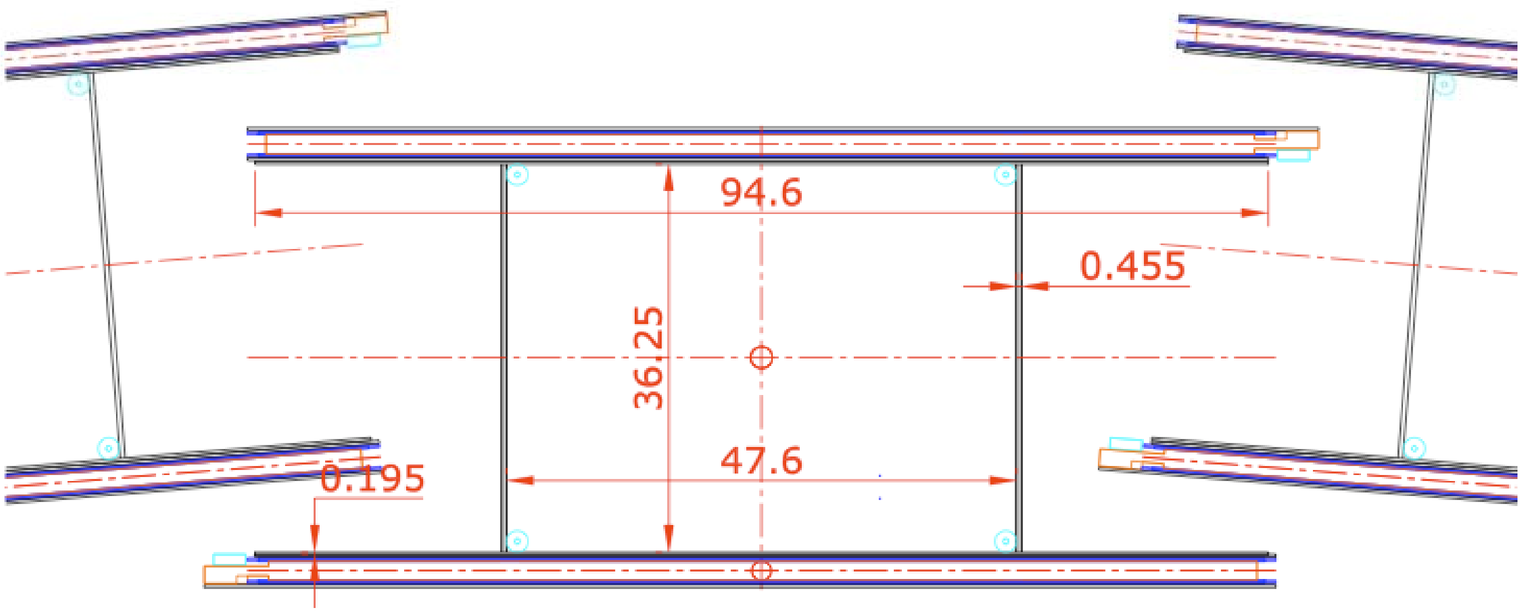
Need Simple, Robust, & Computationally Efficient approach

- **Break the problem in manageable chunks**
- **Process each chunk in parallel**

CMS SLHC Tracker
Straw Man Layout Illustrations

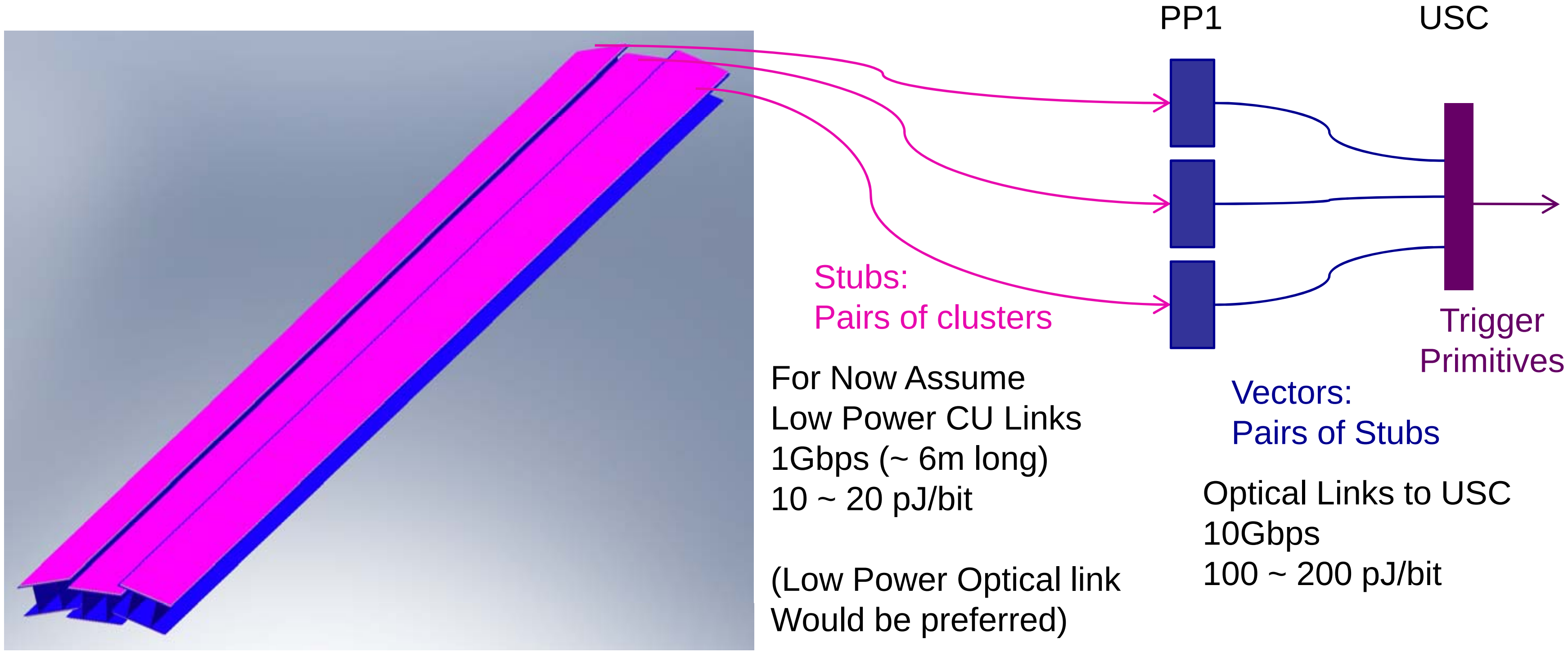
Arrange Modules R-Phi Hermitic Double Stacks:
Sufficient overlap to get all 4 hits in one r-phi secotr or in the neighbor

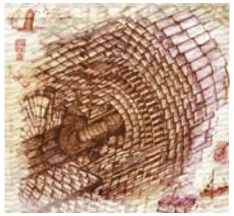
No communication across r-phi sectors



CMS SLHC Tracker
Straw Man Layout Illustrations

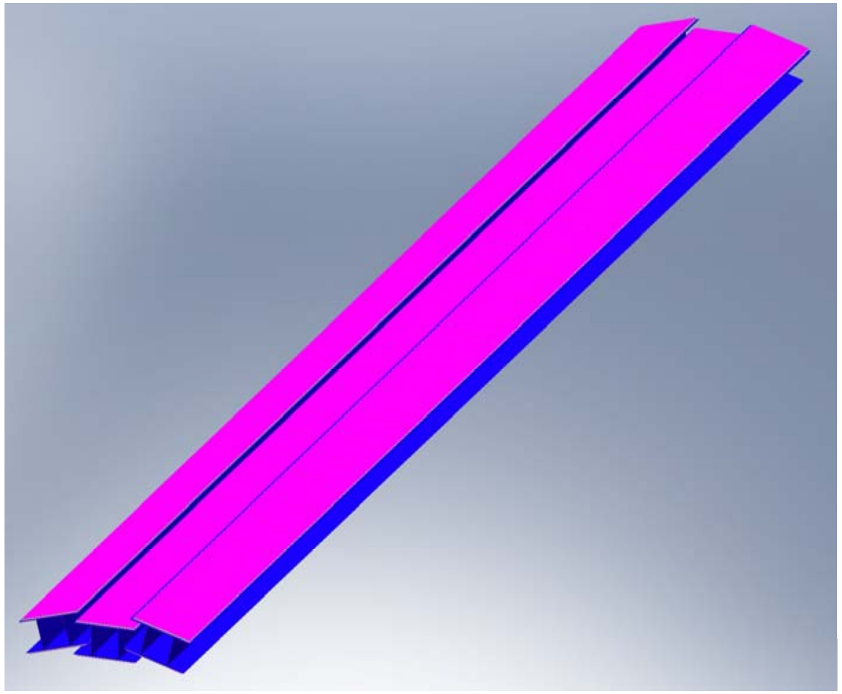
- **Modules are arranged on long ROD's or BEAMS, to form long barrels**
- **Bring all Track Stubs from a ROD or BEAM to a Trigger Board**
- **Process Track Stubs each of these in parallel to form Track Vectors**
- **At next level, resolve ambiguities, assemble Trigger Primitives**

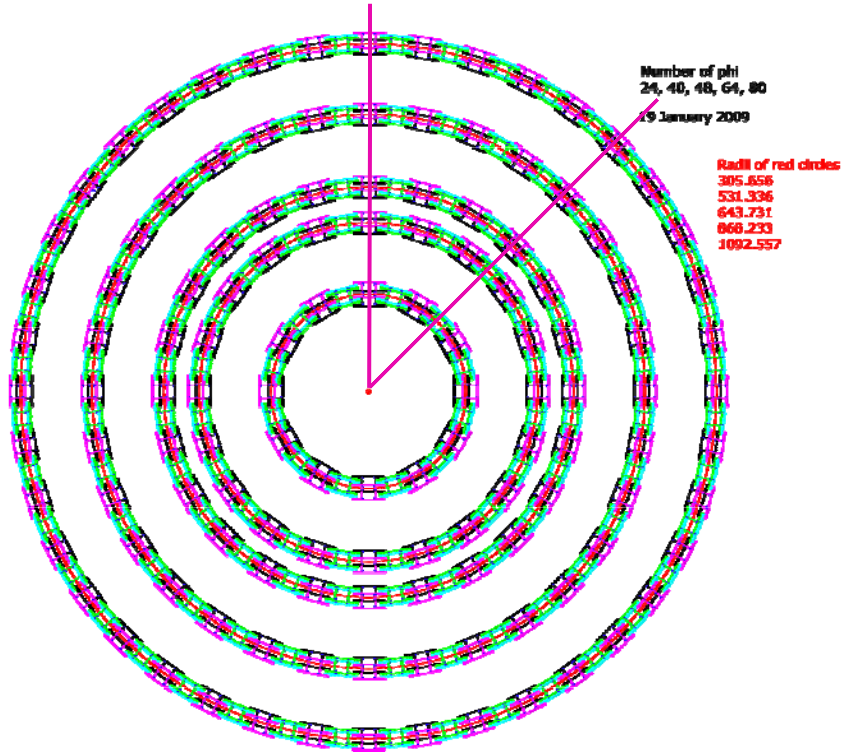


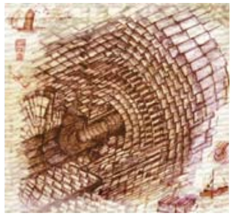


CMS SLHC Tracker
Straw Man Layout Illustrations

- **Projective Layout in r-phi may be useful**
  - May simplify Assembly of Trigger Primitives, by parallelizing
  - May simplify organization of Services
- **Straw Man B has an octant-wise r-phi projective layout**

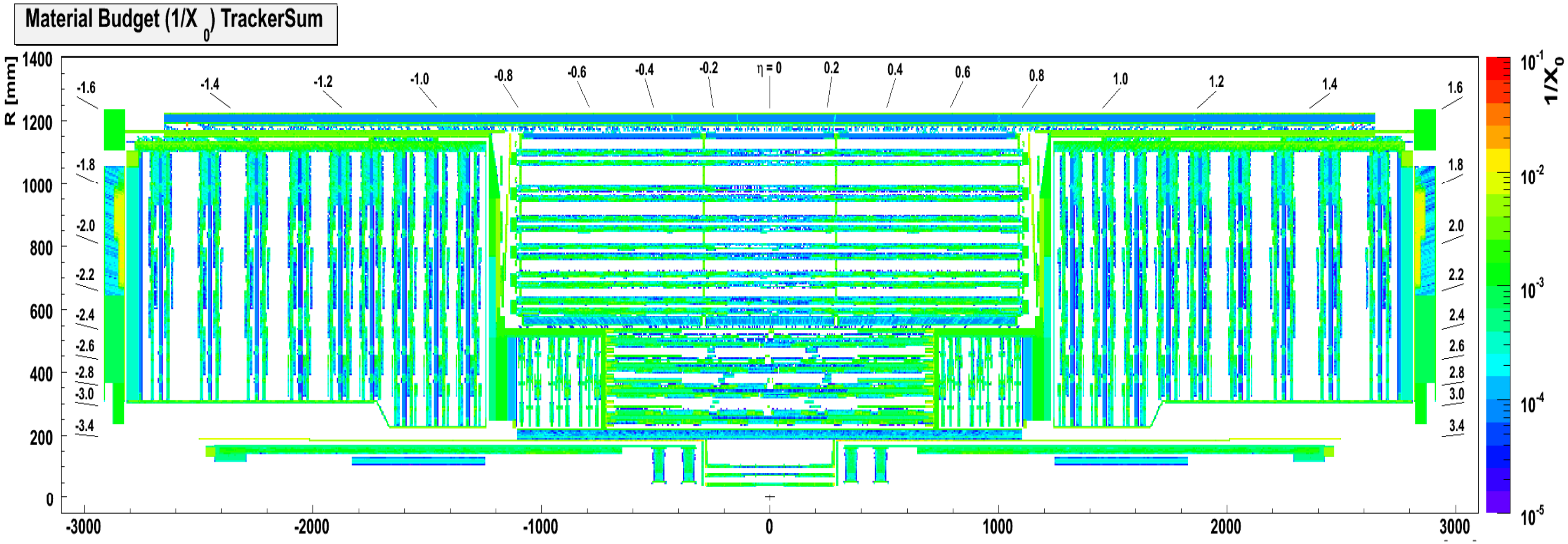


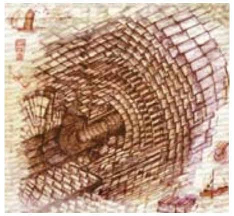




The Dark Side: Material Budget inside the Tracking Volume

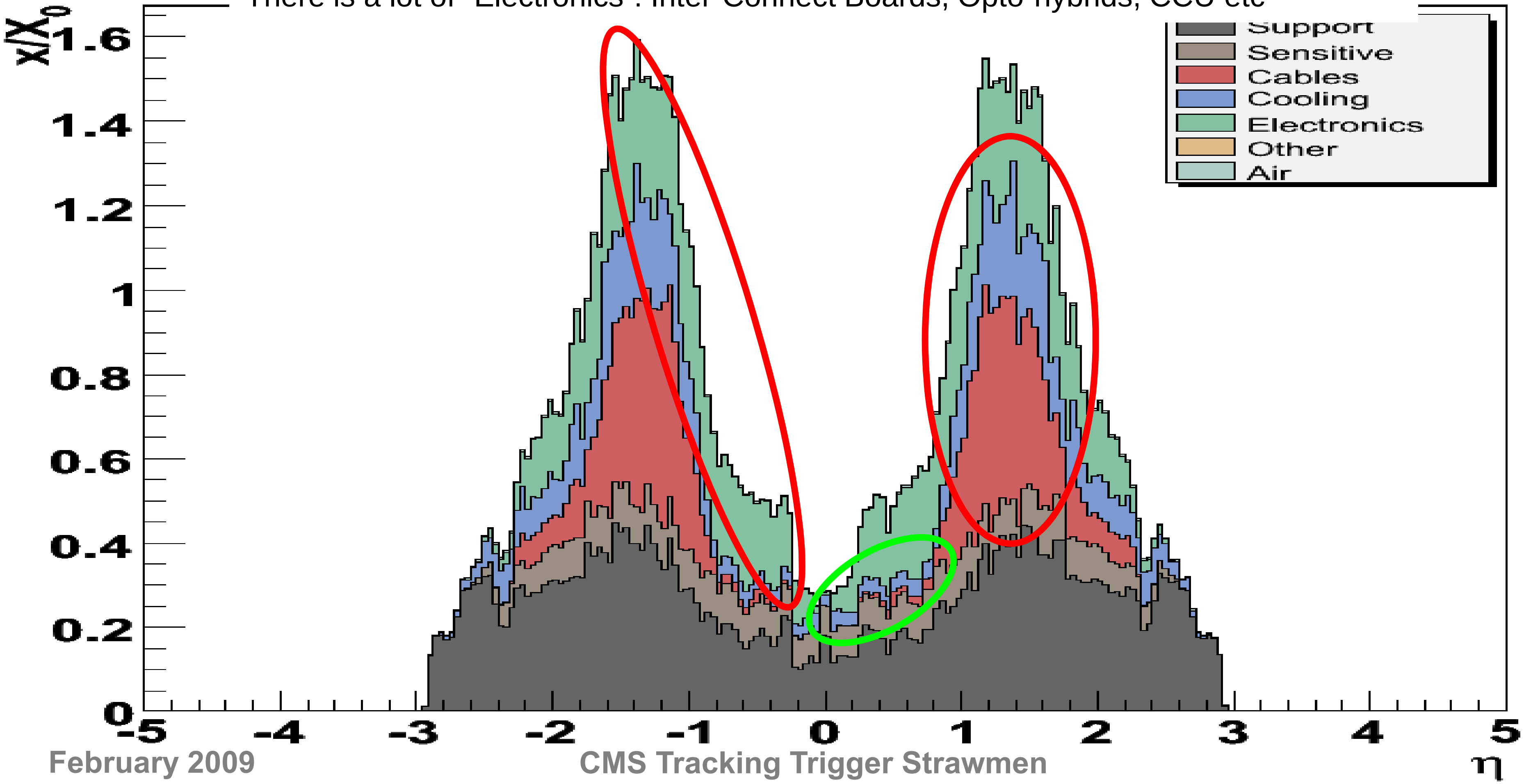
In the present Tracker, pipes & cable are actually relatively light within Barrels
They blow up when exit barrels: connectors, manifolds, light-heavy transition, routing

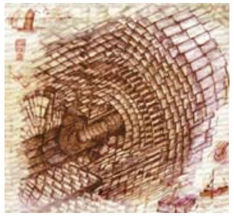




The Dark Side: Material Budget inside the Tracking Volume

In the present Tracker, pipes & cable are actually relatively light within Barrels
They blow up when exit barrels: connectors, manifolds, light-heavy transition, routing
There is a lot of "Electronics": Inter-Connect Boards, Opto-hybrids, CCU etc

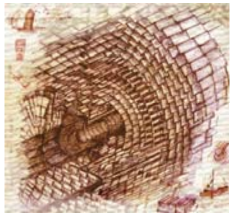




The Dark Side:
Material Budget inside the Tracking Volume

- **Long Barrels provide opportunity to substantially reduce material by removing transition regions to the bulkheads**
  - Expect extended low mass central region
- **Long Barrels are at a disadvantage at large η**
  - Geometric penalty for long barrels at η of 2.5 ~ 1 / $\tan\theta$ ~ 5
  - In addition, at high η accumulate services (cables) for all modules along barrel

- **Optimize Mechanics (BEAMS) and Cooling (CO_2)**
- **Minimize cable cross-section using DC-DC power distribution**
  - Use thin Cu clad Al core twisted pair cables for power, data & control
  - Serial Power is fall-back option
- **Minimize off module electronics / interconnect boards**
  - Aim to eliminate all but DC-DC boards, close to module



Summary and Conclusions

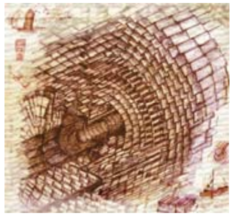
The CMS Tracker Upgrade for the SLHC is aimed at:

- **Improving on the present Tracking Performance for the SLHC**
  - **Improved granularity and reduced material budget**
- **Integrating an Effective and Robust L1 Tracking Trigger**
  - **Local Data Reduction and Stub / Track Vector Generation**
  - **Very fine Granularity (1 ~ 2mm long pixels) for Primary Vertex association**

These are challenging but well motivated goals:

- **A light, highly segmented Tracker with 3D tracking and L1 Triggering capability could be a game changing detector at the SLHC**

Backup Slides

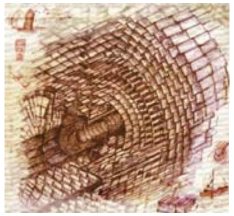


Some Numbers

- **Material Budget ~ Material / cm^2**
  - Consider rates and power / cm^2
  - Nb normalize to cm^2 of Silicon
  - 1 module = 2 sensitive layers = 2 * x*y cm^2 (eg 2 * $100cm^2$)

- **Present CMS Tracker Event Read-Out ~ 4 channels / cm^2 @ 100KHz**
  - Data Rate ~ 4MHz / cm^2 (analogue info ~ 10bits equivalent)

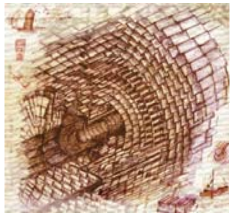
- **Present CMS Tracker Power Inside Volume ~ 33kW over ~ $210m^2$**
  - Power Density ~ 16mW /cm^2 inside Tracking volume
  - 6 Single-Sided + 4 Double-Sided = 14 Sensitive Layers



Data Transmission, Reduction, Power Density

In the following Assume

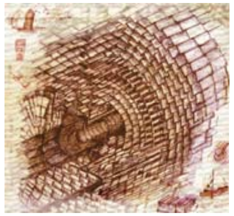
- **Pixel Dimension ~ 100um * 1mm**
  - 1’000 Pixels /cm^2
  - (more on this later)
- **~ 18 bits / L1 hit Address & Time Stamp info within Module**
  - Assume no analogue information for L1
- **~ 24 bits / L1 hit Address & Time Stamp info from Module**
- **32 bits / Read-Out hit info inside Tracker**
  - Assume ~ 8 bits analogue information for Read-Out
  - Nb if “Short Strips” ~ 32bit address field is reduced by ~ 5bits
    - ~ 20% reduction in Address Information for ~ 32 fewer channels / cm^2



Data Transmission, Reduction, Power Density

In the following Assume

- **Zero Suppressed Read-Out**
  - Data rates ~ driven by Occupancy, NOT by Channel Count
- **De-randomized Read-Out from Module to USC**
  - Available Bandwidth ~ Average Bandwidth, with * 2 safety margin
  - Non De-randomized within Module: Available Bandwidth ~ 10 * Average
- **Reduce Output Data Rates from Module by ~ 2 * 10**
  - 1 pair of accepted clusters = 1 datum per Hit Pair Output from Module
  - Accept ~ 1 / 10 Hit Pairs: Pt Threshold 1 ~ 2 GeV
- **Reduce Output Data Rates from ROD by ~ 5**
  - 2 accepted cluster pairs = 2 data per Track Vector Output from ROD
  - Accept ~ 1 / 5 Track Vectors: Pt Threshold ~ 2 GeV



Data Transmission, Reduction, Power Density

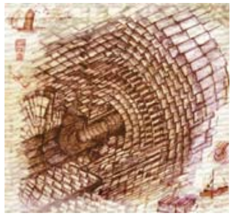
At R ~ 35cm

Based on 1 / 2*10 off Module * 1 / 5 off BEAM data rate reduction

- **Total Power Budget L1 & Read-Out Data Transmission @ R ~ 35cm**
  - Inside Tracking Volume: ~ 3 mW/cm^2
  - Compares with ~ 16mW /cm^2 inside present Strip Tracker volume
  - At Bulkhead: ~ 7 mW/cm^2 (L1 + Read-Out)

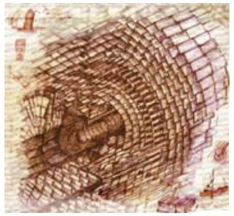
- **A L1 Track Trigger based on the scheme presented here is NOT ruled out by the Power requirements for the L1 Data Transfer**

- **Challenges for Data Transmission & Reduction include:**
  - Module interconnect technology
  - High rate (1Gb/s) Low Mass Link over length of BEAM to PP1
  - De-randomized L1 data transfer protocol
  - Hit Doublet (on Module) & Track Vector Logic (at PP1 at least for R ~ 35cm)



Front-End Power for “Long Pixel” Tracker

- **Power of present CMS Pixel ROC ~ 30uW / channel**
  - **100um * 150um Pixel, Power Density ~ 200mW / cm^2**
    - **Pixel Front-End Read-Out chip Power Density ~ 16 * Strips**
    - **Pixel Channel Density ~ 1’500 * Strips !**
- **Best estimate for SLHC in the range of 25 ~ 60uW / channel for 100um * 1 ~ 2mm Long Pixels**
  - **Depending or Radius (hit rate) and logic complexity**
- **Results in 20 ~ 50mW / cm^2**
  - **Includes ~ 3mW/cm^2 for Data Transmission inside TK Volume**
  - **Includes 25% Power dissipation in DC-DC + Cables**
  - **Compares with ~ 16mW /cm^2 inside present Strip Tracker volume**
  - **Long Pixel Channel Density 100 ~ 200 * Strips**
- **Long Pixels not ruled out by Front-End Power requirements**



Straw Man B
Material Budget inside Tracking Volume: First Preliminary Indications

Preliminary Straw Man Material Budget indications based on initial set of assumptions
Supports the potential advantage of long barrels for an extended "clean" central region: look forward to improved estimates