Versatile Link Project Status

F. Vasey on behalf of the project steering board

With input from C. Issever J. Troska J. Ye A. Prosser

Some Lessons learned from LHC

https://edms.cern.ch/document/882775/3.8

System

...

- Avoid use of single fibres and pigtails on detector
- Do not allow excessive fibre-slack without corresponding management scheme.
- Use ruggedized ribbon/fiber only.

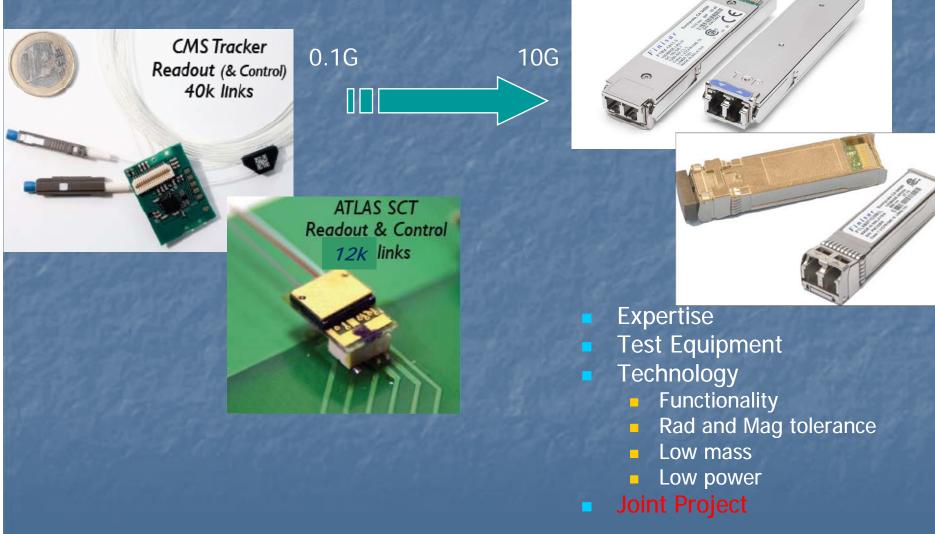
QA

...

Develop and distribute tools which allow prototyping and testing

Concept for SLHC: Pluggable Transceiver with electrical and optical connections Customized for HEP environment Standard for test systems and off detector

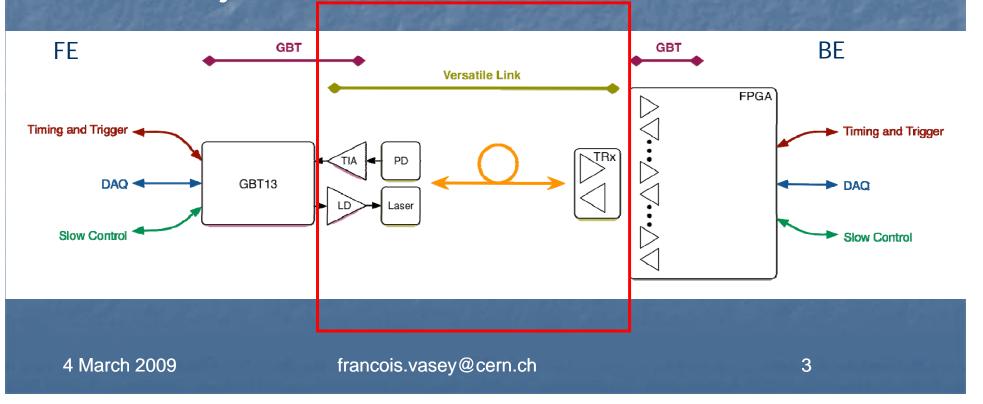
LHC > SLHC Migration Path



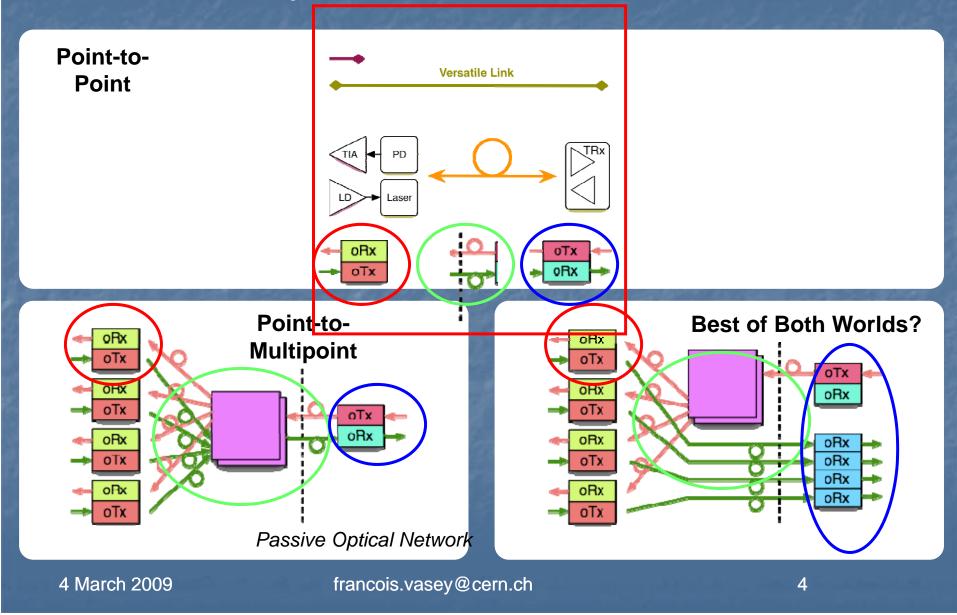
Versatile Link Project Description

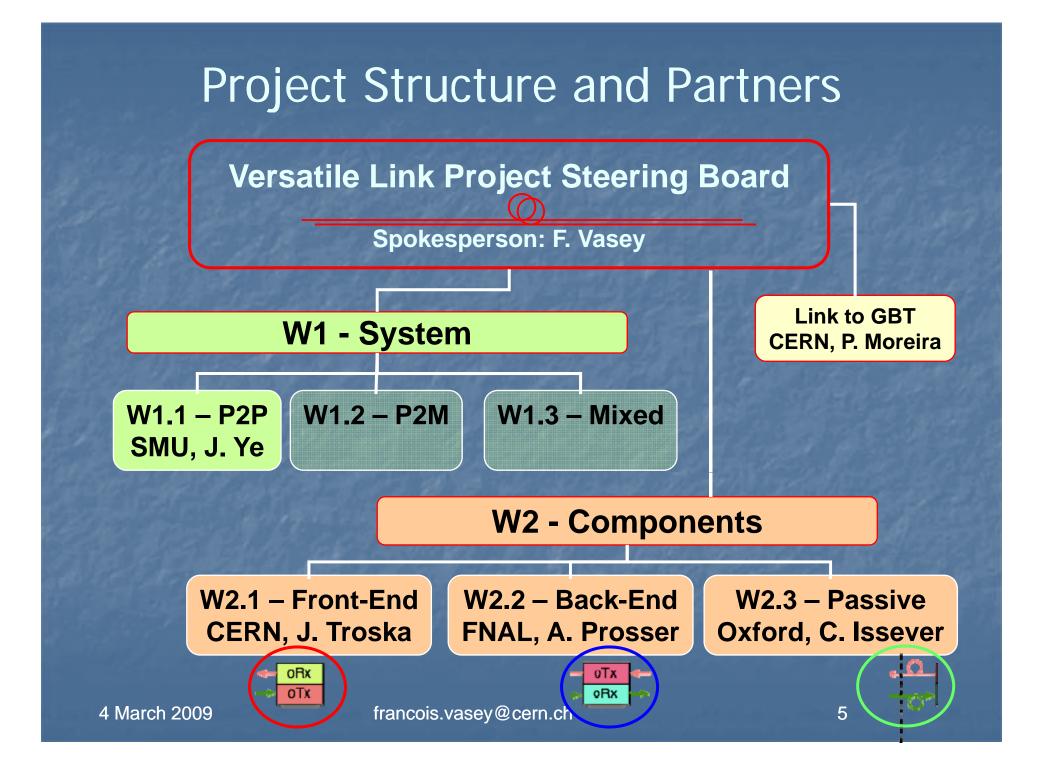
- Optical Physical layer linking front- to back-end
 Bidirectional, ~5Gbps
 - Versatile
 - Multimode (850nm) and Singlemode (1310nm) versions
 - Point to Point and Point to Multipoint architectures

Joint Project



Optical Link Architectures





The Versatile Link Project

- Project proposal submitted to ATLAS and CMS SLHC upgrade steering groups in Nov07
- Project endorsed by ATLAS and CMS in early 2008
- Kick-off Meeting 10 Apr 2008
 - phase 1 proof of concept based on tentative specifications, partial tests and early prototypes
 - duration: 18 months, till 30 Sep 09
 - Phase 2: feasibility demonstration based on complete specifications and exhaustive tests on final prototypes
 - Oct 09 Apr11
 - Phase 3: pre-production readiness based on frozen specifications, and completed technical-commercial actions
 - Apr11 Oct12

The Versatile Link Project

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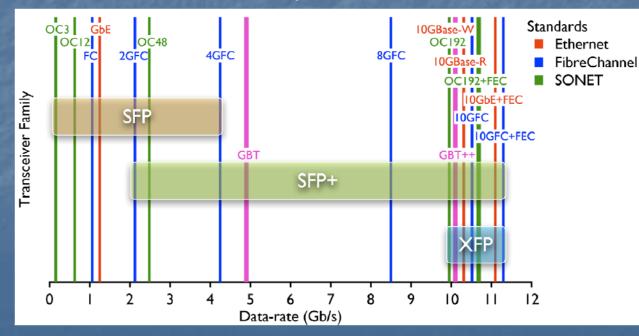
Concept for SLHC:

Pluggable Transceiver with electrical and optical connections Customized for HEP environment Standard for test systems and off detector

WP2.1 Front end components: Versatile TransceiverWP2.3 Passive componentsWP2.2 Back end componentsWP1.1 System

WP2.1 Versatile Transceiver VTRx

- Bi-directional Module with connector interface
- Based upon an acknowledged standard
- Work with Industrial partner early-on
- Low Mass & Volume
- Minimize material, avoid metals
- Non-magnetic, capable of operating in a magnetic field
 - Requires replacement of ferrite bead used in laser bias network
- MM 850nm & SM 1310nm versions
- Bitrate determined by ASICs: 5 10 Gbps

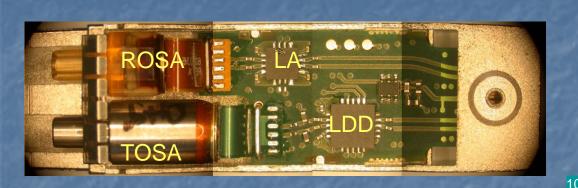


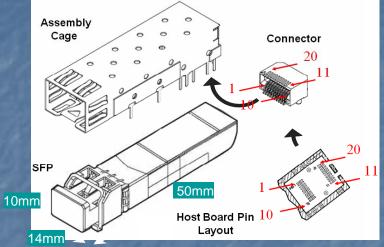


J. Troska



WP 2.1 VTRx packaging: SFP+





ASICs

- Laser Driver (LDD) GBLD
- TIA GBTIA
- LA not foreseen (inc. in GBTIA)
- No microcontroller
- TOSA Rad Hard Laser
- ROSA Rad Hard PIN + GBTIA
- Keep Std. Host board connector
- Remove material from std. SFP+ housing
 - Must test EMI tolerance and emission
- No cage at FE, alternate fixing T.B.D.
- Thermal impedance

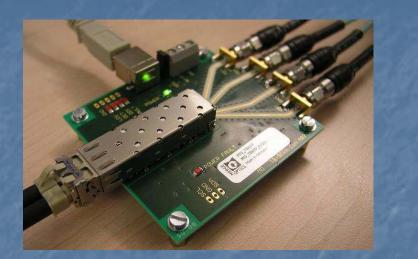
GBTIA and GBLD designed and produced

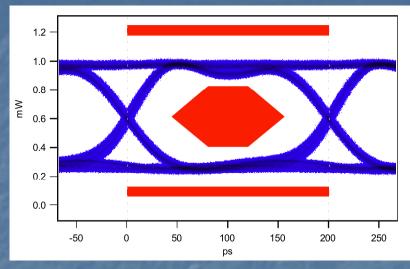
TOSAs and ROSAs under evaluation

Stripped TRx prototype being ordered

4 March 2009

WP 2.1 VTRx and TOSA Functionality Testing





Automated Testing

- BER measured with FPGA-based BERT with TRx in loopback
- Power consumption measured in loopback configuration
- Figure of merit proposed to compare different devices
- Standard method for providing bias to laser diode uses a network based on inductors
- Magnetic field tolerance not guaranteed due to saturation of commonly used core materials
- Custom design based on ceramic-core inductors proven to have excellent functionality at target bit-rate
- Evaluation of laser diode transfer characteristics started
- Enables correct matching of Laser Driver to Laser
- Provides key ingredient for Laser Driver design and functional simulation

For details, see TWEPP08 Paper:

http://indico.cern.ch/contributionDisplay.py?contribId=59&sessionId=12&confId=21985

4 March 2009

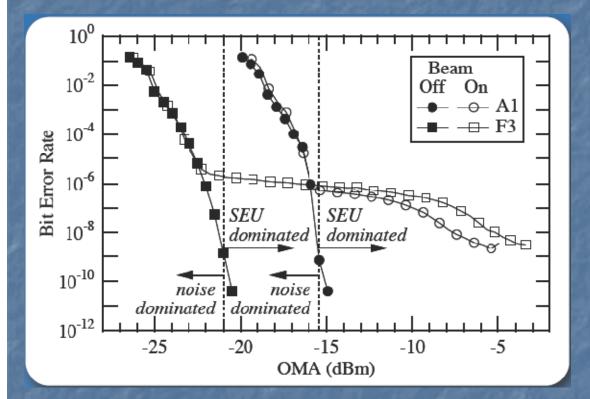
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WP 2.1 Radiation Testing

- VTRx laser and pin need to be tested for total dose, total fluence, SEU resistance
- Optical System Irradiation Guidelines established by opto WG
- https://edms.cern.ch/document/882783/2.6
- Some data available from total fluence tests to SLHC levels, but none from SEU tests at Gbps bit rates
- Error Correction scheme (FEC) to be selected depends on typical SEU error pattern
- SEU test carried out at PSI in December 2007, analysis of results presented at RADECS & TWEPP 2008.
- Total fluence tests planed for mid-2009
- Selection of candidate devices at 1310nm and 850nm ongoing

WP 2.1 Dec 07 SEU Irradiation Test Results

63MeV protons, 8x10⁸ p/cm²/s



Trend

- Several orders of magnitude difference in response between devices smallest device performs best
- ROSA (square symbols) not much worse than bare PINs
- BER independent of Datarate for bare PINs
- At least in 1-2.5Gbps range
- Burst Errors observed
 - max. 10-bits long in PINs
 - max. 00's bits long in ROSAs
 - Error correction and SEU mitigation mandatory

4 March 2009

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For details, see TWEPP08 Paper: http://indico.cern.ch/contributionDisplay.py?contribId=88&sessionId=12&confId=21985

WP2.3 Passive Components



Phase 1 program:

- Irradiation testing
- Mechanical testing (reliability)
- Environmental testing

Components

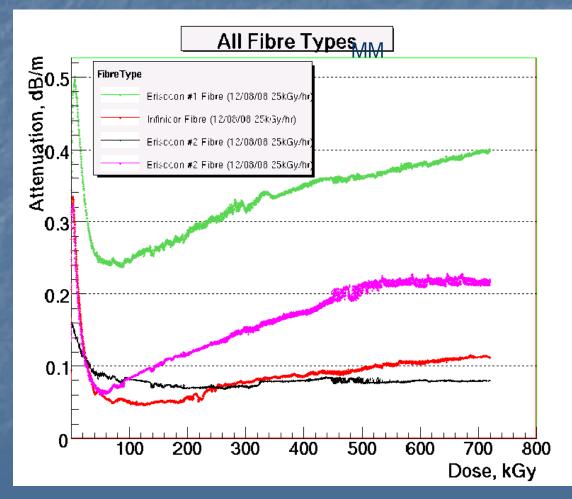
- Fibers
- Cables
- Connectors
- Splitters
- Mux
- Legacy fiber, connectors, patch-panels

WP2.3 Passive Components: total dose irradiation tests (MM)

Status:

Gamma irradiation test carried out to 700 kGy

- 4 MM fibres @ 850nm
- MM fused taper splitter
- SM LC-LC connectors
- Good first results obtained, identified 2 MM candidates
- Results paper in preparation



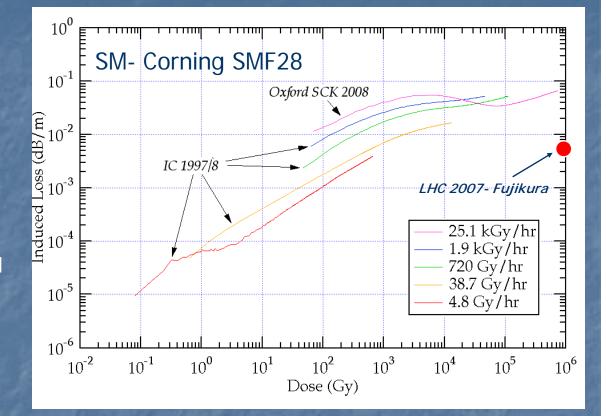
WP2.3 Passive Components: total dose irradiation tests (SM)

Status:

Gamma irradiation test carried out to 700 kGy

- 1 SM fibre @ 1310nm (SMF28)
- SM PLCC splitter
- SM LC-LC connectors

 Results paper in preparation
 Mechanical stress tests started with SMF28 fibre
 LHC-machine fiber irradiated to 1MGy: 5e⁻³ dB/m



Plans for 2009:

Continue market surveys for fibres and splitters Prepare next gamma radiation test:

Fibres at low and high dose rates, low temperature

Splitters to be measured before and after irrad

Setup environmental tests for fibres, splitters and connectors

Continue mechanical tests, also with irradiated fibres and connectors

4 March 2009

WP2.2 Back-end Components

Phase 1 program:

- Identification of 10Gbps components including:
 - Point to point transceivers
 - Passive Optical Network transceivers
 - Array transmitters and receivers
 - High power transmitters
- Testing Operations
 - Configure a test lab at Fermilab
 - Carry out initial tests on selected components
 - Report on results and procedures

Status:

- First 6 Samples of Transceiver Components received
- Automated testing started
- Bit-Error-Rate/sensitivity tests carried out based on Myrinet 10G NICs

Plans:

- Progress Test Automation (Labview, LXI, C++)
- Carry Out Eye Pattern Measurement Tests
- Implement BER test based on FPGA tester
- Test more samples









WP1.1 System

phase 1 workprogram:

- Development of P2P demonstrator based on commercial transceivers.
- Development of test bench(es) for components and systems
- Development of test procedures.

Status:

J. Ye Southern Methodist University

oTx

oRx

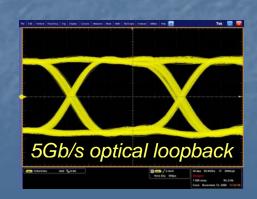
oRx

- SFP+ carrier board has been designed and fabricated. With a locp otx back (oTx to oRx via fiber) configuration, a 10 Gbps optical serial link has been demonstrated with AFBR-700SDZ (10Gb, 850 nm)
- Equipment is in place for 10 Gbps tests:
 - 12Gbps BERT.
 - 20GHz real-time scope with 8GHz differential probe.
 - O/E module with 12GHz bandwidth.
 - Sampling scope with 10GHz optical, 50 GHz electrical input modules.
- New collaborator (IPAS) participates to this work package.

Plans:

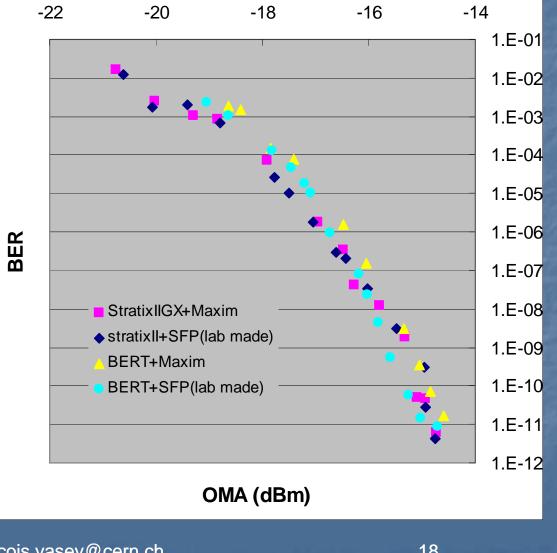
- With equipment in lab, and commercial transceivers, a full P2P 10 Gbps link will be demonstrated.
- With Stratix II GX programmed as the BERT (signal generator and bit error rate checker), a portable 6 Gbps test bench will be developed and supplied to project partners.
- Tests will be carried out with the 12 Gbps BERT and with Stratix II GX based test bench. Testing procedures will be studied and defined through this process.





WP1.1 BER comparison

Comparison of 5G BER tests performed with: lab BER tester FPGA tester



Summary

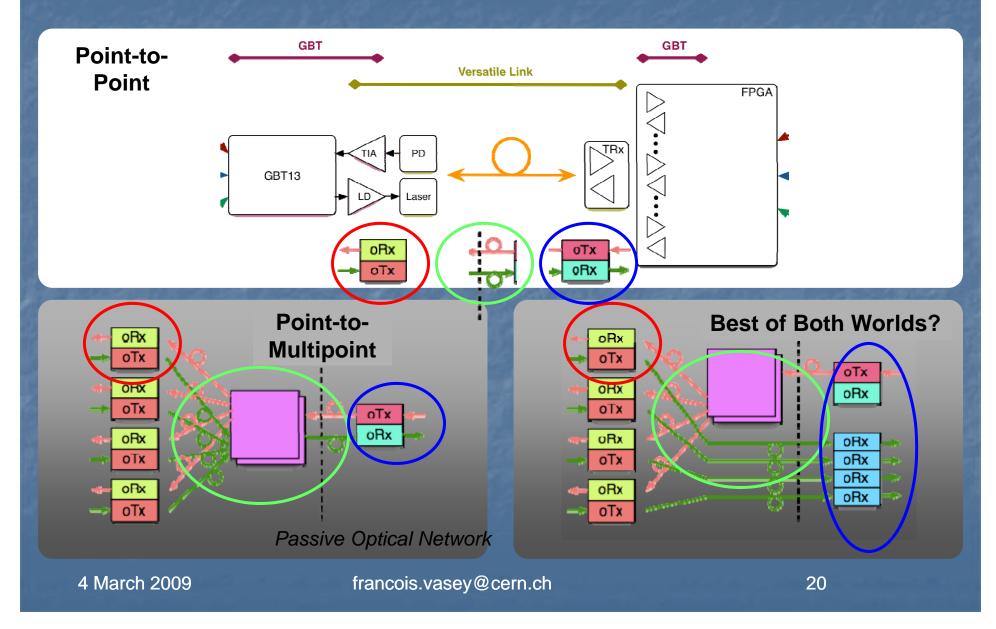
- Versatile Link aims to develop a bi-directional optical physical layer to link SLHC front- and back-ends
- Target Speed is 5Gb/s (depends largely on the user-specified chipset)
- Work being carried out both at the system and component level
- Collaboration between: CERN, Fermilab, Oxford, SMU
- MM (850nm) and SM (1310nm) variants will be proposed
- Multiple Point-to-Point and Point-to-Multipoint will be supported

Good progress has been shown in all areas:

- Proof of concept will be demonstrated at TWEPP-09
 - a tentative specification based on past experience
 - a non-exhaustive portfolio of components meeting (even partially) the tentative specification (SM and MM, P2P)
 - a front end TRx prototype package
 - test bench(es) for components and systems
 - preliminary irradiation test results
 - preliminary functionality test results for components and systems
 - a set of recommendations for phase 2.
- feasibility demonstration: Oct 09 Apr11
- pre-production readiness: Apr11-Oct12

Yearly project progress review in Oxford on 5 and 6 March 2009

Optical Link Architectures



Credits

CERN

Jan Troska, Luis Amaral, Stefanos Dris, Alberto Jimenez Pacheco, Christophe Sigaud, Sergio Silva, Csaba Soos, Pavel Stejskal, François Vasey

Fermilab

- Alan Prosser, Mark Bowden, John Chramowicz
- Oxford, IPAS, CERN
 - Cigdem Issever, K. Dunn, Alex Gerardin, Todd Huffman, S.C. Lee, Z. Liang, Z. Meng, A. Povey, Tony Weidberg
- Southern Methodist University
 - Jingbo Ye, Andie Liu, Kent Liu, Annie Xiang