TOFFEE

a fully custom amplifier-comparator chip for timing applications with silicon detectors

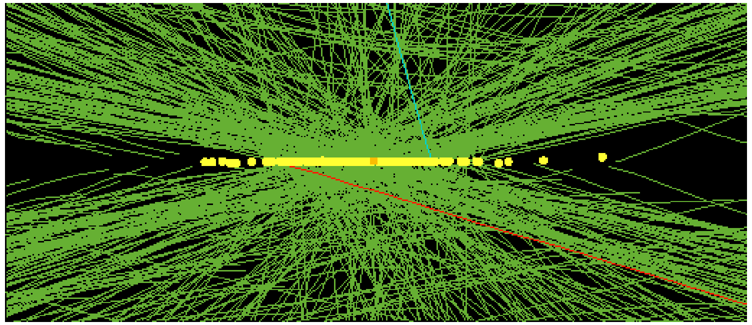
Francesca Cenna

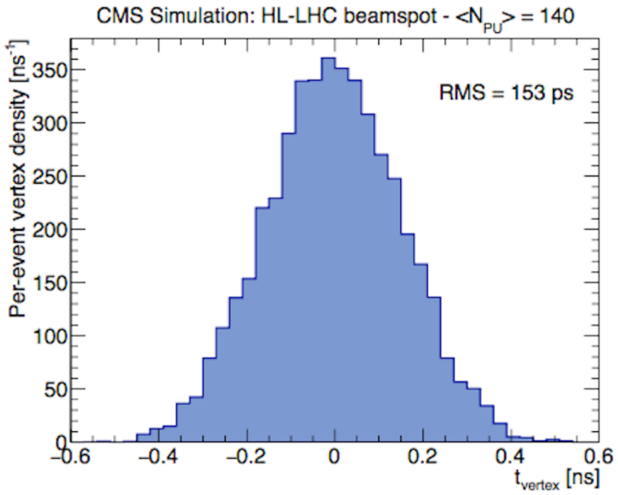
N. Cartiglia, A. Di Francesco, J. Olave, M. Da Rocha Rolo, A. Rivetti, J. Varela

Why TOFFEE

TOFFEE rises from the need to read out **silicon detectors designed for timing**

Time-tagging will be a major concern in the future HL-LHC environment:





- **150-200 events/bunch crossing**
- **Time RMS between vertexes ~ 150 ps**, according to CMS simulations

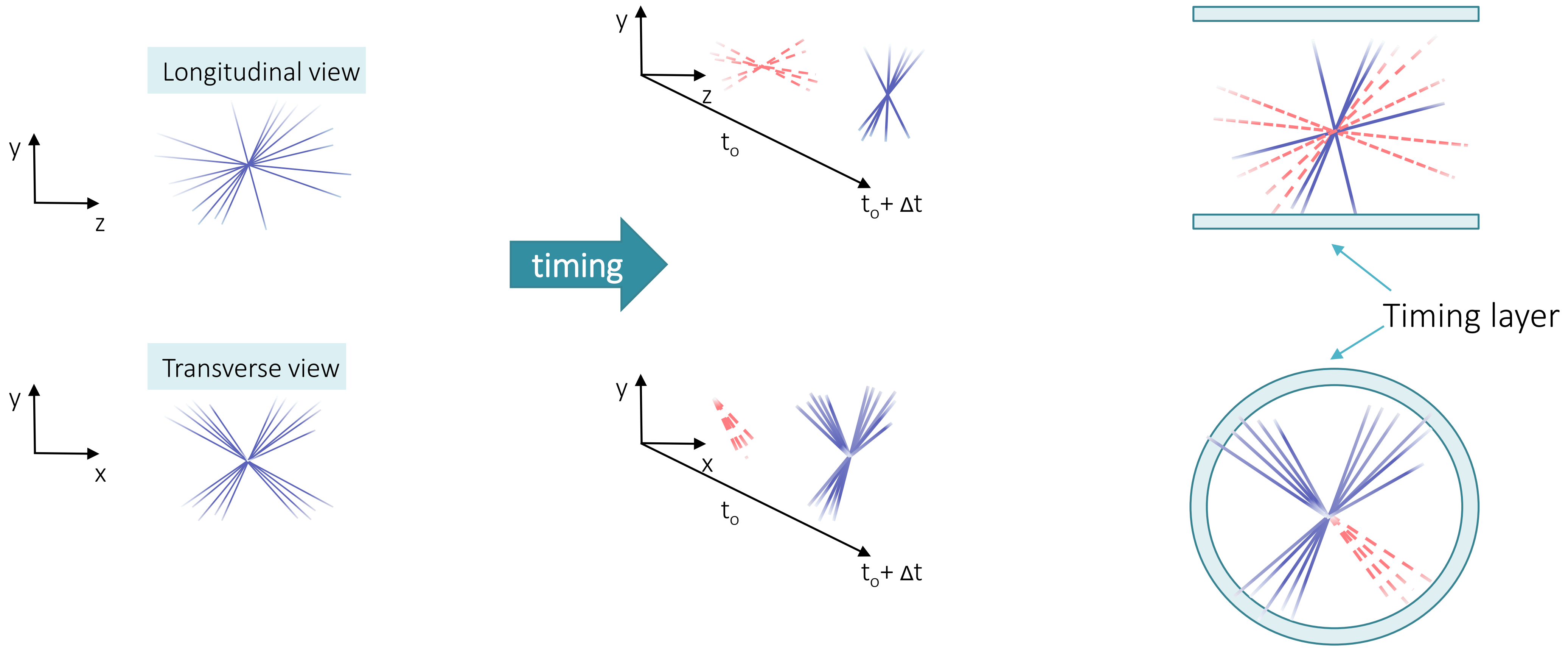
reconstruction of time information allows to **distinguish different overlapping events**

The «z by timing» coordinate will be calculated according to $\Delta z = c\,\Delta(t_1 - t_2)/2$

➡ **We plan to reconstruct the time information with σ_t ~20 ps**
i.e. z position with an accuracy of ~ 4 mm

Timing in event reconstruction

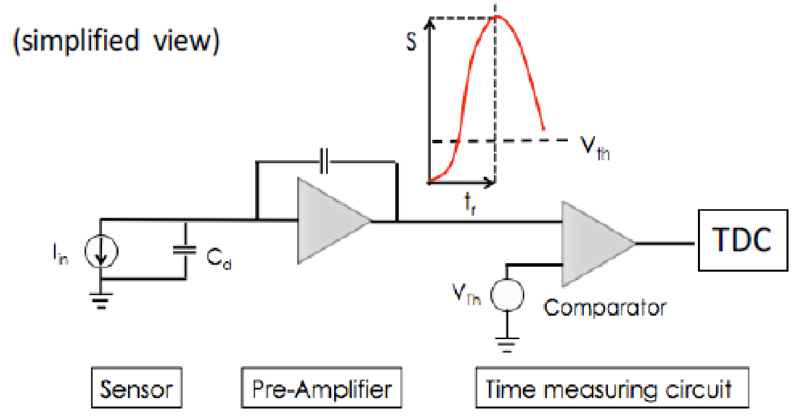
Timing allows to resolve different events otherwise undistinguishable by adding an extra dimension



Time resolution

Time is set when the signal crosses the comparator threshold

The timing capabilities are determined by the characteristics of the signal at the output of the preamplifier and by the TDC binning.



$$\sigma_t^2 = \left(\frac{N}{\frac{dV}{dt}}\right)^2 + \left(\frac{\delta_{Bin}}{\sqrt{12}}\right)^2 + \sigma_{Time\ Walk}^2$$

Noise and steepness of the signal

TDC contribution

Sensor signal shape variations due to non homogeneous energy deposition (Landau fluctuations)
main contribution to jitter

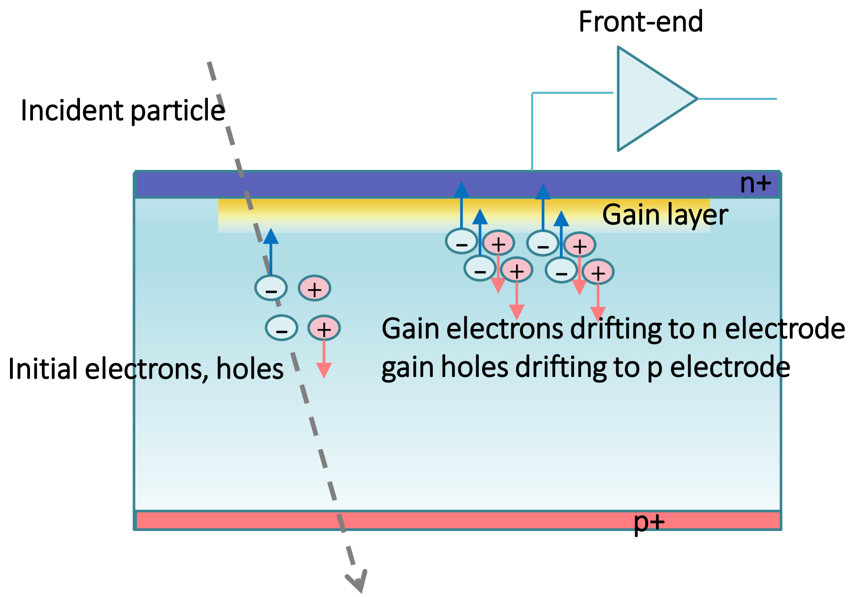
Required:
- Noise minimization
- Large and uniform signals
- Short rise time

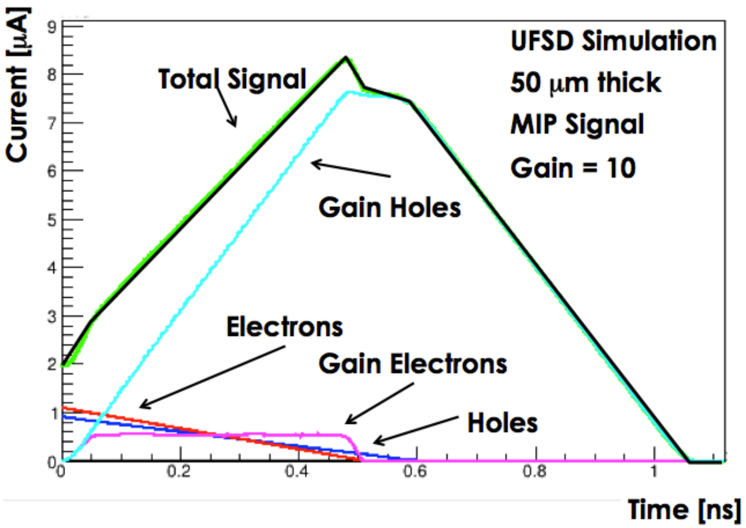
FAST SENSOR + FAST READOUT!

Ultra Fast Silicon Detectors

UFSD have been studied to reconstruct the **"time coordinate"** with a silicon detector

- They have a particular signal shape due to **charge multiplication**
- Electrons multiply when crossing a **high electric field layer** (gain layer) generating **additional electrons and holes** (holes multiplication is negligible)
- The main part of the signal is **produced by gain holes** drifting to p electrode
- UFSD have **low gain** (~ 10): low shot noise, milder electric fields, possible electrode segmentation, behavior similar to standard silicon detectors





UFSD – slew rate and thickness

The shape of the signal depends on the sensor thickness:

- **Amplitude** depends on the **gain value**
- **Length** depends on sensor **thickness**

For a fixed gain:

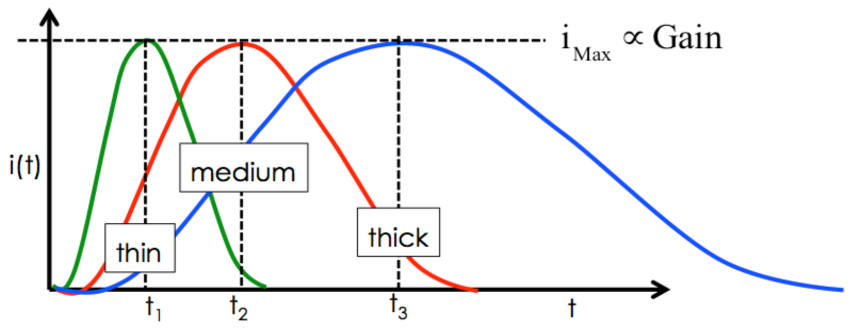
- Amplitude = constant
- Rise time decreases ~ 1/thickness

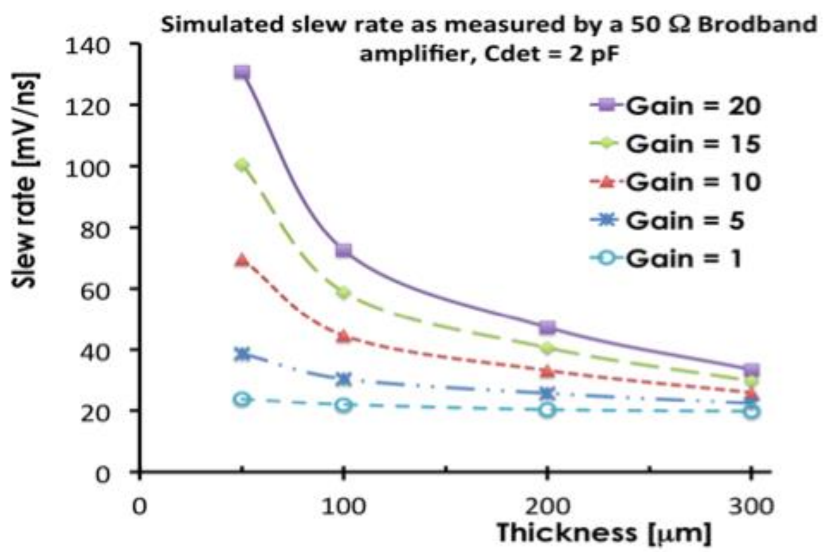
Slew rate:

- Increases with gain
- Increases ~ 1/thickness

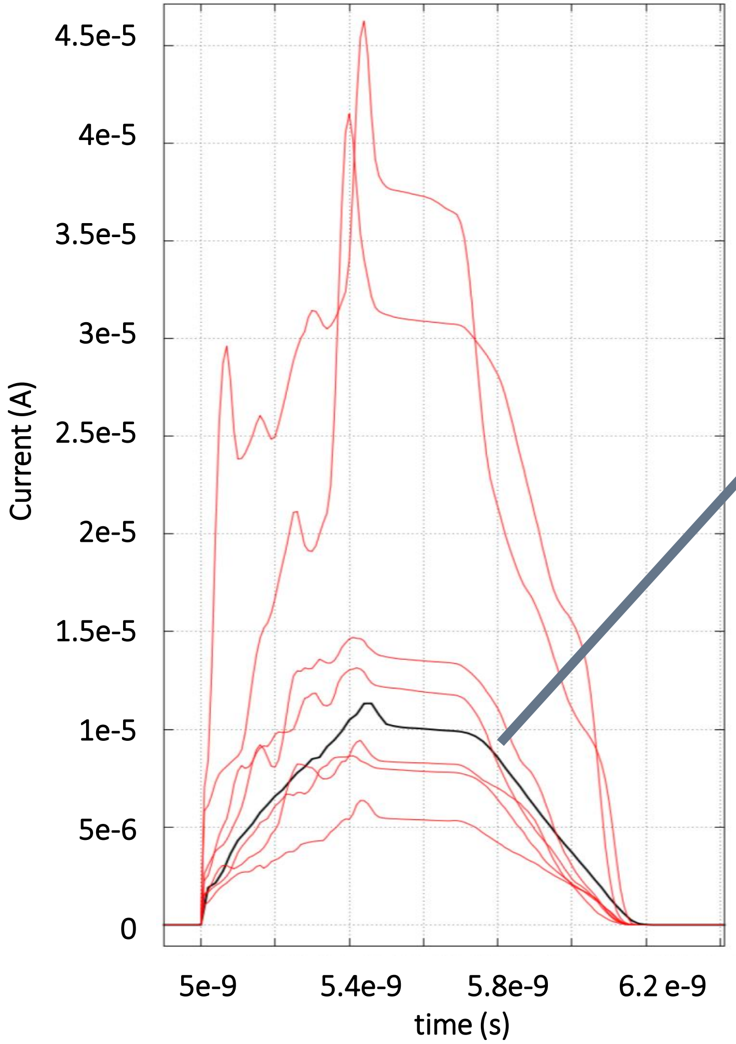
➡ The key for a fast sensor is then:

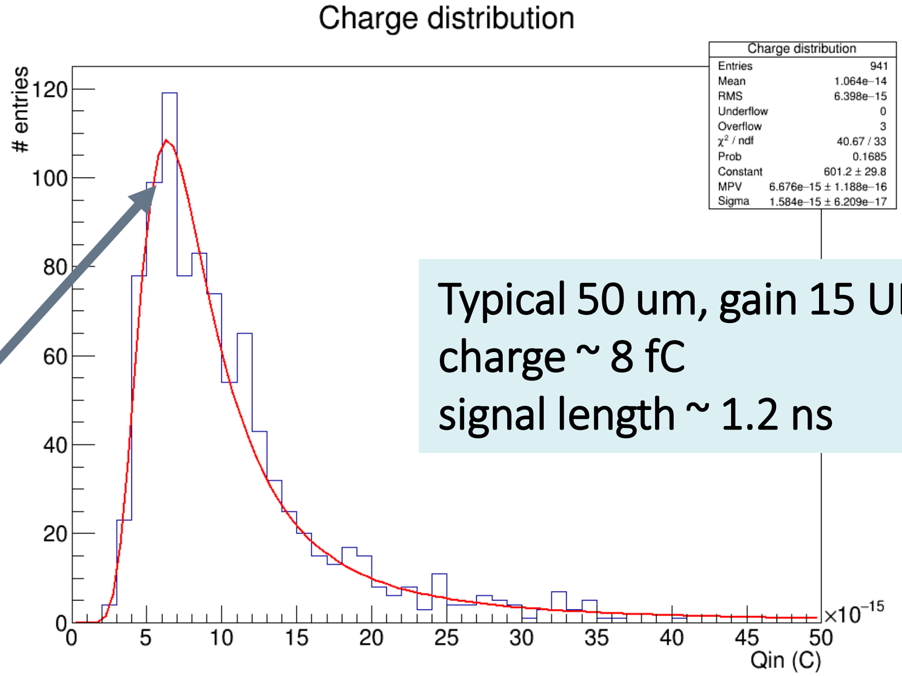
- thin bulk
- charge multiplication





50 um UFSD signals





Typical 50 um, gain 15 UFSD MIP signal
charge ~ 8 fC
signal length ~ 1.2 ns

We have a fast sensor providing steep signals

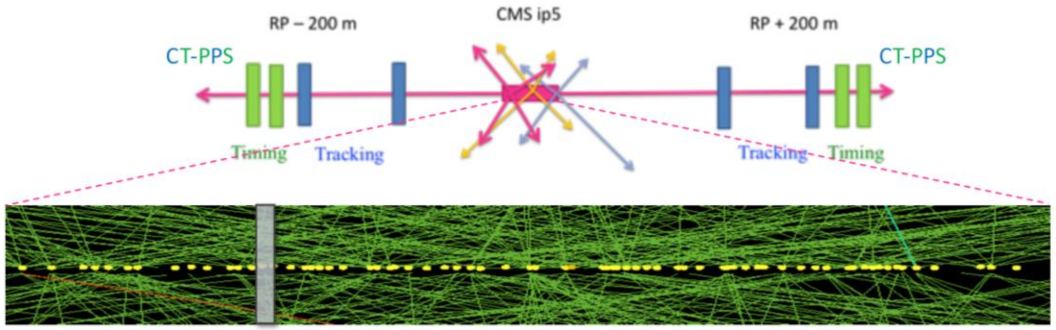
➡ we need a fast readout electronics to reach the best time resolution!

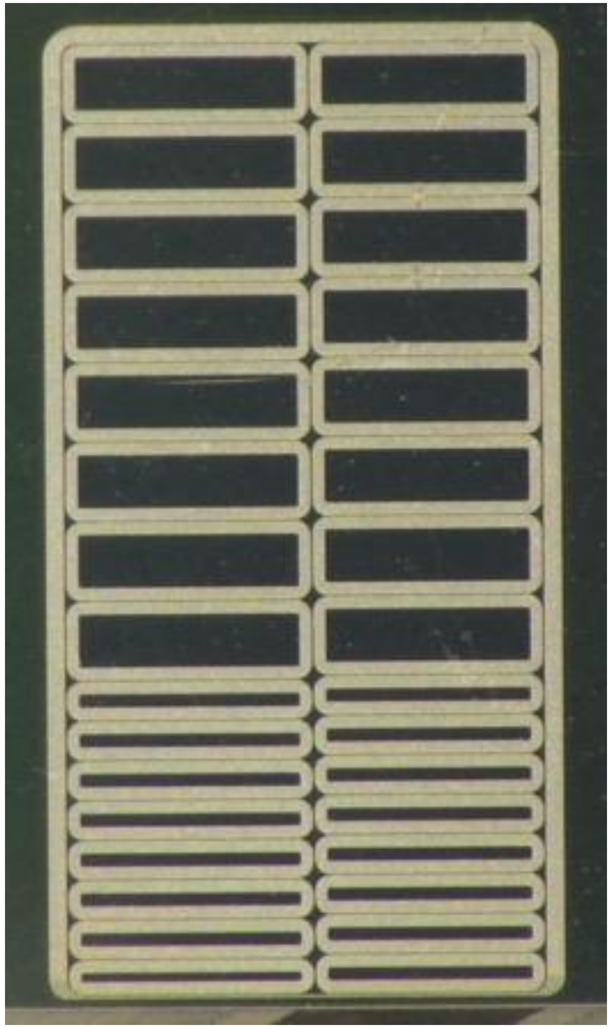
The sensor – CT-PPS

This UFSD is specifically designed for **CMS-Totem Precision Proton Spectrometer** and produced by CNM

- 50 um thick
- Gain ~ 15
- 32 fat strip array:
  - 16 thinner 3 mm x 0.5 mm (closer to beam line),
  - 16 thicker 3 mm x 1 mm
- 50 um dead space between pads
- C_{det} = 6 pF (thinner strips), 12 pF (thicker strips). Only geometry dependent

The signal from each pad will be detected by a **DC-coupled front-end** mounted close to the detector module inside PPS roman pot (RP)





12 mm

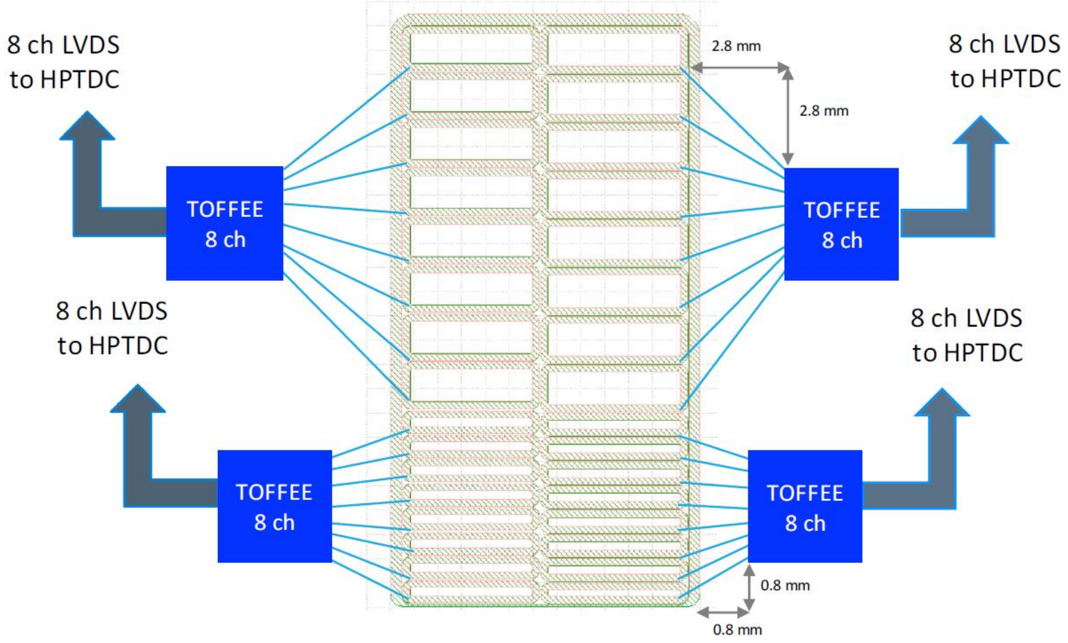
6 mm

TOFFEE - overview

TOFFEE is designed in UMC 110 nm CMOS technology.

The ASIC has 8 channels, each channel consists of:

- Amplifier
- Single threshold discriminator
- Delay line to stretch discriminator output: High Precision TDC (HPTDC) reads pulses wider than 10ns
- LVDS driver for HPTDC connection

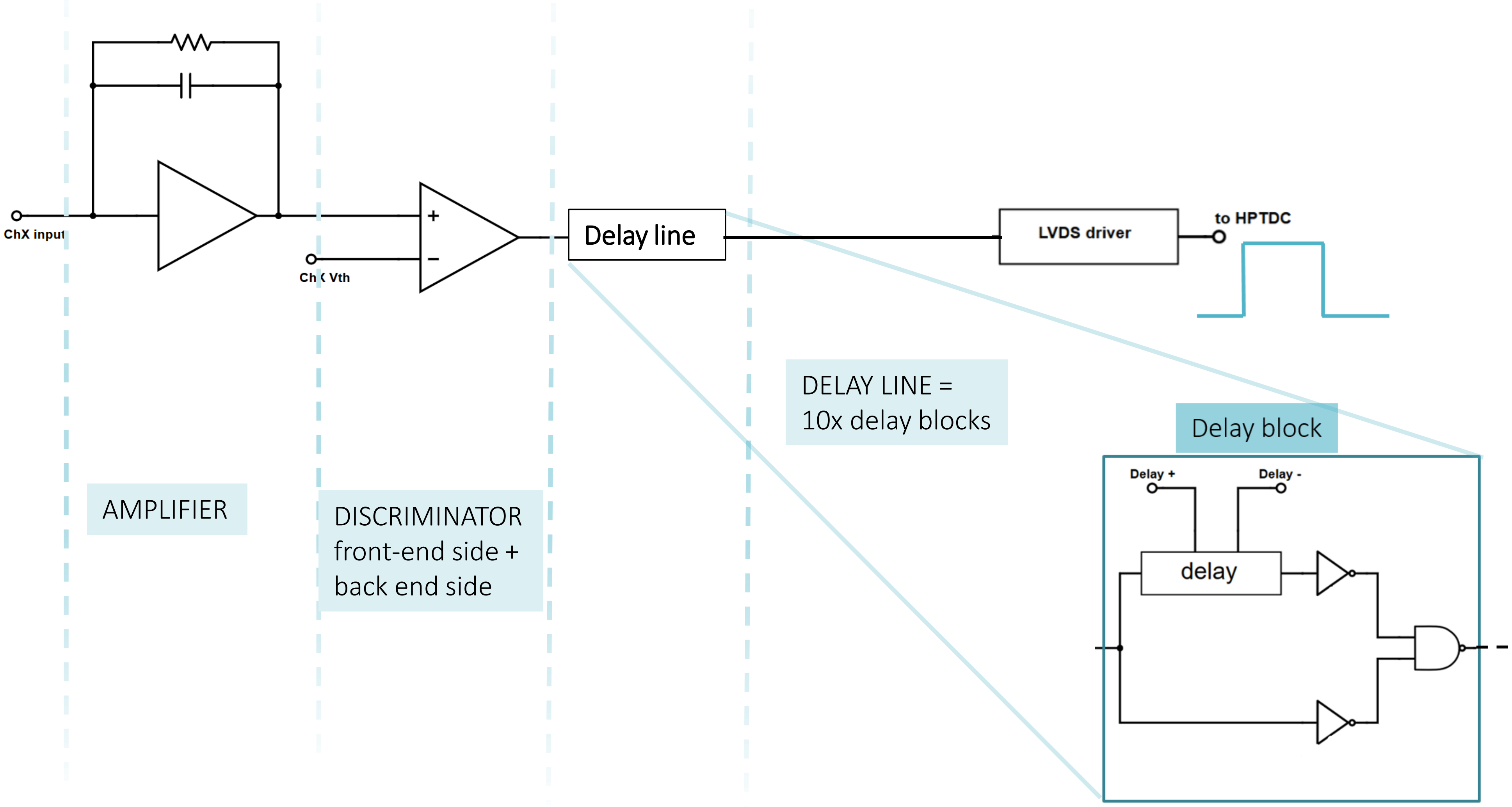


It is optimized for a sensor capacitance of 5-10 pF and an input charge between 3 fC and 60 fC

The output is sent out of the roman pot to the existing HPTDC board through LVDS connections (32 pairs per detector module)

To read out a CT-PPS UFSD minimizing wire-bond length → 4 TOFFEEs

TOFFEE – signal processing chain



TOFFEE – specifications

Dynamic range: 60fC (linear preamplifier in the range 3fC – 60fC)

Preamplifier gain: ~ 7 mV/fC

GBW: 14 GHz

RMS noise at Cdet= 6 pF: 800 uV

Discriminator output width: 2 – 14 ns

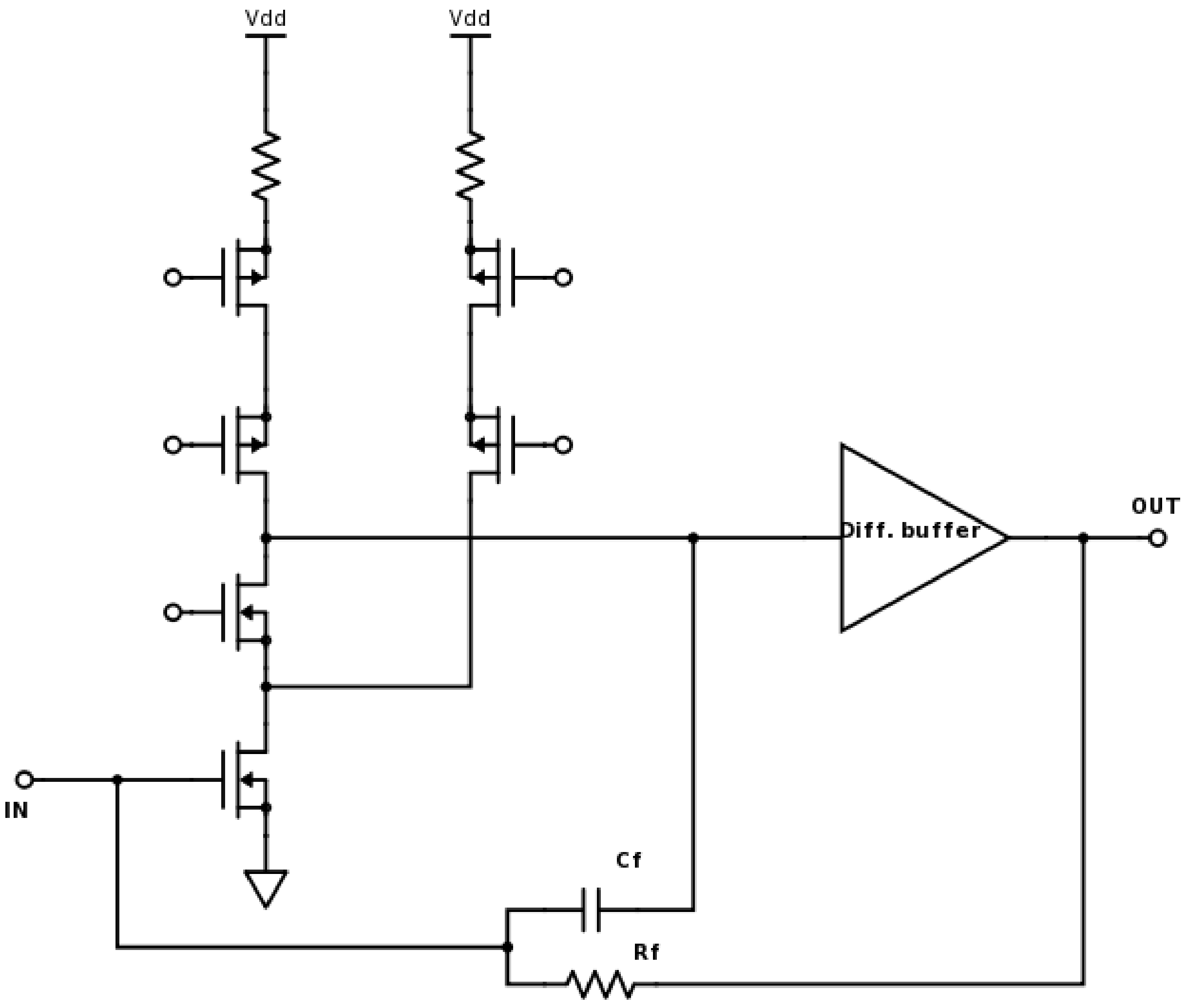
Delay line: 10 delay unit blocks, adding up to 12 ns to discriminator output to match HPTDC requirements

Power consumption: 18mW per channel

AVDD: 1.2V

DVDD IO: 2.5V

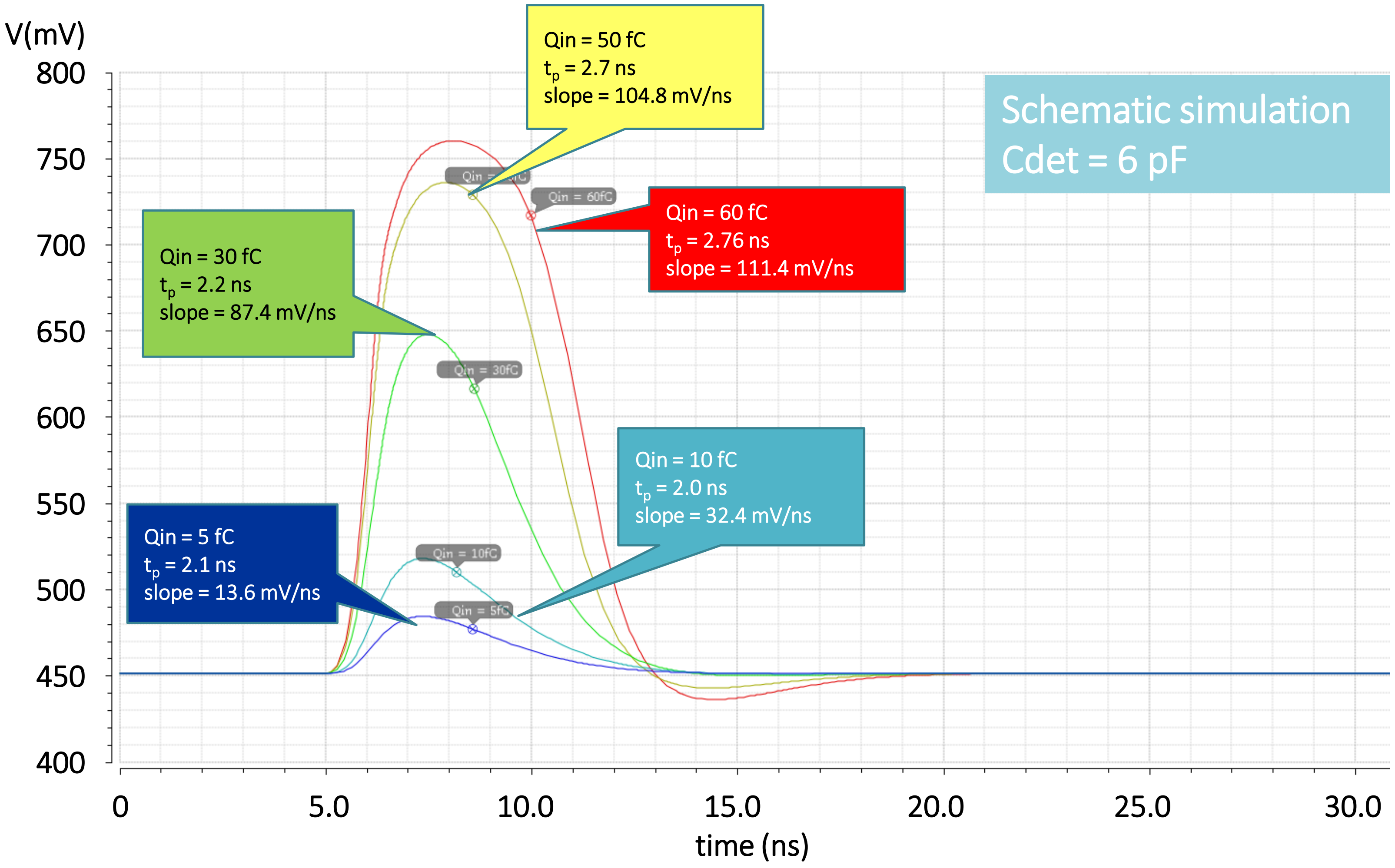
Expected dose at CT-PPS roman pot: NIEL ~ 7 $*10^{14}$ n_{eq}/cm^2 , TID ~ 80 Mrad



Preamplifier architecture

- Cascode amplifier with split current sources
- Right branch injects high current in the input transistor
- Resistors for noise shielding
- Differential buffer for load driving

Preamplifier signal (I)



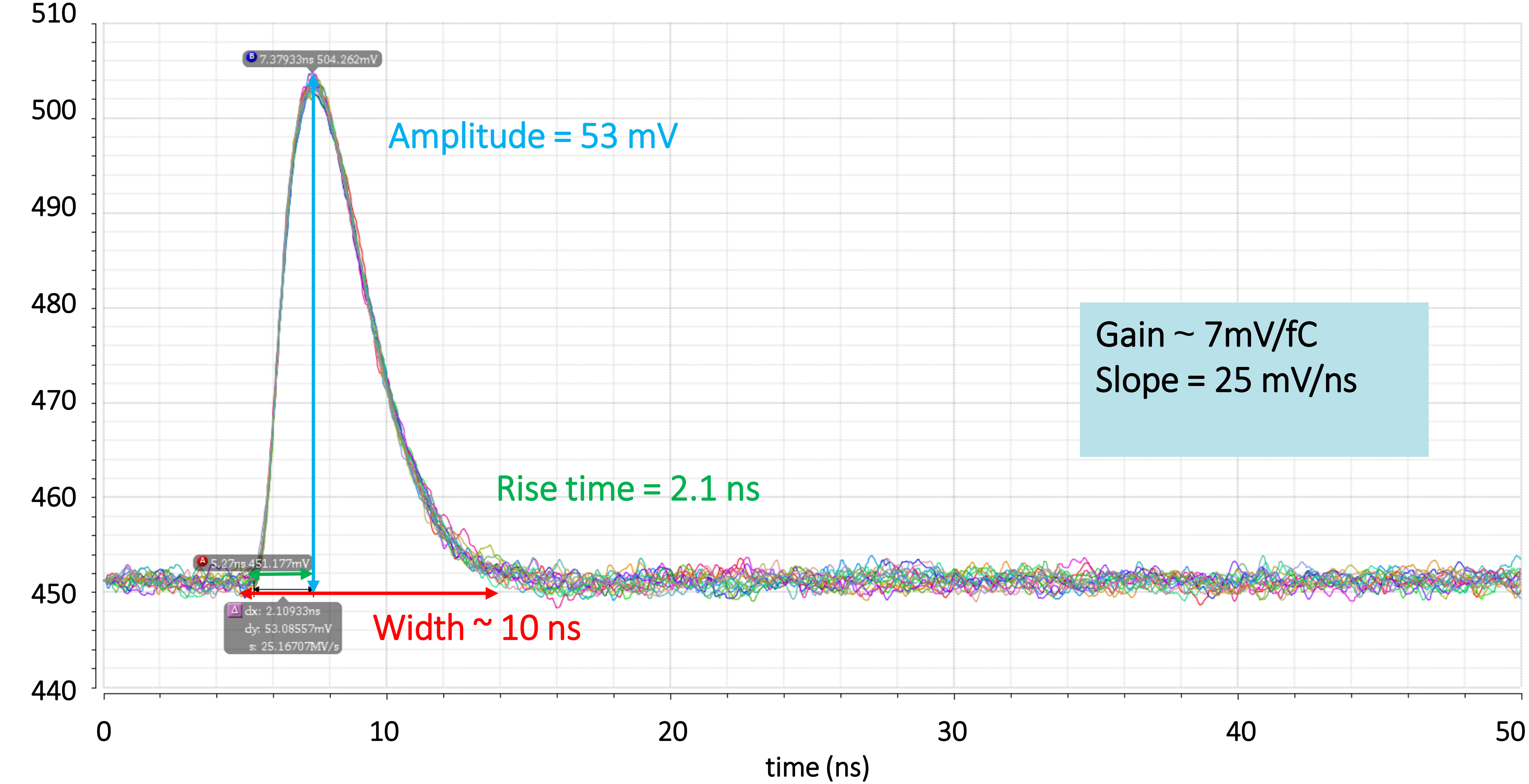
The preamplifier signal has

- **fast rise time**: ~ 2 ns schematic, < 3 ns postlayout
- **high slope**

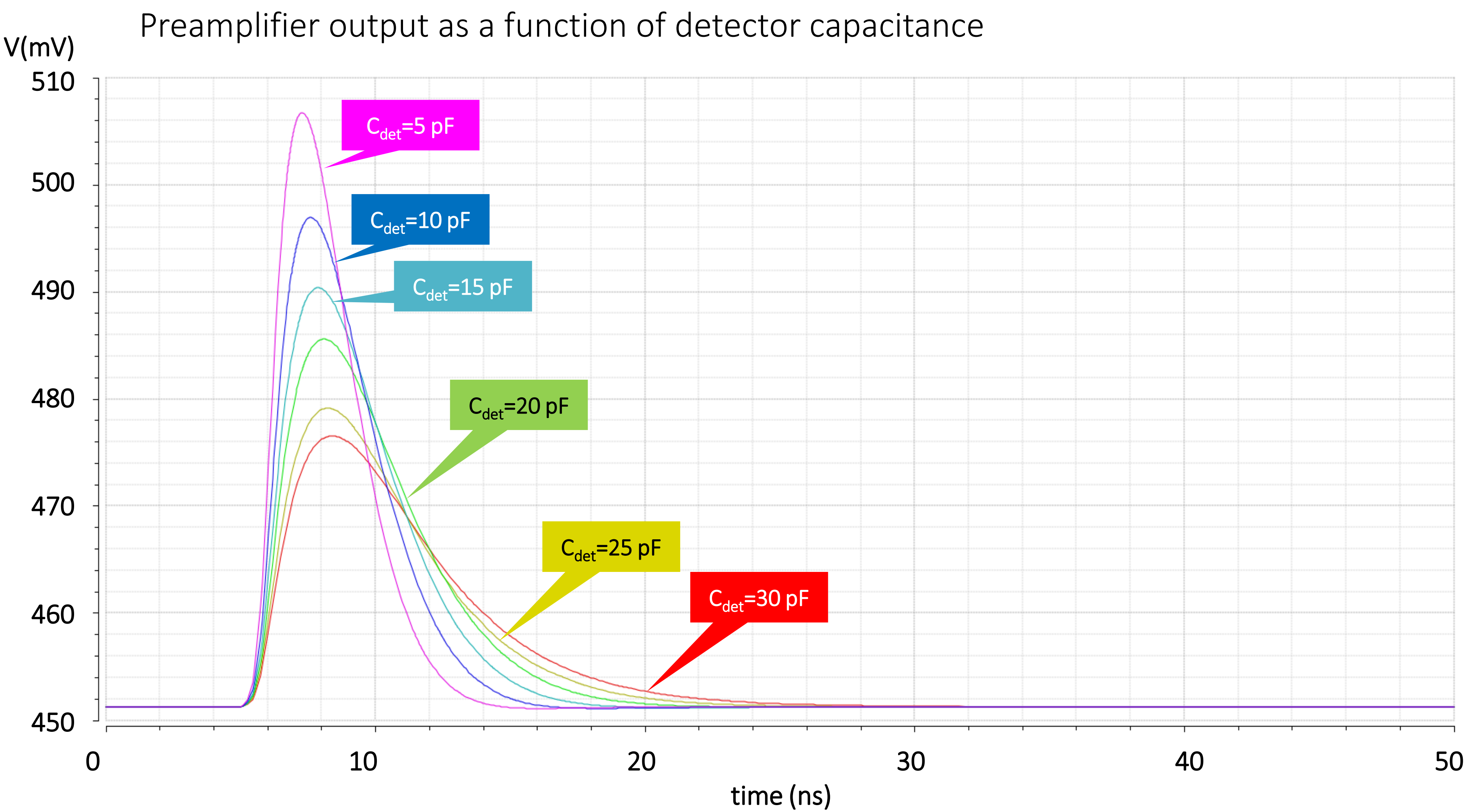
Requires high GBW amplifier (main power contribution)

Preamplifier signal (II)

Preamplifier response to typical 50 um UFSD MIP signal (Q_{in} = 8 fC) at C_{det} = 6 pF. Transient noise simulation

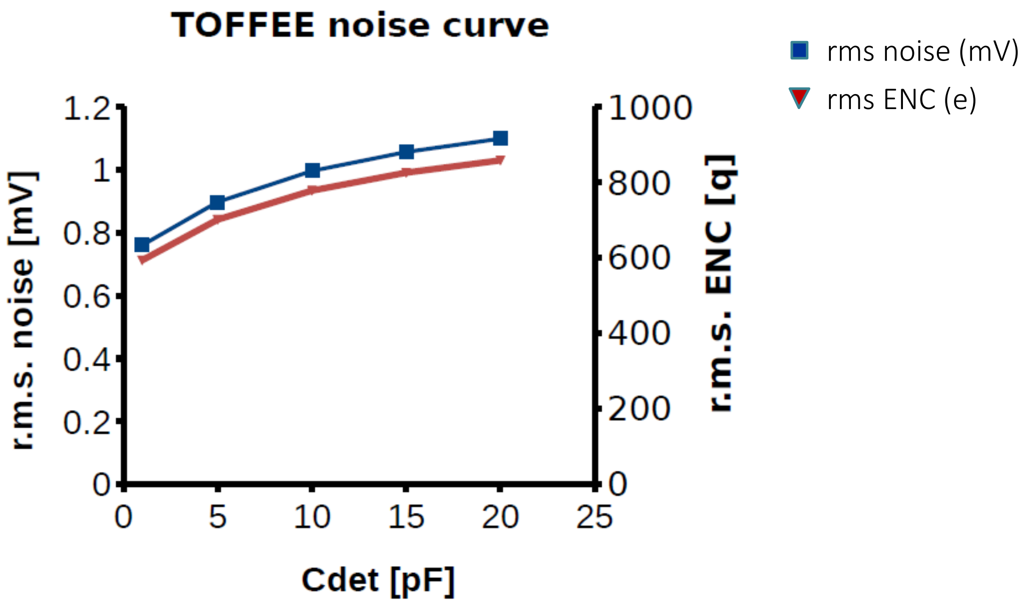


Preamplifier signal (III)

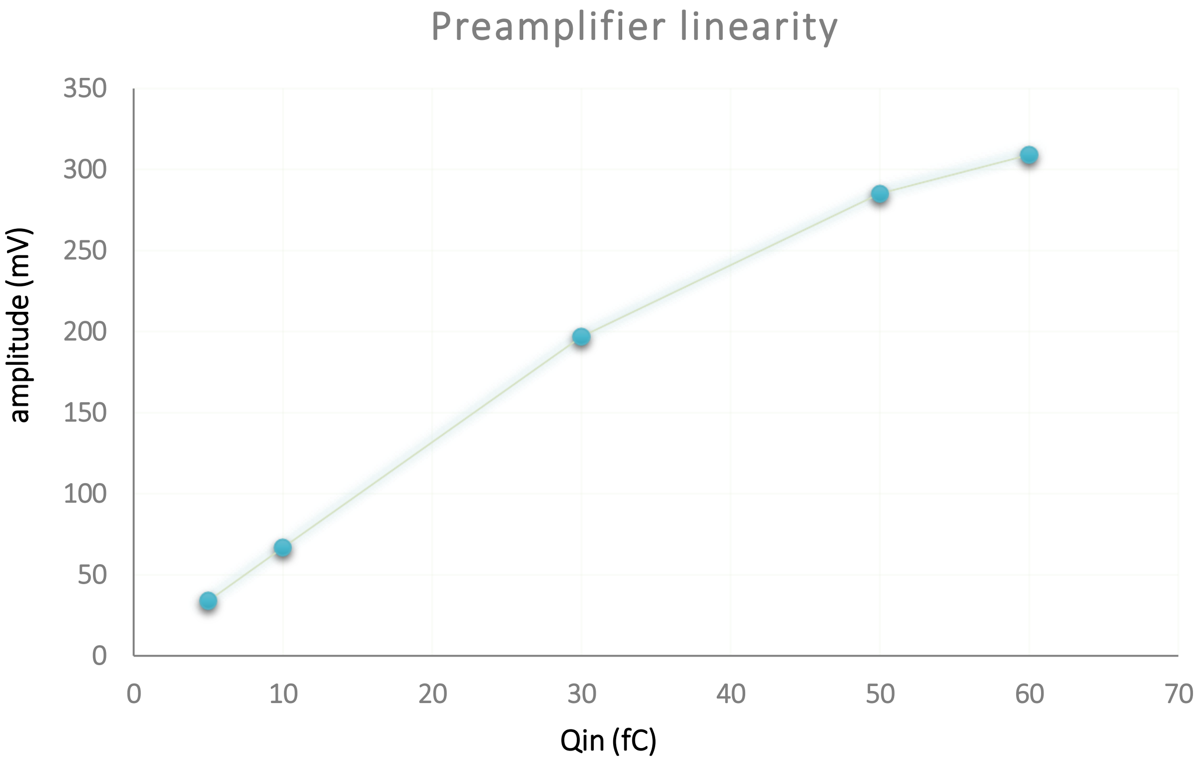


Preamp noise curve and linearity

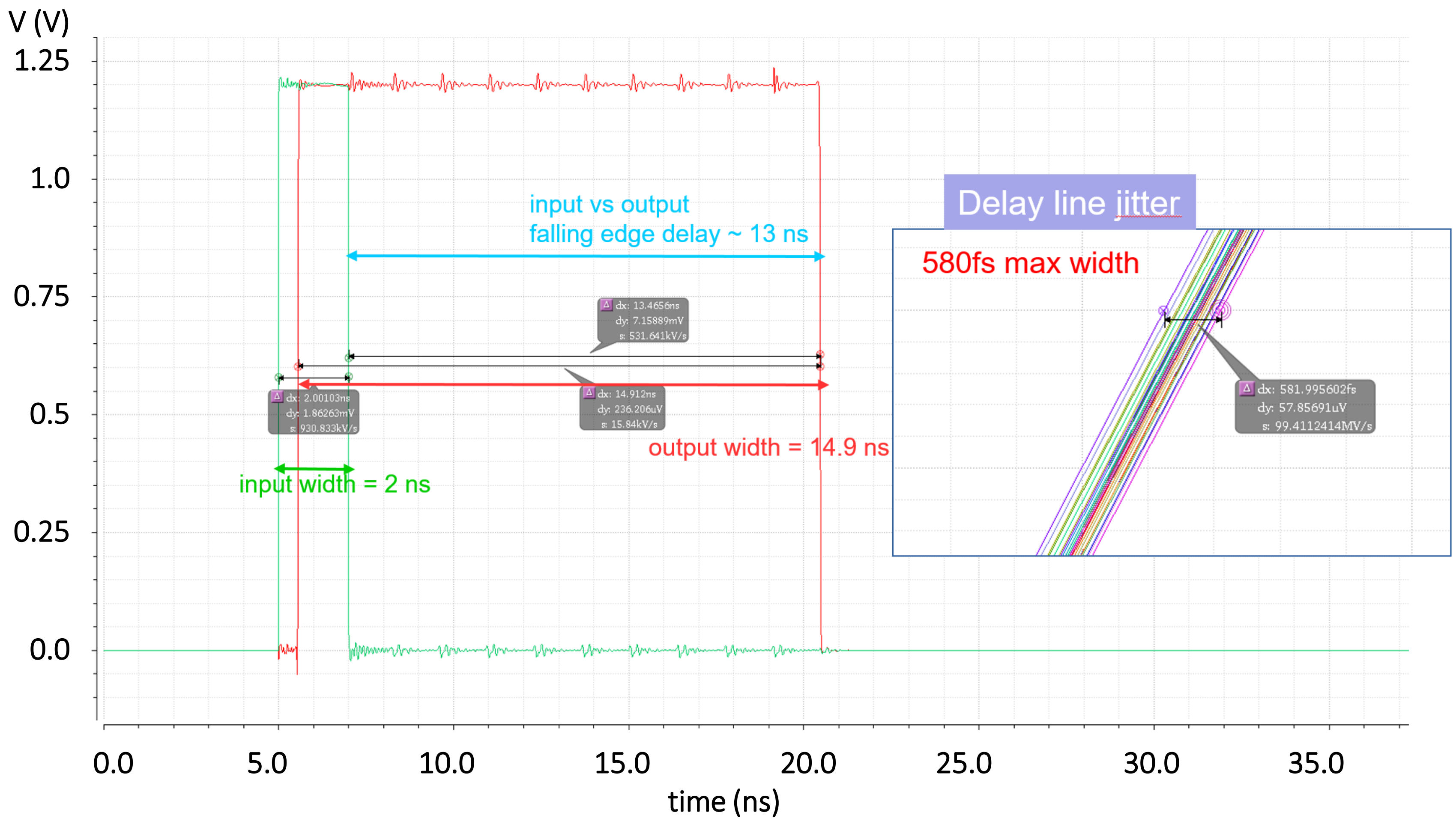
Simulated amplifier output noise as a function of detector capacitance



Preamplifier gain linearity as a function of input charge

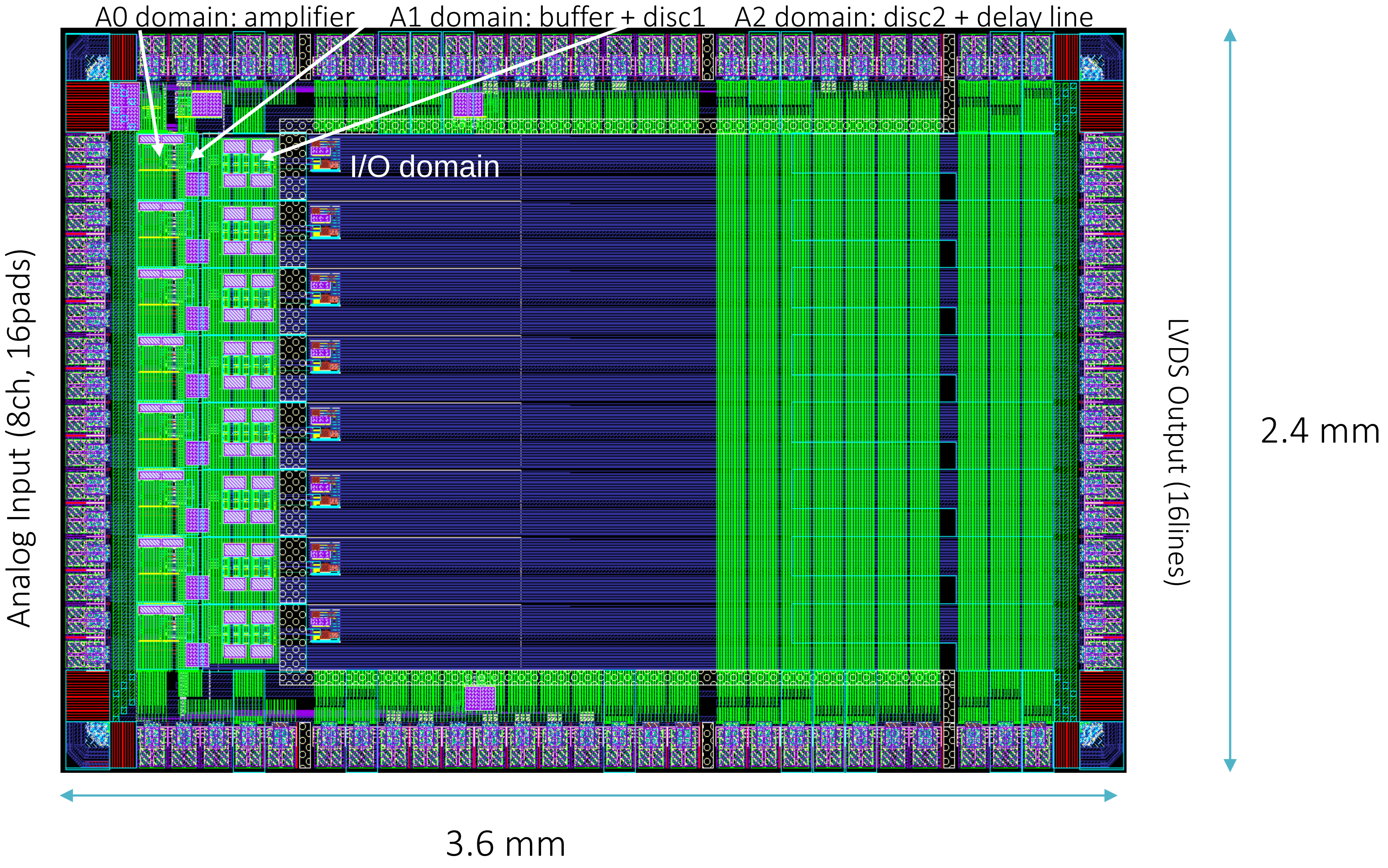


Delay line



V (V)
1.25
1.0
0.75
0.5
0.25
0.0
input vs output
falling edge delay ~ 13 ns
dx: 13.4656ns
dy: 7.15889mV
s: 531.641kV/s
dx: 2.00103ns
dy: 1.86263mV
s: 930.833kV/s
dx: 14.912ns
dy: 236.206uV
s: 15.84kV/s
output width = 14.9 ns
input width = 2 ns
Delay line jitter
580fs max width
dx: 581.995602fs
dy: 57.85691uV
s: 99.4112414MV/s
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
time (ns)

TOFFEE - layout



TOFFEE – simulated time resolution

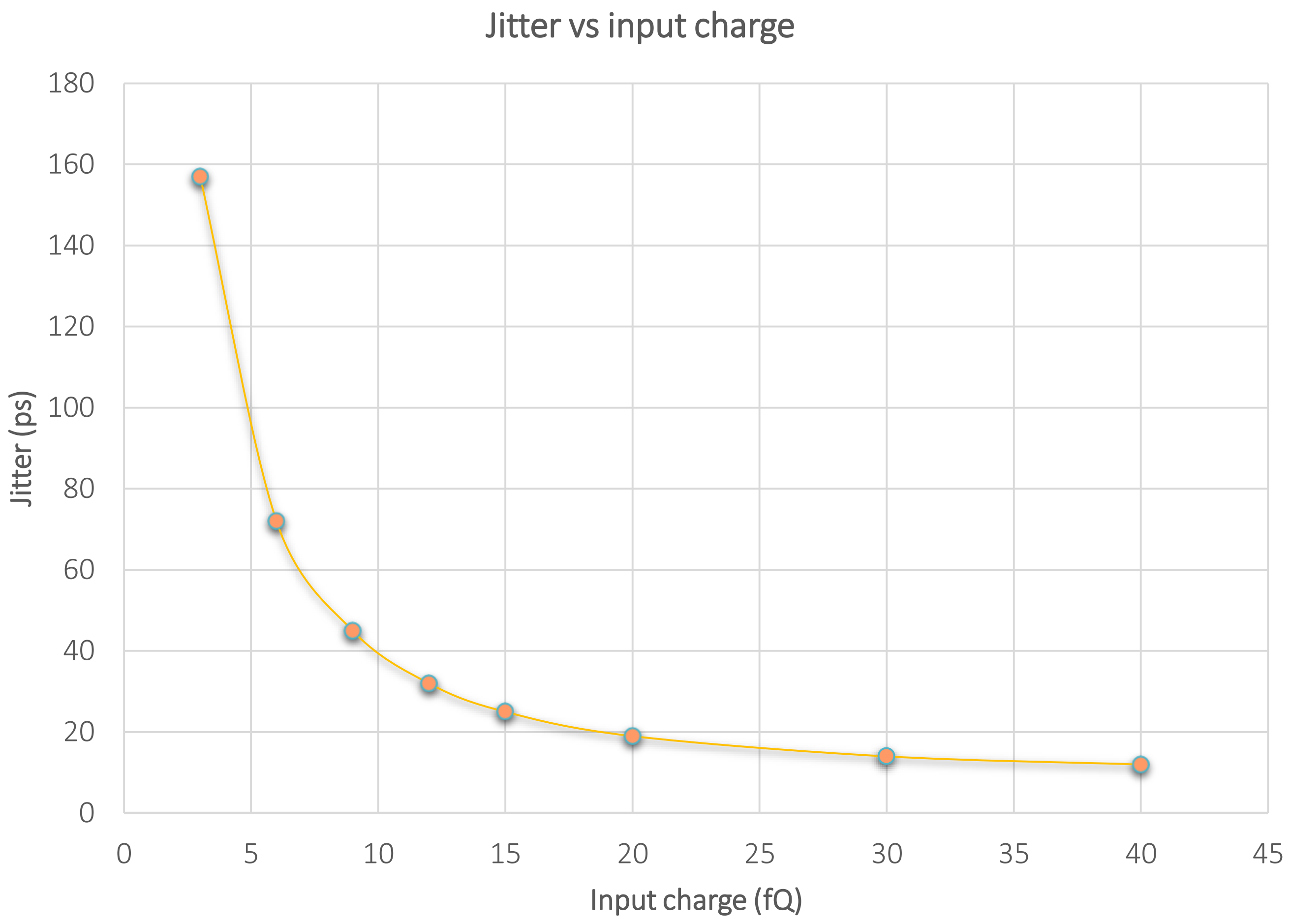
Realistic estimation of jitter as a function of input charge with parasitics.

A time resolution of **~ 45 ps** is expected for **1 single detector + readout module** for a MIP signal

Time resolution can be further improved by putting more planes in parallel, e.g. for 4 planes

$$\sigma_t = \frac{jitter}{\sqrt{N\ planes}}$$

~ 22 ps



Characterization and test activities (I)

TOFFEE is ready for testing. Two dedicated boards have been designed:

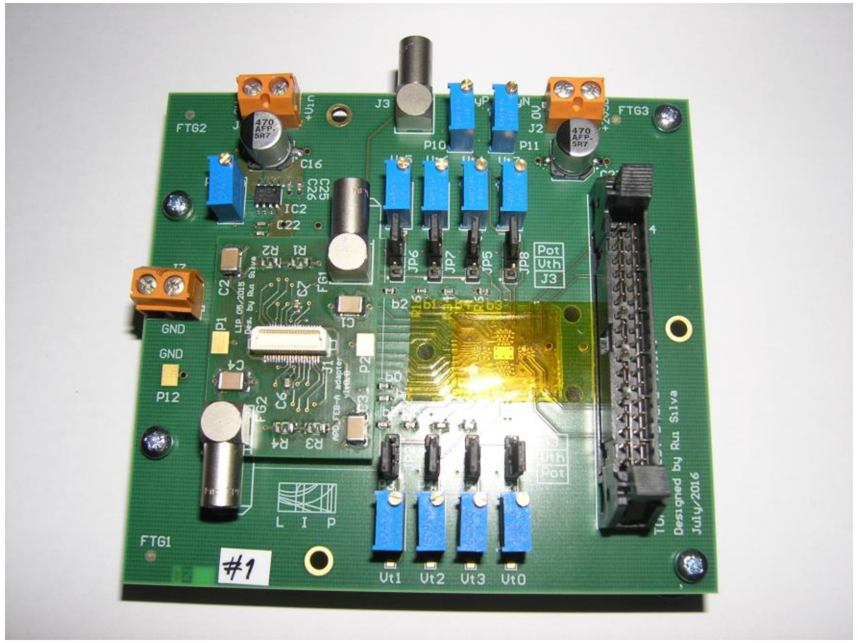
- **LIP board** (by R. Silva): TOFFEE + RMD APDs
- **Turin board** (by M. Mignone): TOFFEE + CT-PPS UFSD

Both have:

- external bias to find the best setting
- trimmers for discriminator threshold tuning

On LIP board: SAMTEC connector for APD adapter board

On Turin board: UFSD glued directly on the board, very close to the chip



LIP board for TOFFEE + APD adapter

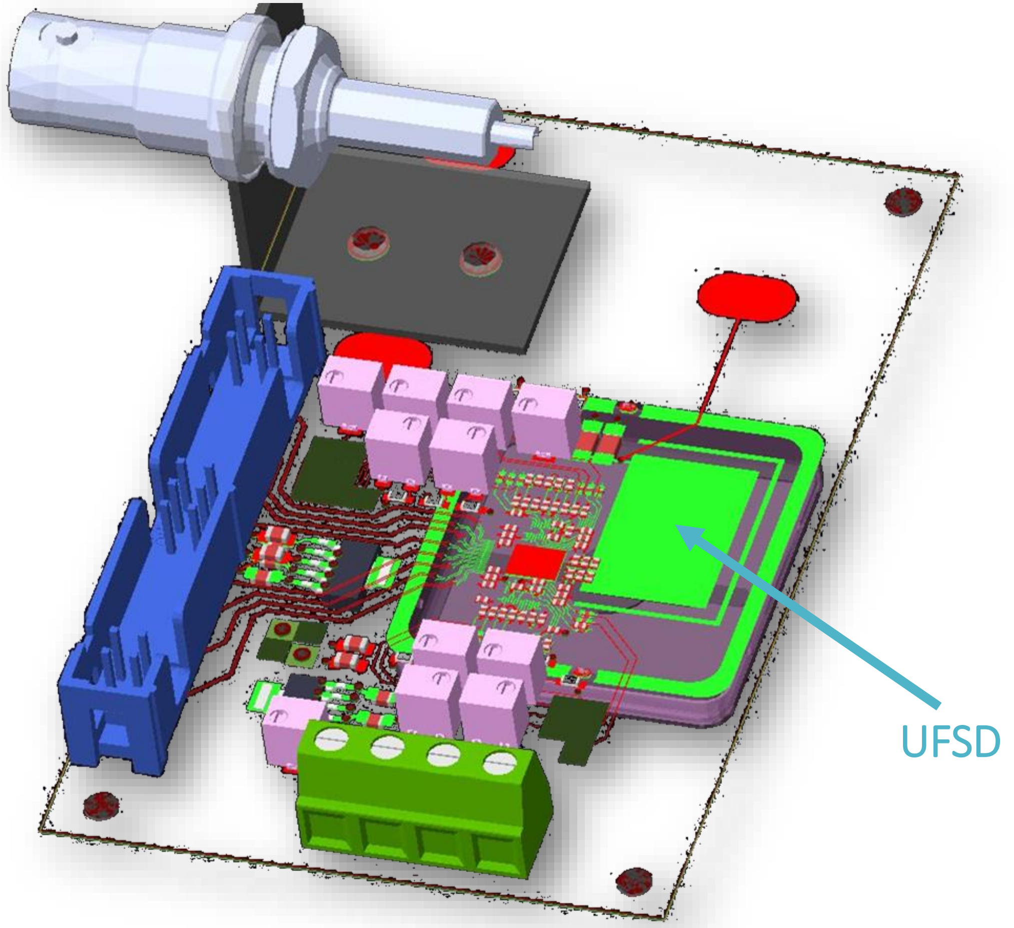
Characterization and test activities (II)

Testing is scheduled for October (LIP board + APDs)

and November/December (Turin board + UFSD)

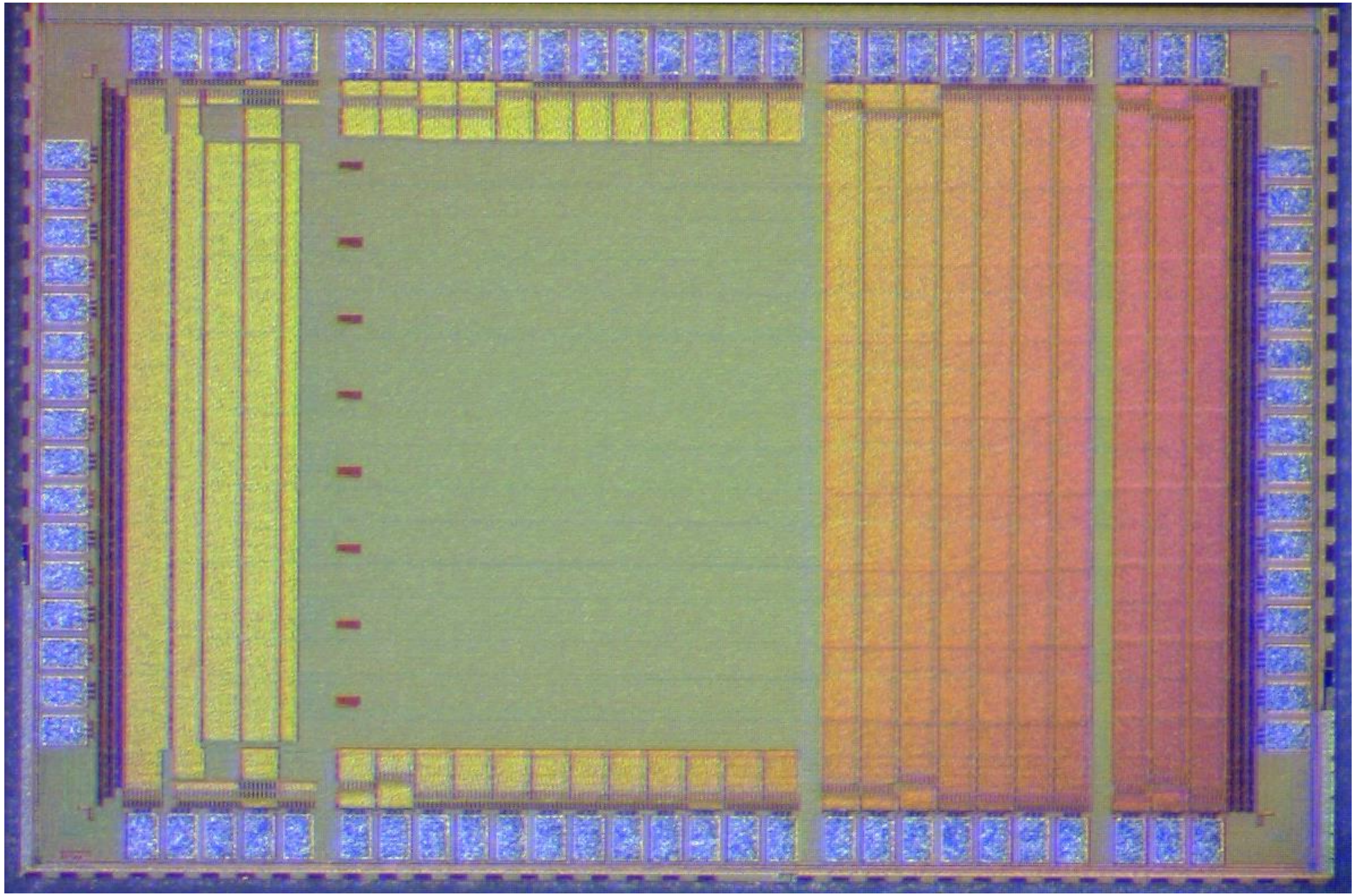
Foreseen tests involve:

- Amplifier linearity
- Dynamic range
- Gain measure
- Noise tests
- Laser tests

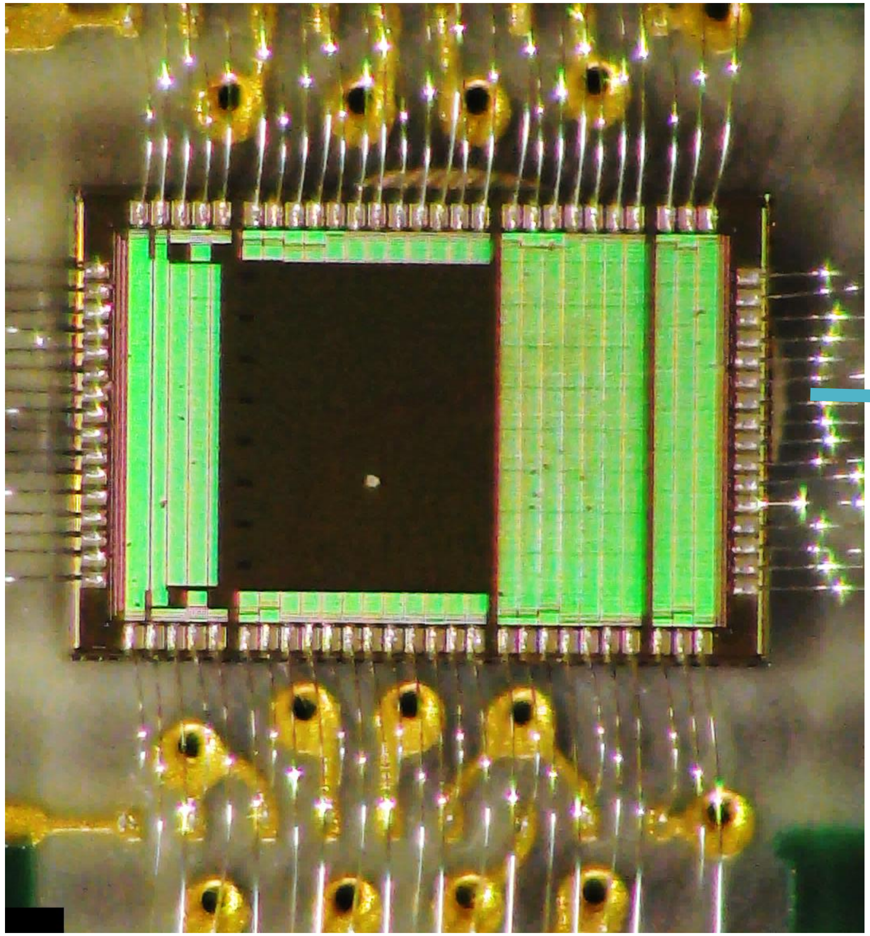


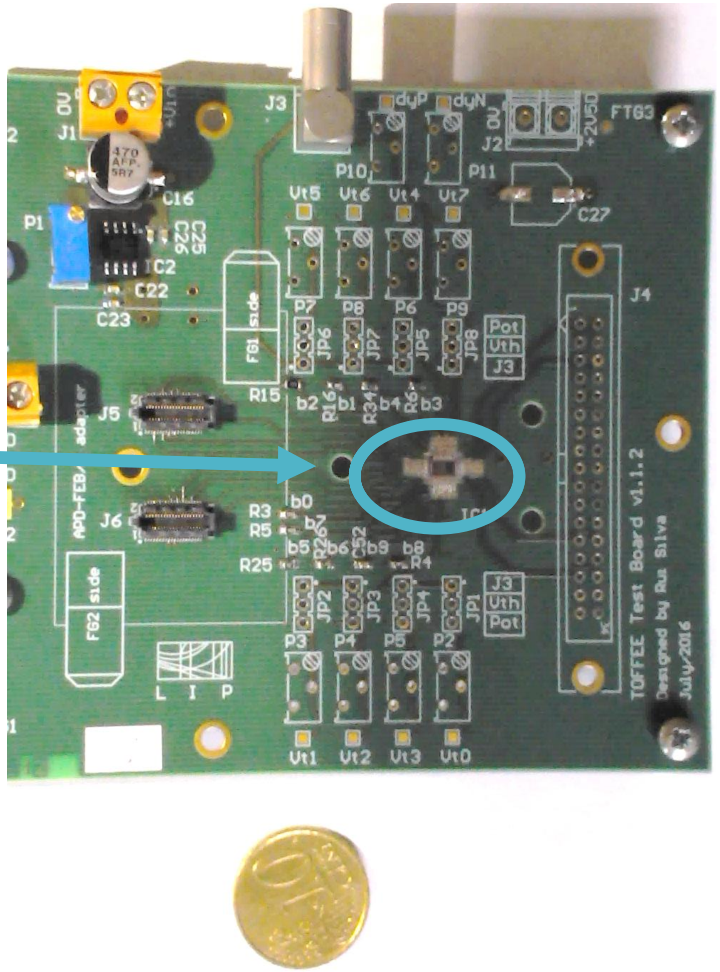
Turin board+ UFSD

TOFFEE

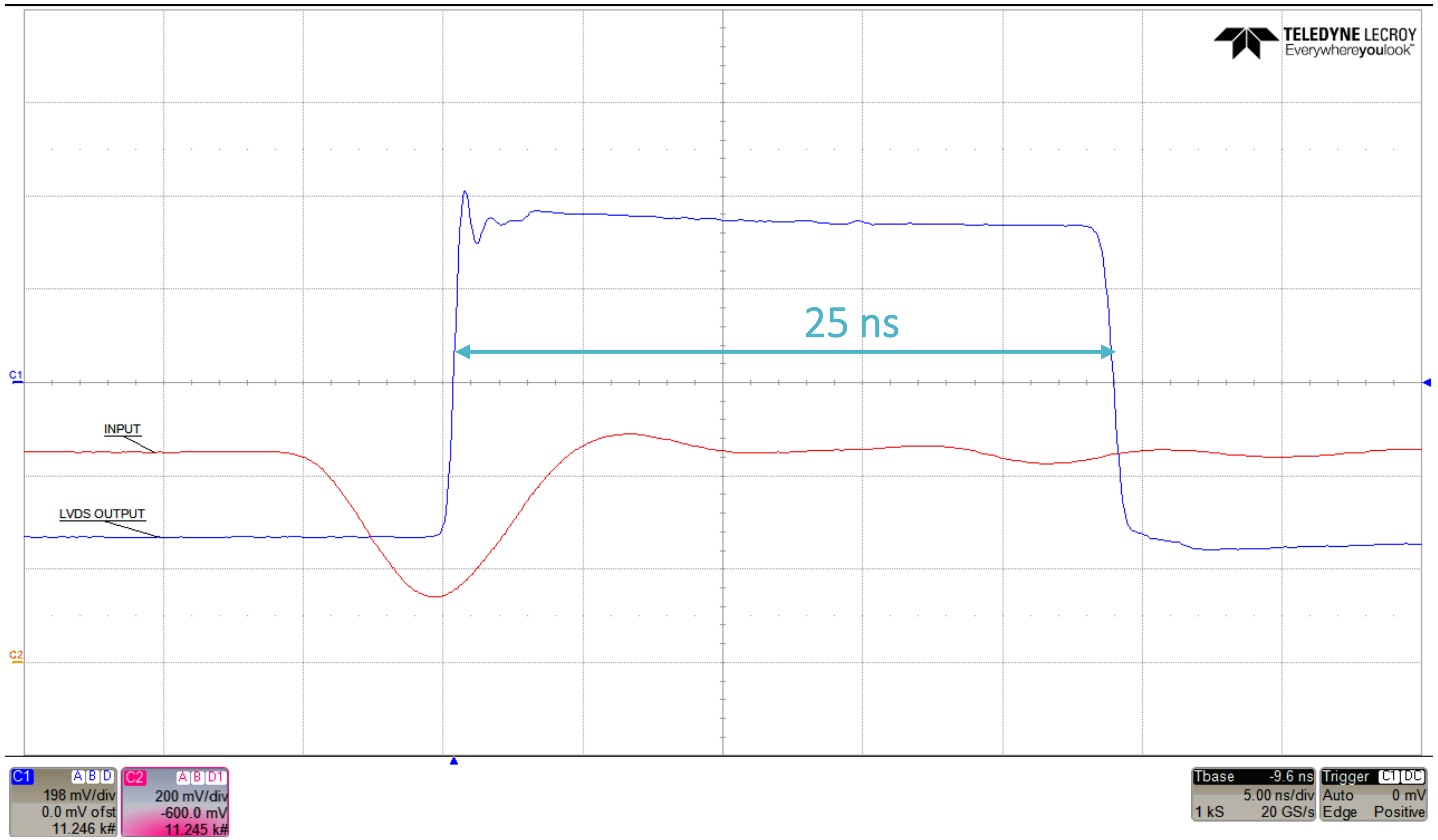


TOFFEE wire-bonded to LIP board





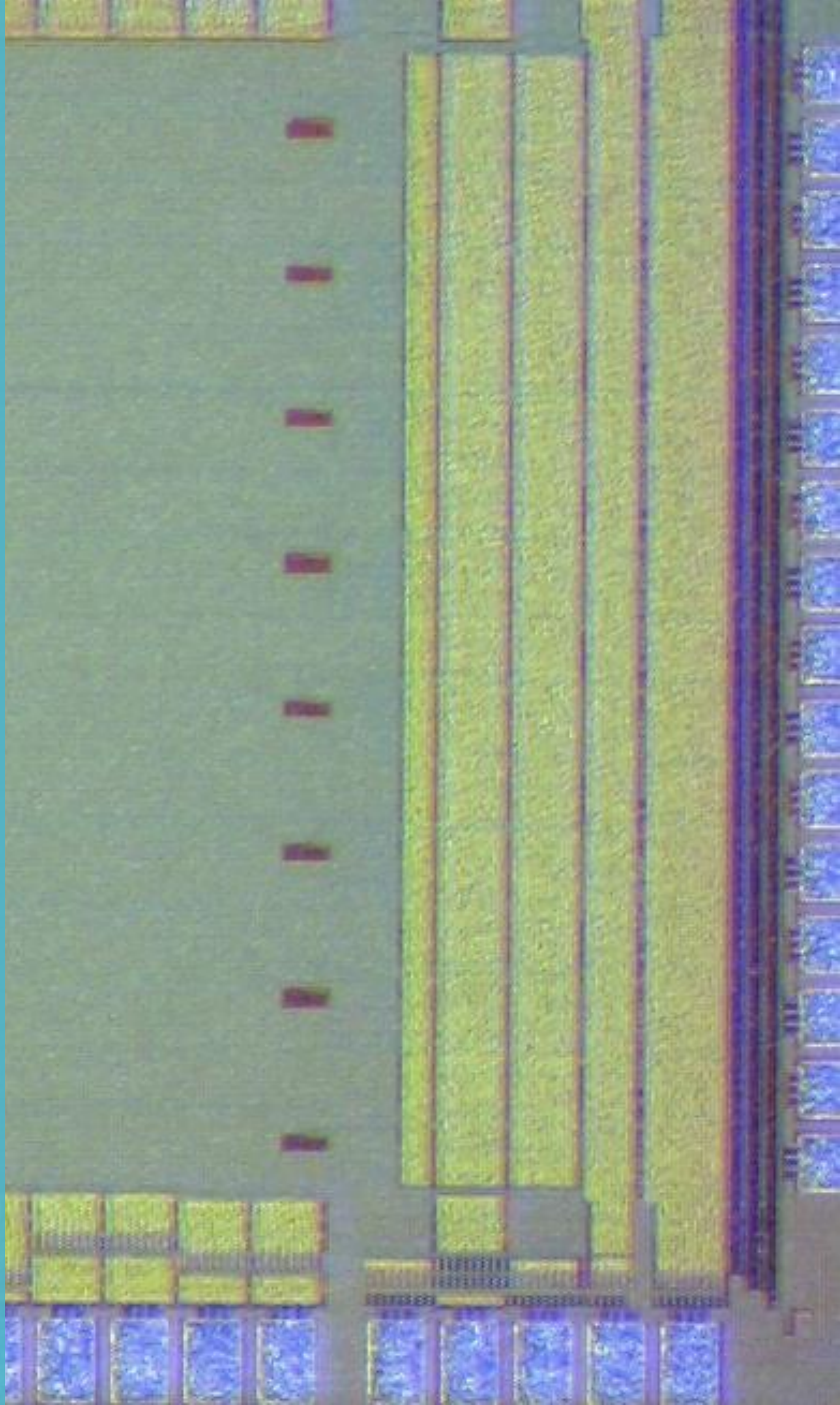
TOFFEE output



- Preliminary test to check TOFFEE's status with LIP board
- Chip response to 400 mV high, 10 ns wide pulse

Conclusions and outlook

- We have developed a fully-custom amplifier + comparator ASIC to read-out silicon detectors for timing
- TOFFEE’s amplifier rise time (~ 2-3 ns) and slope (> 20 mV/ns) allow to minimize front-end jitter.
- TOFFEE + UFSD simulated time resolution is ~ 45 ps for a MIP signal for a single module. By using 4 modules this value drops to ~ 22 ps
- First test results will be available by the end of October
- An improved version is foreseen for winter 2016-17



Thank you for your attention!

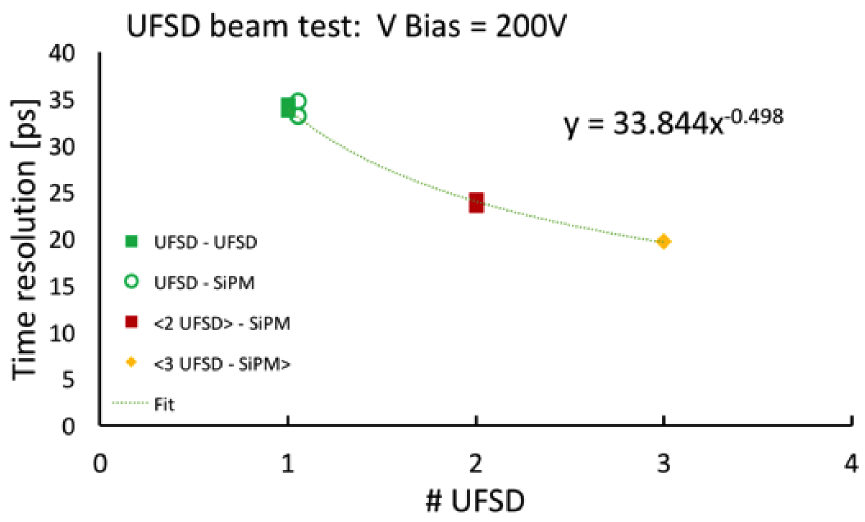
BACKUP

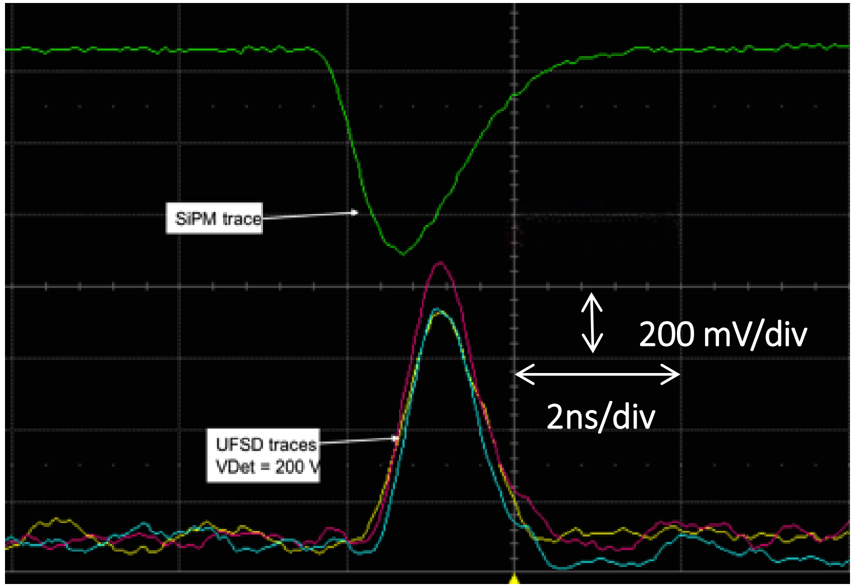
UFSD 50 um – beam test results

CNM 50 um UFSD have been tested in August 2016 at CERN

- Fully custom readout by UCSC + additional gain stage
- very accurate SiPM as trigger (~ 15 ps)

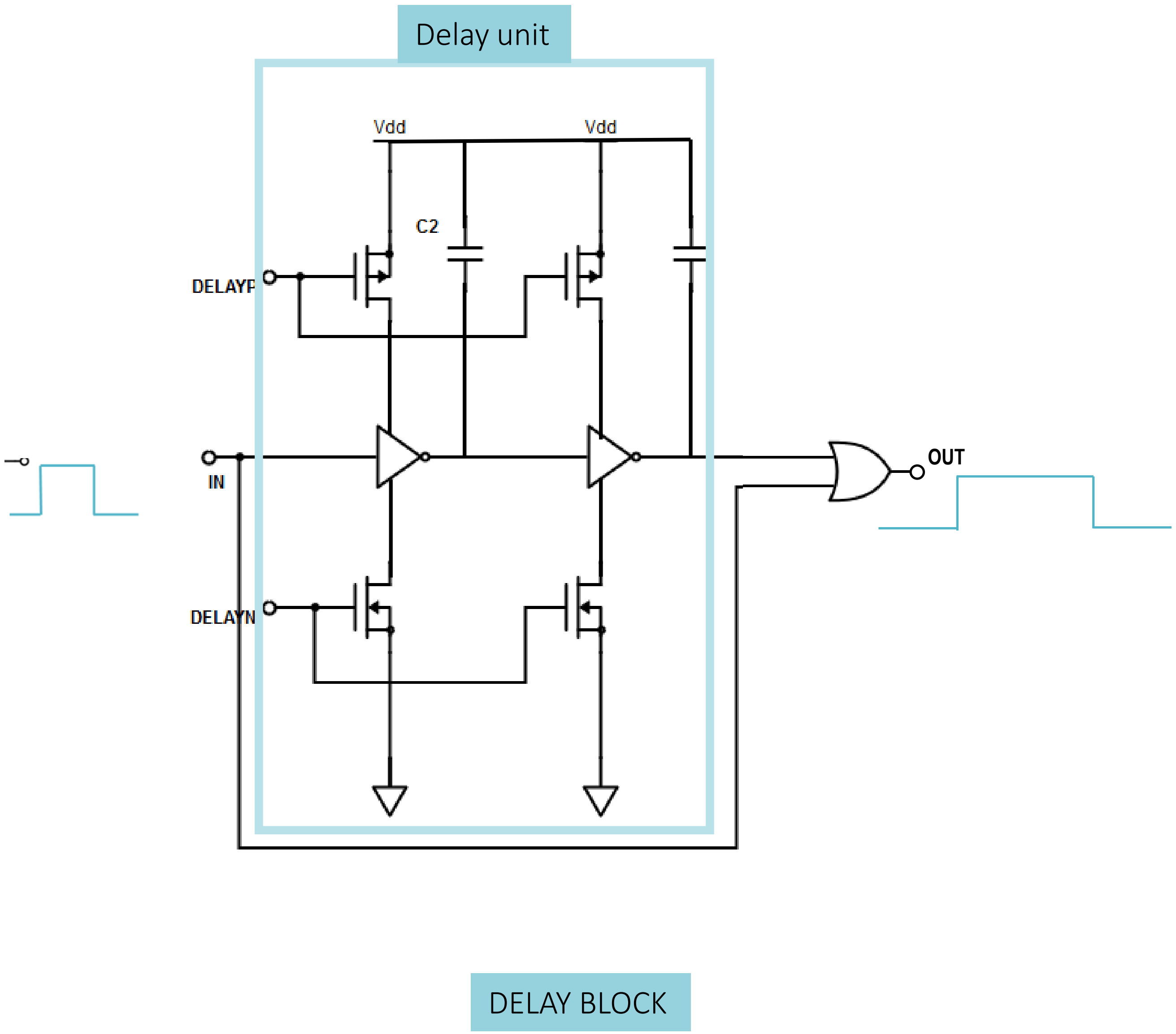
Time resolution as difference UCSC readout – SiPM





UFSD signal read by broad-band amplifier + calibration SiPM trace

An excellent time resolution with 50 um thick UFSD is achievable!



Delay line

- Delay line stretches discriminator output
- Each delay line block is composed by a delay unit and an OR gate
- Delay unit output and input are sent to OR gate
- Each delay block is repeated 10 times to reach the desired output width