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Design and measurements of 10 bit pipeline ADC for the Luminosity Detector at ILC

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The design and preliminary measurement results of a prototype 10 bit pipline ADC for the Luminosity Detector (LumiCal) at the International Linear Collider (ILC) are presented. The motivation for the chosen architecture is presented and followed by the description of the core blocks. The prototype was fabricated in 0.35 um CMOS technology. The preliminary measurements of static (INL, DNL) and dynamic (SHNR, THD) parameters were performed to understand and quantify the circuit performance. The ADC was found to be fully functional for sampling frequencies up to about 40 MHz. The measurements performed at 30 MHz sampling showed the INL below 1 LSB and the DNL below 0.5 LSB.

Summary

Two analog to digital conversion schemes are presently under study for the Luminosity Detector readout. One with relatively slow ADC per each front-end channel and one with faster ADC per group of (about) 8 channels. First option would be the simplest solution from the design point of view while the second one would save the area. The ILC bunch crossing rate is about 3 millions event per second so the first option (ADC per channel) would require an ADC with sampling rate of about 3 Msample/s while the second would require a sampling rate of about 24 Msample/s.

The aim of this work was to design an ADC working up to about 30 MHz sampling frequency. One of the most efficient architectures assuring a good compromise between the speed, the area and the power consumption is a pipeline ADC. This architecture was chosen for the LumiCal data conversion. Since in the ILC experiment each 1 ms active beam time will be followed by 200 ms pause the requirements on readout electronics power dissipation may be strongly relaxed if the powering is switched off in the pause.

The present ADC design consist of sample-and-hold circuit, 9 1.5-bit pipeline stages and digital correction logic. The whole ADC is fully differential. Each pipeline stage contains two pairs of sampling and feedback capacitors, telescopic gain boosted amplifier, two dynamic latch comparators, several switches and small logic block. To save the area and the power scaling of capacitors and currents is implemented in the following stages. In addition the power and the clock switching off is implemented.

The prototype ADC was fabricated in 2-poly, 4-metal, 3.3 V, 0.35 um technology. A dedicated test setup based on Xilinx FPGA, allowing ADC tests up to about 100 MHz sampling frequency, was build. The preliminary tests showed full functionality of the prototype. The static measurements were performed for 30 MHz nominal sampling frequency and input voltage range between $1 - 2$ V, corresponding (after single-ended to differential conversion) to 2 V full differential input range. The results were analyzed using standard histograming method. The measured DNL was found to be less than ±0.5 LSB (the worst case was 0.4 LSB) while the INL was less than ±0.9 LSB.

The effective number of bits calculated from static INL reached about 9.6. No missing codes were found. The preliminary dynamic measurements were performed with a sin-wave input. The Signal to Non Harmonic Ratio (SNHR) of about 57 dB was measured. The Total Harmonic Distortion (THD) of about -56 dB was measured. These first results of dynamic measurements require further studies since the measured values may be affected by the test setup. In particular by the sin-wave distortion of the signal generator and by the single-to-differential conversion (on PCB) before the ADC. The measured ADC current consumption was about 10 mA for analog blocks and 6 mA for digital part at smapling frequency 30 MHz.

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