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Design of High Dynamic Range Digital to Analog Converters for Calibration of the CALICE readout electronics

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The ILC ECAL front-end chip will integrate many functions of the readout electronics including a DAC dedicated to calibration. We present two versions of DAC with respectively 12 and 14 bits, designed in a CMOS 0.35µm process. Both are based on segmented arrays of switched capacitors controlled by a Dynamic Element Matching (DEM) algorithm. A full differential architecture is used, and the amplifiers can be put into a standby mode reducing the power dissipation. The 12 bit DAC features an INL lower than 0.4 LSB at 5MHz, and dissipates less than 7mW. The 14 bit DAC is an improved version of the 12 bit design.

Summary

The ILC ECAL front-end chip will integrate many functions of the readout electronics. Due to mechanical constraints, no package will be used and the dies have to be located in cavities dogged in the printed circuit board. Consequently the electronics has to be fully integrated and no discrete components can be used. This multi-channel chip also requires a high dynamic DAC dedicated to calibration. Since calibration process can be carried out at intermediate frequencies, the key issues for such a DAC are the INL and the power consumption. Switched capacitor DAC are well suited to meet these requirements. The linearity of a design implemented in standard CMOS process is limited by the matching errors of its analogue components. For more than 10 bit the required capacitor matching is difficult to obtain and linearization techniques have to be used. High resolution over-sampled delta sigma converters commonly use a DEM algorithm to cancel the matching errors. The DEM allows such DAC to turn the harmonic distortion into noise which is then reduced by a low pass filter. When used in a calibration process the DAC has to provide a sequence of DC values, each value corresponding to a calibration point. In this case the DEM can be effective if several samples are accumulated for each calibration point. The mean value of the resulting distribution will provide with accuracy the output value of the circuit under calibration.

The aim of the first design was to reach a 12 bit resolution. This dynamic range is below the ILC ECAL requirements but will allow the design methodology to be validated. This full differential DAC comprises two 6 bit capacitor arrays connected together through a segmentation capacitor. The network stores a charge proportional to the DAC input code. This charge is then shared with a feedback capacitor using Direct Charge Transfer (DCT). The DCT architecture exhibits two important advantages. At first, the OTA does not have to charge the feedback capacitor and its power consumption can be maintained low even for large capacitor values. Moreover, the charge sharing also acts as a first order low pass filter that reduces the noise induced by the DEM. The test result shows that the DEM allows the chip to reach a 12 bit resolution. The DAC features an INL lower than 0.4 LSB up to a 5MHz frequency. The power consumption is lower than 7mW.

The 14 bit design is also based on segmented arrays of switched capacitors performing DCT with a feedback capacitor. The 14 bits are divided into three sub-arrays: 5 MSB, 5 ISB (Intermediate Significant Bits) and 4 LSB. The DAC integrates two OTA, the first one processes the ISB and LSB arrays and the other one is dedicated to the MSB array. Compared to the first design, this topology dramatically reduces the sensitivity to parasitic capacitors. The test of this 14 bit design will be carried out in the forthcoming weeks and the results will be presented.

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