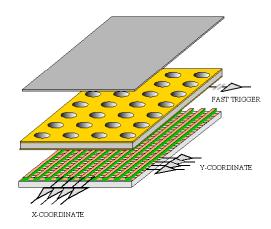
## **Read-out boards**

Rui de Oliveira 16/02/2009 RD51 WG1 workshop Geneva



## Content

- PCB structures
- 1 direction read out board
- 2 directions
- 3 directions
- PAD
- Pixel
- Special
  - Active read out board
  - Grounding and capacitive couplings
  - Resistive spark protection
  - Resistive sharing



## Single sided



CERN max size: 2000 x 600

Board thickness: 12um to 6mm

Metal: 2um to 200um

Limitation : exposure 2000x600

dev, etch: 600 width

Materials: rigid glass epoxy etc...

flex



#### Double sided +PTH

Drilling: 0.2 mm CNC min , 50um micro-vias

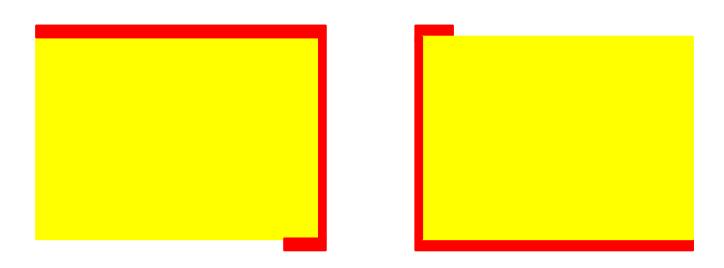
CERN max size: 1200 x 600 rigid boards

1600 x 600 flex boards

Limitation due to plating baths Board thickness: 12um to 6mm

Metal: 15um to 200um in the holes, 2 um min elsewhere

Materials: glass epoxy, polyimide



### Multi layer + PTH

Drilling: 0.2 mm CNC min CERN max size: 600 x 600

Board thickness : 6mm max

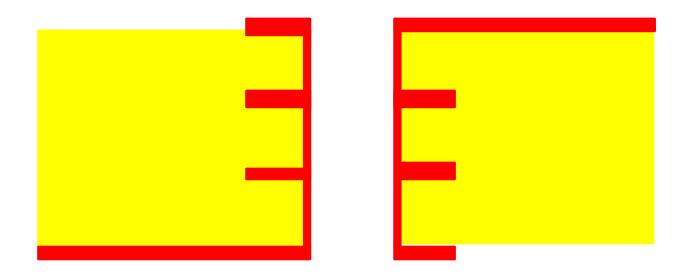
Metal:15um to 200um

Limitation due to: press and plating

Number of layers up to 20

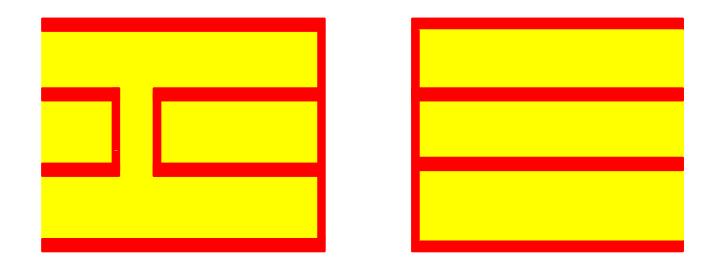
Thickness of one layer: 12um min

Materials: Epoxy, Kapton ...



## Multi layer + burried Vias +PTH

Same limitations as multi layers boards Burried vias: 50um min Chemical, and 0.2mm for CNC drilling



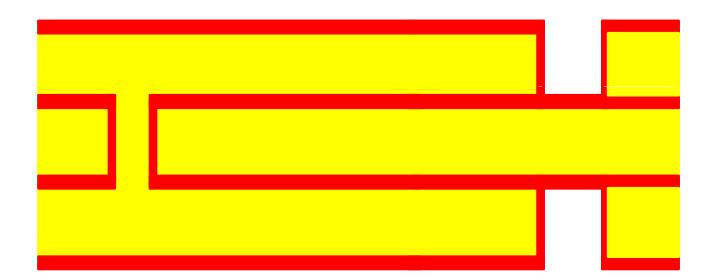
## Multi layer + burried Vias +blind vias

Same limitations as multi layers boards

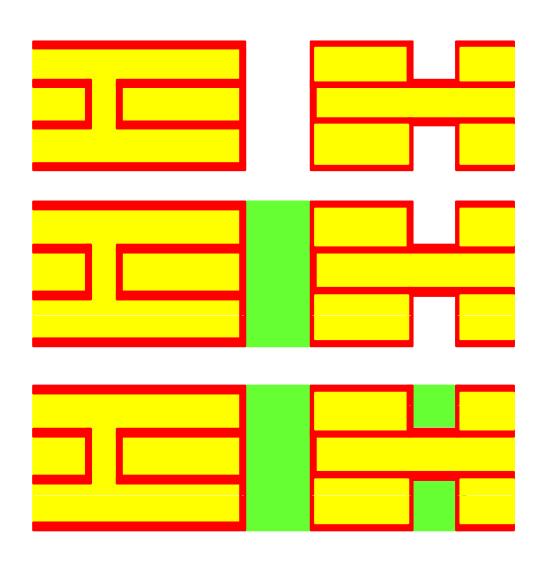
Burried vias: 50um min for Chemical vias and 0.2mm for CNC drilling

Blind vias: hole diameter/ hole depth > 1

Hermetic by process

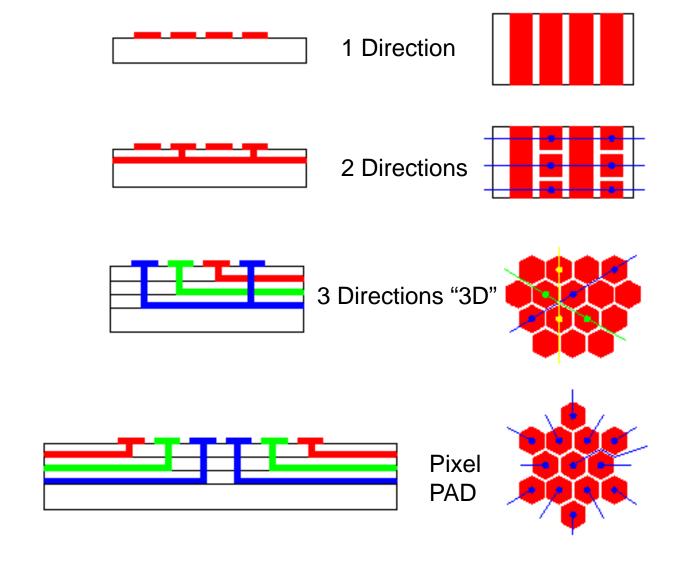


## Multi layer + burried Vias +blind vias+ PTH



Hole and via filling Conductive or Dielectric resin Not gas tight

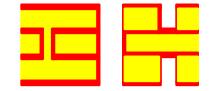
## **Readout Circuits**



## Demin experiment

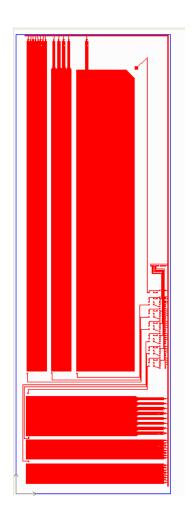


Multilayer + PTH+ Burried +blind



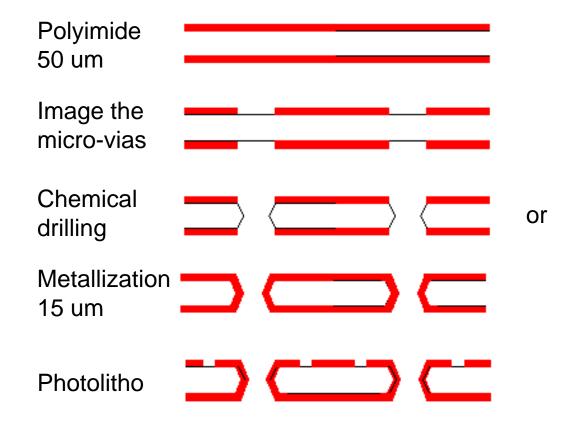
Single direction read out board with shielding and reduced copper in the active region.

Max size 600mm x 600mm

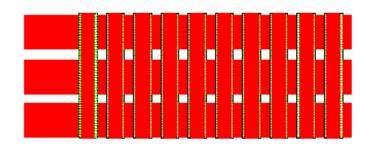




ATLAS Muon detector Upgrade test Single side rigid epoxy board 17um copper on 2mm glass epoxy 1500mm x 500 mm

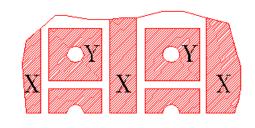


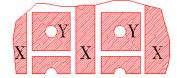




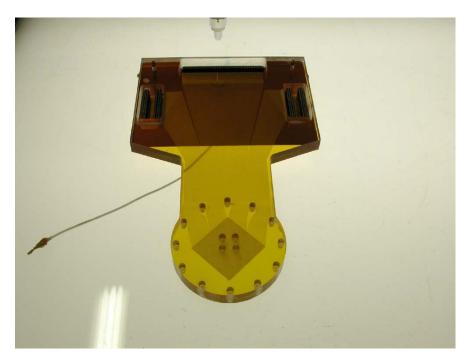
area of X and Y adjusted To share the signals

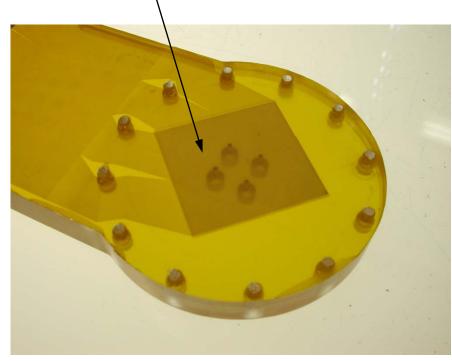
area of X = area of Y





#### Readout active area





2D readout board glued on low intrinsic radiation Plexiglas substrate CAST experiment 400 um pitch min 600mm x 450mm max size

Compass experiment 33cm x 33cm active area

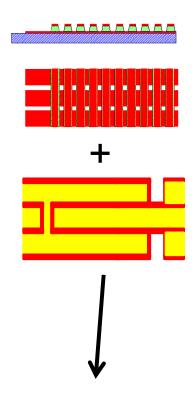
NA 49 half cylindrical detector.

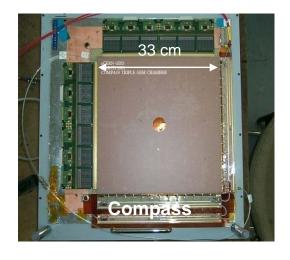
Max size: 600 x 450

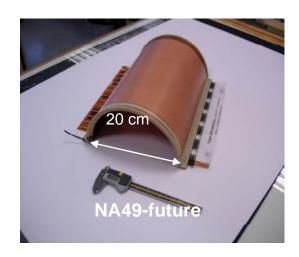
Limited by raw material, press and plating baths

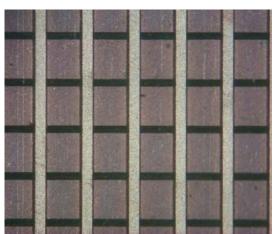
Minimum thickness: 35 to 50 um Kapton + 5um

copper + Honey comb structure

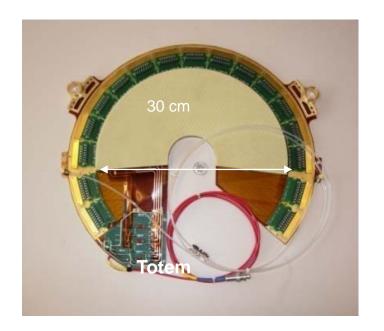






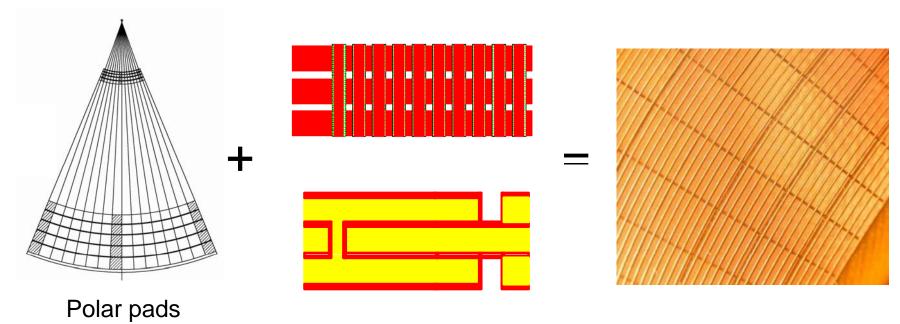


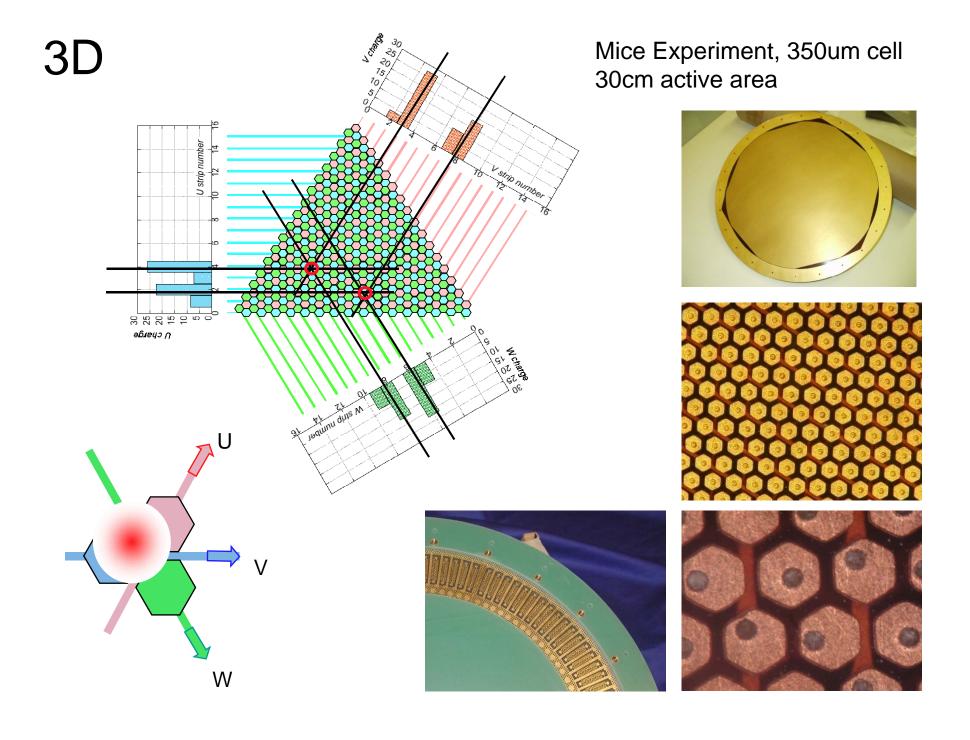
400 um pitch X and Y



**TOTEM** experiment

Max size for this technology: 600mm x 450mm

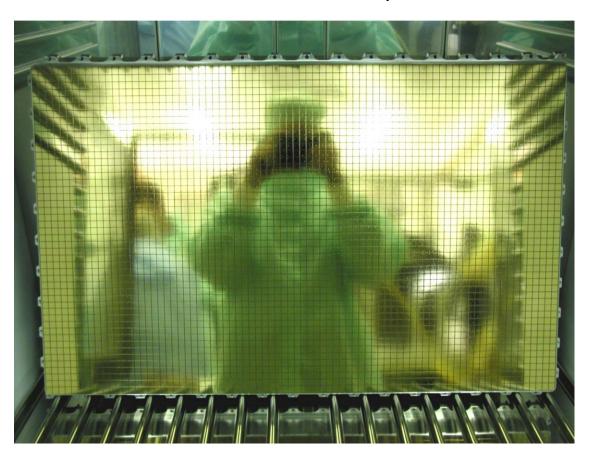


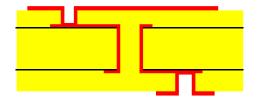


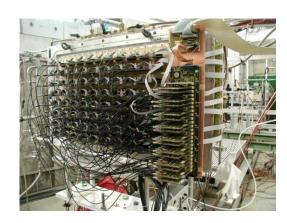
#### PAD

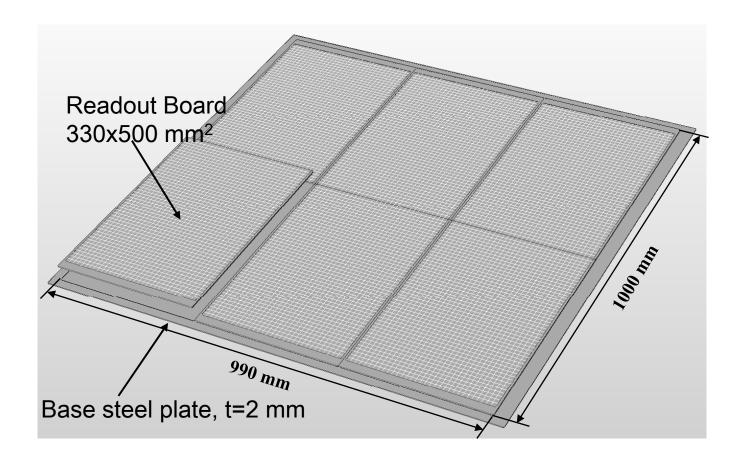
Alice HMPID cell made of 2 PCBs

- -Hermetic by design
- -Special NI/AU and polishing for CSI deposition
- -Front end electronics in the back
- Max size : 600 x 500 per board



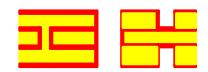


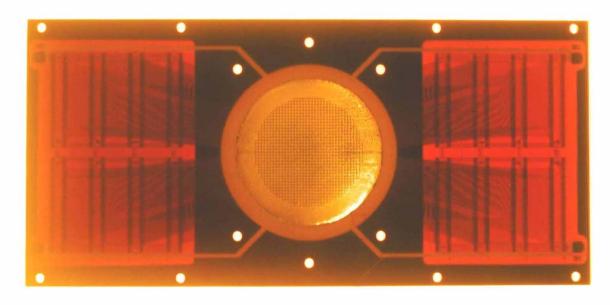




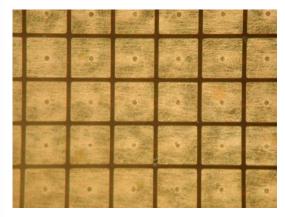
Example of sharing for larger read out board

## Pixel





1024 pads on a diameter of 35mm 8 layer PCB INFN PISA GEM detector



Close-up view Pad: 1mm Pitch: 1.05mm

Biggest problems:

-Line width

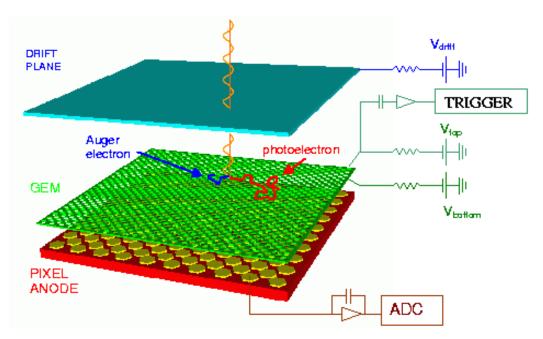
-layer count

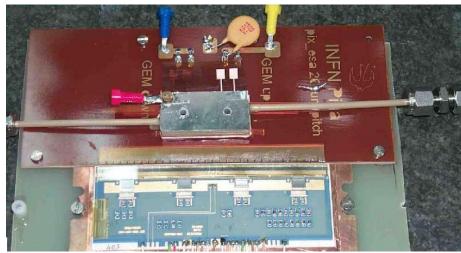
Limitations:

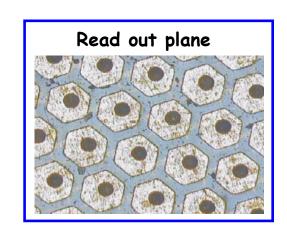
- 600mm x 450mm Process

- Density of connections 3cm x 3cm

#### Pixel read-out: an example, the PCB approach

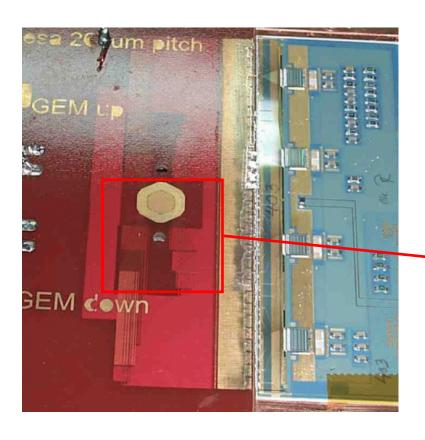






• Read out pitch: 260 µm

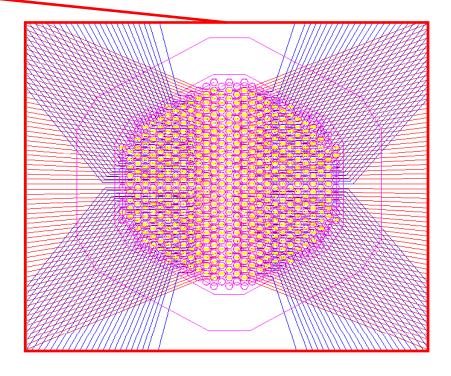
512 electronic channels from a few mm<sup>2</sup> active area are individually read out by means of a multi-layer PCB fan out



#### PCB approach

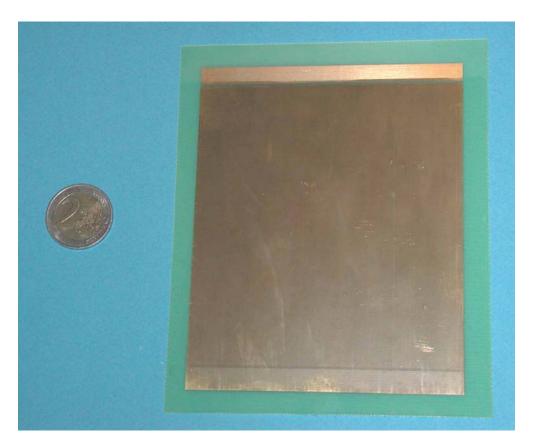
- 6 layers SBU (sequential build up) with 40um microvias.
- Minimum track width and space 40um

- Crosstalk between adjacent channels (signals traveling close to each other for several cm).
- Not negligible noise (high input capacitance to the preamplifiers).

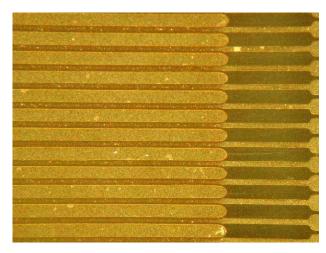


## **ACTIVE** read-out

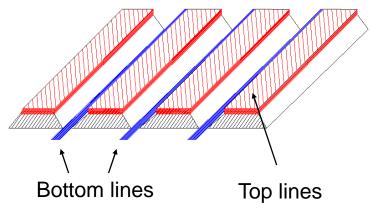
## Micro-groove



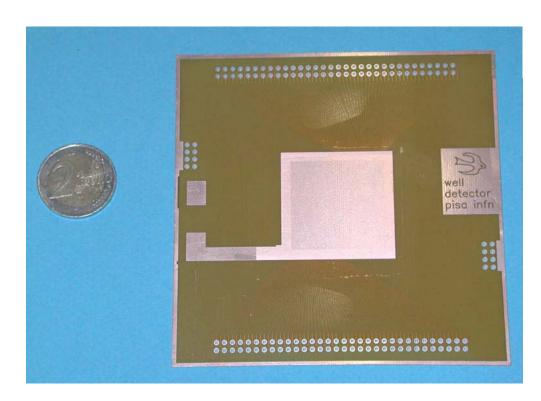
12 x 10cm groove detector Close to a MSGC INFN PISA/CERN

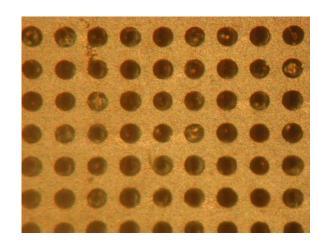


Close-up view

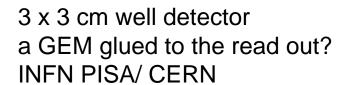


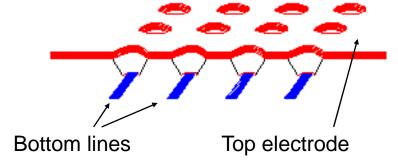
## Micro-well



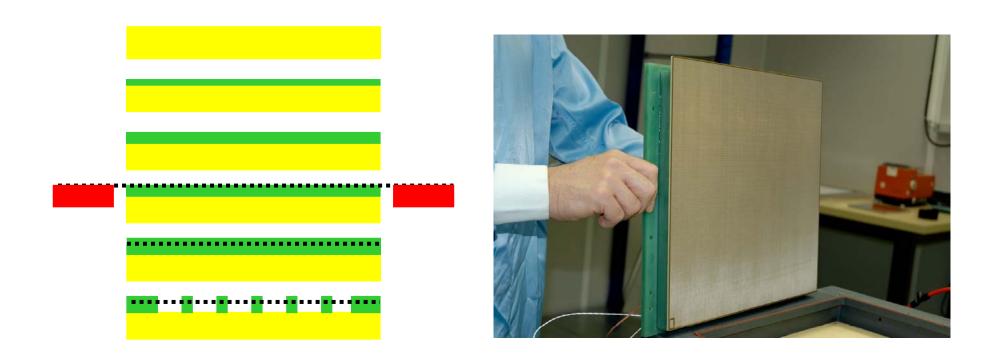


Close-up view





# Micromegas Bulk and Micro-Bulk

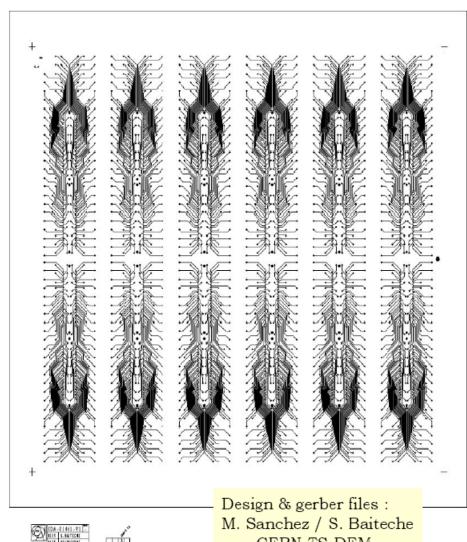


T2K experiment, 84 Modules in production at CERN

# Grounding and capacitive couplings

any effect?
One example

## T2K bulk detector Inner layer

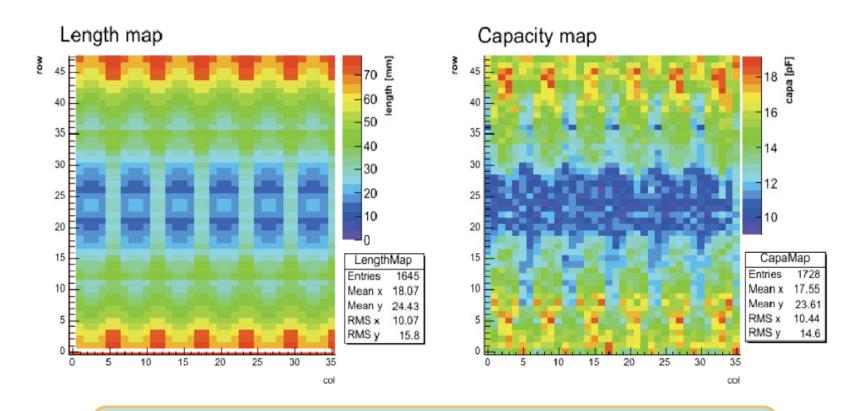








#### MM1-001 results: Capacity correction

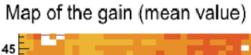


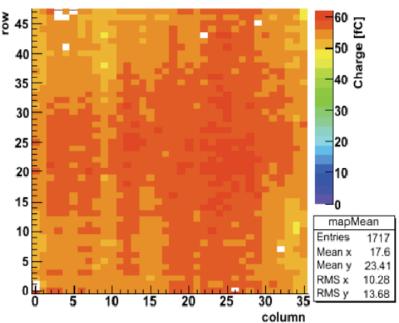
## Capacitance depends on length of connecting lines Capacitance changes gain



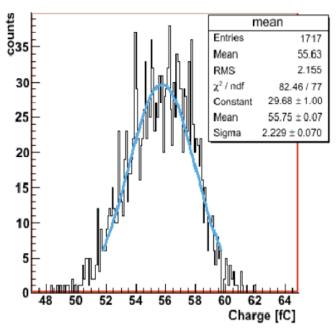
#### MM1-001 results: Gain

## Gain variation: 4%





#### Distribution of the mean





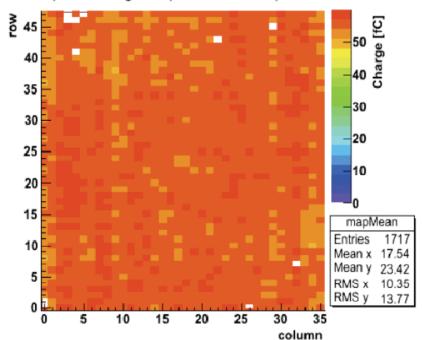
#### MM1-001 results: Gain corrected



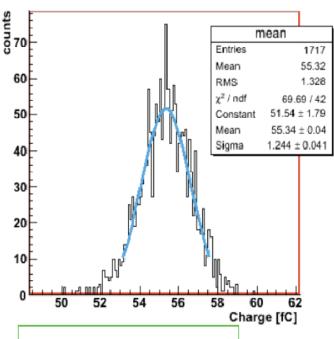
$$G_{corr} = \frac{G_i}{G_{fec}(x)} \times G_{moy}(14)$$

Gain variation: 2.2%



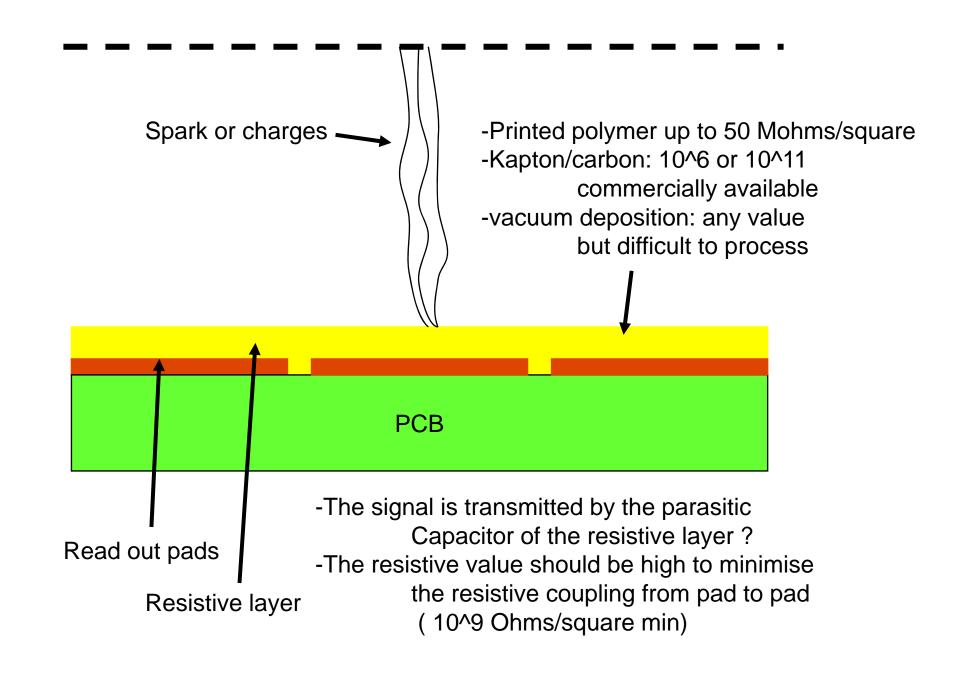


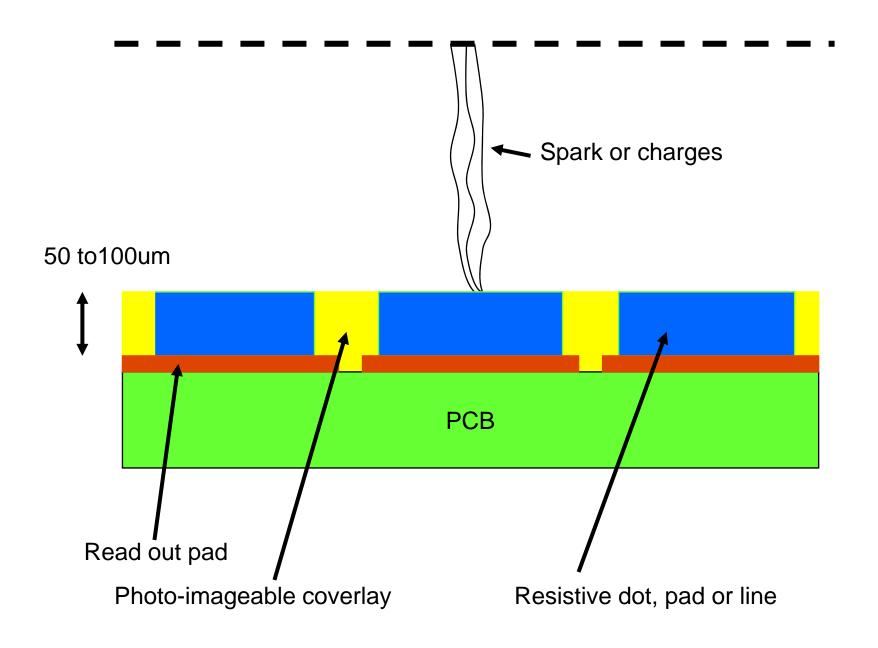
#### Distribution of the mean

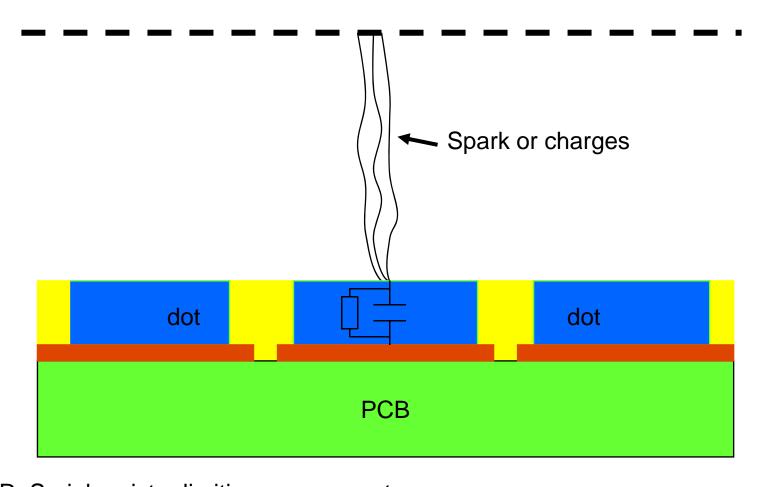


Gain: ~1550

## Resistive spark protection

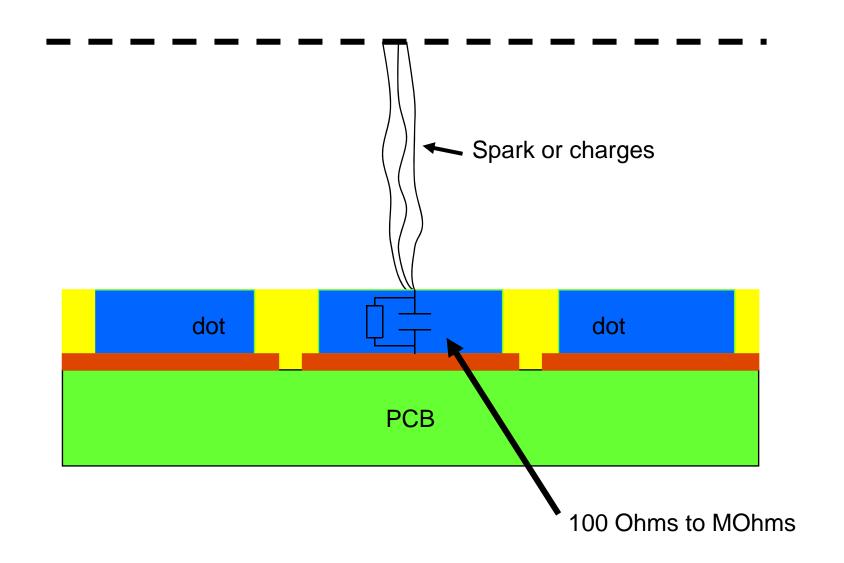


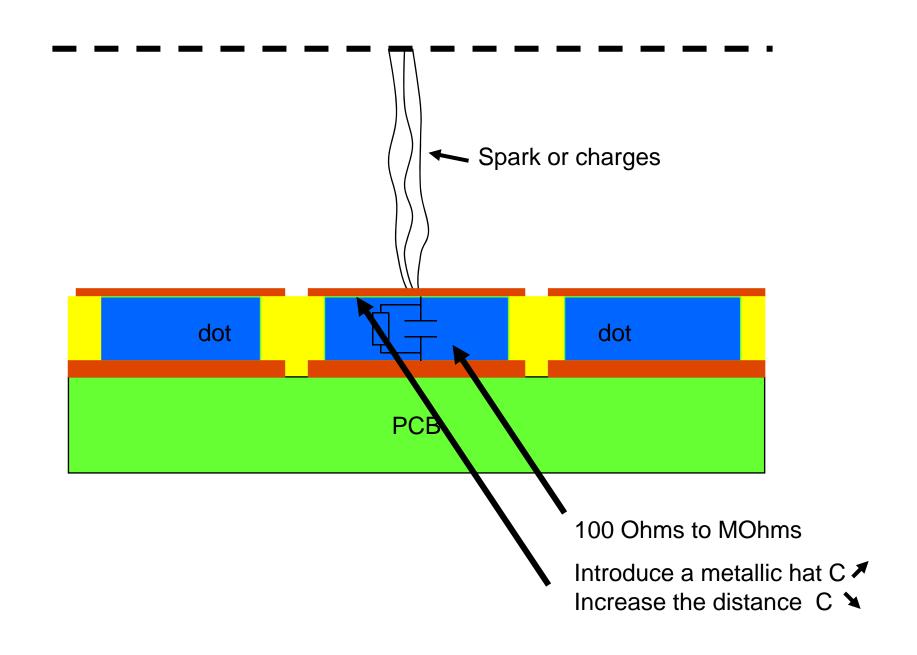


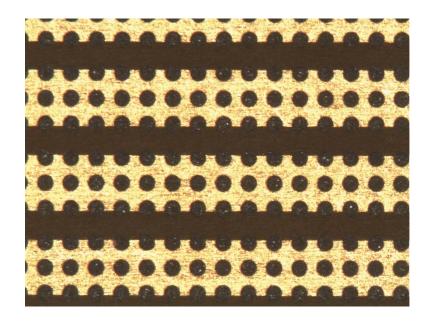


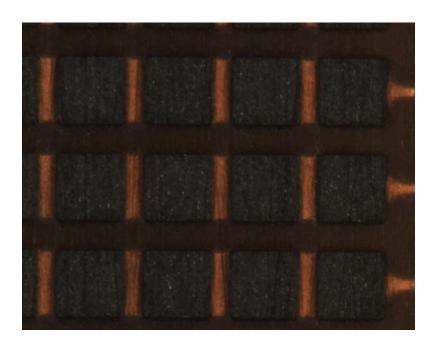
R: Serial resistor limiting max current
High enough to limit energy of spark?
Low enough to remove charges
C: Serial parasitic capacitor High pass filter
High enough to transfert signal charges
Dielectric quality--> spark protection?

C or R doing spark protection?









#### Dot architecture

-Min: 0.15mm diameter

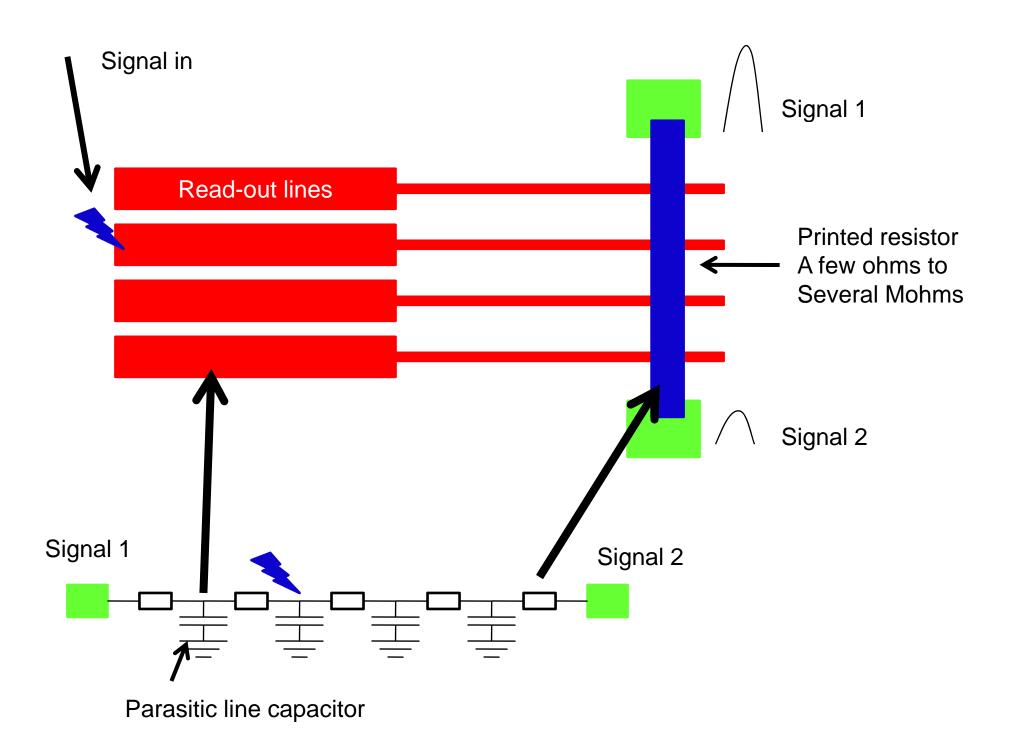
-Pitch: 0.25mm

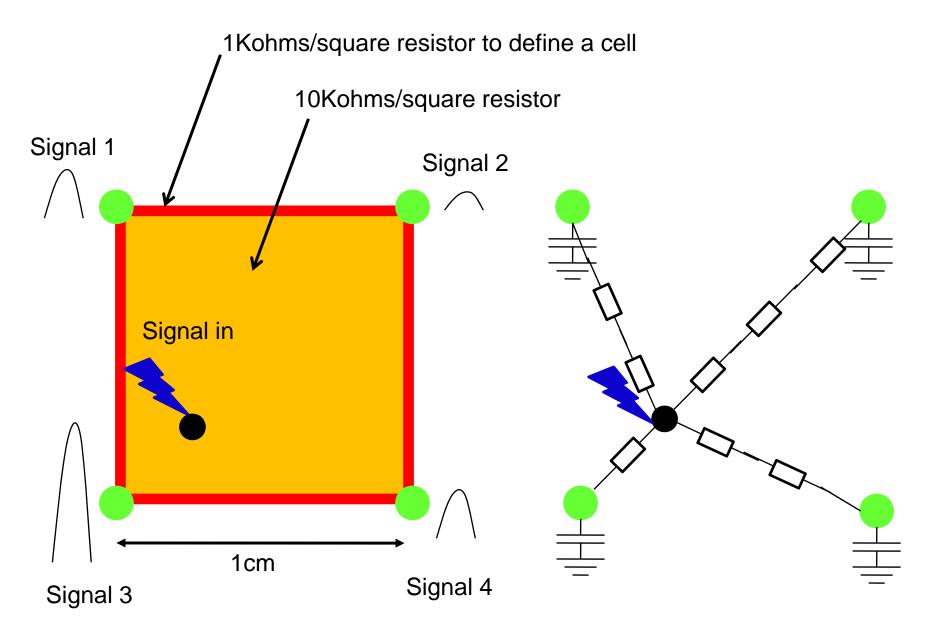
-Possibility to avoid alignment

between track and dots

Pad architecture -needs alignment

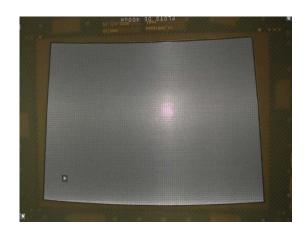
## Resistive spreading



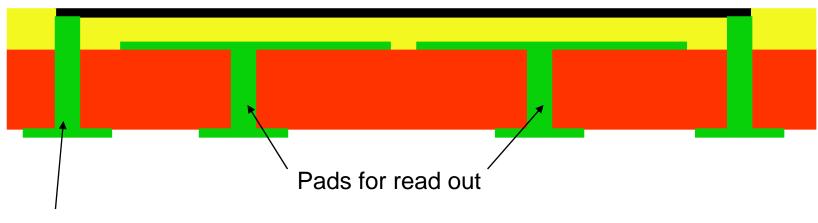


Nuclear instruments and Methods in Physics Research A 523 (2004) 287-301

Copper
Prepreg defining the capacitor dielectric
FR4
resistive layer for charge spreading

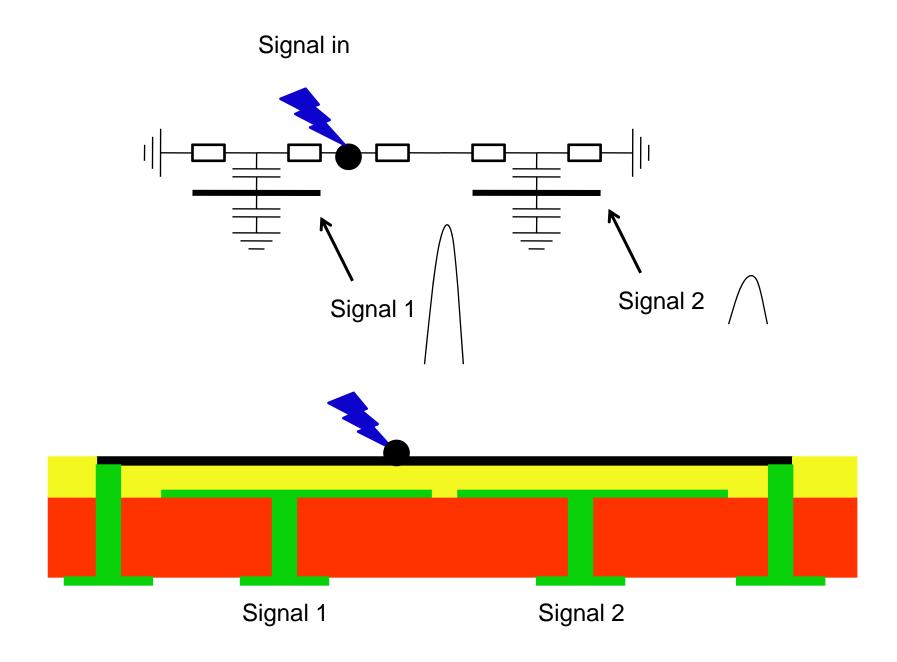


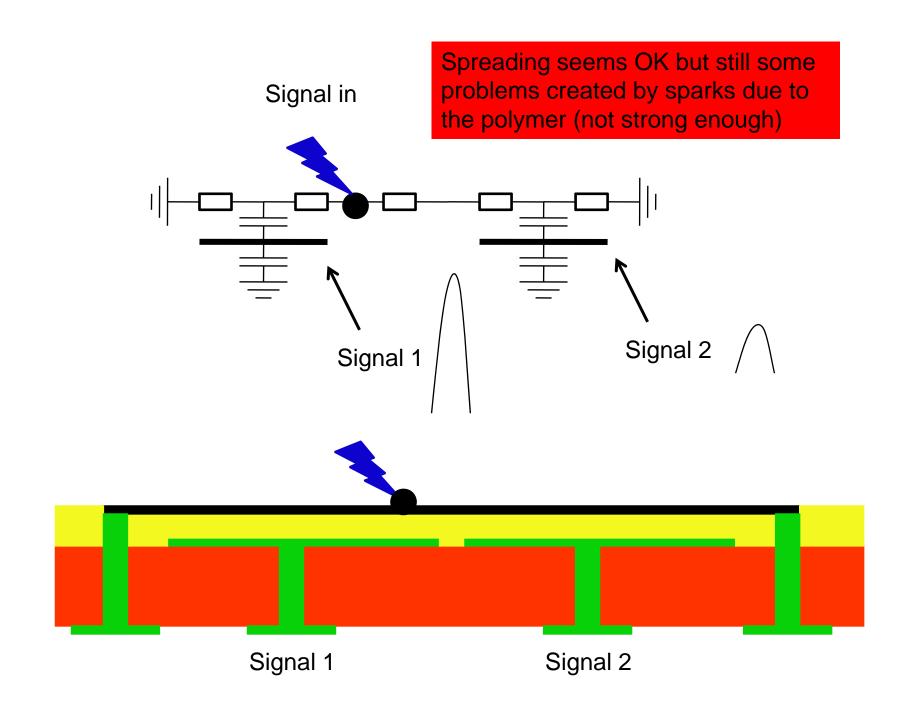
200mm x 150mm Bulk micromegas with Resistive spreading

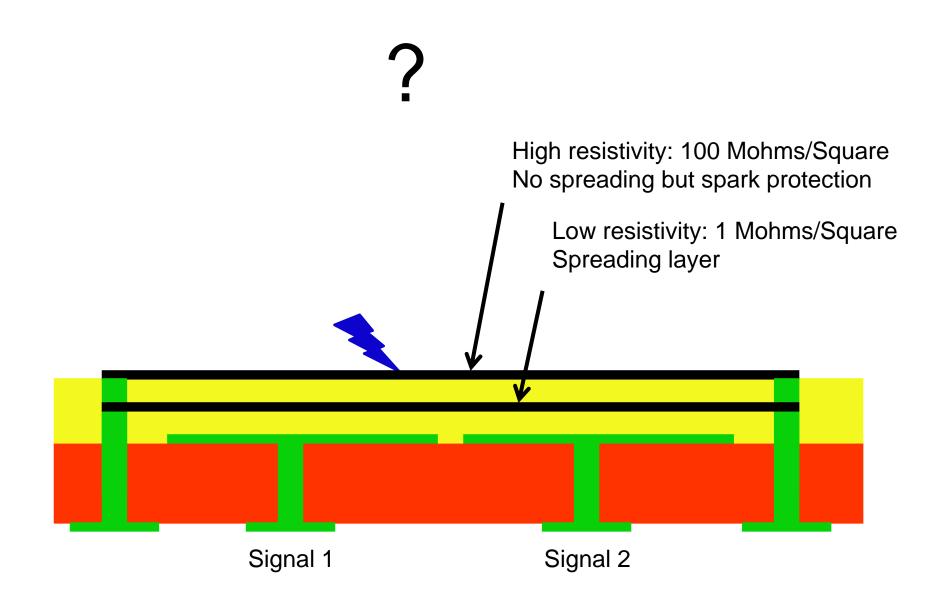


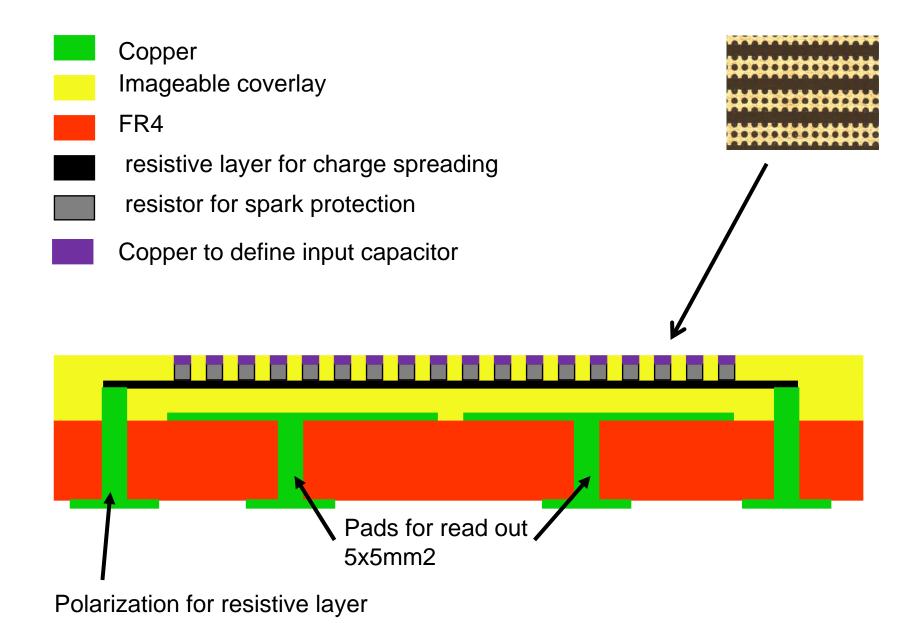
resistive layer polarization

For details contact Paul Colas









## Thank you