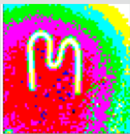

# 3D PACKAGING SOLUTIONS FOR FUTURE PIXEL DETECTORS

Timo Tick – CERN

2.4.2009

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# Outline

- Motivation
- Pixel detectors - Currently used packaging technology
- 3D packaging concept
- Trough Silicon Vias (TSV)
  - TSV fabrication process
  - Medipix2 collaboration's and VTT's joint TSV development project
  - Test vehicle
- Area Array solder joints between silicon detectors and a substrate
  - Challenges
  - Substrate candidates
  - Area array solder joint reliability
- Conclusions

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# Motivation

- In the upcoming luminosity upgrade of the LHC hybrid pixel detectors are considered to be used more extensively
  - Closer to the beam:
    - Smaller material budget, pixel size, dead space
  - Further away from the beam
    - Larger areas, Cost efficiency

- New techniques are needed to realize these detector surfaces with low costs

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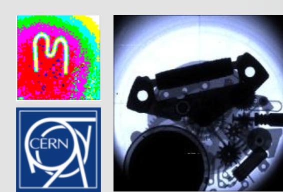
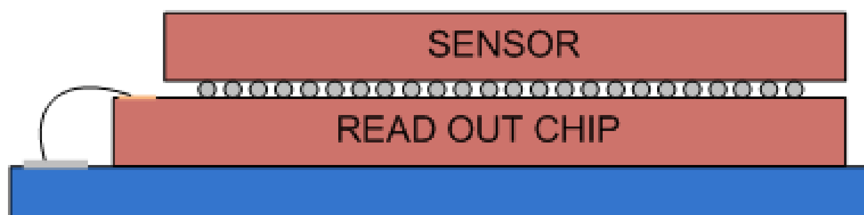
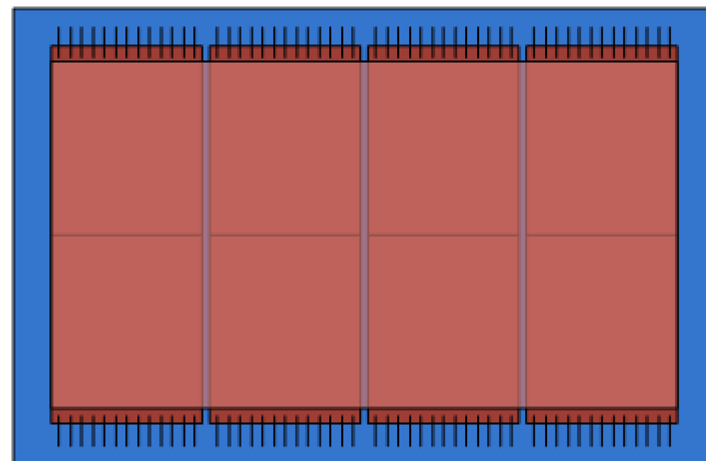
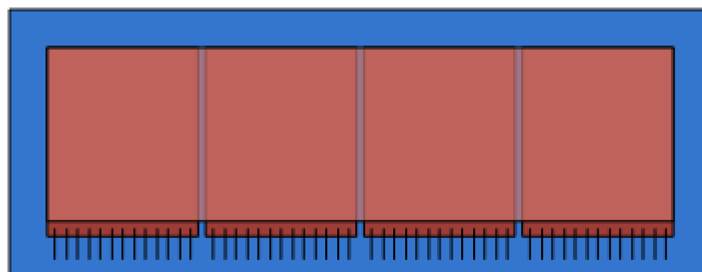


# Currently used technology

- Sensor chips are flip-chip bonded to the Read out Chips (RoCs)
- Detector assembly is wire bonded to a circuit board
- Ladders: multiple RoC's in a row on a single sensor
- Two row ladders possible





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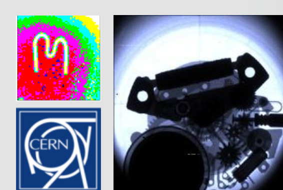
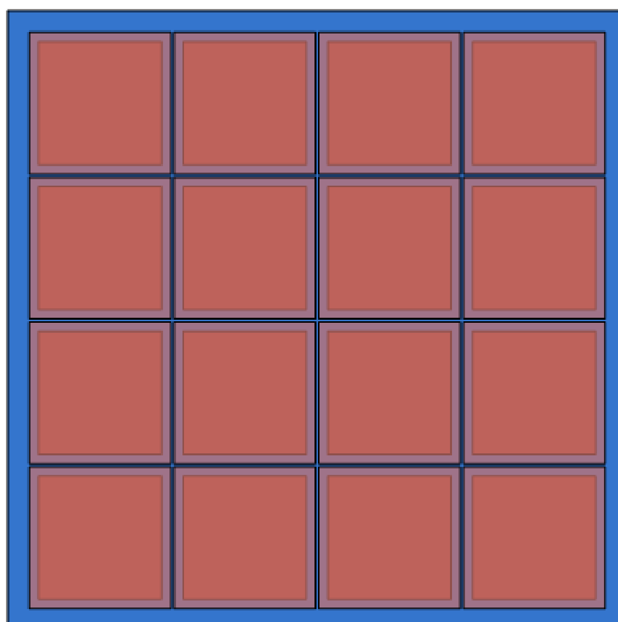
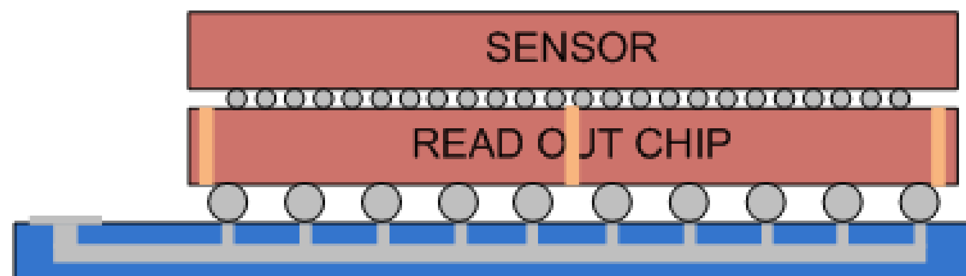


# 3D packaging concept

- Sensor and RoC are flip chip joined
- Detector I/O signals are taken through RoC with Through Silicon Vias (TSV) and redistributed
- Detector assembly is attached on a circuit board with Ball Grid Array (BGA) solder joint
- Large area tiling:
  - Module of multiple RoC’s on a single large sensor
  - Multiple modules of single RoC on a sensor tiled on a large substrate



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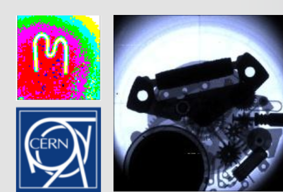

# 3D packaging challenges

1. TSV process has to be developed
   - Multiple providers of TSV processing are required in the future; high energy physics community is working with multiple partners: IMEC, IZM, VTT

2. The feasibility of bonding LARGE silicon chips with BGA solder joints has to be evaluated
   - Currently no work is being done?

3. The Sensor – to - RoC bump bonding costs have to be reduced
   - The cost of bump bonding a single detector unit has been ≈ 200 €
   - Bump bonding is the most expensive phase in life cycle of detectors
   - Work that aims to significantly lower bump bonding costs has been started at CERN

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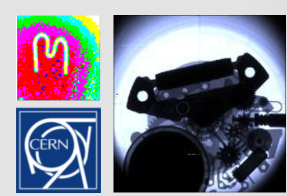

# Challenge 1: Through silicon vias

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# CERN – VTT TSV project

- Medipix collaboration has started a join development project with VTT (Technical Research Centre of Finland) to establish a TSV process for Medipix chips
  - Medipix project utilizes the technologies developed for particle detection in high energy physics experiments for medical imaging purposes
- VTT has previously participated in bump bonding of detectors for CERN (ALICE & LHCb) and Medipix collaboration
- VTT possesses the required equipment and expertise to create suitable TSV process for CERN's needs
- The aim is to develop via-last Cu TSV filling process, which could be later used in production of 3D detector assemblies

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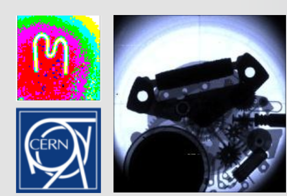
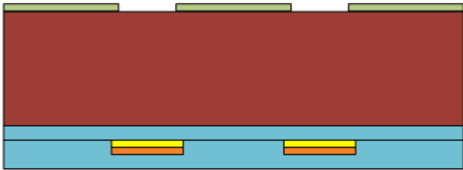


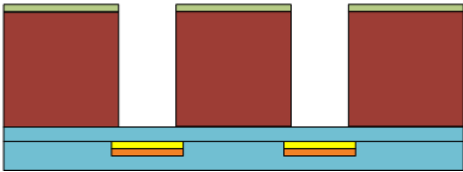
# TSV Fabrication

1. Wafer with buried TSV landing pads

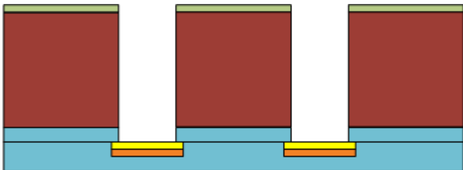
2. Deposit etch mask



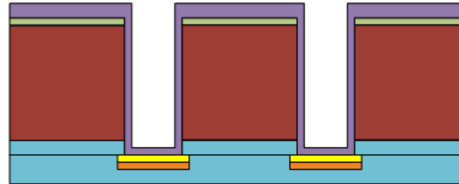
3. Etch vias



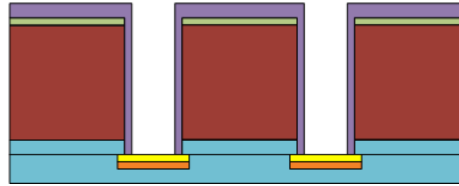
4. Etch through insulation



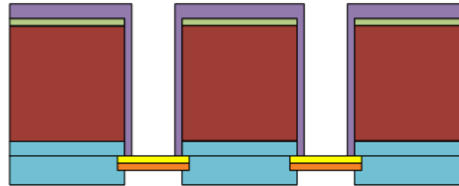
5. Deposit insulation and barrier



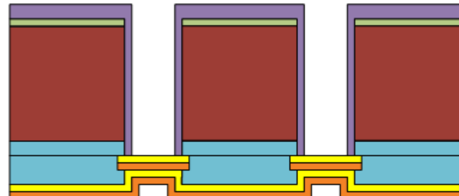
6. Etch insulation



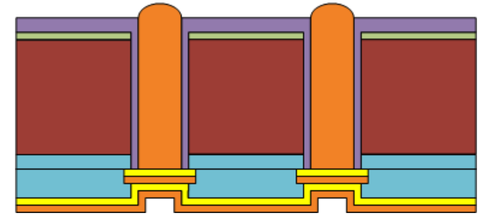
7. Reveal landing pads (active side)



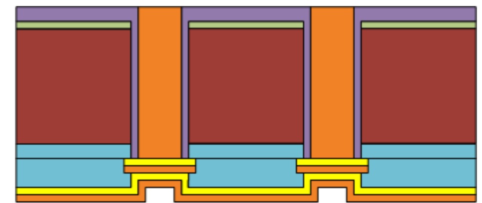
8. Deposit field metal



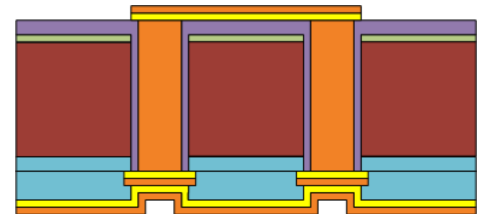
9. Electroplate copper



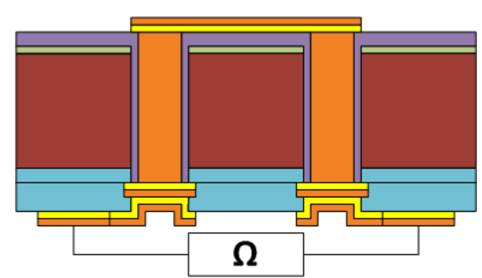
10. CMP



11. Rerouting

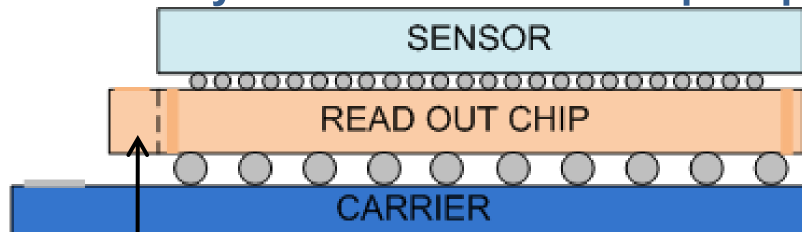


12. UBM



# Test Vehicle

- A test vehicle has been designed at CERN that can be used in the development and evaluation of all the three key technologies:
  - Through Silicon Vias, Low cost bump bonding, Large area BGA interconnections on different substrates
- Additionally the test vehicle can also be used to develop and evaluate assembly procedures and equipment
- Medipix3 look-alike
  - Dummy RoC: Same size, flip chip pad positions, TSV count and positions
  - Dummy Sensor
  - Daisy chain structures of flip chip bumps, TSV's and BGA joints




Probing pads can be diced off for 2D tiling of structures.

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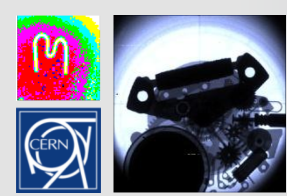


## Challenge 2: Area array solder joints

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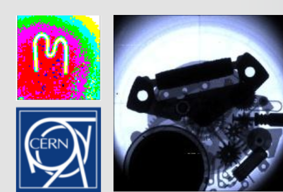
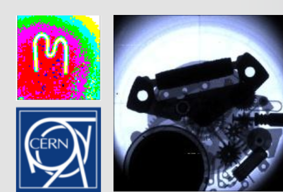


# Potential substrate materials

- **Glass epoxy laminates (FR4): Traditional circuit board**
  - Cheap and very mature technology
  - High density wiring (HDI built-up technology)
- **Low Temperature Cofired Ceramics (LTCC): Multilayer ceramic circuit board**
  - Mature technology
  - High density wiring
- **Carbon Composite Laminates (CCL): FR4 board with carbon composite sheets**
  - Compatible with traditional process -> cheap
  - Compatible with HDI built-up technology

| | Silicon | Low Temperature Cofired Ceramics (LTCC) | Glass Epoxy Laminates (FR-4) | Carbon Composite Laminate (CCL) |
|---|---|---|---|---|
| CTE [ppm/K] | 2.6 | 6-7 | 16 | 1-10 |
| Thermal Conductivity [W/mK] | 13 | 2 | 0.25 | 80 |
| Density [g/cm$^2$] | 2.3 | 3 | 1.9 | 1.55 |
| Relative Permittivity | 11.7 | 5-8 | 4-5 | NA |
| Young's modulus [GPa] | 130 | 350 | 15 | 170 |
| | Si | LTCC | FR4 | CCL |
| Via size [um] | <1 | 100 | 50 | 50 |
| Through substrate via size [um] | 10-50 | 100 | 100 | 100 |
| Line width | <1 | 100 | 50 | 50 |
| Line pitch | <1 | 200 | 100 | 100 |
| Substrate thickness | 100-300 | 500-5000 | 500-5000 | 500-5000 |



# Area array solder joint reliability

- Due to the different Coefficients of Thermal Expansion (CTE) of the silicon detector and substrate materials shear stress is experienced at BGA joints when the assembly undergoes a change in temperature (T)
- Solder joint's shear stress ξ follows the relation:

$$\xi \propto \frac{\Delta CTE \cdot \Delta T \cdot \text{Distance from Neutral Point}}{\text{Stand off Height}}$$

- The number of cycles to failure for Pb-Sn solder joints is known to follow the Coffin – Manson relationship

$$N_f \propto \left(\frac{1}{\xi}\right)^{1.9}$$

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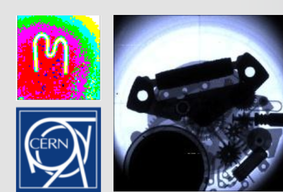
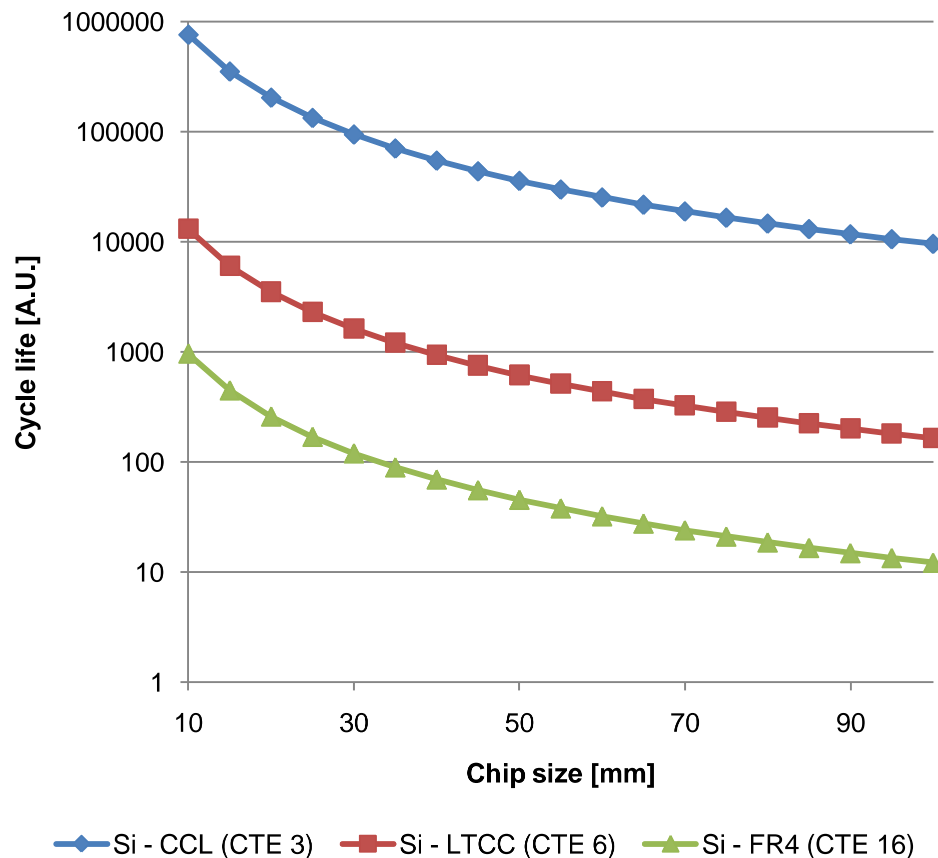


# Area array solder joint reliability

- Cycle life calculations for chips mounted on CLL, LTCC and FR4 substrates (Substrate Temp = Chip Temp)

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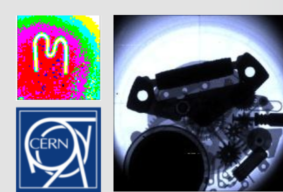

# Area array solder joint reliability

- Cycle life of joints when chip is running at different temperature than substrate
- Chip size 20x20mm, Ball size 0.5 mm

# Area array solder joint reliability

- It is impossible to define real life reliability of BGA bonded pixel detectors without accelerated environmental tests (and/or FEM modeling)
- Not much data available about the reliability of LARGE (e.g. the 10x10 cm designs proposed for CMS upgrade) silicon chips FC/BGA mounted on various substrates
  - Large chips such as high end processors are normally mounted on small chip carrier boards with underfill and they have much higher I/O counts (smaller bumps)
- Design rules need to be established
  - To avoid the evident problems of not having enough reliability
  - And to avoid sacrificing the performance or cost advantages on having too much reliability
- Finally, what is reliable enough?

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# Conclusions

- 3 dimensional packaging offers many advantages for pixel detectors:
  - Shorter interconnections → faster signal transmission & lower power consumption
  - Area-array tiling possibility → enables large-area tiling of detectors with single chip assemblies
- Work is being done under three subjects:
  - Trough silicon vias process is being developed together with VTT
  - Feasibility of joining large chips on various substrates with BGA solder joints is being studied
  - Low cost bump bonding techniques are being studied

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