An integrated DC-DC step-up charge pump for the serial powering scheme in ABCN (130nm)

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ACEOLE Six Months Meeting

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Outline

- Motivation,
- Proposed powering scheme for new ATLAS Inner Tracker,
  - Serial powering,
  - DC-DC conversion,
- Proposed scheme for serial powering,
- Overview of step-up charge pumps,
- Switched capacitor voltage doubler,
- Overview of step-down converters,
- Results from Cadence simulations,
- What has been done and plans for the future.

Some facts about powering in current ATLAS Inner Tracker

- The ATLAS Pixel and SCT power cables are above 100 m long and their resistance can be as high as 4.5 Ω,
- Power consumed by the SCT front-end electronics is 25 kW, a similar amount is lost in the power cables,
- Each front-end power module has its own power supply channel and cable,
- The space available for power cables from the tracker through the ATLAS detector is strictly limited and cannot be increased.

Requirements for new ATLAS Inner Tracker

After the High Luminocity Upgrade

- The number of channels in SLHC tracker will be increased 10 times,
- The readout chips of the upgraded ATLAS tracker will operate at a reduced voltage but will consume similar currents as the current tracker,

The new solution for power management has to be found

Requirements for voltages and currents (128 channels / chip)

ASICs for new ALTAS Inner Tracker will be designed in CMOS 130nm (or below) technology

Current requirements:

$$I_{analog} < I_{digital}$$

Estimation for currents

$$I_{analog} \approx 16mA \text{ (short strips option)},$$
$$I_{analog} \approx 32mA \text{ (long strips option)}.$$

$$I_{digital} \approx 51mA$$

Voltage requirements:

$$V_{analog} > V_{digital}$$

Two power domains (contributes significantly to power saving)

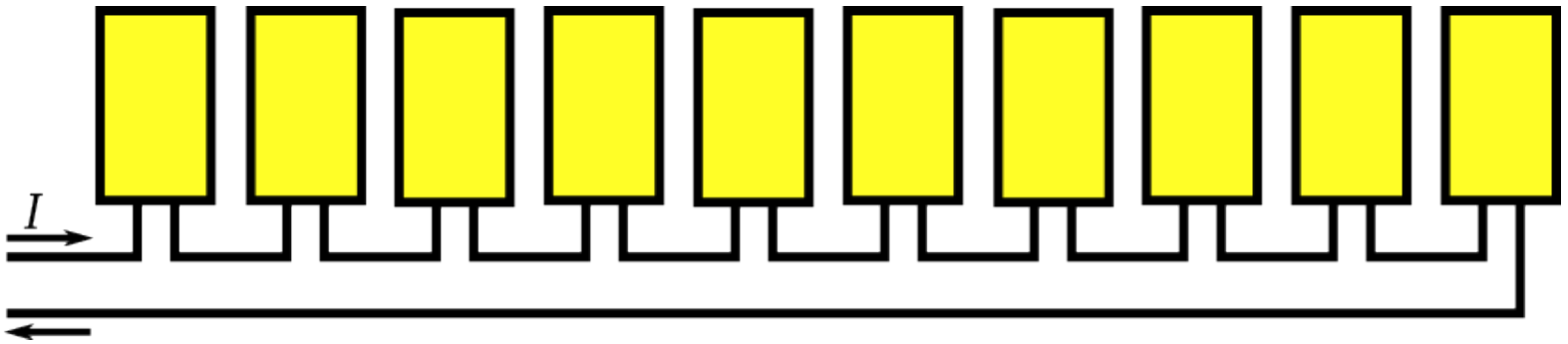
$$V_{analog} = 1.2V$$

$$V_{digital} = 0.9V$$

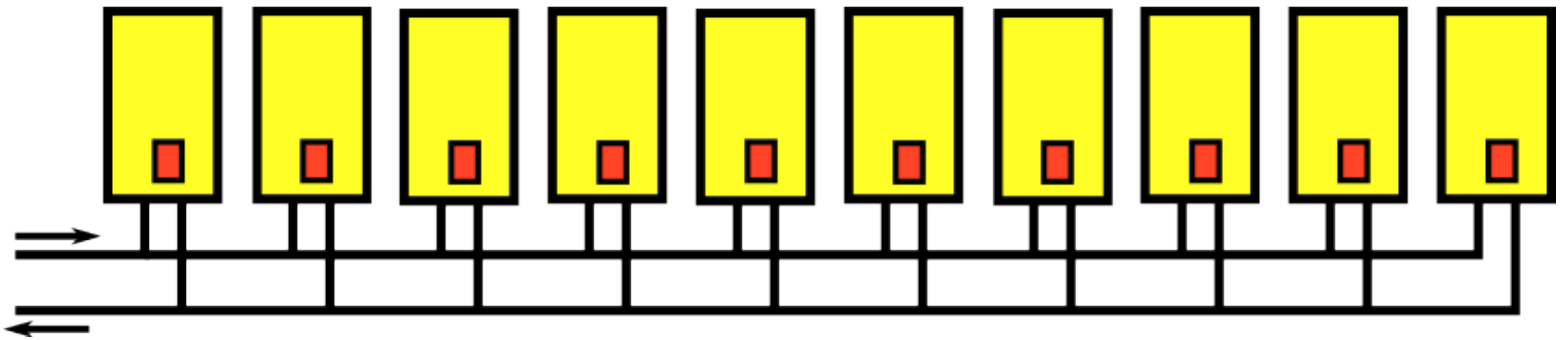
Possible solutions to the power distribution problem

Different powering schemes have been investigated

- Serial powering of detector modules

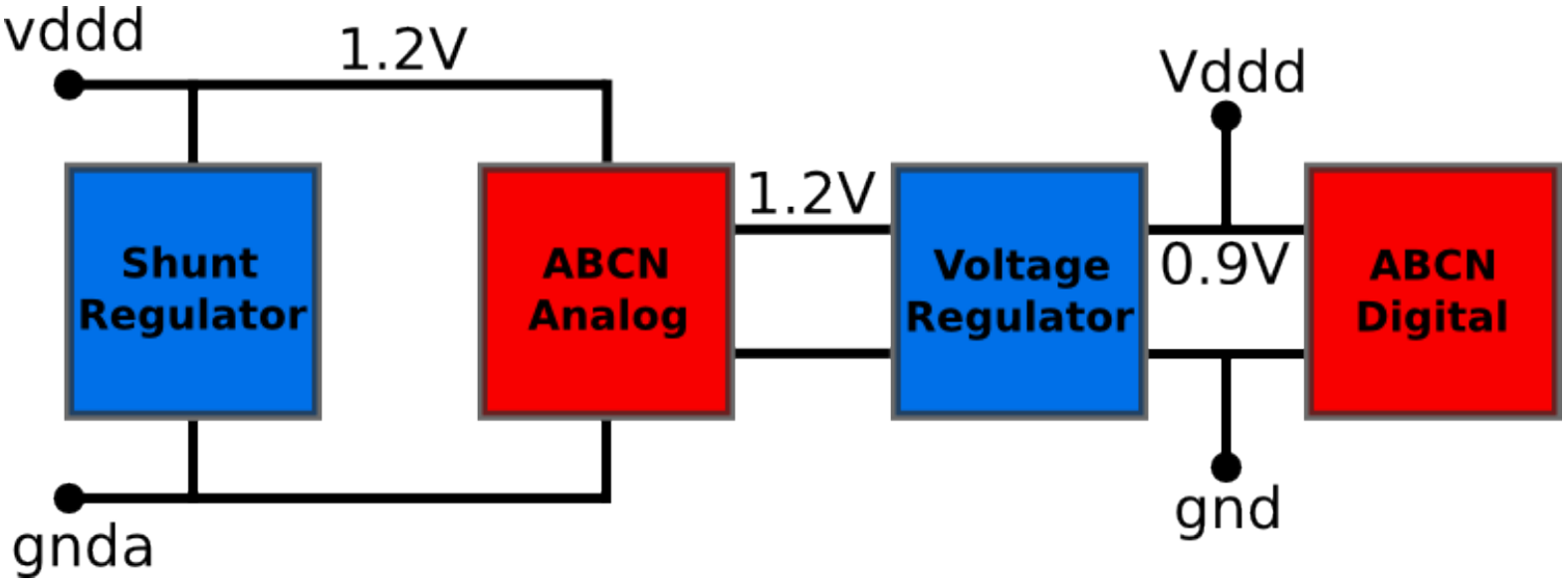


- Parallel (or independent) powering of detector modules combined with DC-DC conversion



Possible schema of power management in ABCN (130nm)

1

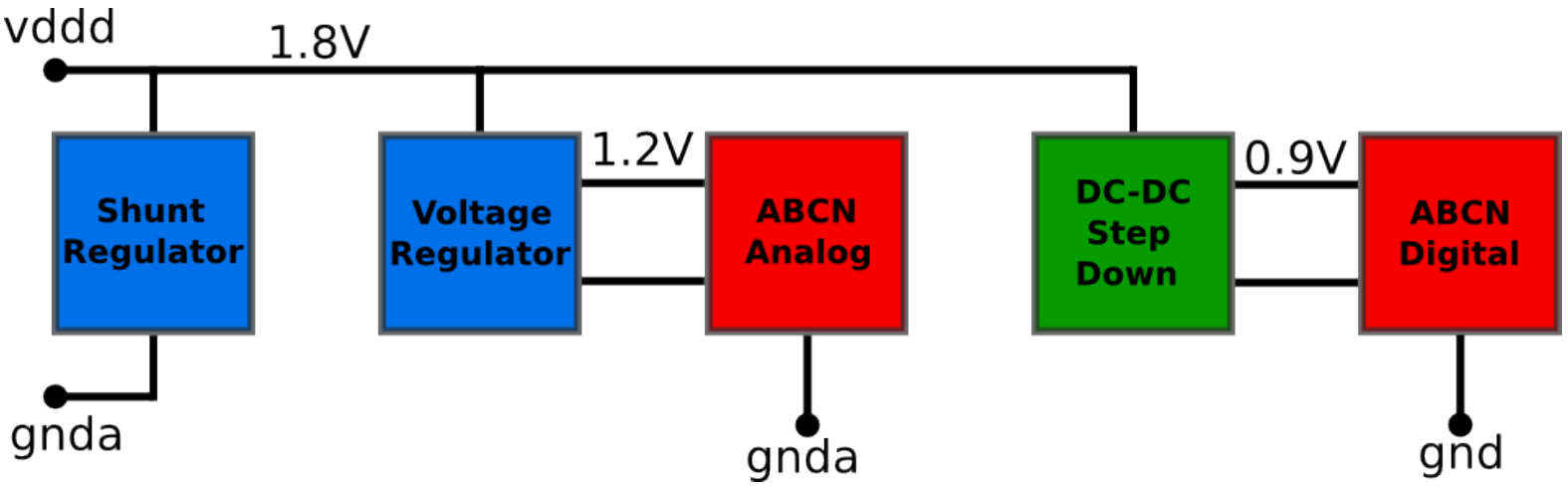


(+) Reasonable efficiency,

(−) Low quality of analog supply (no voltage regulator).

Possible schema of power management in ABCN (130nm)

2

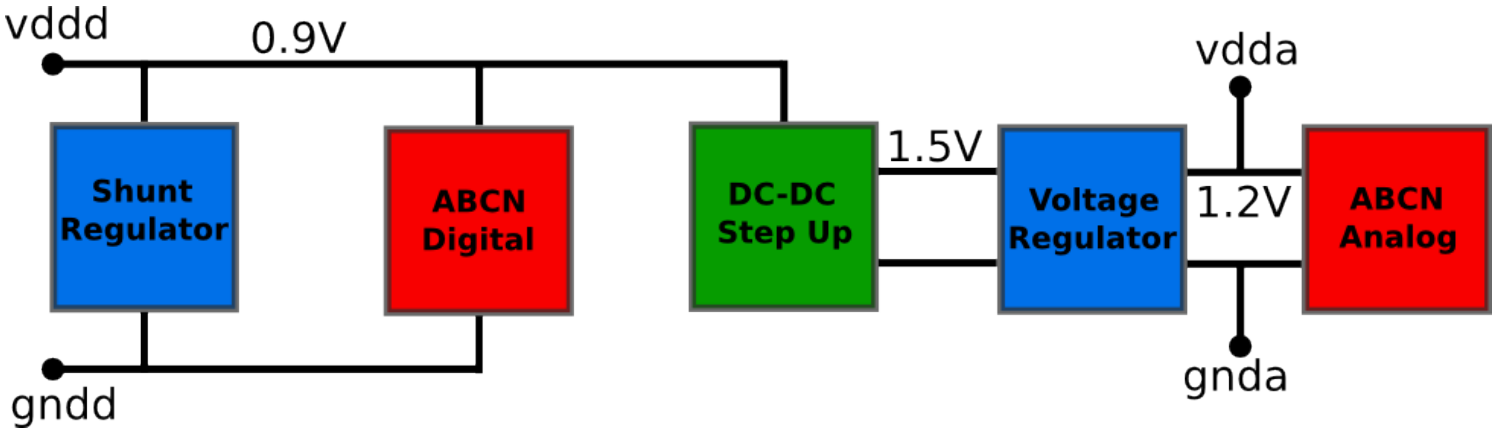


(+) Easy to obtain good quality of analog supply (voltage regulator with high drop $\Rightarrow$ easy to obtain good filtering efficiency),

(−) No regulation on digital power line (required low impedance of DC-DC since variable current is consumed in digital part).

Possible schema of power management in ABCN (130nm) (the most preferable solution)

3



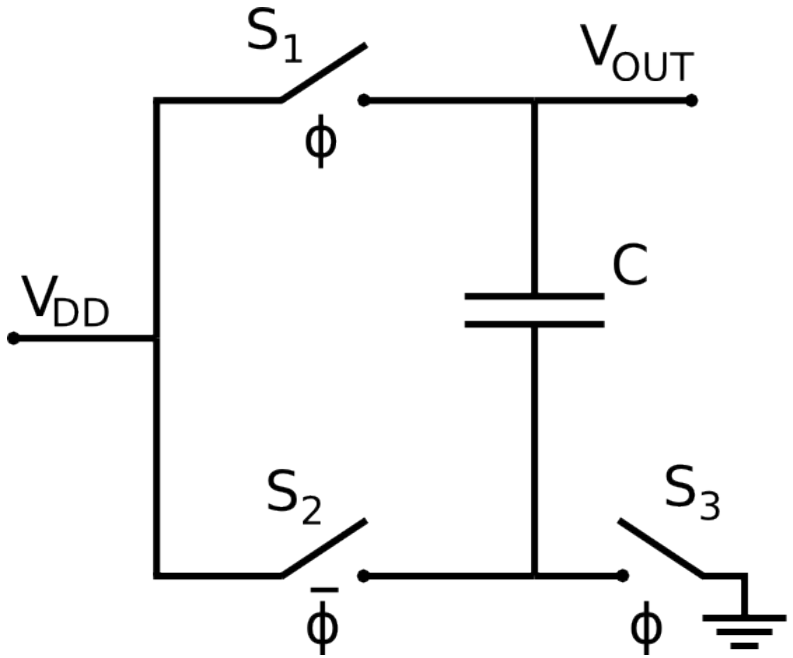
(+) Good quality of analog and digital voltage,

- low output impedance of shunt regulator,
- possibility to use classical linear regulator $\Rightarrow$ good filtering efficiency,

No regulation on DC-DC but constant power consumption in analog part.

Overview of the simplest voltage doubler

Charge pumps are circuits that generate a voltage larger than the supply voltage from which they operate



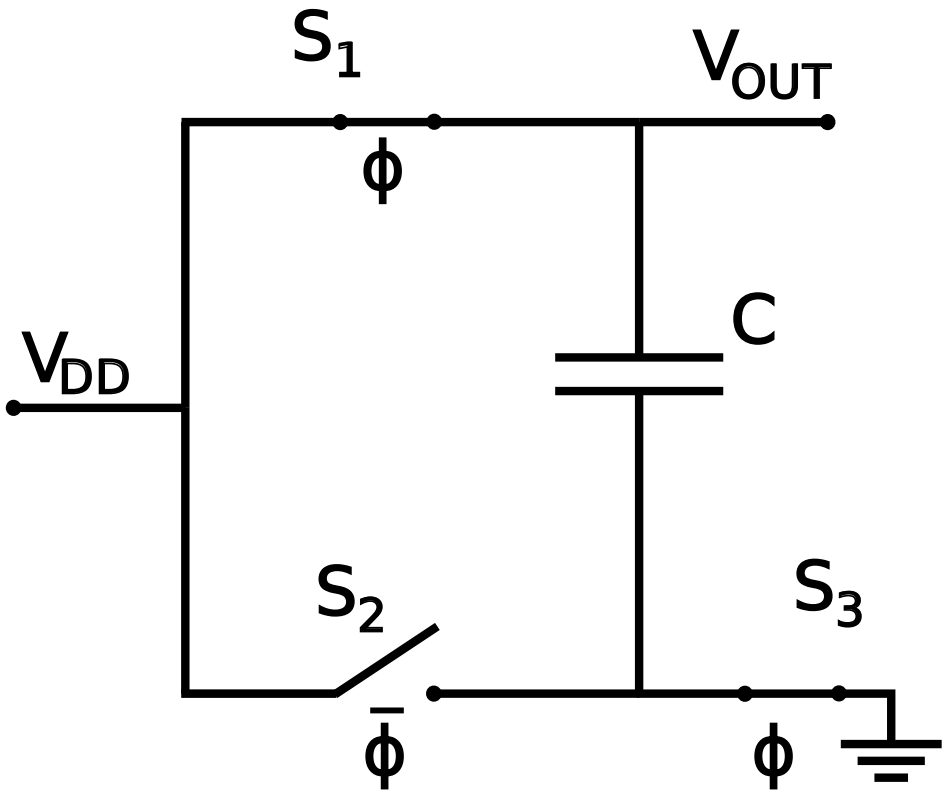
$$(V_{OUT} - V_{DD})\,C = V_{DD}C$$

and therefore

$$V_{OUT} = 2V_{DD}$$

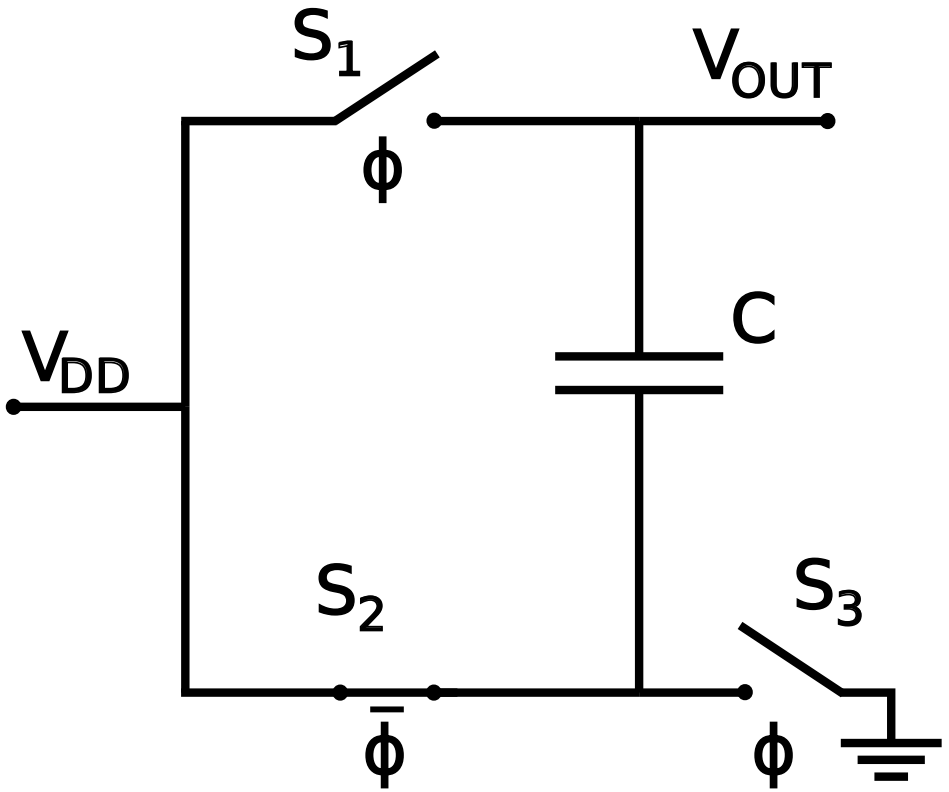
Simple voltage doubler (Phase 1)

- Switches S_1 and S_3 are closed,
- Switch S_2 is opened,
- Capacitor is charged to the supply voltage V_{DD}

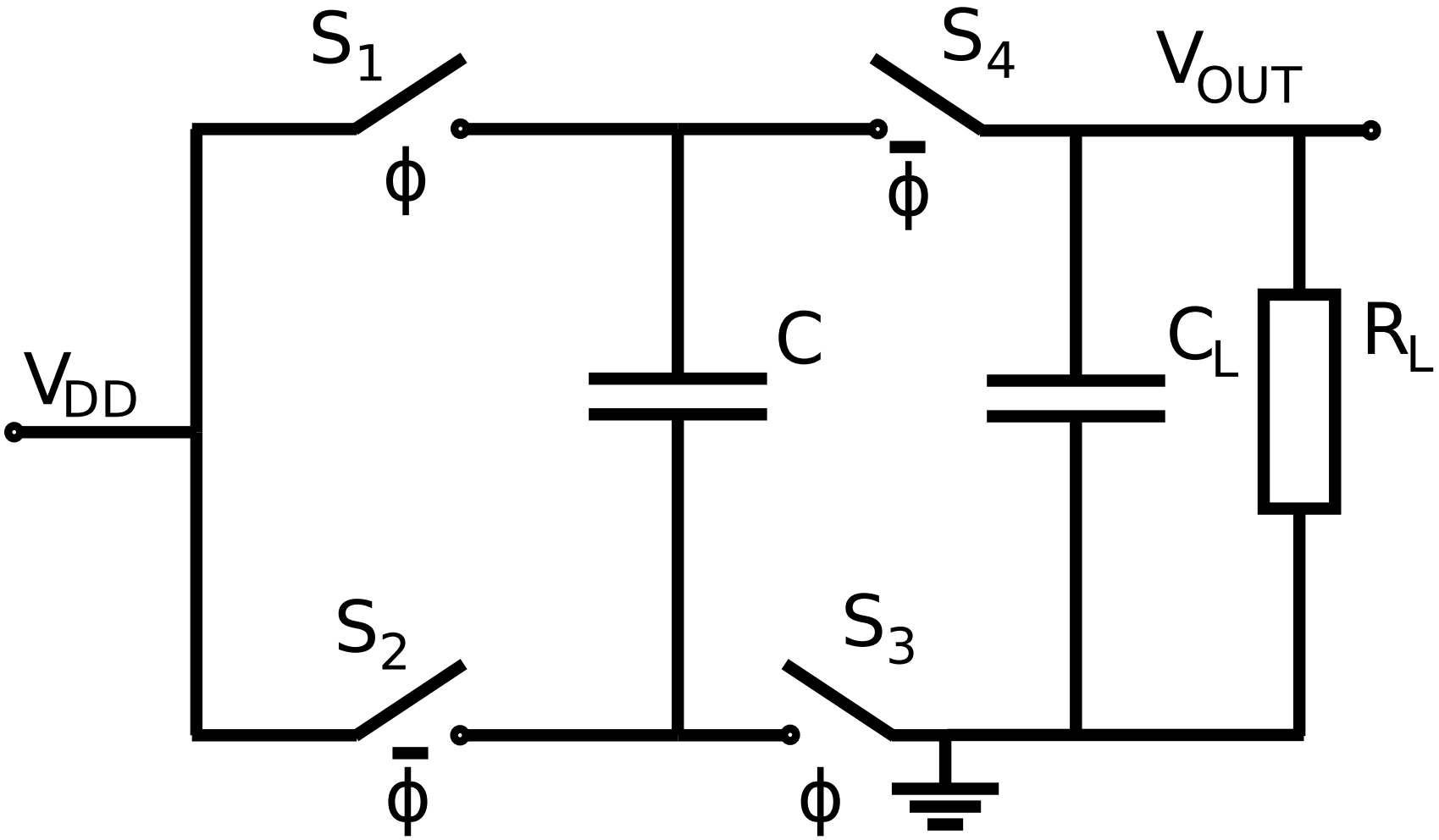


Simple voltage doubler (Phase 2)

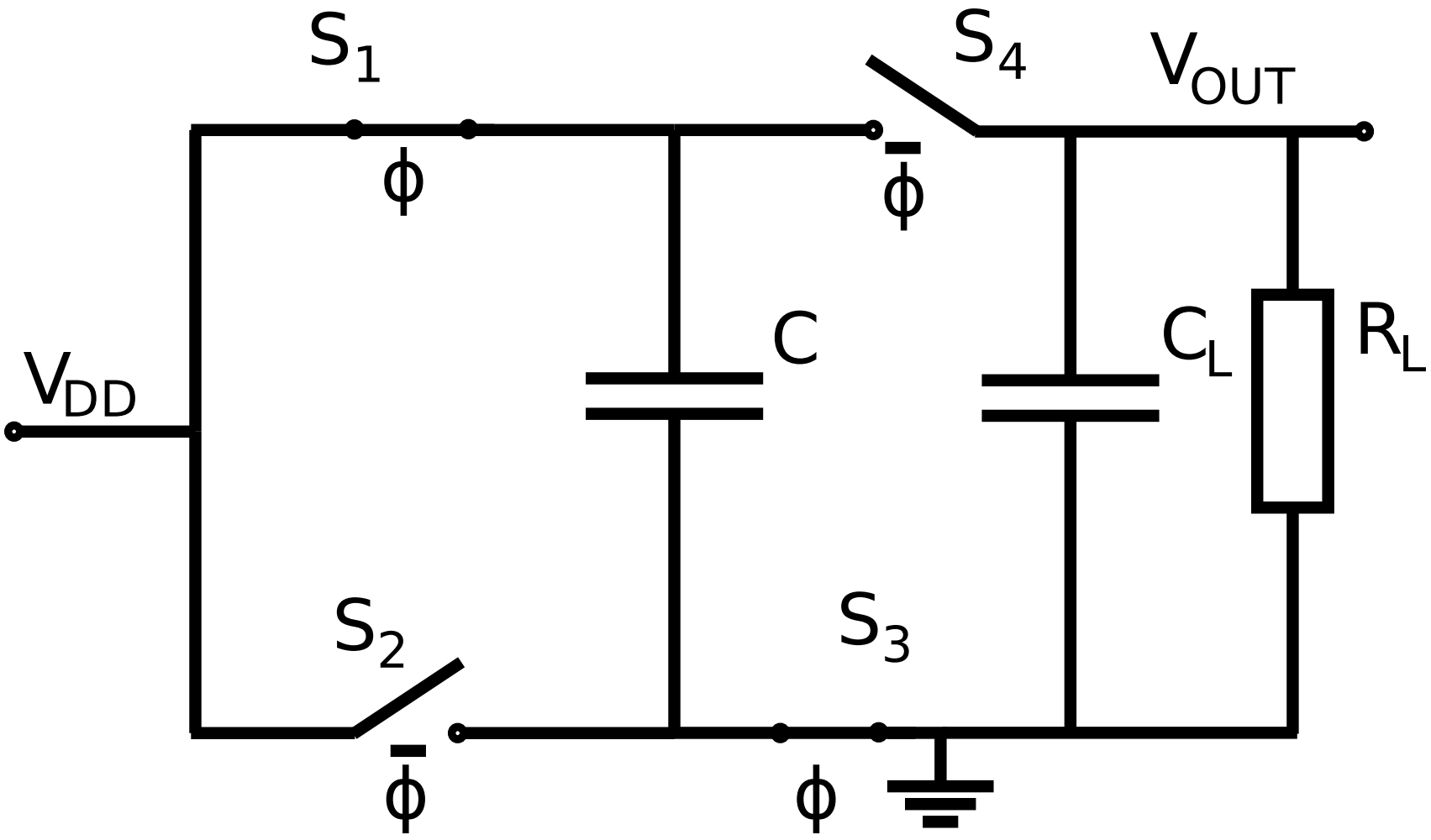
- Switches S_1 and S_3 are opened,
- Switch S_2 is closed,
- Bottom plate of the capacitor on V_{DD}, while the capacitor maintains its charge $V_{DD}C$ (from the previous phase).



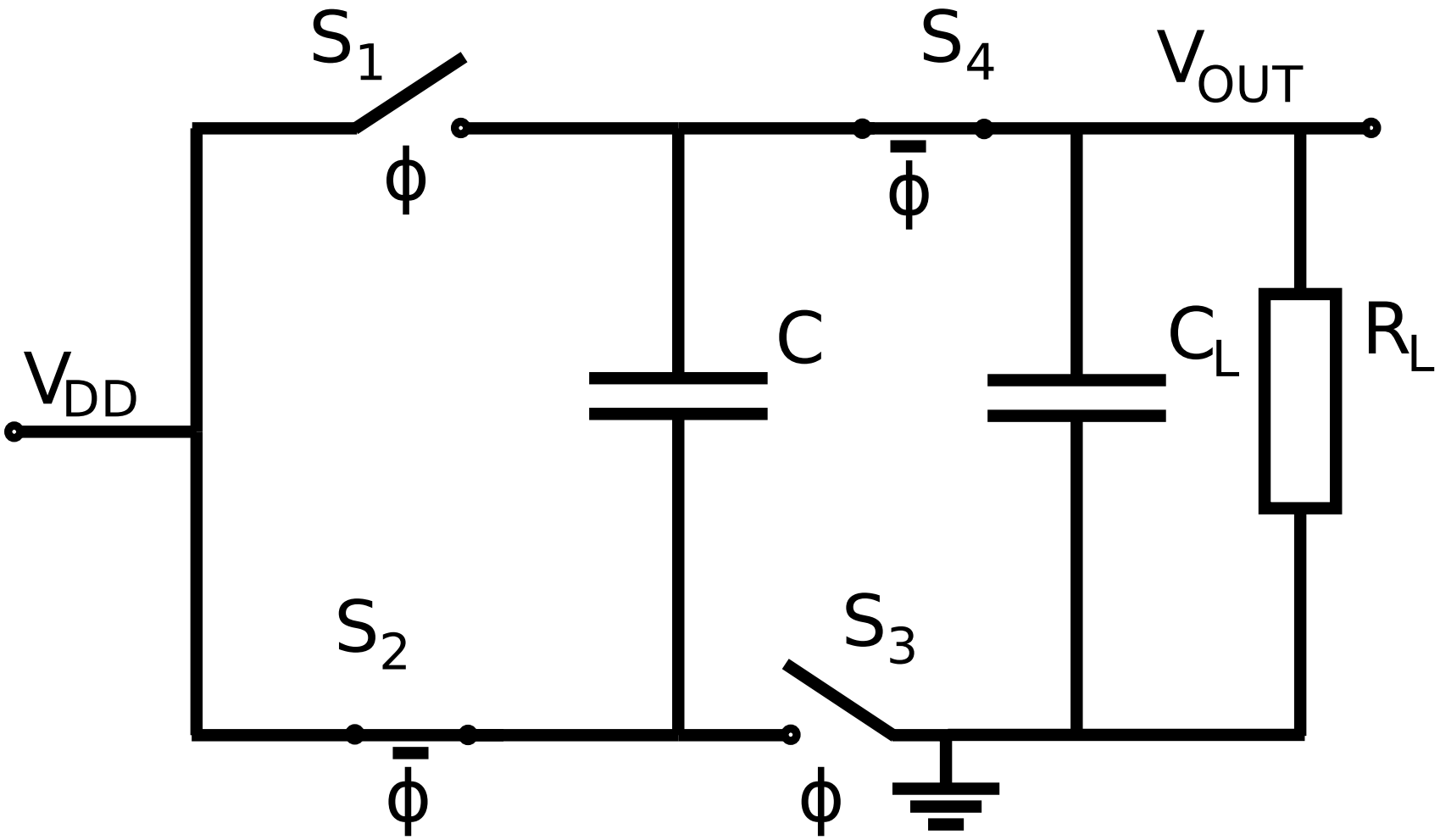
Practical voltage doubler with filtering capacitance



Practical voltage doubler (Phase 1)

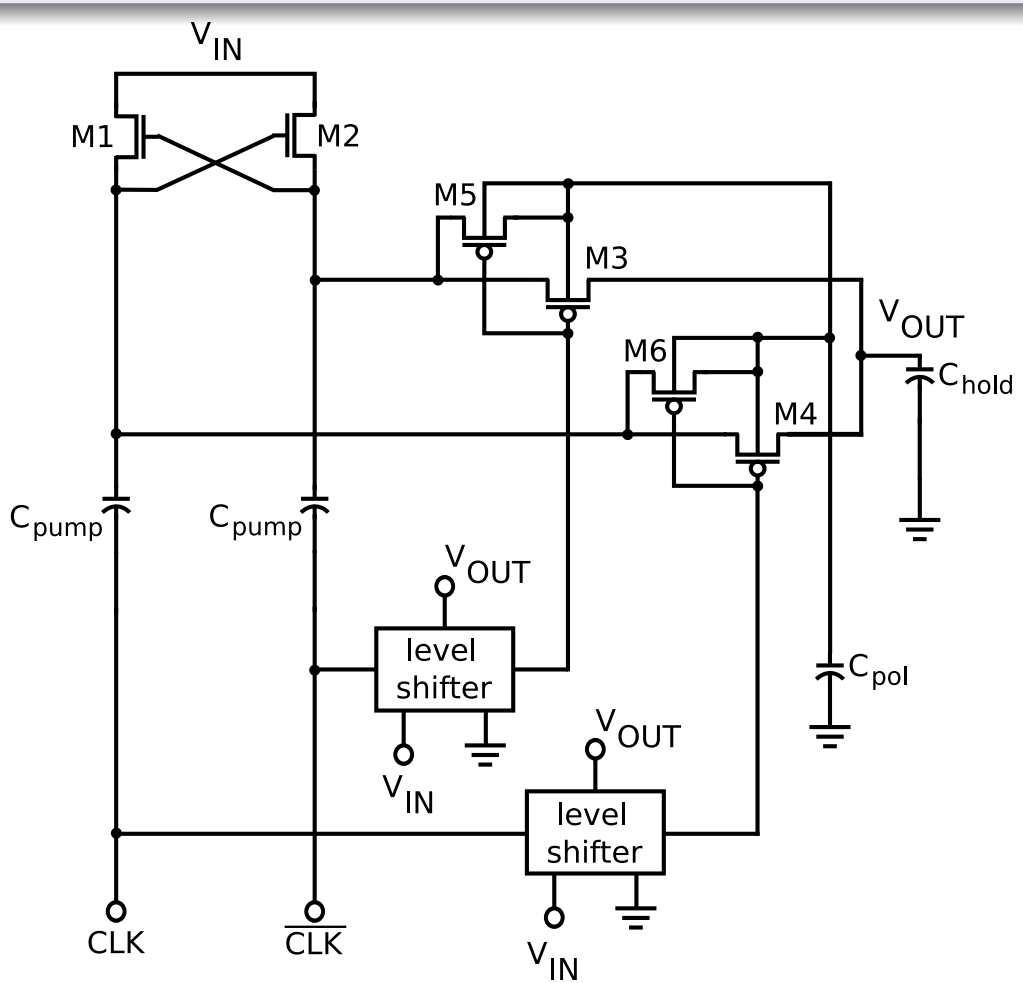


Practical voltage doubler (Phase 2)



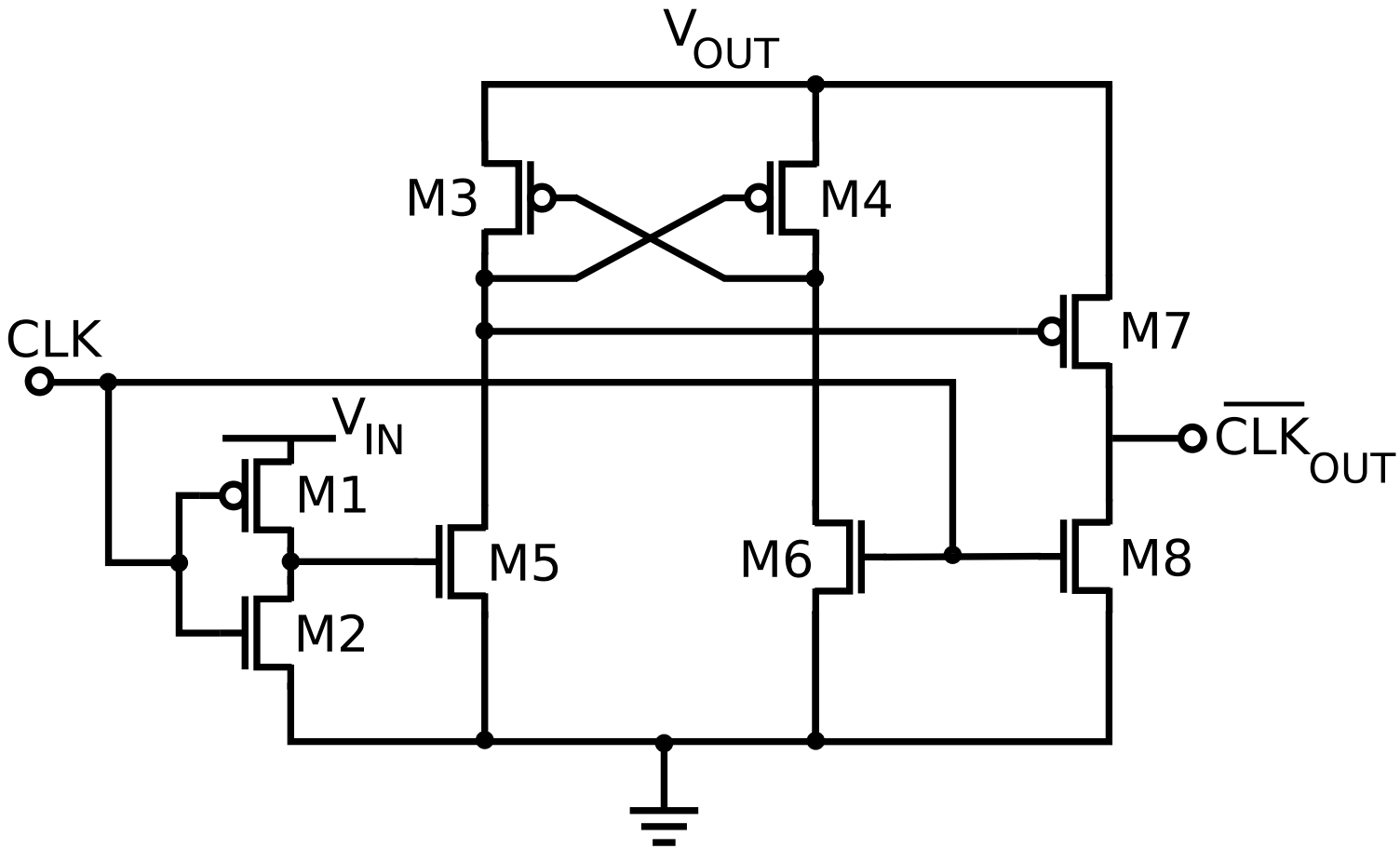
Solution for voltage doubler pumping on both clock edges

- Transistors (low V_{Th}) M1 and M2 use thin (2.2nm) gate oxide,
- Transistors M3 - M6 use thick (5.2nm) gate oxide,
- $V_{IN} = 0.9V$, $C_{PUMP} = 470nF$, $C_{HOLD} = 470nF$, $C_{POL} = 10pF$.

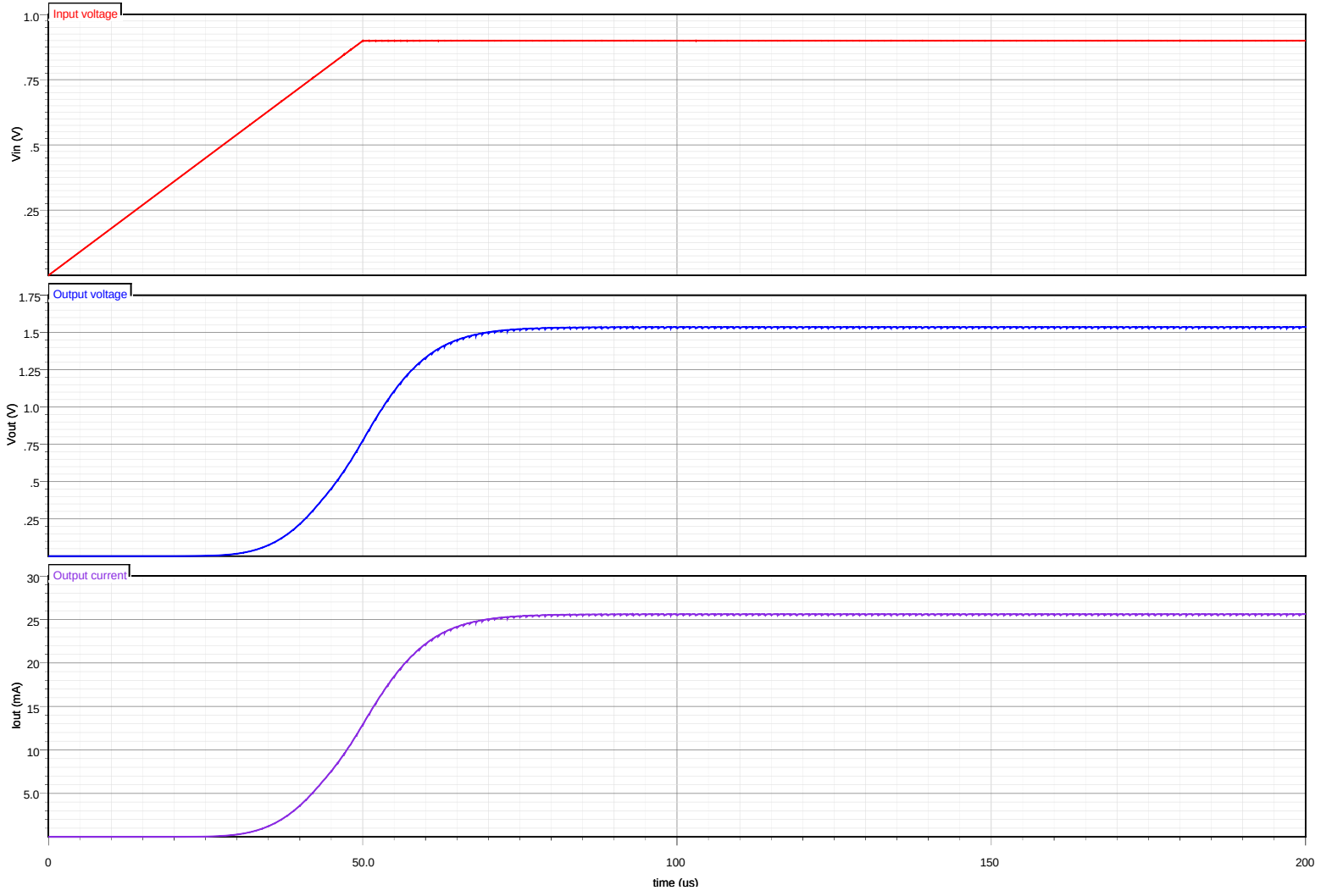


Practical solution for level shifter

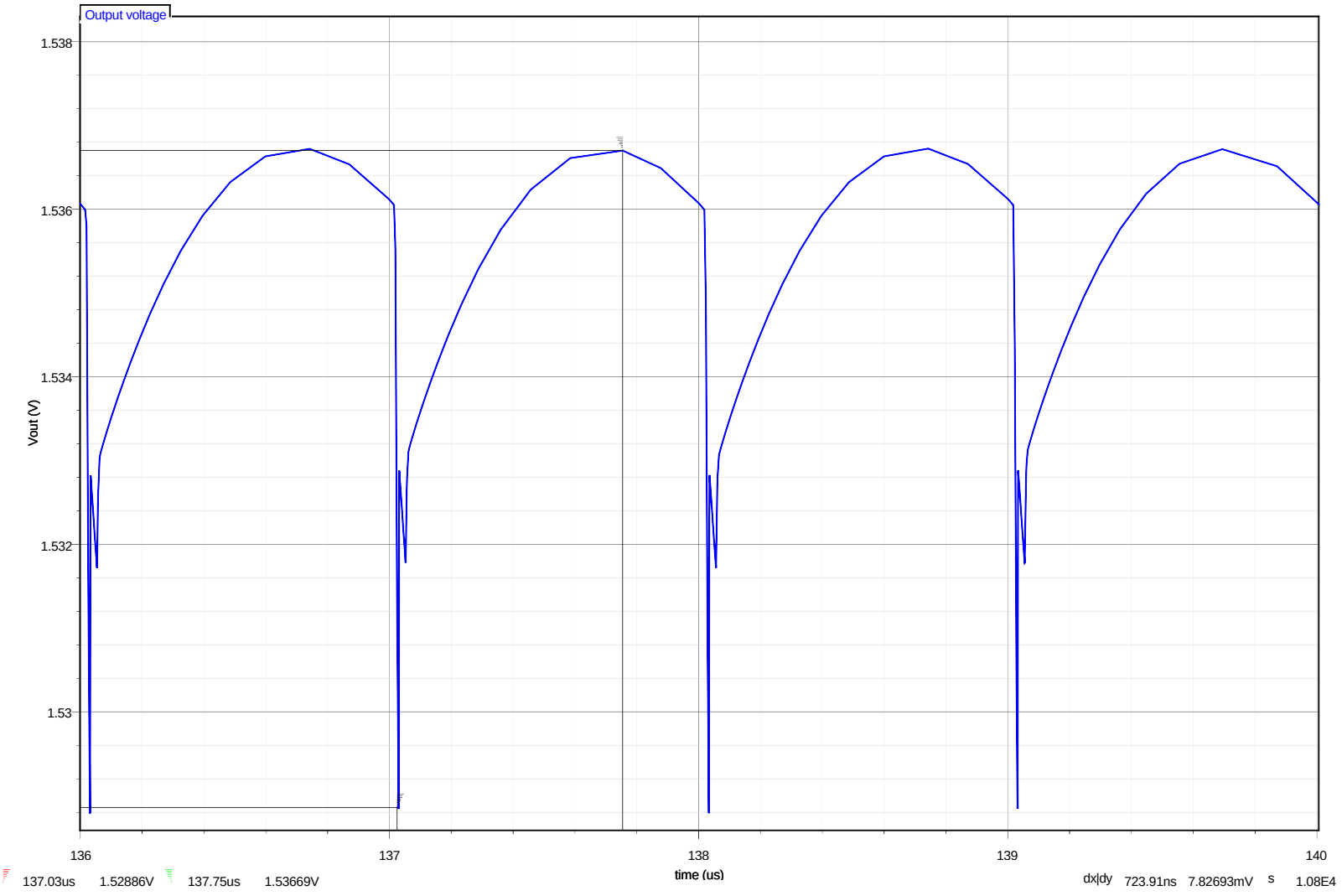
- Transistors M_1 - M_8 use thick (5.2nm) gate oxide.
- Main part of the circuit powered from output voltage, V_{OUT}.



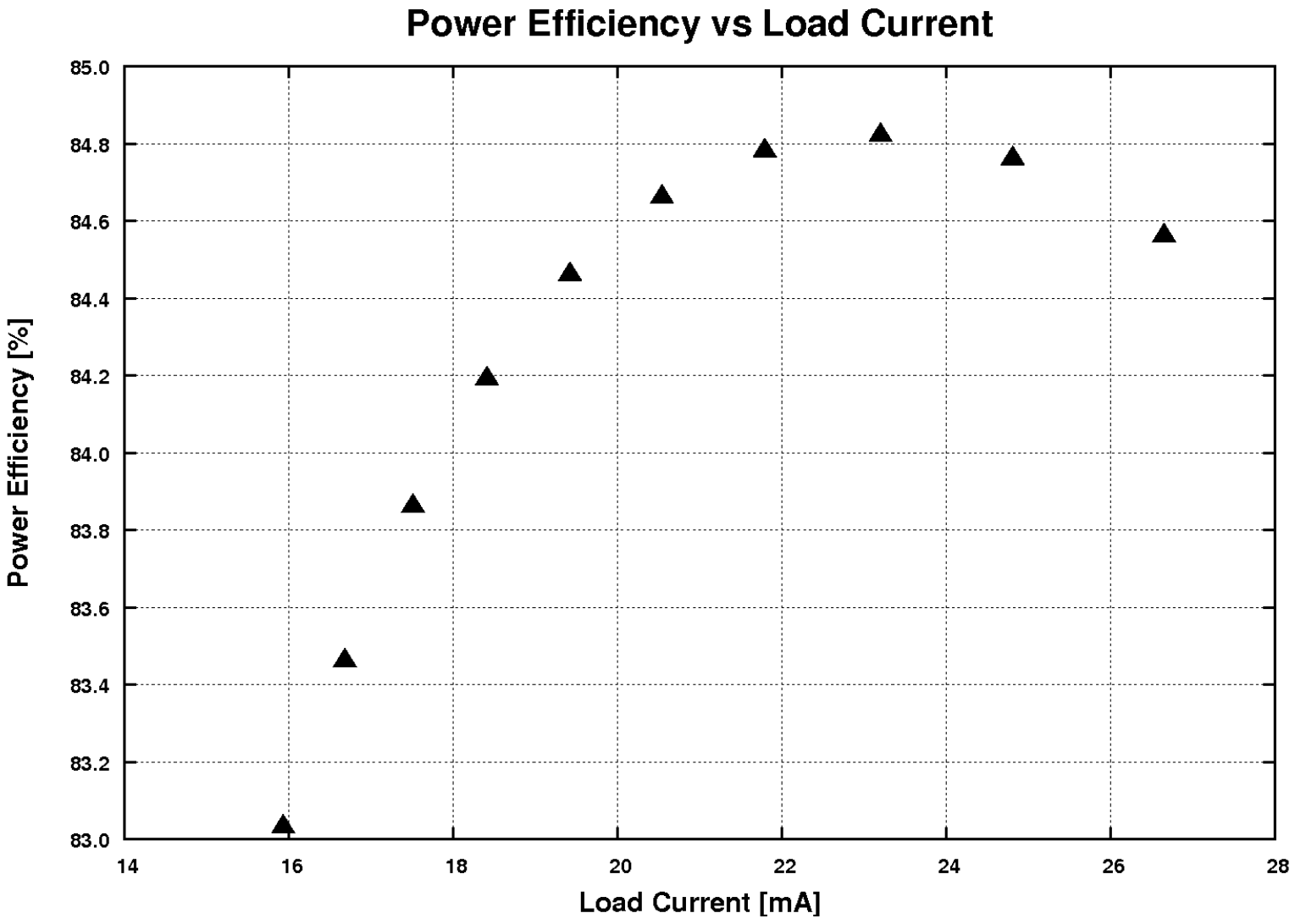
Input voltage, output voltage and output current vs. time



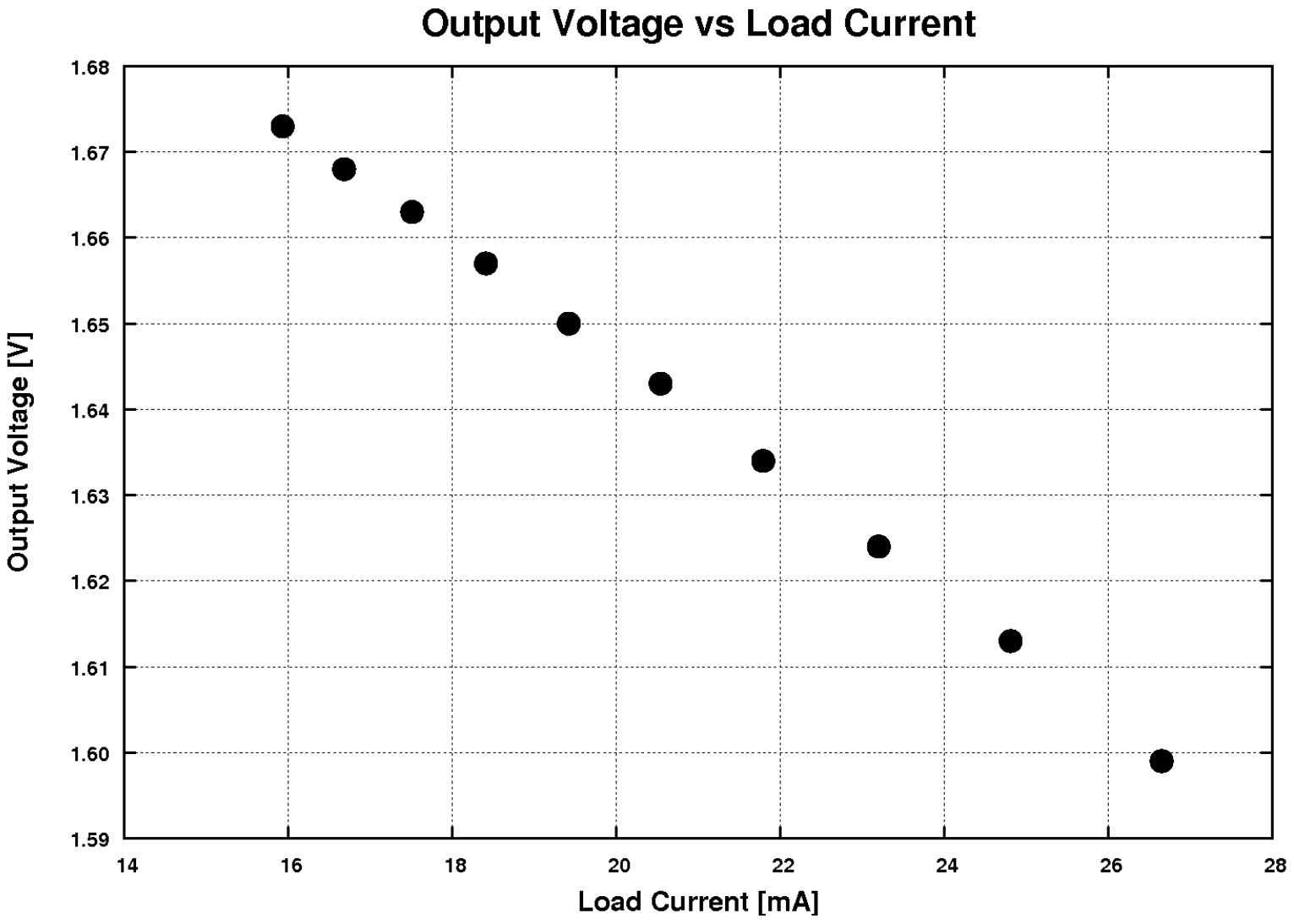
Voltage output ripples vs. time



Power efficiency vs. load current



Output voltage vs. load current

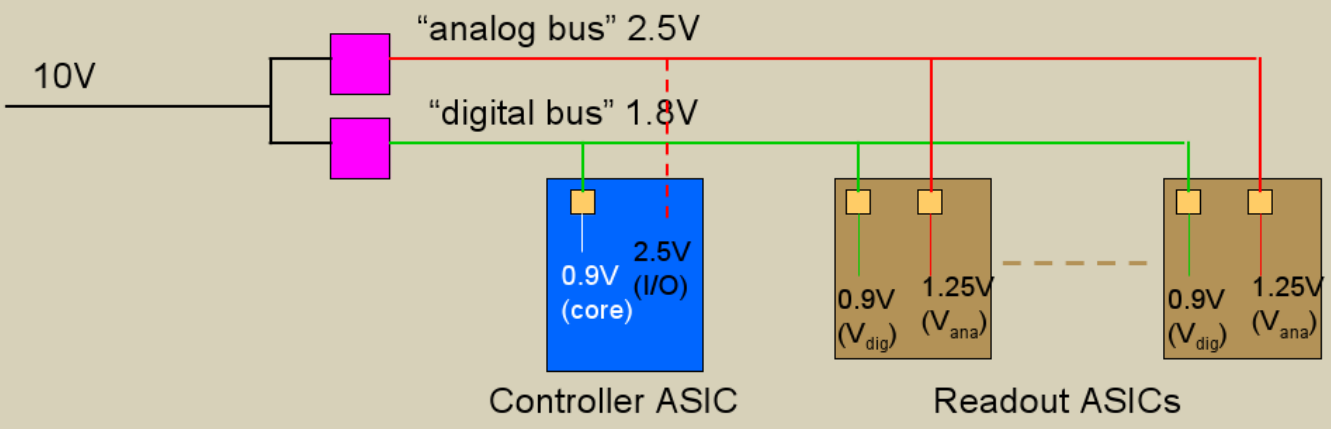


Status of step-up charge pomp design

- READY:
  - design study,
  - simulation in Cadence,
  - optimisation of the circuit **(82% - 85% of efficiency)**.
- TO BE DONE:
  - process corner simulations,
  - layout (submission planned in the end of the year).

Prototyping the step-down switched capacitor converter for DC-DC powering scheme

Proposed power distribution scheme



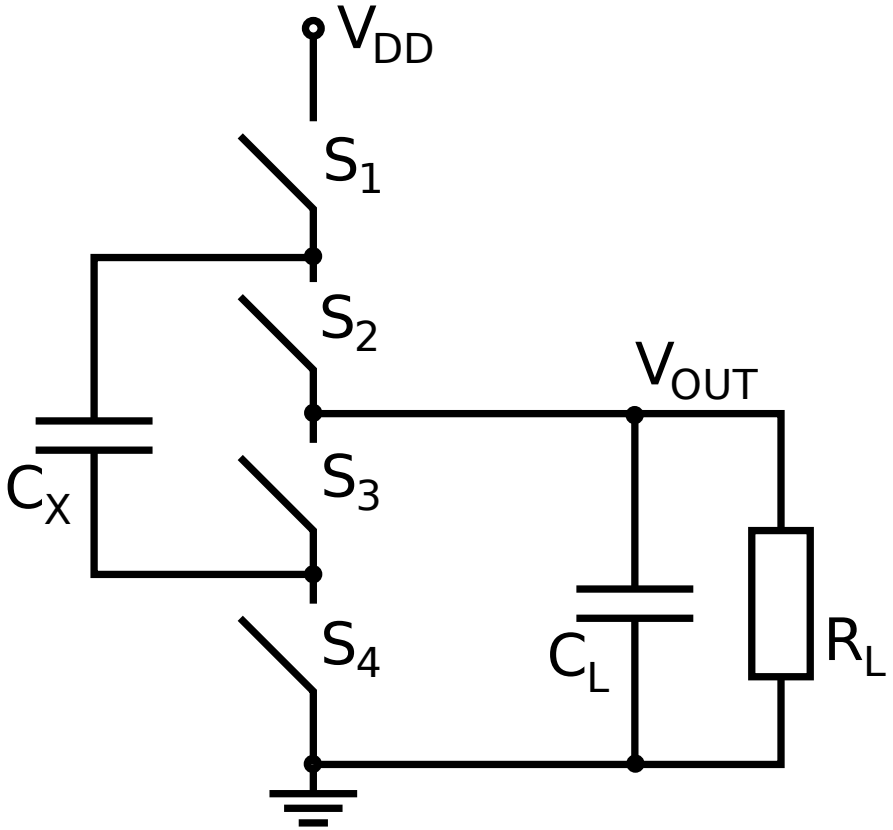
Conversion stage 1 (ratio 4-5.5)
-Vin=10V => high-V technology
-Same ASIC development for analog and digital, only feedback resistive bridge is different

Conversion stage 2 (ratio 2)
- Embedded in controller or readout ASIC
- Closely same converter for analog and digital (different current, hence different size of switching transistors): macros (IP blocks) in same technology

Simple switched capacitor DC-DC step-down converter

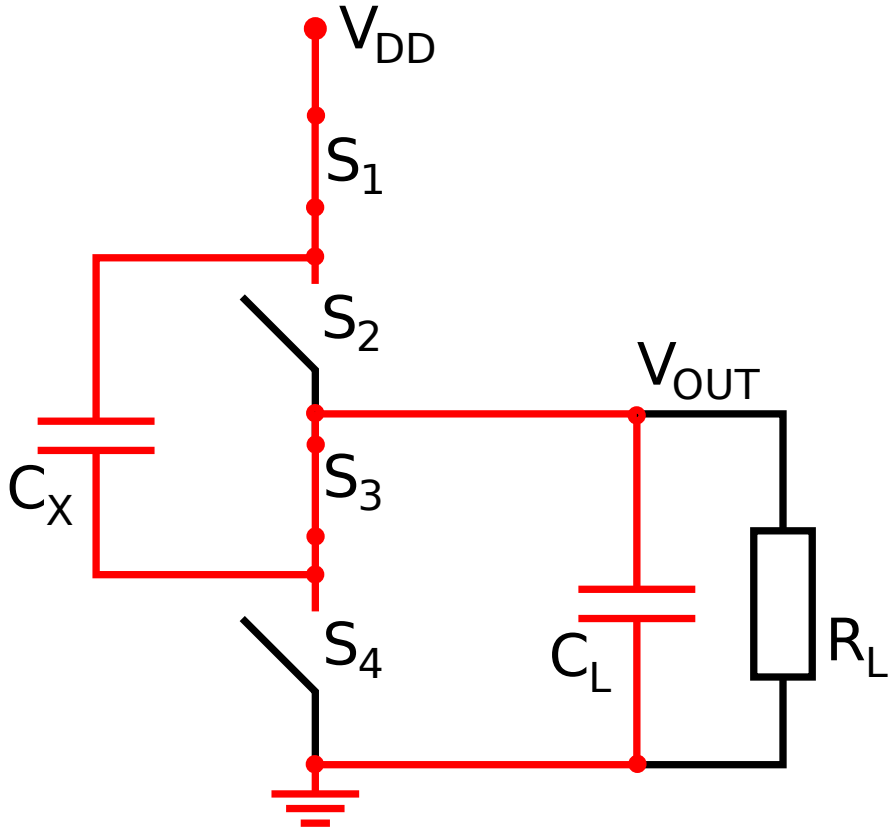
The simplest model contains:

- Four switches,
- Two capacitors.



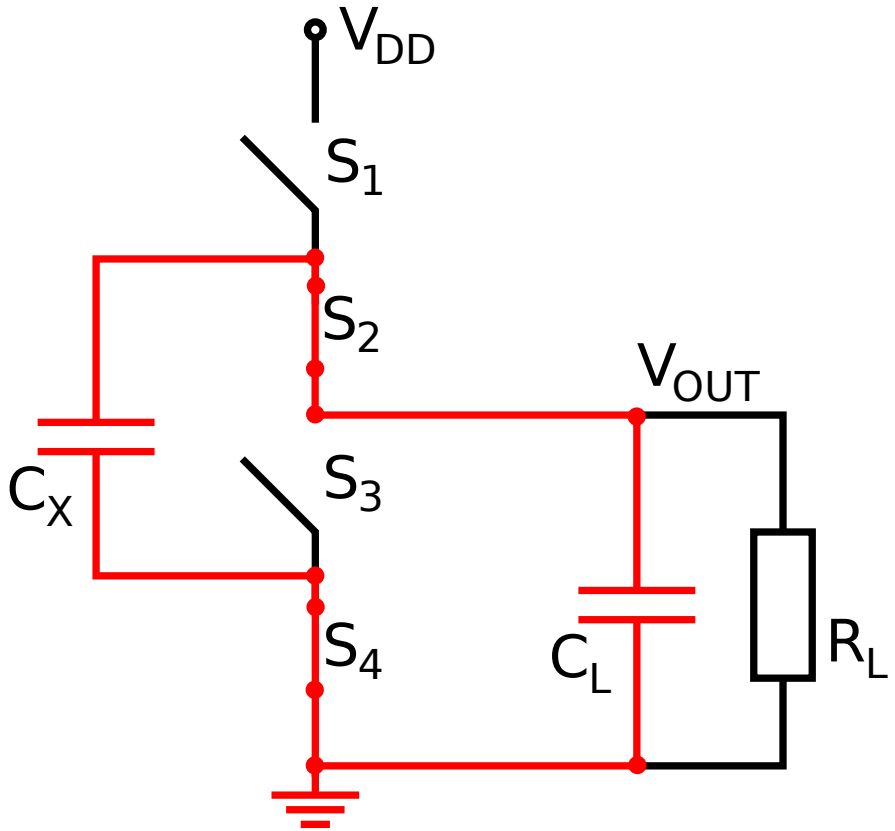
Simple step-down converter (Phase 1)

- Switches S_1 and S_3 are closed,
- Switches S_2 and S_4 are opened,
- C_X and C_L are connected in series.



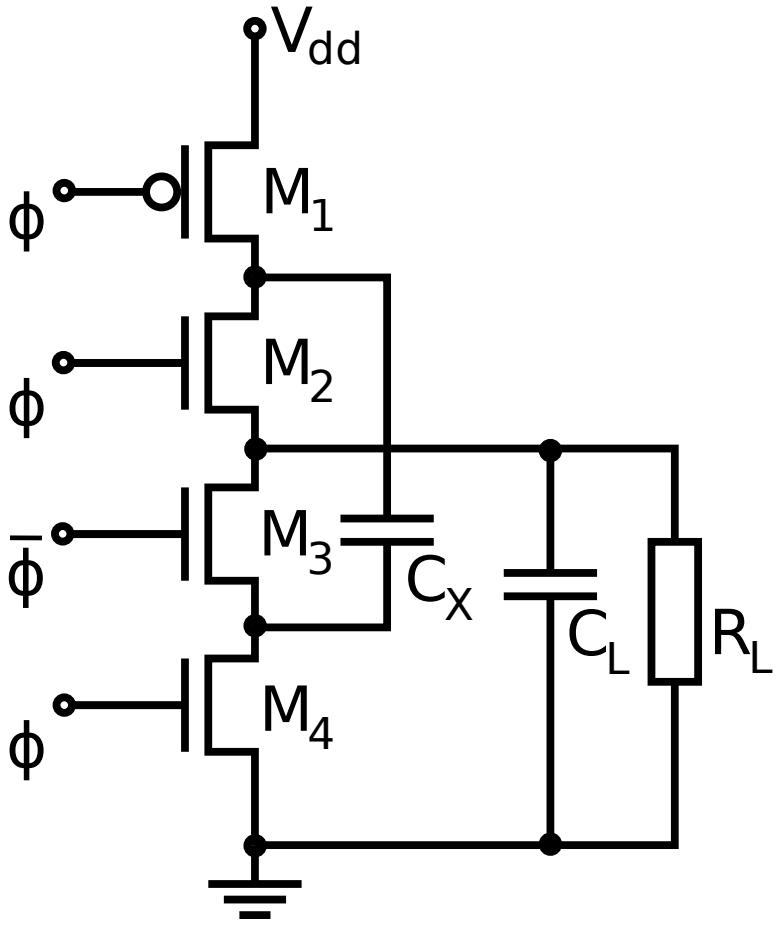
Simple step-down converter (Phase 2)

- Switches S_1 and S_3 are opened,
- Switches S_2 and S_4 are closed,
- C_X and C_L are connected in parallel.

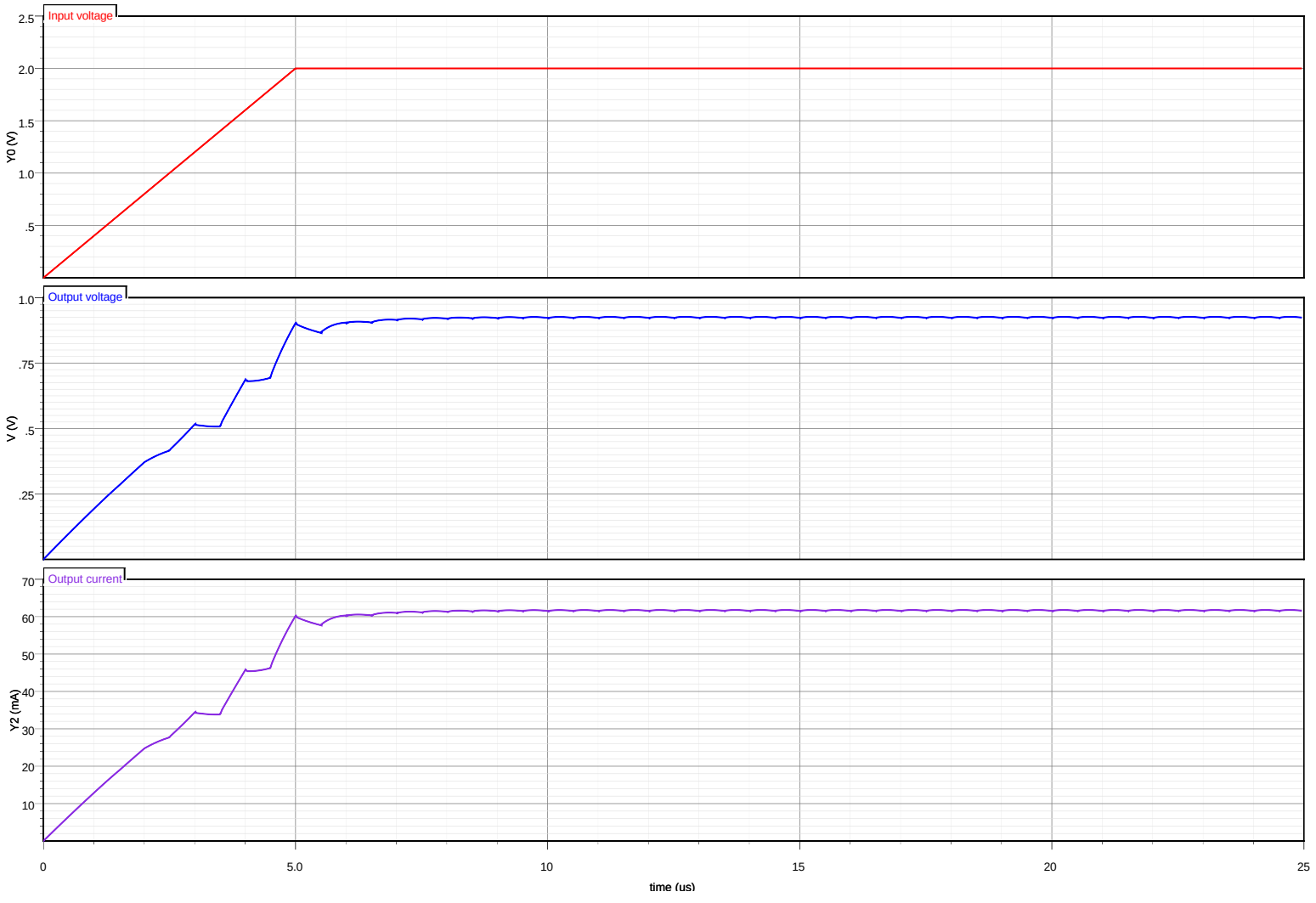


Practical solution for step-down converter

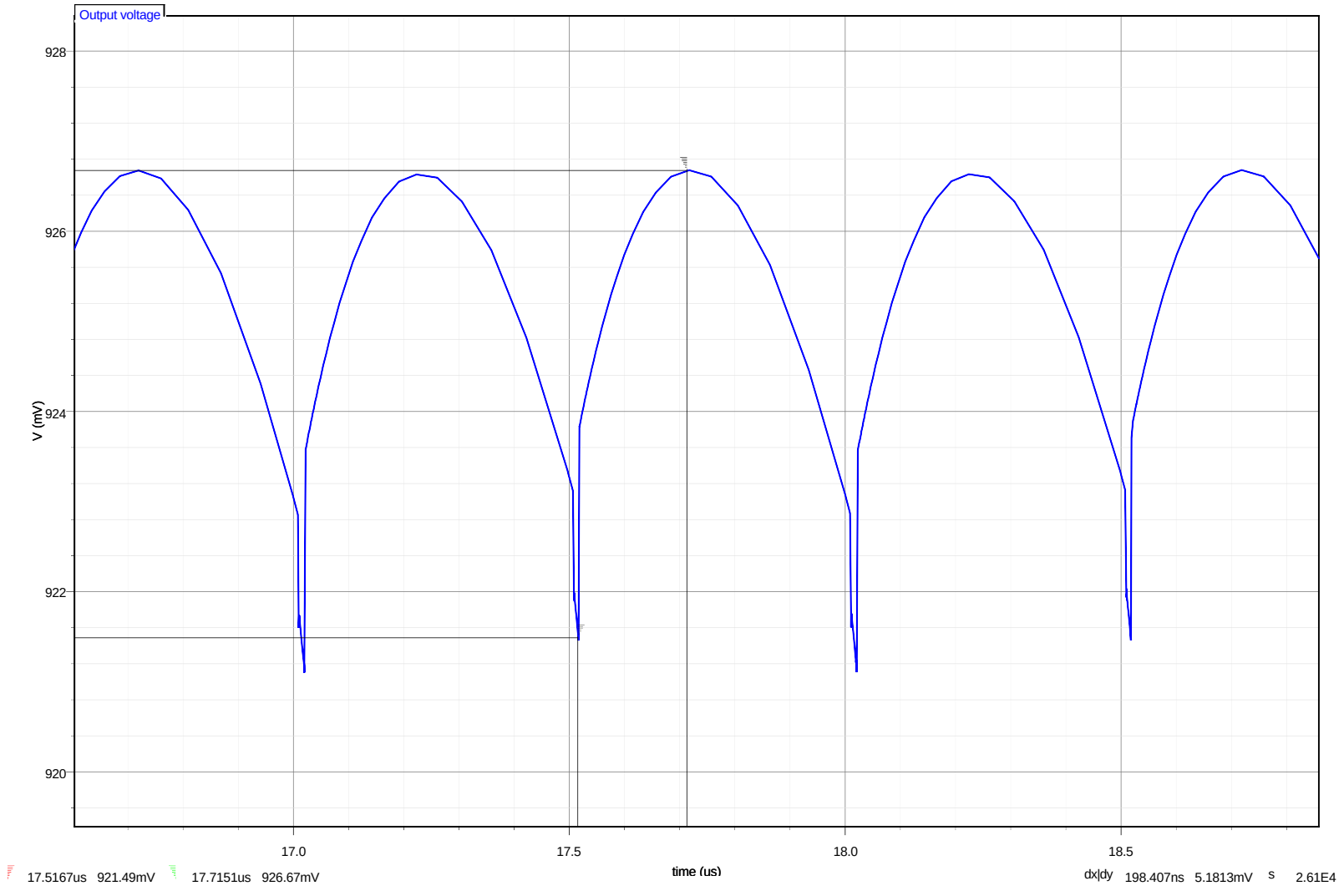
- Four transistors: 1 x PMOS & 3 x NMOS, two capacitors: C_X & C_L,
- Transistor M_1 (PMOS) uses thick gate oxide,
- Transistors M_2 - M_4 (tripple-well NMOS) also with thick gate oxide.



Input voltage, output voltage and output current vs. time



Voltage output ripples vs. time



Status of step-down converter design

- READY:
  - analithical model of DC-DC step-down pump (from F. Faccio & S. Michelis),
  - design study,
  - preliminary simulations using Cadence shows efficiency up to 92%.
- TO BE DONE:
  - optimisation of the circuit,
  - process corner simulations,
  - layout (submission planned in the end of the year).

Thank you for your attention!