Transceivers for Passive Optical Networks

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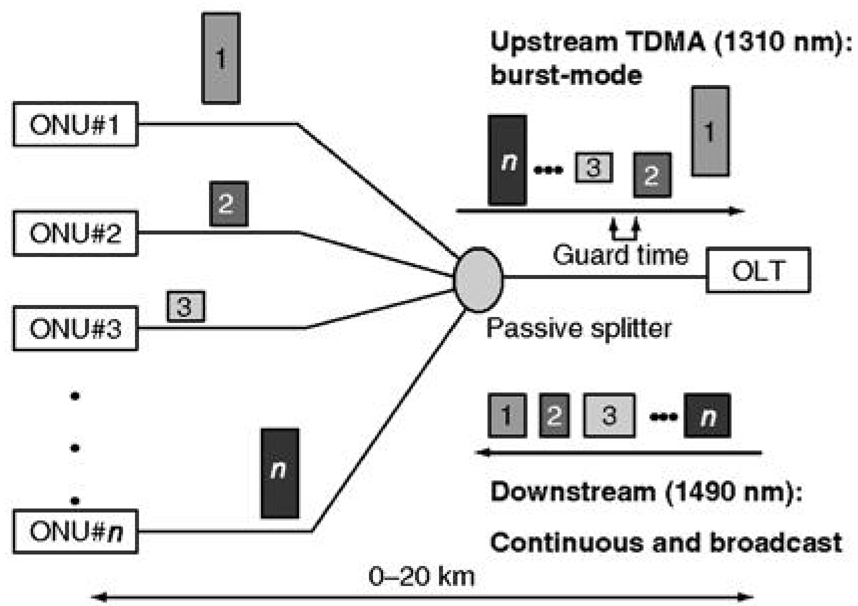
Preface

- Overview of Passive Optical Networks (PON)
- Overview of the structure of a PON Transceiver (TRX)
- Transmitter (TX) design challenges and solutions
- Receiver (RX) design challenges and solutions

PONs : System Overview

- Optical fiber access network primarily employing passive optical components and configured around a splitter/combiner
- Several protocols currently standardised: Ethernet PON (EPON), Broadband PON (BPON), Giga-bit PON (GPON)
- Max Physical Reach is 20km (Max Diff. Reach 20km)
- Current PONs use Time Division Multiplexing (TDM) to multiplex data in the downstream and Time Division Multiple Access (TDMA) to provide multiple access to users in the upstream



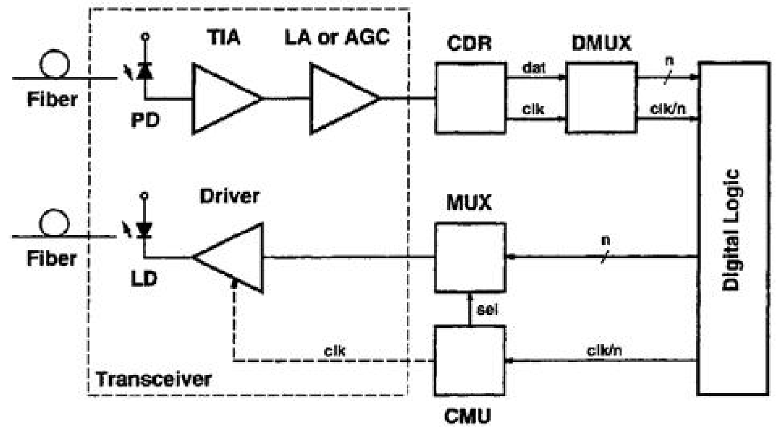
Architecture of a TDM PON

PONs: Implications on TRX Design

- Main challenge is to design the transceivers for the upstream, because of the bursty nature of traffic
- To avoid interference in the upstream and increase bandwidth efficiency the Optical Network Unit (ONU) TX needs to have:
  - Fast Rise/Fall Time – to minimise guard time
  - High Extinction Ratio (ratio of optical power when a “1” and a “0” is transmitted)
  - Stable output power during transmission
- The Optical Line Terminal (OLT) RX needs to be able to receive packets with large differences in optical power and phase alignment:
  - High sensitivity
  - High Dynamic Range (ratio of maximum to minimum detectable power) – effect of differential reach
  - Fast Response

PON Transceivers: Transmitter Structure

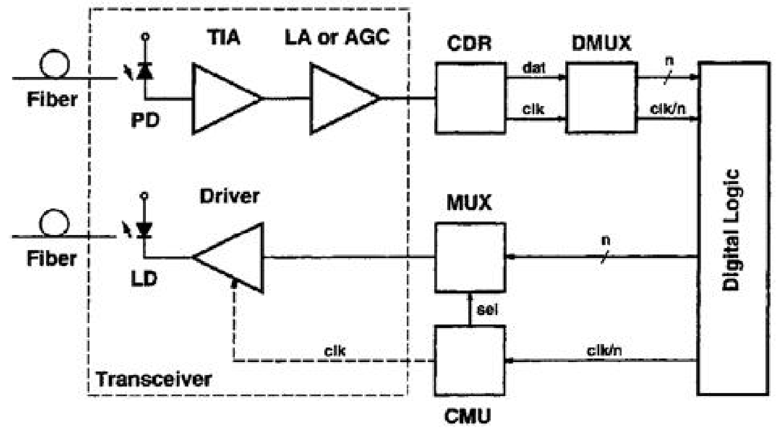
- Transmitter:
  - Driver – Modulates the current of the laser diode (Laser Driver), or the voltage across a modulator (modulator driver) when external modulation is used
  - The Laser Diode – Generates the optical signal



Block diagram of an optical Transceiver

PON Transceivers: Receiver Structure

- Receiver:
  - Photodiode (PD) – Receives optical signal and converts it to current
  - Transimpedance Amplifier (TIA) – Amplifies current and converts it to voltage
  - Main Amplifier (MA) realised as a Limiting Amplifier (LA) or Automatic Gain Control (AGC) amplifier- Further amplifies the voltage
- Also the Clock and Data Recovery (CDR) circuit although typically is not part of the receiver will be discussed – Extracts clock signal and retimes data signal



Block diagram of an optical Transceiver

PON Transmitters: Design Challenges

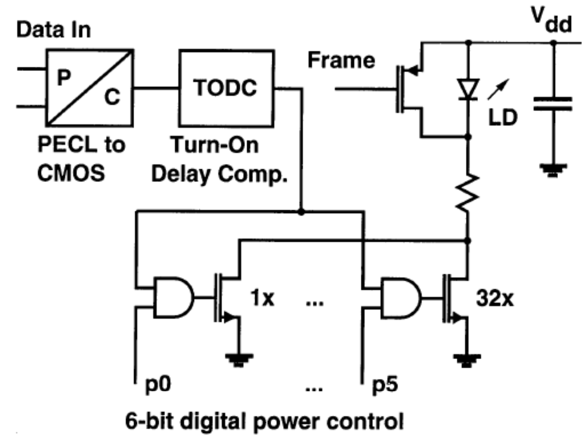
- Laser => Which type should be used?
- Laser Driver:
  - High Extinction Ratio (especially interburst) required => Laser current should be switched off during ‘0’s and especially between bursts
  - Turn On/Off Time should be minimized => Laser Bias Current should always be above threshold – always on
  - Stable point of operation + average emitted power is less than average burst power in burst-mode => Automatic Power Control cannot be based on average power

PON Transmitters: Lasers

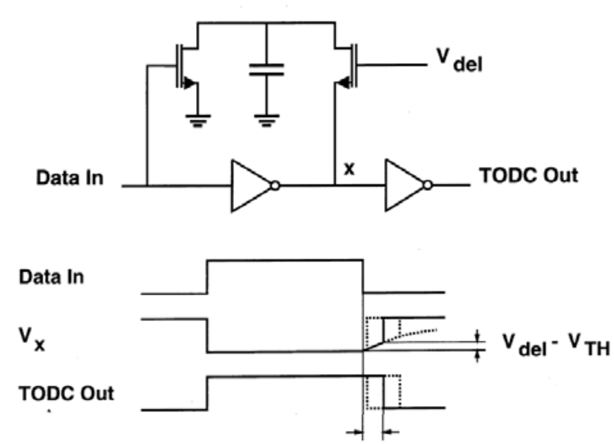
- Only additional requirement for a laser in burst-mode operation is fast on/off time
- Choice of the laser type is mostly affected by other parameters – power budget, power budget penalties, cost
- OLT needs a 1490 nm laser (usually DFB-DBR)
- ONU needs 1310 nm F-P laser – cost is more important for ONU

PON Transmitters: Laser Driver

- Laser current should be switched off during '0's and especially between bursts + Laser Bias Current should always be above threshold – *conflicting requirements*
- Commonly the bias current is set to zero only between bursts and it is set above threshold for the duration of the burst
- There are designs that suggest switching the laser current off even during '0's
- In both cases Turn-on Delay Compensation (TODC) circuitry is required
- Also use of a shunt transistor to rapidly drain the carriers from the laser can be used



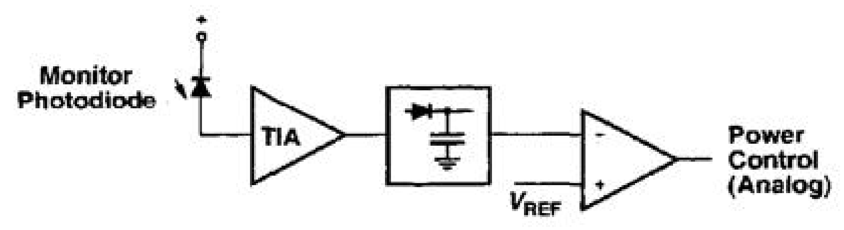
Laser driver circuit with digital power control and turn-on delay compensation



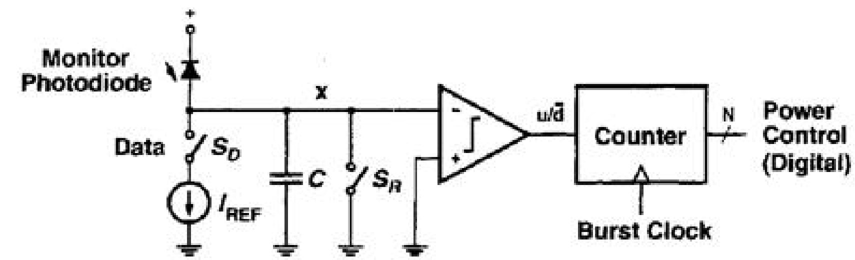
Turn-on Delay Compensation

PON Transmitters: Laser Driver

- Automatic Power Control (APC) in burst-mode operation cannot be based on average power
- Use of peak power for Automatic Power Control
- Both analog and digital circuitry exists
- Optical APC has also been suggested
- The same circuit can be used to perform end of life detection, using a lower current or voltage reference



Burst-mode APC (analog)



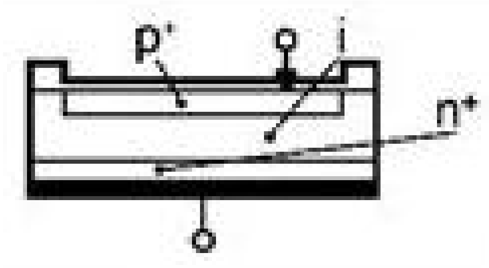
Burst-mode APC (digital)

PON Receivers: Design Challenges

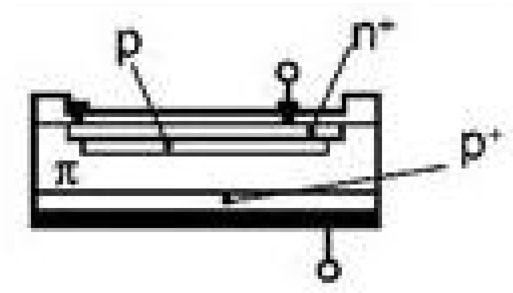
- Photodiode => use of PIN or Avalanche (APD) ?
- TIA and MA:
  - High Sensitivity + High Dynamic Range Required => Output should remain within the range of operation of CDR regardless of the input amplitude
  - Fast Response + Average Value of input signal not constant => AC-coupling may not be feasible to remove offsets
  - Fast Response + Variable Decision Threshold => Decision Threshold Control becomes more challenging and critical

PON Receivers: PIN vs APD

- High receiver sensitivity is required
- Avalanche Photodiode has higher sensitivity, due to Avalanche Gain mechanism
- But:
  - More expensive
    - More difficult to fabricate, due to complex structure
  - Additional noise introduced, due to random nature of gain mechanism
  - High bias voltage needs to be applied
  - Temperature compensation circuitry is needed due to gain/temperature dependency
  - Careful choice of avalanche gain – it affects max bit rate, due to gain-bandwidth product, sensitivity and dynamic range



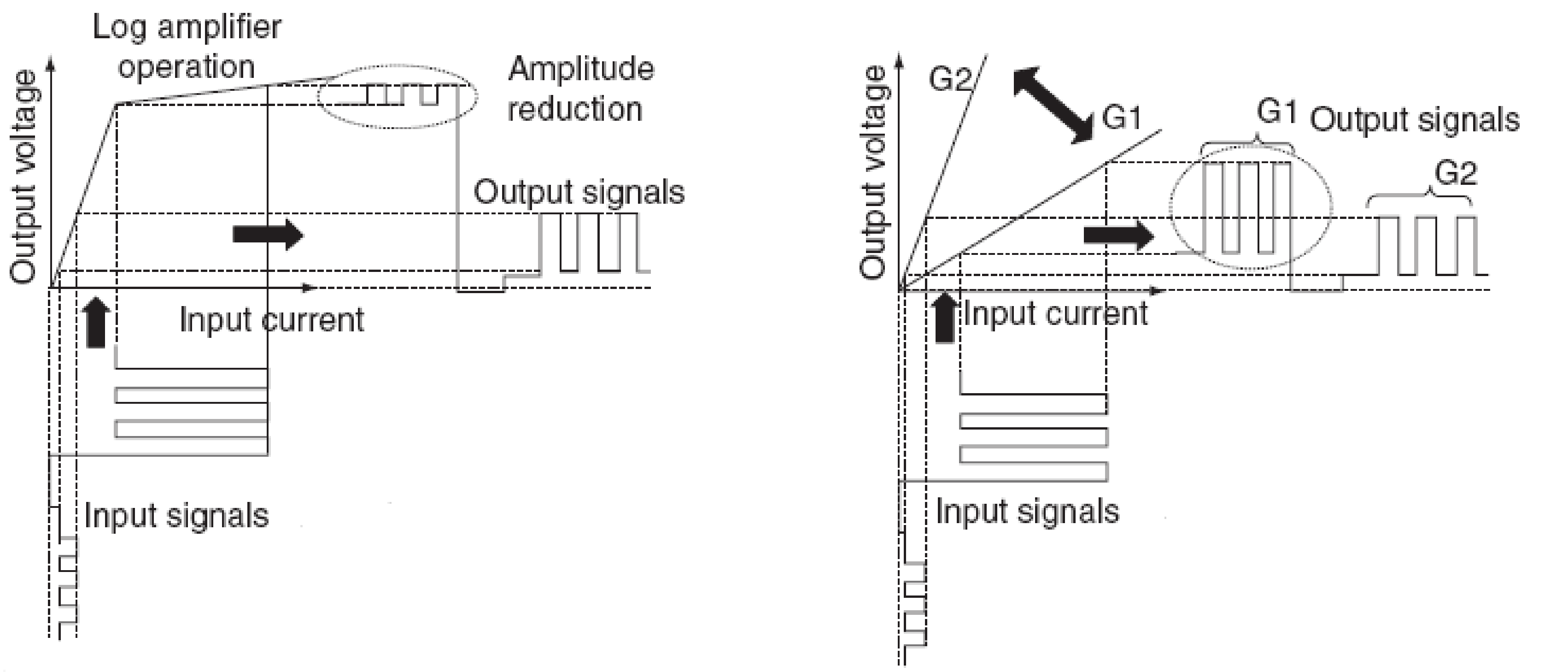
PIN Photodiode



Avalanche Photodiode

PON Receivers: TIA and MA

- Output should remain within the range of CDR acceptable input for a wide range of input amplitude
- Variable gain is needed – higher for smaller amplitude, lower for large amplitude => Use of Automatic Gain Control (AGC) or Limiting Amplifier (LA)



Operating principle of Limiting Amplifier and Automatic Gain Control

PON Receivers: TIA and MA

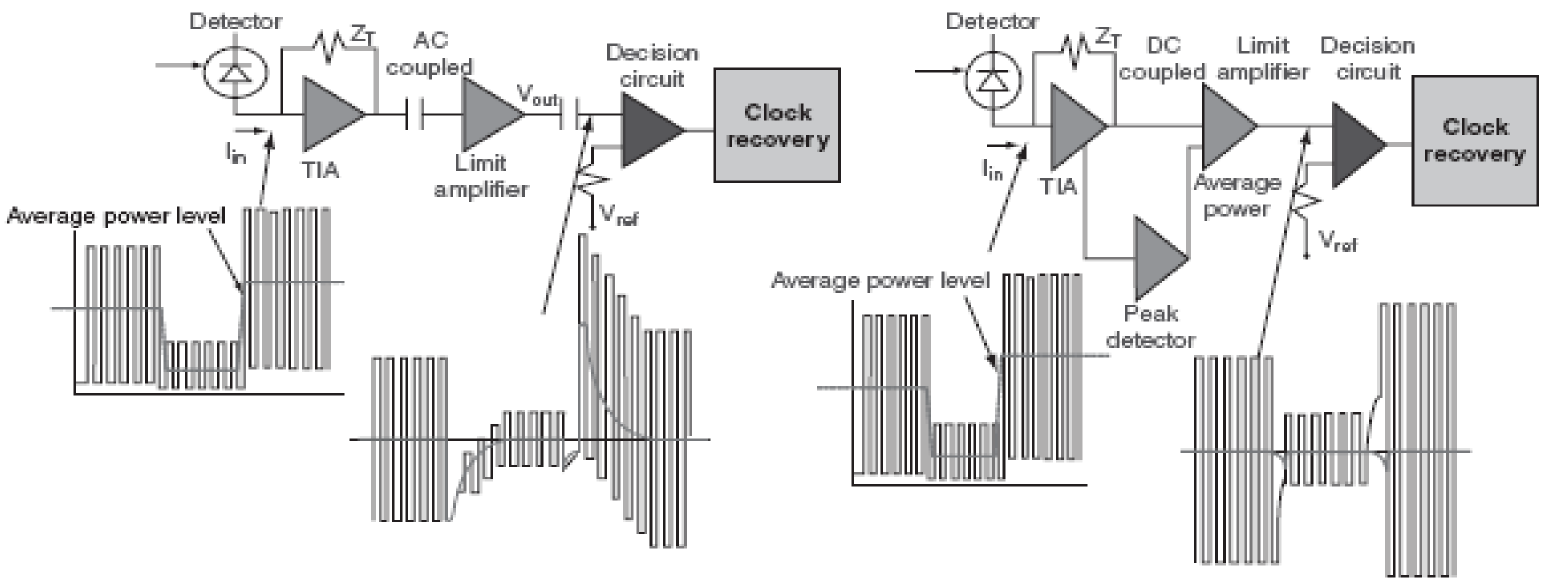
- LA vs AGC:
  - Limiting Amplifier is easier to design
  - Has superior performance (power dissipation, bandwidth, noise) compared to an AGC realized in the same technology
  - But, linear transfer function of AGC preserves signal waveform, allowing analog signal processing (equalization, soft-decision decoding) to be performed on the output signal

PON Receivers: TIA and MA

- AC coupling, which is used in continuous mode for threshold and offset control may not be feasible in burst-mode receivers
- Use of DC coupling with Threshold and Offset Control

Or

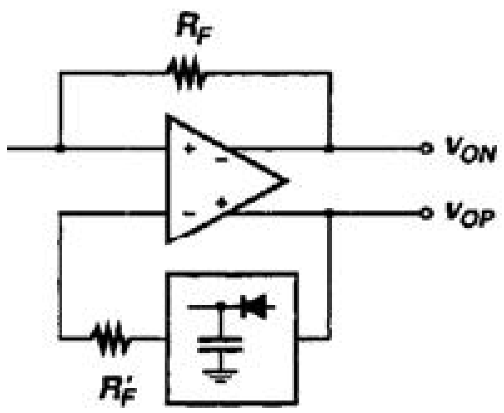
- Use of AC coupling with small capacitors (EPON only)



AC vs DC Coupling

PON Receivers: TIA and MA

- Fast and adaptive decision threshold Control is required
- Use of Threshold and Offset Control Circuitry (LA)

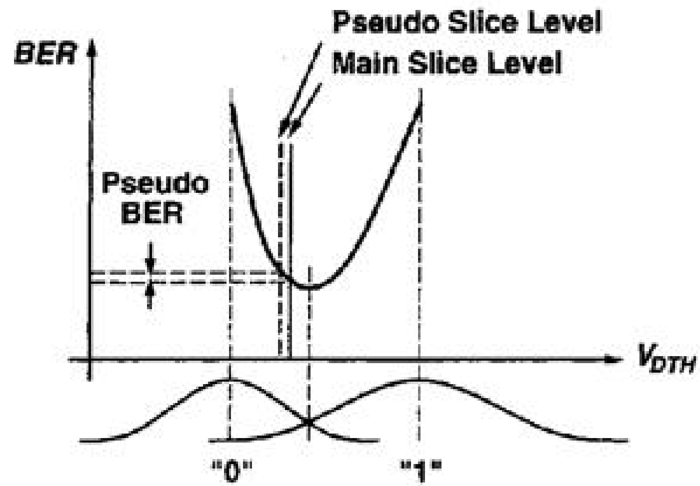


Example of an Automatic Threshold Control Circuit

Output of a fully-differential amplifier without and with offset control

PON Receivers: Decision Threshold Control

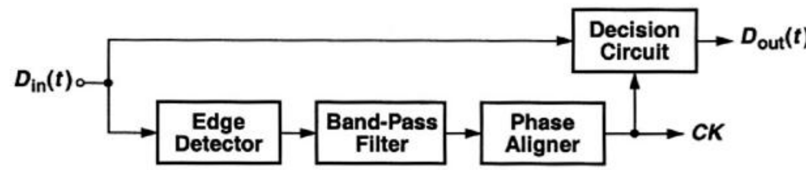
- Use of AGC allows analog signal processing to be performed on the output signal
- Slice Level Steering:
  - Put pseudo slice level slightly above main slice level and measure pseudo BER
  - Put pseudo slice level below main slice level and measure pseudo BER
  - Adjust main slice level towards direction with smaller pseudo BER
- Also, the preamble can be used to determine decision threshold



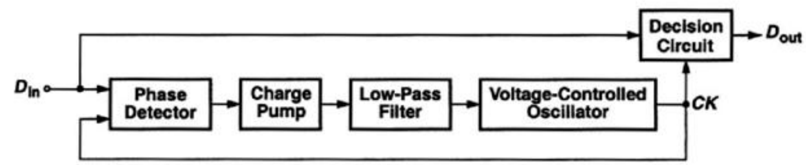
Slice level steering

PON Receivers: CDR

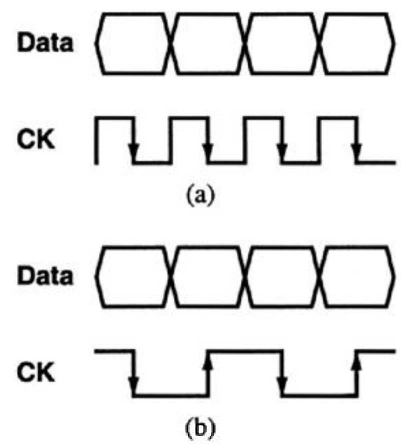
- Clock and Data Recovery (CDR) architectures can be broadly divided into two categories:
  - Open Loop – not used in PON TRXs
  - Phase Locking – further subdivided into:
    - Full Rate
    - Half Rate – Gaining more attention as data rate for future PONs reaches 10Gbps



Generic Open-Loop CDR Architecture



Generic Phase-Locking CDR Architecture



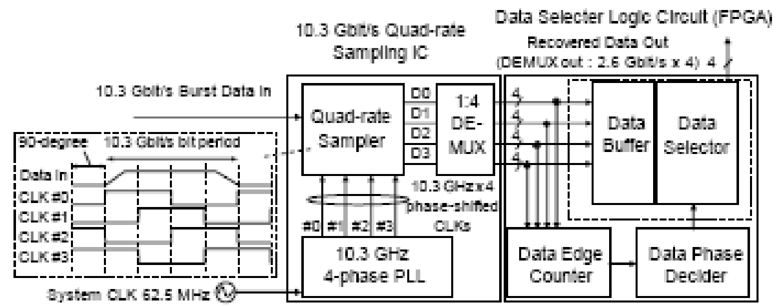
Full and Half rate CDR operation

PON Receivers: CDR

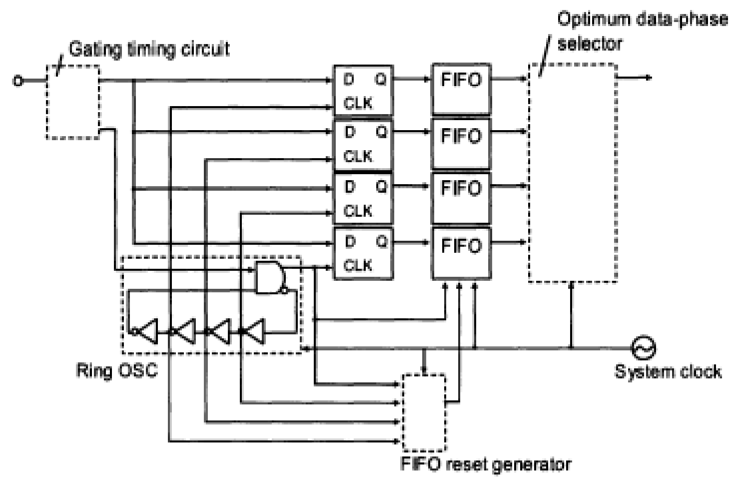
- The main techniques utilized by recent implementations of rapid response CDR circuits are:
  - Over-sampling the signal using multi-phase clocks
  - Using a gated voltage-controlled oscillator
- The drawback of the first approach is the very high sampling frequency, while for the second the low tolerance to distortion

PON Receivers: CDR

- Solutions suggested include:
  - Parallel processing
  - Hybrid architecture using gated oscillator with a ring to produce the multi-phase clock
- CDR circuits that don't follow any of the above approaches can also be found:
  - Use of second-order PLL
  - Use of injection-locked oscillator and taking advantage of the relaxation oscillation



CDR using parallel processing



CDR using hybrid approach

Summary

- Passive Optical Networks require burst-mode operation in upstream direction due to bandwidth sharing among attached users
- Implications for Transmitters
  - High Extinction Ratio
  - Fast Turn on/off
  - Stable operation over duration of transmission
- Implications for Receivers
  - Large differences in phase and amplitude of received signals
  - Fast response required