Laboratoire de l'Accélérateur Linéaire (IN2P3-CNRS) Orsay, France

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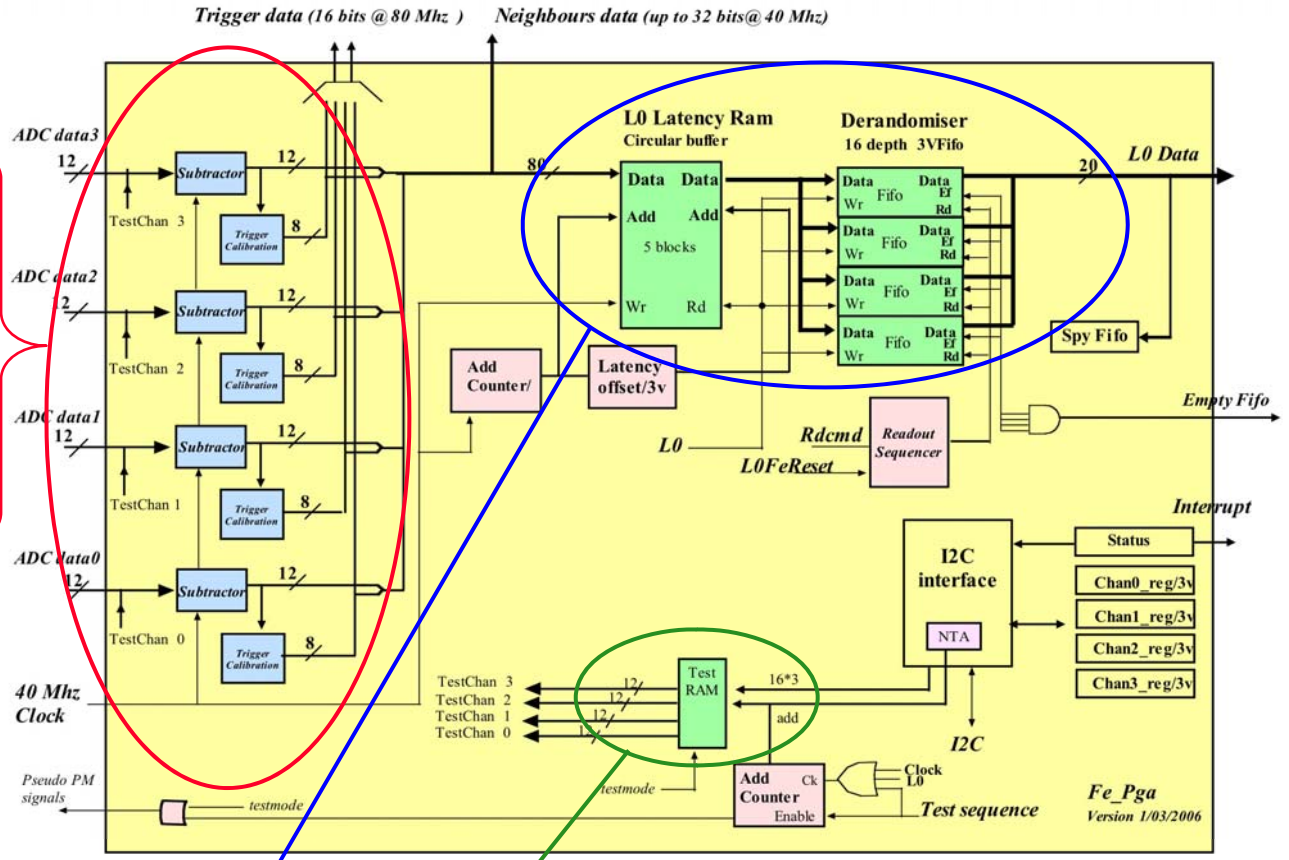
April 8-9th 2009

Choice of Front-End FPGA

- **ECAL/HCAL Front-END Card : FEPGA functionalities reminder**
- **Integrated Design Environment :**
  - **IDE Actel Libero**
  - **Debug tools : Identify, Silicon explorer (Actel antifuse only !)**
- **Axcelerator family (current Front end FPGA)**
  - **Device architecture reminder**
  - **Layout : Front-end FPGA firmware inside AX250**
- **PA3 family**
  - **Device architecture**
  - **Example of Front-end FPGA firmware inside A3PE600**
  - **Estimation of needed resource in PA3 family**
  - **Possible target**
  - **Compilation inside possible target**
  - **Possibilities of migration inside PA3 family**
- **Summary table (price, resources, ..)**

FrontEnd PGA functionalities : reminder

- **4 functional blocks :**
  - The first one processes the input ADC data, which needs to be re-synchronized (each ADC has its own clock), and processed to remove the low frequency noise and to subtract the pedestal
  - The second block produces the trigger data, converting the 12 bits of the ADC to 8 bits

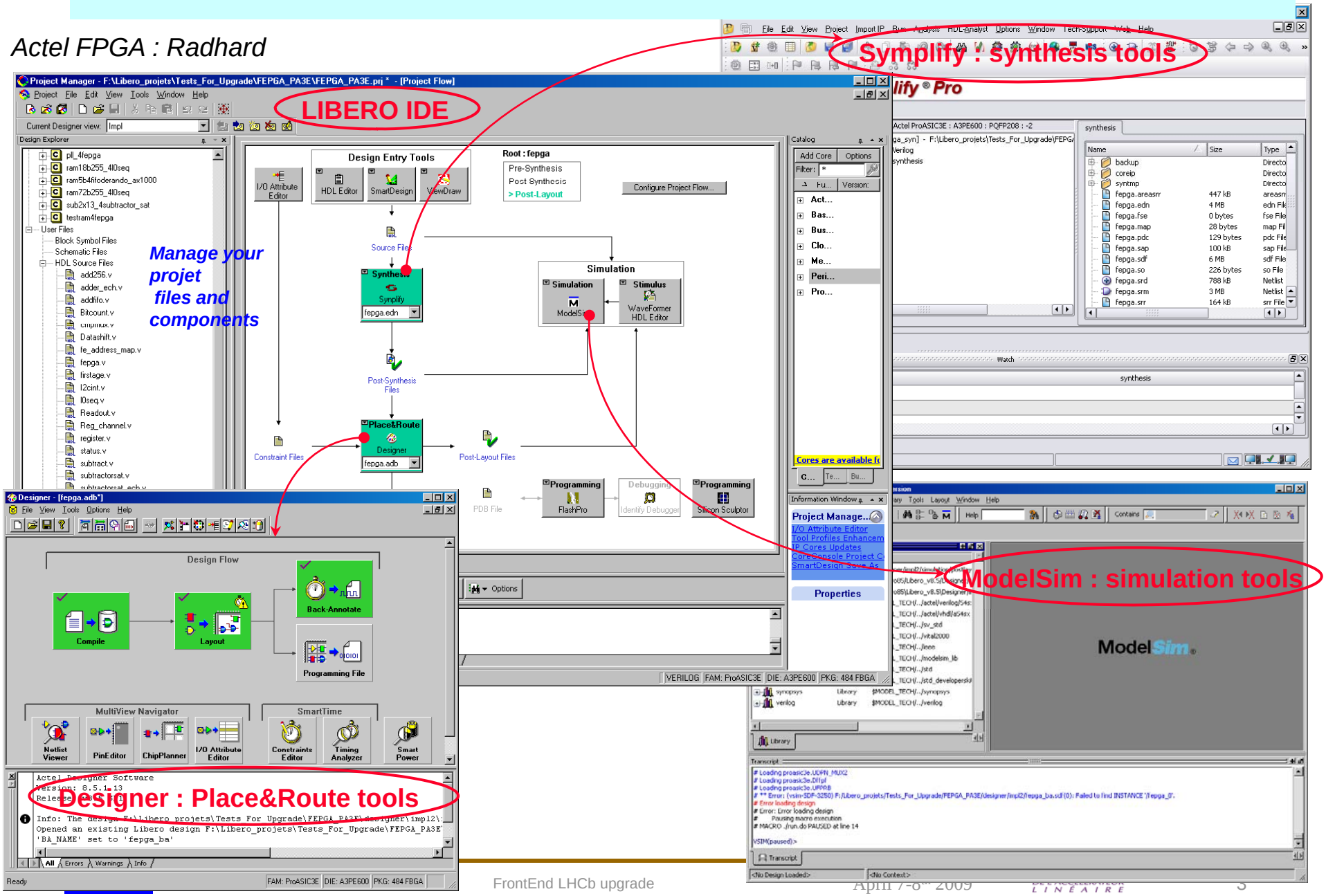


- The third block is in charge of storing the data (80 bits per FE-PGA) during the L0 latency, and to send it up upon L0-Yes to the SEQ-PGA
- The last block permits injecting test values at the input, in place of the ADC values, in order to check the proper behaviour of the card.

LHCb FEB note : Christophe, Frédéric, Jacques, …

Actel Libero : Integrated Design Environment

Actel FPGA : Radhard



Debug tools : Silicon Explorer - Identify

Silicon Explorer :

Integrated verification and logic analysis tool for antifuse devices ONLY

↓

Silicon Explorer shortens the FPGA design verification process by providing a tightly integrated suite of tools and capabilities that enable rapid isolation of functional and timing problems

↓

There's no need to relayout, recompile, or redo any part of your design to complete the verification process.

Christophe, Frédéric and Jacques are expert !

Identify : (free)

In-system debugging tool for Actel's flash devices

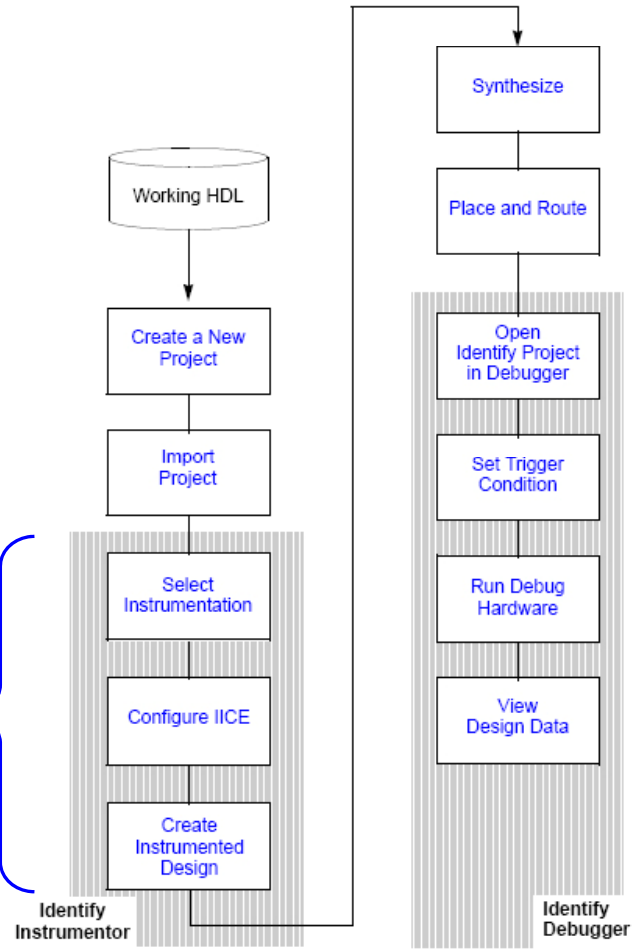


Figure 1: Identify RTL Debugger Design Flow

Identify implementation :

- Need to recompile and relayout a part of your design (incremental option)
- Use logic and RAM block of the device
- Read data spyed by JTAG

Axcelerator Family device architecture (antifuse technology)

Basic cell : SuperCluster

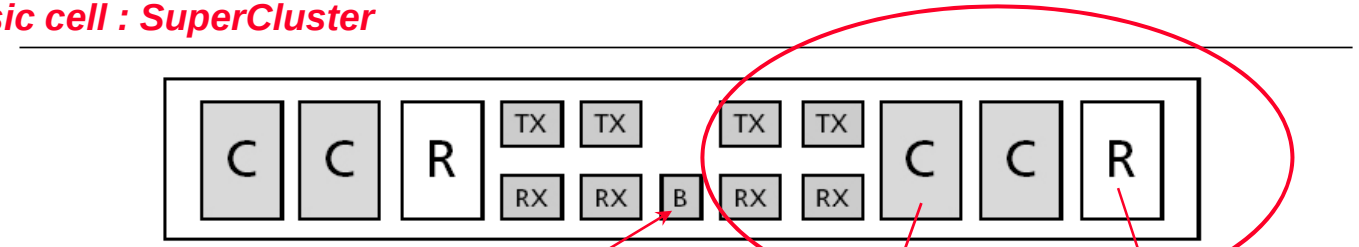
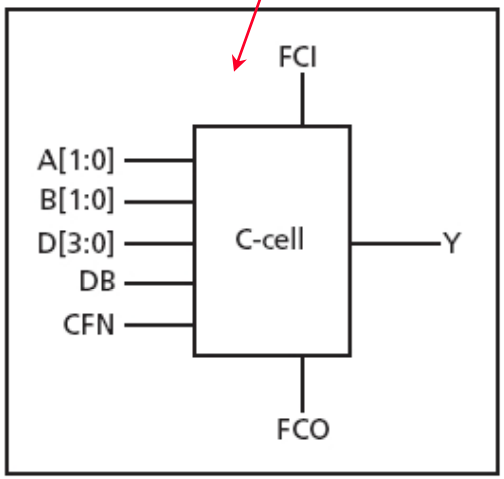


Figure 1-4 • **AX SuperCluster**

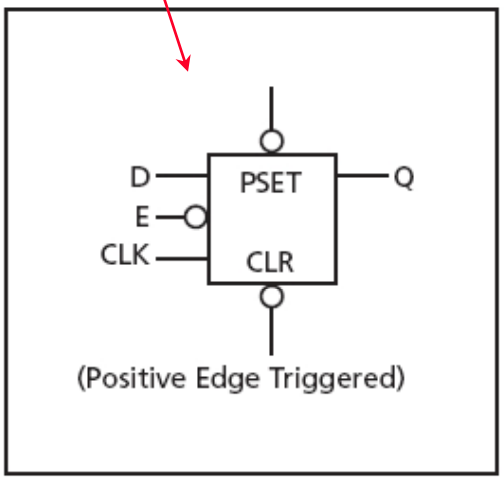
Independent Buffer

Cluster :

2 x C-Cells
1 x R-Cell
2x TX (Transmit buffers)
2x RX (Receive buffers)



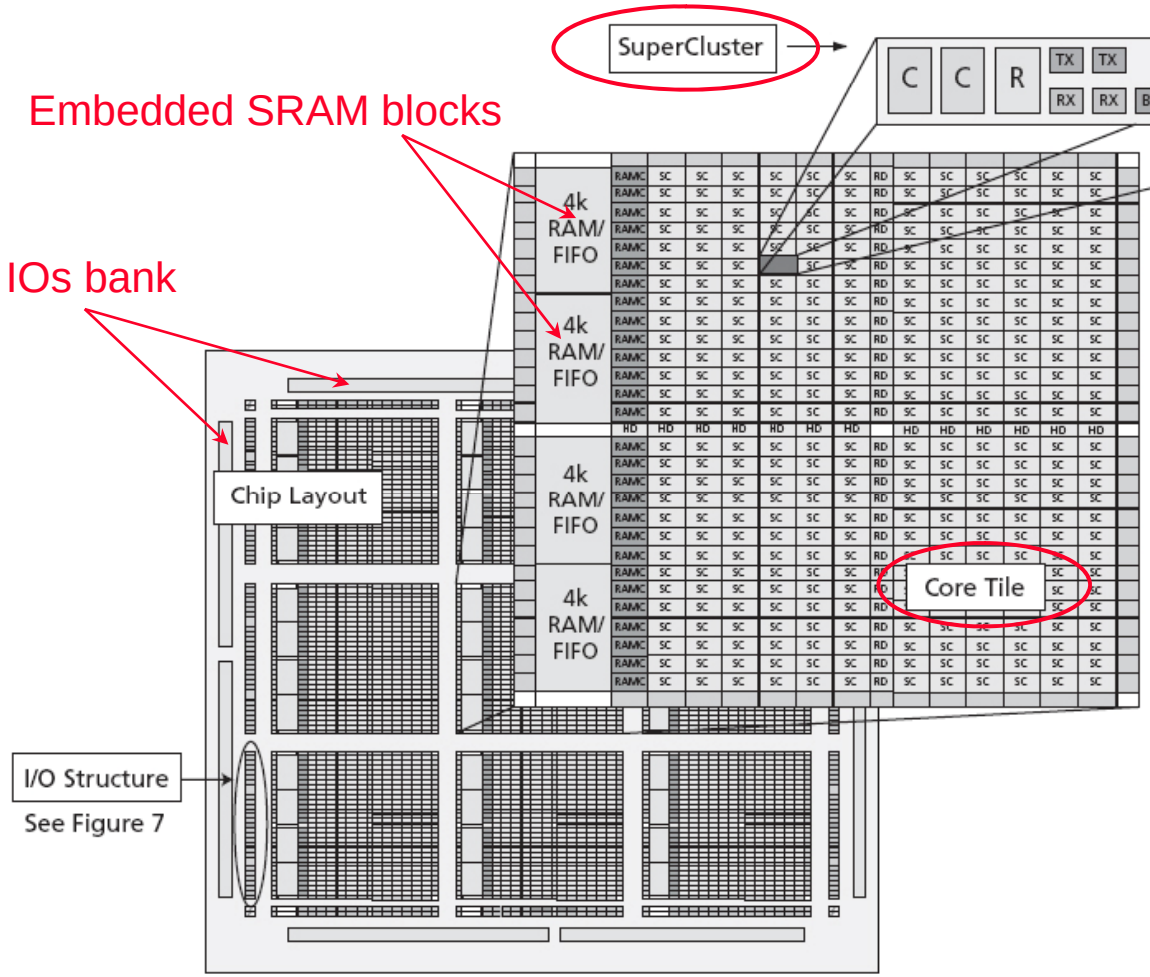
Combinatorial cell



Register cell

Axcelerator Family device architecture (antifuse technology)

Axcelerator Family FPGAs



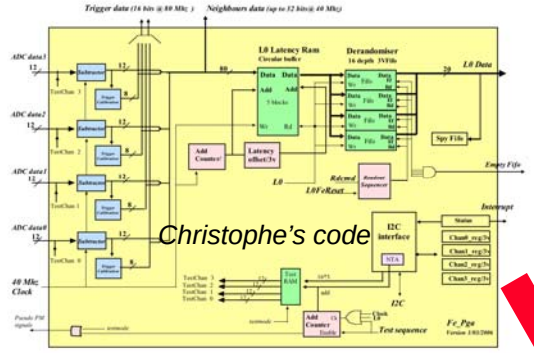
Current FEPGA

Axcelerator family

Device	AX125	AX250	AX500	AX1000	AX2000
Capacity (in Equivalent System Gates)	125,000	250,000	500,000	1,000,000	2,000,000
Typical Gates	82,000	154,000	286,000	612,000	1,060,000
Modules					
Register (R-cells)	672	1,408	2,688	6,048	10,752
Combinatorial (C-cells)	1,344	2,816	5,376	12,096	21,504
Maximum Flip-Flops	1,344	2,816	5,376	12,096	21,504
Embedded RAM/FIFO					
Number of Core RAM Blocks	4	12	16	36	64
Total Bits of Core RAM	18,432	55,296	73,728	165,888	294,912
Clocks (Segmentable)					
Hardwired	4	4	4	4	4
Routed	4	4	4	4	4
PLLs	8	8	8	8	8
I/Os					
I/O Banks	8	8	8	8	8
Maximum User I/Os	168	248	336	516	684
Maximum LVDS Channels	84	124	168	258	342
Total I/O Registers	504	744	1,008	1,548	2,052
Speed Grades	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2
Temperature Grades	C, I	C, I, M, B	C, I, M, B	C, I, M, B	C, I, M, B
Package					
CSP	180				
PQFP		208	208		
BGA				729	
FBGA	256, 324	256, 484	484, 676	484, 676, 896	896, 1152
CQFP		208, 352	208, 352	352	256, 352
CCGA/LGA				624	624

Figure 1-6 • **AX Device Architecture (AX1000 shown)**

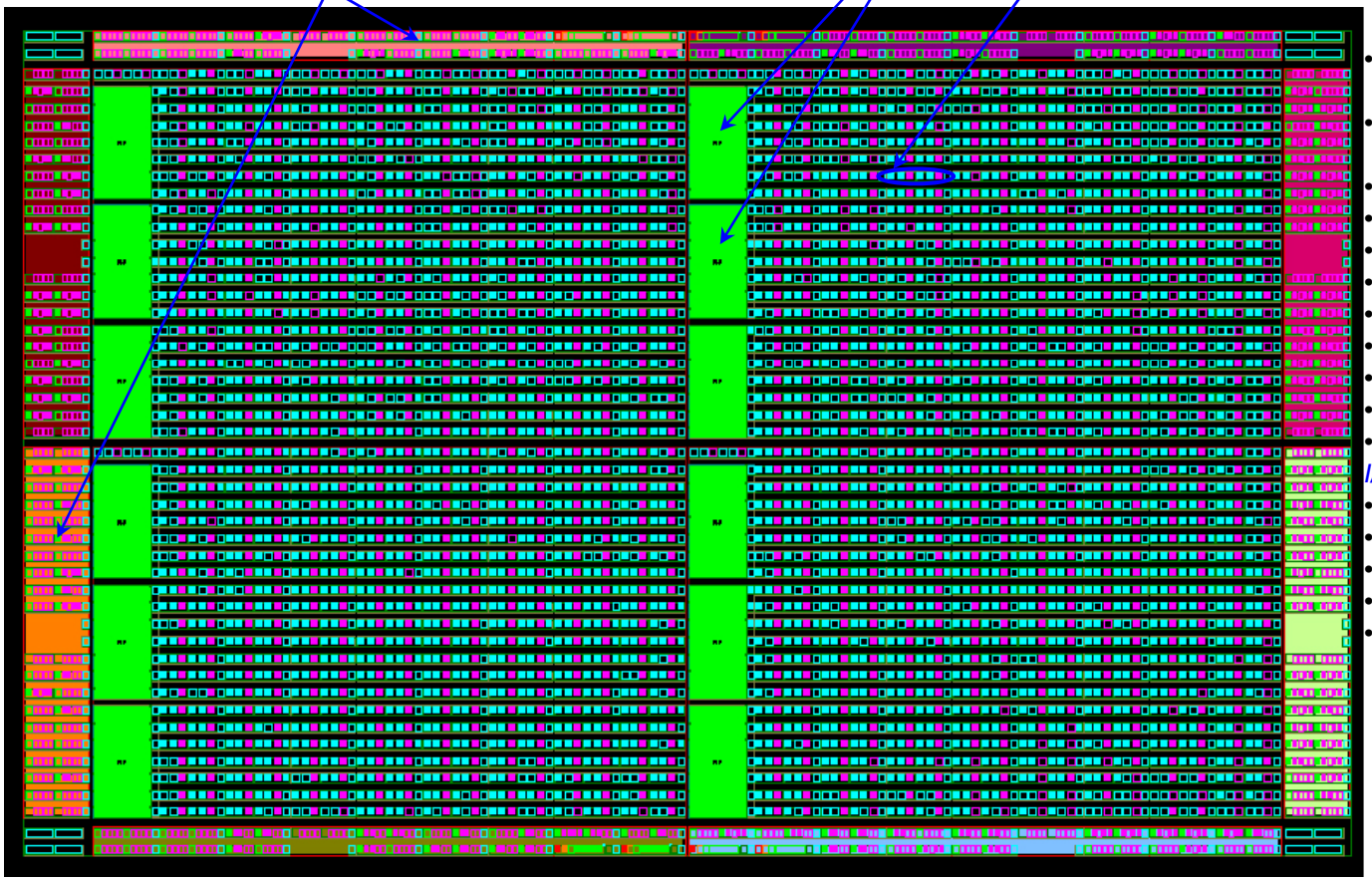
FEPGA firmware inside AX250



RAMBlock

IOs Banks

1 SuperCluster



Compile report:

==========

Family : Axcelerator

Device : ***AX250***

Package : ***484 FBGA***

Post-Combiner device utilization:

- SEQUENTIAL (R-cells)
  Used: 1249 Total: 1408 ***(88.71%)***
- COMB (C-cells)
  Used: 2181 Total: 2816 ***(77.45%)***
- LOGIC (R+C cells)
  Used: 3430 Total: 4224 ***(81.20%)***
- RAM/FIFO Used: 12 Total: 12
- IO w/Clocks Used: 148 Total: 248
- CLOCK (Routed) Used: 3 Total: 4
- PLL Used: 2 Total: 8
- Input I/O Register : 0
- Output I/O Register : 0
- DDR Register : 0
- Comb-Comb (CC) : 0
- Carry Chain : 65

I/O Information:

- Input Pads : 63
- Output Pads : 84
- Bidirectional Pads : 1
- Differential Input Pairs : 0
- Differential Output Pairs : 0

ProASIC3 Family device architecture (Flash technology)

Basic cell : VersaTile

Each Versatile can be configured as :
(by programming the appropriate flash switch interconnections)

- A three input logic funtion
- A D-flip-flop (with or without enable)
- A latch

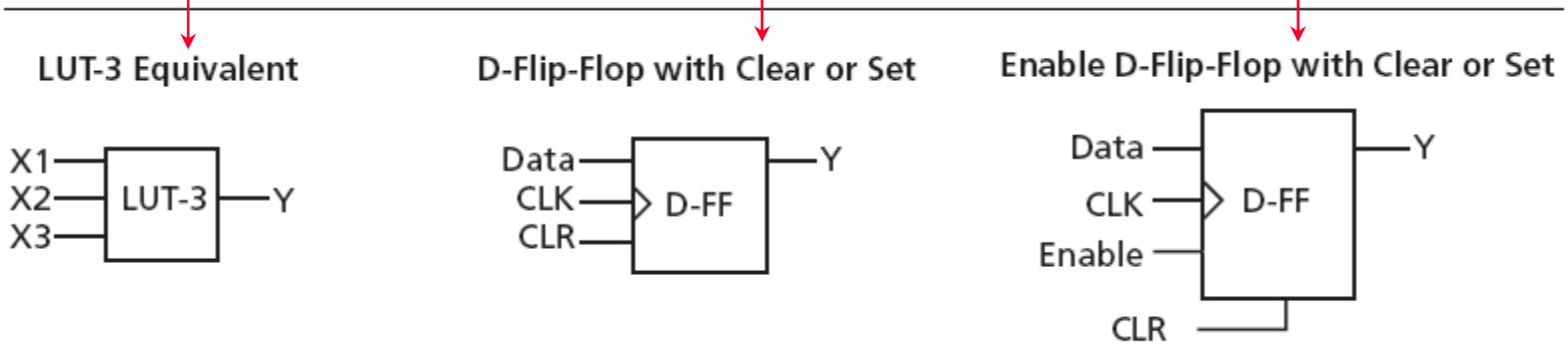


Figure 1-2 • **VersaTile Configurations**

ProASIC3 Family architecture (Flash technology)

A sea of VersaTile

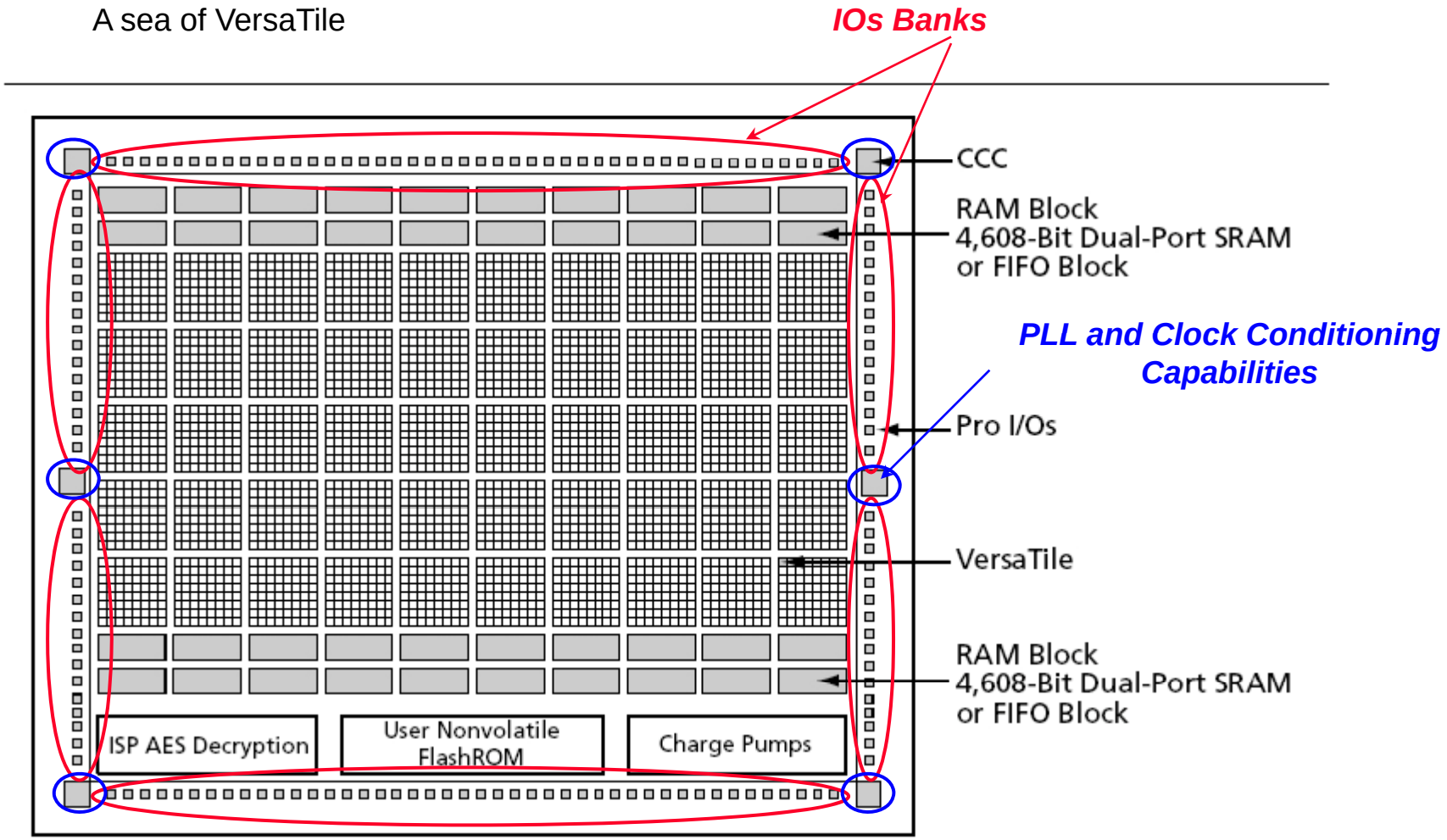
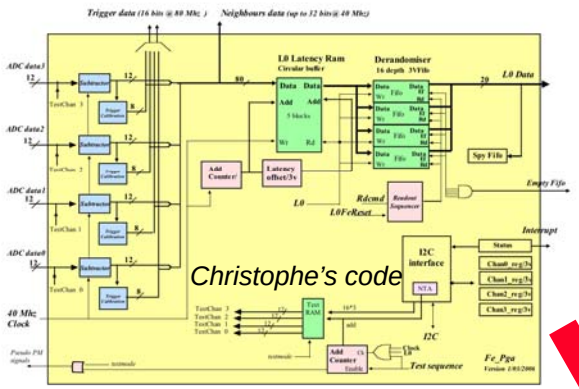


Figure 1-1 • **ProASIC3E Device Architecture Overview**

Example of FEPGA firmware inside PA3E: A3PE600



Compile report:

x 1.6 (R+C Cells)

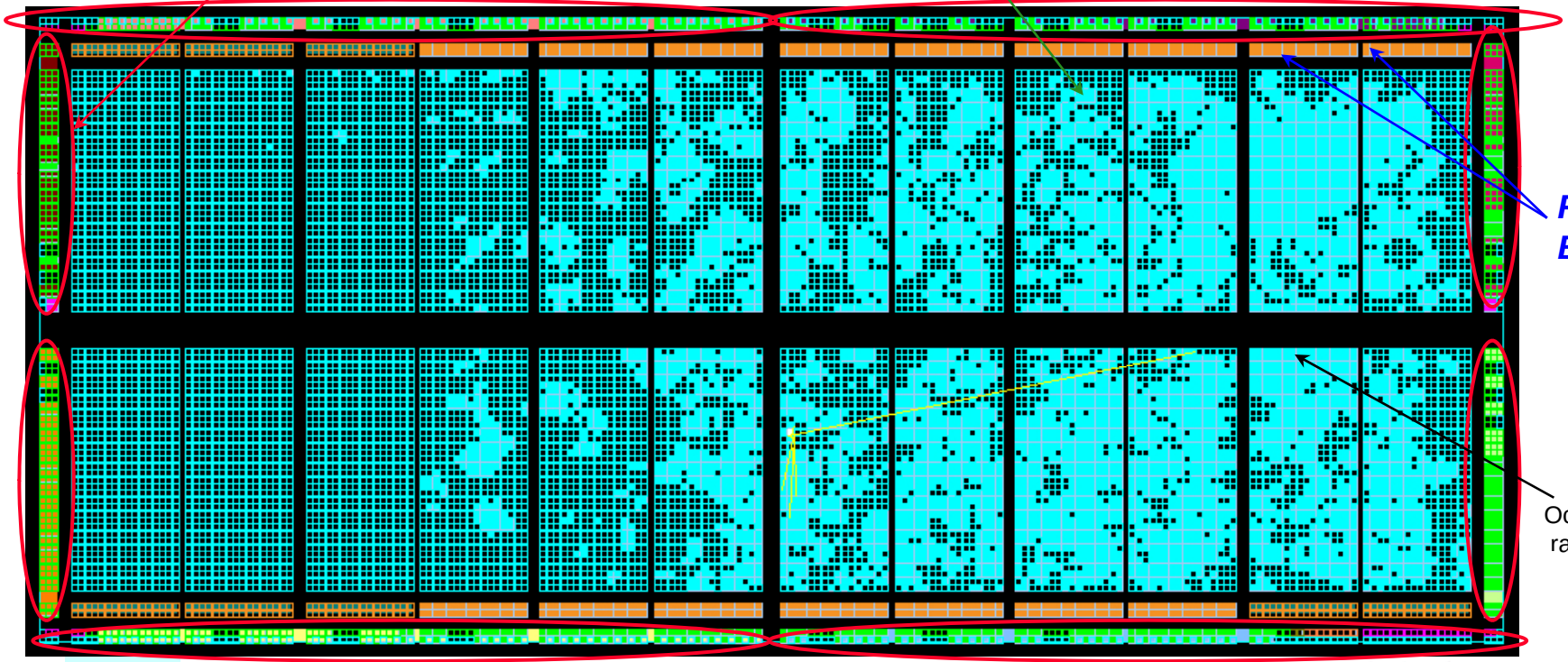
==========

- CORE(VersaTiles) : ***Used: 5374*** Total: 13824 (38.87%)
- IO (W/ clocks) ***Used: 147*** Total: 270 (54.44%)
- Differential IO Used: 0 Total: 135 (0.00%)
- GLOBAL (Chip+Quadrant) Used: 6 Total: 18 (33.33%)
- PLL Used: 2 Total: 6 (33.33%)
- RAM/FIFO ***Used: 16*** Total: 24 (66.67%)

Family : ProASIC3E
Device : A3PE600
Package : 484 FBGA

IOs Banks

VersaTiles



RAM Block

Occupancy rate

Estimation of needed resources in ProASIC3 family

	Curent FEPGA 4 Channels (AX250)	Futur FEPGA 8 Channels (PA3 Family ?)	Futur FEPGA 8 Channels (AX 500) *(BackUp solution !)*
IOs	148	~ 260 *(Jacques calculation !)*	317 (FG 484) 336 (FG 676)
IOs Banks	8	8 *4 is too few considering IOs diversity (GBT, ADC, …)*	8
RAM Blocks	12 (L0 Latency Derandomiser)	~ 26 *Packing (~24)* *Test RAM (~2)*	16
Cells	3430 (R+C Cells) (~ 5374 Versatiles)	~ 11000 Versatiles	8064 (R+C Cells)
PLL	8 (used: 2)	1 ?	8

IOs : 96 ADC + 32 Trigger + 48 neighbour + (58 ou 28) GBT + 21 Divers = 253 ou 225

Packing : 96 bits during N samples if N=1024 => 24 Blocks RAM

Possible target in A3P family

ProASIC3 Devices	A3P015	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
CoreMP7 Devices								M7A3P1000
Cortex-M1 Devices					M1A3P250	M1A3P400	M1A3P600	M1A3P1000
System Gates	15,000	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000
Typical Equivalent Macrocells	128	256	512	1,024	2,048	–	–	–
VersaTiles (D-Flip-Flop)	384	768	1,536	3,072	6,144	9,216	13,824	24,576
RAM kbits (1,024 bits)	–	–	18	36	36	54	108	144
4,608-Bit Blocks	–	–	4	8	8	12	24	32
FlashROM Bits	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024
Secure (AES) ISP [1]	–	–	Yes	Yes	Yes	Yes	Yes	Yes
PLLs	–	–	1	1	1	1	1	1
VersaNet Globals[2]	6	6	18	18	18	18	18	18
I/O Standards	Std. & Hot Swap	Std. & Hot Swap	Std.+	Std.+	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS
I/O Banks (+JTAG)	2	2	2	2	4	4	4	4
Maximum User I/Os	49	81	96	133	157	194	235	300
Speed Grades	-F, Std.	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2
Temperature Grades	C, I	C, I	C, I, T	C, I, T	C, I, T	C, I	C, I	C, I, T, M
Single-Ended I/Os / Differential I/O Pairs								
QN48		34						
QN68	49	49						
QN132		81	80	84	87/19[3]			
VQ100		77	71	71	68/13			
TQ144			91	100				
PQ208				133	151/34	151/34	154/35	154/35
FG144			96	97	97/24	97/25	97/25	97/25
FG256					157/38[3]	178/38	177/43	177/44
FG484						194/38	235/60	300/74

1.5 V core operation

A3P1000
Pb number of bank !

4 is too few considering IOs diversity (GBT, ADC, …)

Possible target in A3PE family

ProASIC3E Devices	A3PE600	A3PE1500	A3PE3000
Cortex-M1 Devices		**M1A3PE1500**	**M1A3PE3000**
System Gates	600,000	1,500,000	3,000,000
VersaTiles (D-Flip-Flop)	13,824	38,400	75,264
RAM kbits (1,024 bits)	108	270	504
4,608-Bit Blocks	24	60	112
FlashROM Bits	1,024	1,024	1,024
Secure (AES) ISP	Yes	Yes	Yes
Integrated PLL in CCCs[1]	6	6	6
VersaNet Globals[2]	18	18	18
I/O Standards	Pro	Pro	Pro
I/O Banks (+JTAG)	8	8	8
Maximum User I/Os	270	444	620
Speed Grades	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2
Temperature Grades	C, I	C, I	C, I
Single-Ended I/O / Differential I/O Pairs			
PQ208	147/65	147/65	147/65
FG256	165/79		
FG324			221/110
FG484	270/135	280/139	341/168
FG676		444/222	
FG896			620/310

- 1.5 V core operation
- Bigger than A3P

A3PE1500
Good candidat !

A3PE3000
- Oversize
- Pb of price !

Possible target in A3PL family

ProASIC3L Devices	A3P250L	A3P600L	A3P1000L	A3PE600L	A3PE3000L
Cortex-M1 Devices		M1A3P600L	M1A3P1000L		M1A3PE3000L
System Gates	250,000	600,000	1,000,000	600,000	3,000,000
VersaTiles (D-Flip-Flop)	6,144	13,824	24,576	13,824	75,264
RAM kbits (1,024 bits)	36	108	144	108	504
4,608-Bit Blocks	8	24	32	24	112
FlashROM Bits	1,024	1,024	1,024	1,024	1,024
Secure (AES) ISP[1]	Yes	Yes	Yes	Yes	Yes
Integrated PLLs in CCCs[2]	1	1	1	6	6
VersaNet Globals	18	18	18	18	18
I/O Standards	Std.+/LVDS	Std.+/LVDS	Std.+/LVDS	Pro	Pro
I/O Banks (+JTAG)	4	4	4	8	8
Maximum User I/Os	157	235	300	270	620
Typical Static / Flash*Freeze Power (mW) at Vcc=1.2 V	0.33	0.66	1.06	TBA	3.30
Speed Grades	Std., -1	Std., -1	Std., -1	Std., -1	Std., -1
Temperature Grades	C, I	C, I	C, I	M	C, I, M
Single-Ended I/Os / Differential I/O Pairs					
VQ100	68/13				
PQ208	151/34	154/35	154/35		147/65[2]
FG144	97/24	97/25	97/25		
FG256	157/38	177/43	177/44		
FG324					221/110
FG484		235/60	300/74	270/135	341/168
FG896					620/310

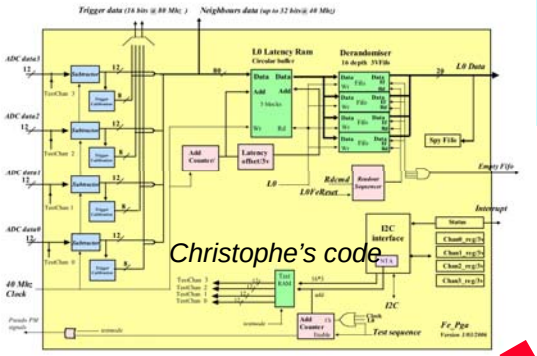
Low power 1.2 to 1.5 V core operation

4 is too few considering IOs diversity (GBT, ADC, …)

A3P1000
Pb number of bank !

A3PE3000
- Oversize
- Pb of price !

Compilation inside possible target : A3PE1500



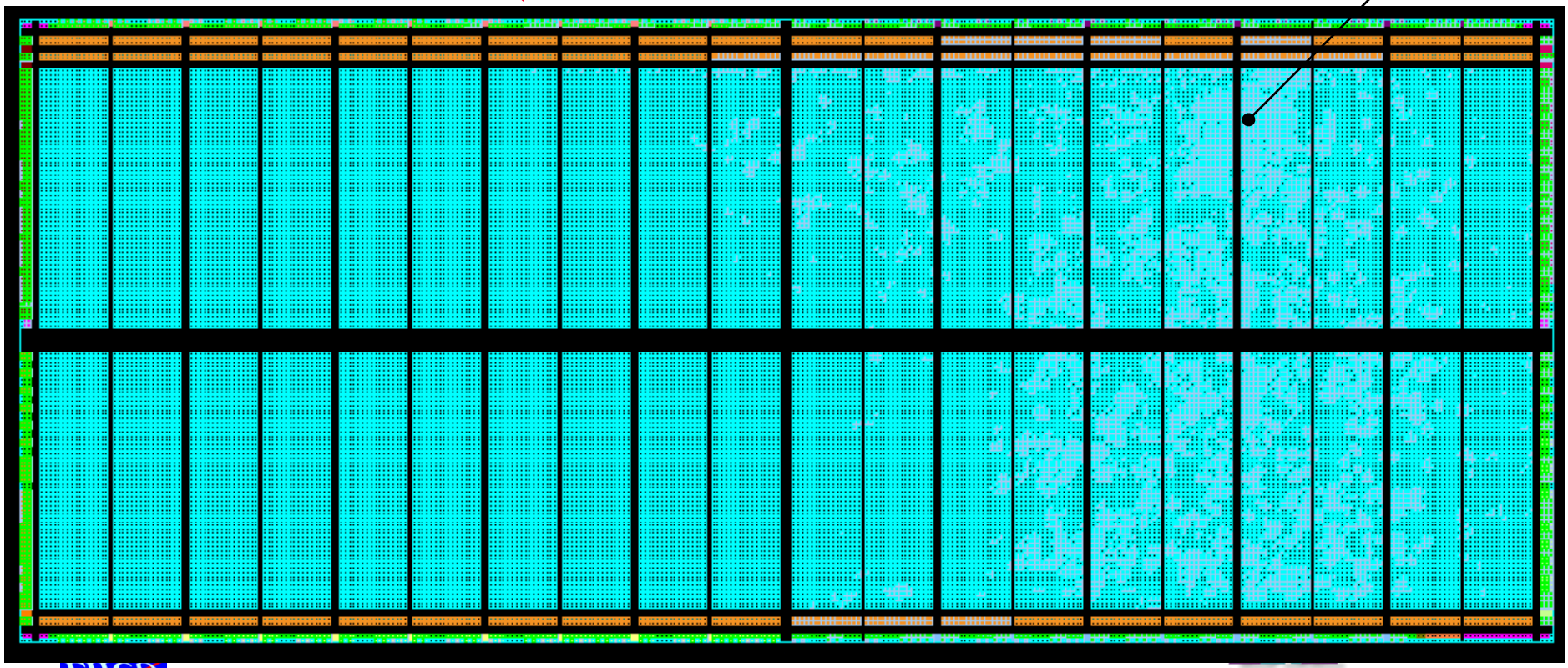
Family : ProASIC3E
Device : A3PE1500
Package : 484
FBGA

Compile report:

==========

CORE	***Used:***	***5374***	Total: 38400	(13.99%)
IO (W/ clocks)	***Used:***	***147***	Total: 280	(52.50%)
Differential IO	Used:	0	Total: 139	(0.00%)
GLOBAL (Chip+Quadrant)	Used:	6	Total: 18	(33.33%)
PLL	Used:	2	Total: 6	(33.33%)
RAM/FIFO	***Used:***	***16***	Total: 60	(26.67%)
Low Static ICC	Used:	0	Total: 1	(0.00%)
FlashROM	Used:	0	Total: 1	(0.00%)
User JTAG	Used:	0	Total: 1	(0.00%)

Occupancy rate



Possibilities of migration inside A3P Family

ProASIC3 Devices	A3P015	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
CoreMP7 Devices								M7A3P1000
Cortex-M1 Devices					M1A3P250	M1A3P400	M1A3P600	M1A3P1000
System Gates	15,000	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000
Typical Equivalent Macrocells	128	256	512	1,024	2,048	–	–	–
VersaTiles (D-Flip-Flop)	384	768	1,536	3,072	6,144	9,216	13,824	24,576
RAM kbits (1,024 bits)	–	–	18	36	36	54	108	144
4,608-Bit Blocks	–	–	4	8	8	12	24	32
FlashROM Bits	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024
Secure (AES) ISP [1]	–	–	Yes	Yes	Yes	Yes	Yes	Yes
PLLs	–	–	1	1	1	1	1	1
VersaNet Globals[2]	6	6	18	18	18	18	18	18
I/O Standards	Std. & Hot Swap	Std. & Hot Swap	Std.+	Std.+	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS
I/O Banks (+JTAG)	2	2	2	2	4	4	4	4
Maximum User I/Os	49	81	96	133	157	194	235	300
Speed Grades	-F, Std.	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2
Temperature Grades	C, I	C, I	C, I, T	C, I, T	C, I, T	C, I	C, I	C, I, T, M
Single-Ended I/Os / Differential I/O Pairs								
QN48		34						
QN68	49	49						
QN132		81	80	84	87/19[3]			
VQ100		77	71	71	68/13			
TQ144			91	100				
PQ208				133	151/34	151/34	154/35	154/35
FG144			96	97	97/24	97/25	97/25	97/25
FG256					157/38[3]	178/38	177/43	177/44
FG484						194/38	235/60	300/74

Migration possible inside the same family :
- From higher to middle density device

Migration possibilitiy between family :
- A3P1000 <-> A3P1000L except pin Flash freeze.
- A3P3000 <-> A3P3000L except pin Flash freeze.

Summary

	Package Pins	IOs Max	IO Bank	VersaTitles or R_Cells C_Cells	BlockRAM (4608 bits Blocks)	PLL	VersaTitles or R_Cells C_Cells used	Resource used with FEPGA fimware	Prices (PU for 1000)
AX250	484 FBGA	248	8	R_Cell : 1408 C_Cell : 2816	12	8	R_Cell : 1249 C_Cell : 2181	R_Cells : 89% C_Cells : 78% - 148 / 248 IOs	PUHT € 42.55
AX500	484 FBGA	317	8		16	8	R_Cell : 1249 (x2) C_Cell : 2181 (x2)		PUHT € 69.8$
	(FG676)	336							
A3P1000	484 FBGA	300	4	24576	32	1	5390 (x2)	- 22% VersaTitles - 147 / 300 IOs	PUHT € 36.90
A3PE600	484 FBGA	270	8	13824	24	6	5374 (x2)	- 40% VersaTitles - 147 / 270 IOs	PUHT € 39.40
A3PE1500	484 FBGA	280	8	38400	60	6	5374 (x2)	- 14% VersaTitles - 147 / 270 IOs	PUHT € 92.10
	(FG676)	444							PUHT € 93.70
A3PE3000	484 FBGA	341	8	75264	112	6	5374 (x2)	- 7% VersaTitles - 147 / 341 IOs	PUHT € 198.10 *
	(FG896)	620							PUHT € 213.30 *
A3P1000L	484 FBGA	300	4	24576	32	1	5345 (x2)	- 22% VersaTitles - 147 / 300 IOs	PUHT € 49.40
A3PE3000L	484 FBGA	341	8	75264	112	6	5345 (x2)	- 7% VersaTitles - 147 / 341 IOs	PUHT € 222.30 *
	(FG896)	620							

Axcelerator

A3P Family

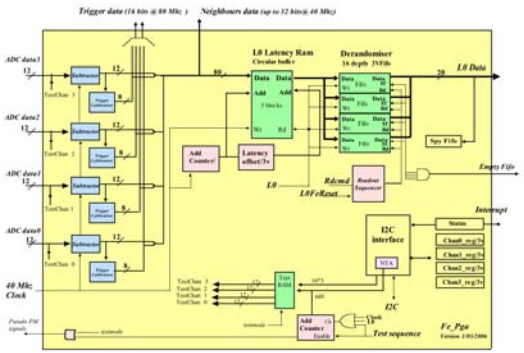
Curent FEPGA 4 Channels

* **LIBERO PLATINUM** X 1 PUHT € 2495

For 8 Channels

Spares

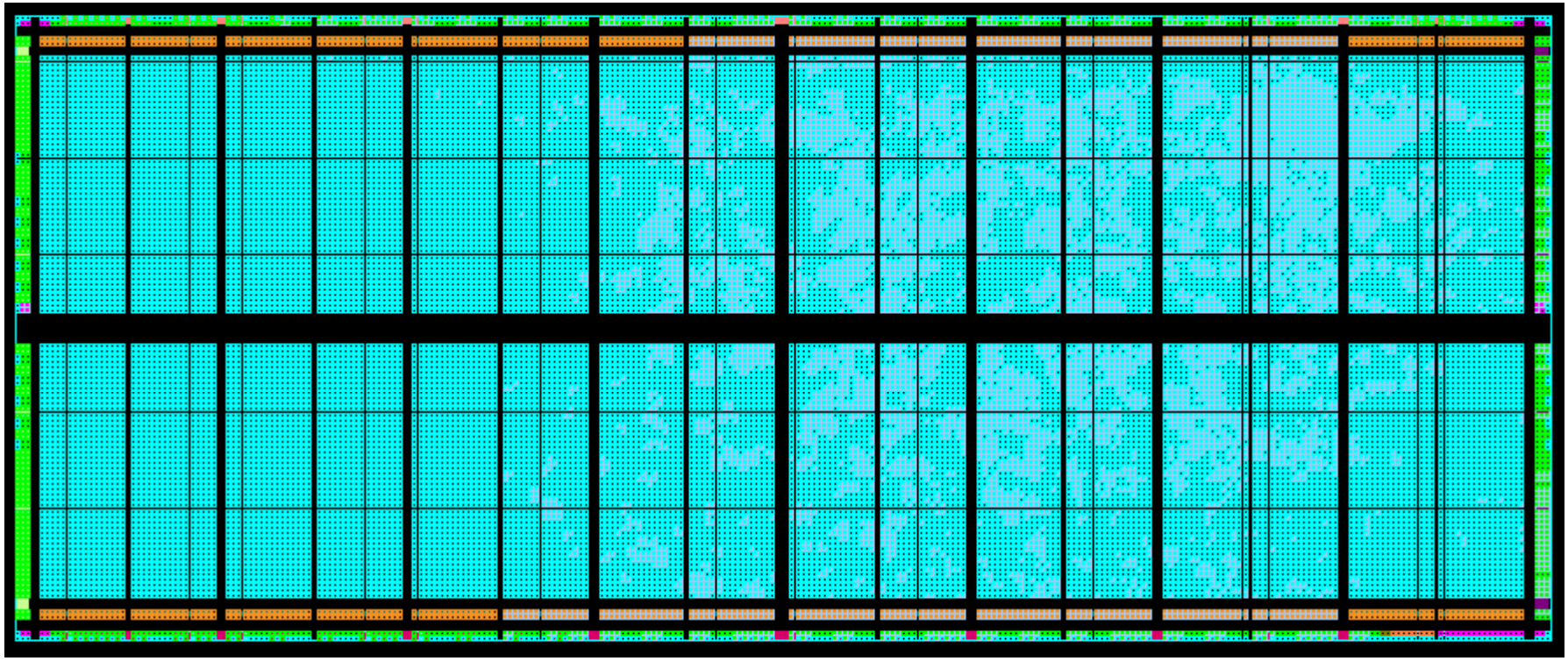
FEPGA firmware inside PA3: A3P1000



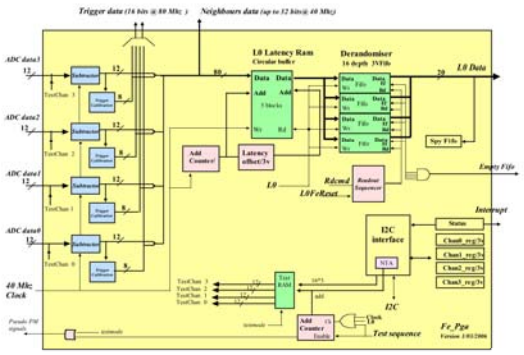
Family : ProASIC3
Device : A3P1000
Package : 484 FBGA

Compile report:
==========

CORE	Used: 5392	Total: 24576	(21.94%)
IO (W/ clocks)	Used: 147	Total: 300	(49.00%)
Differential IO	Used: 0	Total: 74	(0.00%)
GLOBAL (Chip+Quadrant)	Used: 6	Total: 18	(33.33%)
PLL	Used: 1	Total: 1	(100.00%)
RAM/FIFO	Used: 16	Total: 32	(50.00%)
Low Static ICC	Used: 0	Total: 1	(0.00%)
FlashROM	Used: 0	Total: 1	(0.00%)
User JTAG	Used: 0	Total: 1	(0.00%)



FEPGA firmware inside PA3E : A3PE3000



Family : ProASIC3E
Device : A3PE3000
Package : 484 FBGA

LIBERO PLATINUM X 1 PUHT € 2495

Compile report:

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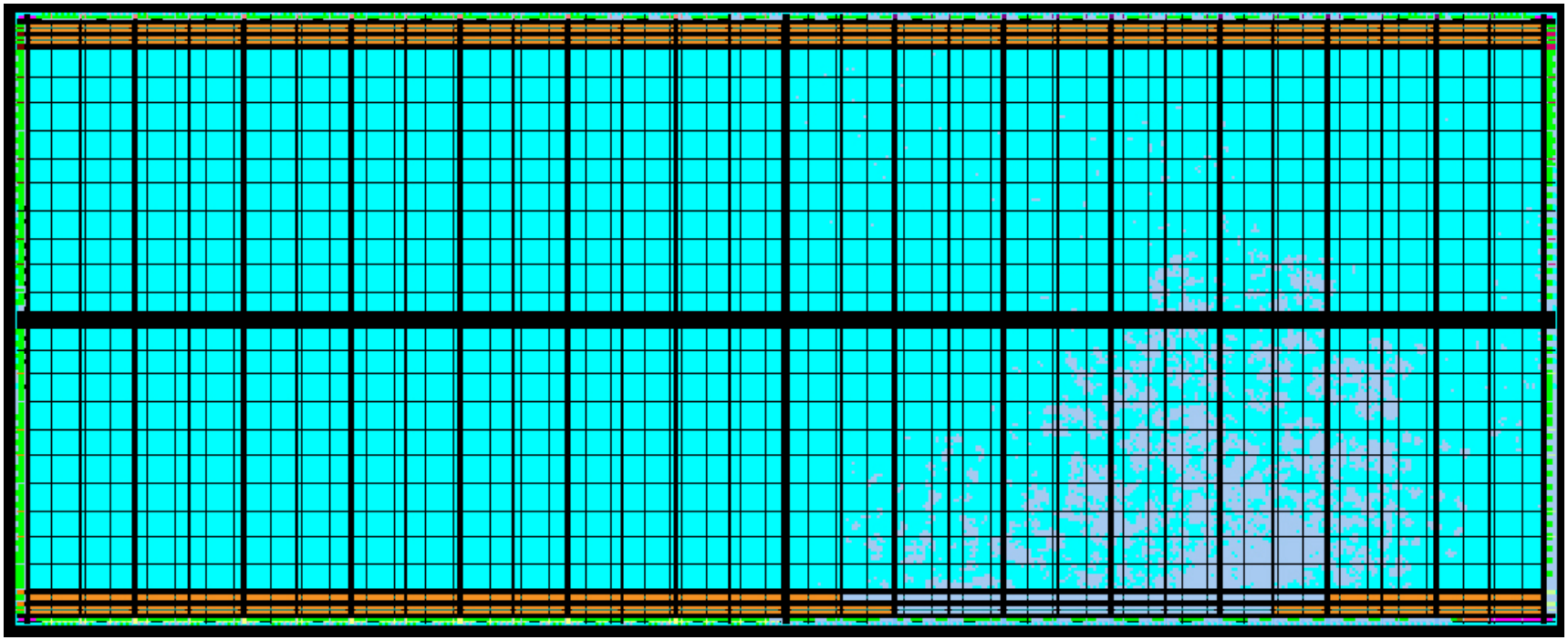
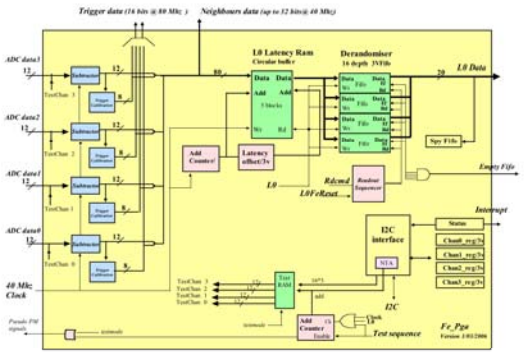
CORE	Used: 5374	Total: 75264	(7.14%)
IO (W/ clocks)	Used: 147	Total: 341	(43.11%)
Differential IO	Used: 0	Total: 168	(0.00%)
GLOBAL (Chip+Quadrant)	Used: 6	Total: 18	(33.33%)
PLL	Used: 2	Total: 6	(33.33%)
RAM/FIFO	Used: 16	Total: 112	(14.29%)
Low Static ICC	Used: 0	Total: 1	(0.00%)
FlashROM	Used: 0	Total: 1	(0.00%)
User JTAG	Used: 0	Total: 1	(0.00%)



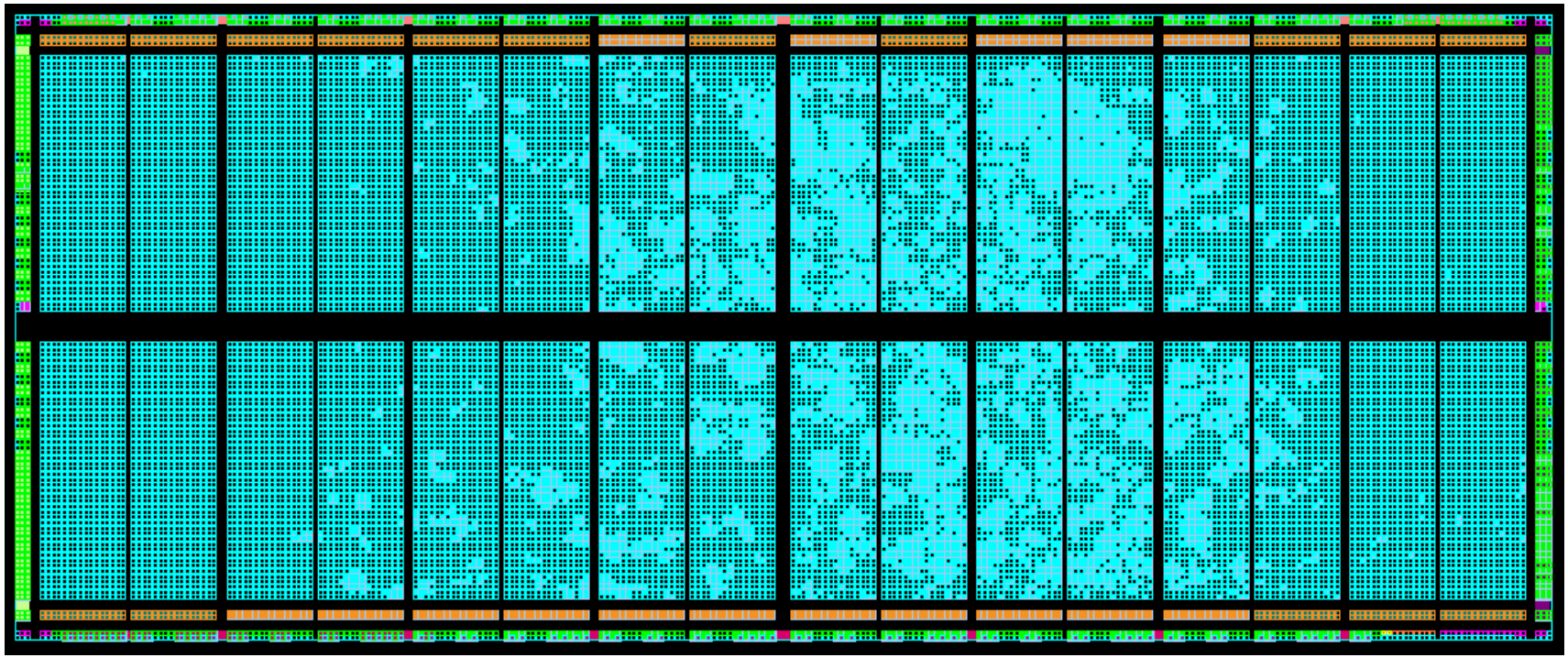
FEPGA firmware inside PA3E : A3P1000L



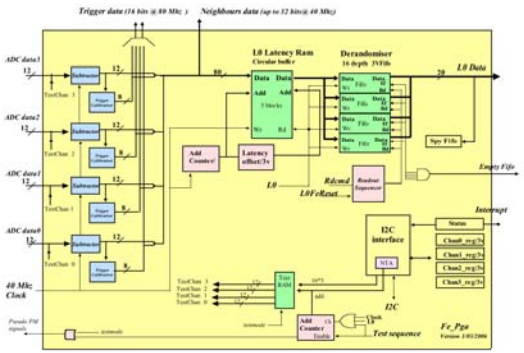
Family : ProASIC3L
Device : A3P1000L
Package : 484 FBGA

Compile report:
==========

CORE	Used:	5345	Total: 24576	(21.75%)
IO (W/ clocks)	Used:	147	Total: 300	(49.00%)
Differential IO	Used:	0	Total: 74	(0.00%)
GLOBAL (Chip+Quadrant)	Used:	6	Total: 18	(33.33%)
PLL	Used:	1	Total: 1	(100.00%)
RAM/FIFO	Used:	16	Total: 32	(50.00%)
Low Static ICC	Used:	0	Total: 1	(0.00%)
FlashROM	Used:	0	Total: 1	(0.00%)
User JTAG	Used:	0	Total: 1	(0.00%)



FEPGA firmware inside PA3E : A3PE3000L



Family : ProASIC3L
Device : A3PE3000L
Package : 484 FBGA

Compile report:
==========

CORE	Used:	5345	Total: 75264	(7.10%)
IO (W/ clocks)	Used:	147	Total: 341	(43.11%)
Differential IO	Used:	0	Total: 168	(0.00%)
GLOBAL (Chip+Quadrant)	Used:	6	Total: 18	(33.33%)
PLL	Used:	1	Total: 6	(16.67%)
RAM/FIFO	Used:	16	Total: 112	(14.29%)
Low Static ICC	Used:	0	Total: 1	(0.00%)
FlashROM	Used:	0	Total: 1	(0.00%)
User JTAG	Used:	0	Total: 1	(0.00%)

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