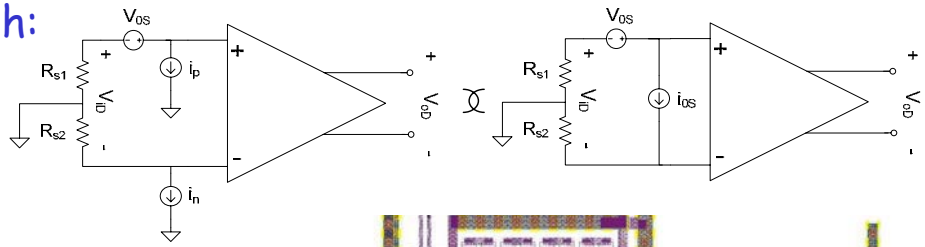
Offset on SPD

Offset: preamplifier

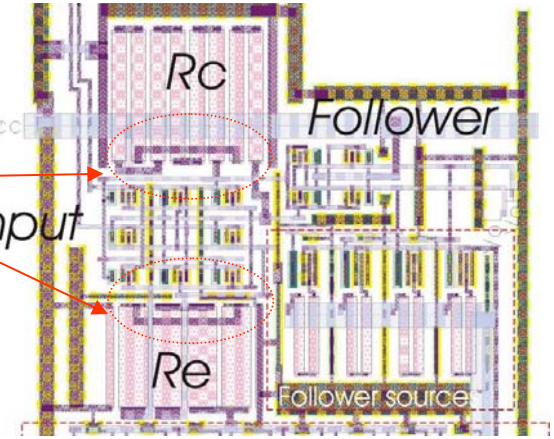
- Preamplifier v_{0SP} as function of device mismatch:

$$V_{0SP} \simeq V_T \left(\frac{\Delta R_C}{R_C} \left(1 + \frac{g_m R_E}{\alpha_F} \right) + \frac{\Delta I_S}{I_S} - \frac{g_m R_E}{\alpha_F} \left(\frac{\Delta R_E}{R_E} - \frac{\Delta \alpha_F}{\alpha_F} \right) \right)$$



- Emitter degeneration does not help.

- In fully balanced circuits mean offset should be 0
  - Schematic it is, layout it is not: path connecting RE and RC component devices is not symmetrical!
  - Average offset: $\mu(v_{0SP})$=-0,75 mV
  - Not corrected: useful to improved dynamic range.



- Random offset std. dev.: yield versus performance:

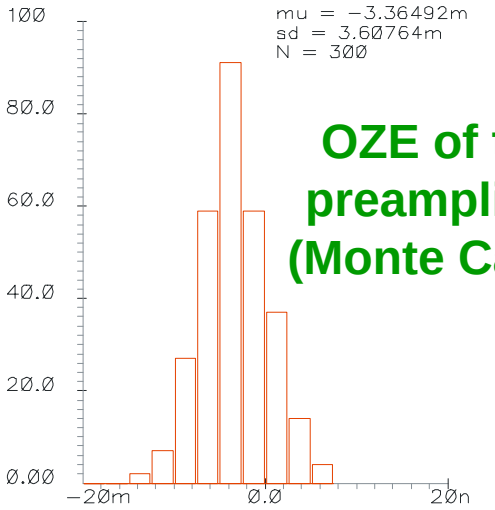
$$\sigma_{V_{0SP}} \simeq V_T \sqrt{\left(\frac{\sigma_{\Delta R_C}}{R_C}\right)^2 \left(1 + \frac{g_m R_E}{\alpha_F}\right)^2 + \left(\frac{\sigma_{\Delta I_S}}{I_S}\right)^2 + \left(\frac{\sigma_{\Delta R_E}}{R_E}\right)^2 \left(\frac{g_m R_E}{\alpha_F}\right)^2 + \left(\frac{\sigma_{\Delta \alpha_F}}{\alpha_F}\right)^2 \left(\frac{g_m R_E}{\alpha_F}\right)^2} \simeq 0{,}8\ mV\ rms$$

- Total output zero error (OZE): v_{0S}, i_{0S}, R_s and DC gain $A_{DD}(0)$:

$$OZE_P = A_{DD}(0)\, IZE_P = A_{DD}(0)\left(V_{0SP} + 2R_S I_{0SP}\right)$$

$$\sigma^2_{OZE_P} = A^2_{DD}(0)\left(\sigma^2_{V_{0SP}} + (2R_S)^2 \sigma^2_{I_{0SP}} + 2(2R_S)\operatorname{cov}(V_{0SP}, I_{0SP})\right) \simeq\Big|_{R_S < 5\,K\Omega} A_{DD}(0)\,\sigma_{V_{0SP}} = 3.6\ mV\ rms$$

$$\mu_{OZE_P} \simeq\Big|_{R_S \ll 5\,K\Omega} A_{DD}(0)\,\mu_{V_{0SP}} = -3.4\ mV$$



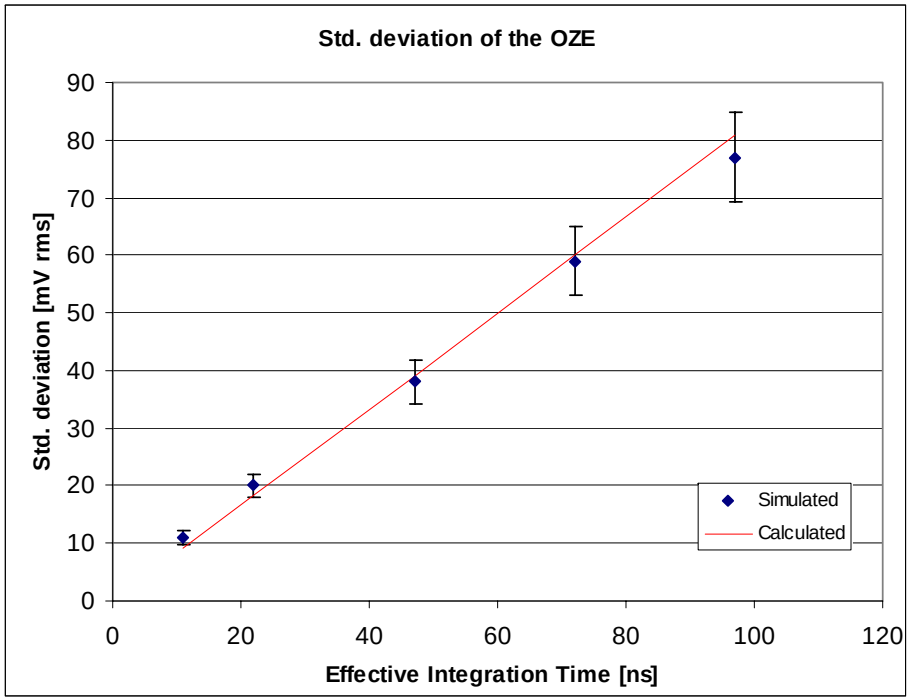
OZE of the preamplifier (Monte Carlo)

Offset: integrator

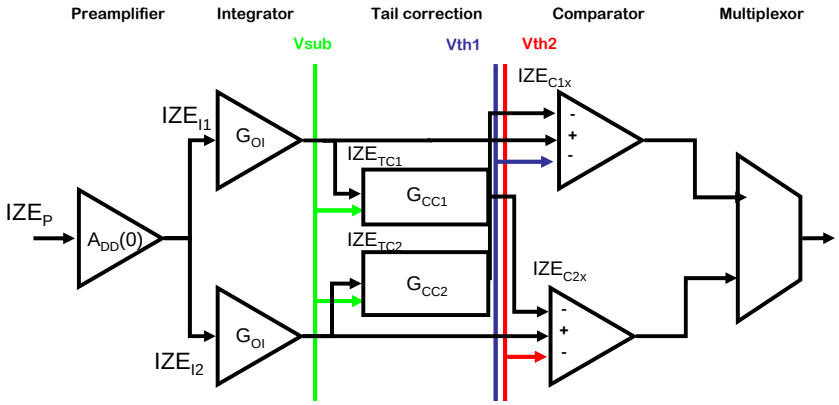
- Main contribution: input differential pair.
- Compute v_{OS} as in preamplifier: $\sigma_{V_{0SI}} = 1.2\ mV\ r.m.s.$
  - Preamplifier low output impedance: i_{OSI} is not relevant.
- Integrator is switching at 40 MHz: Transient response has to be considered!
- OZE depends linearly on T
  - For $T \ll G_{DM0} R_C C_f$:

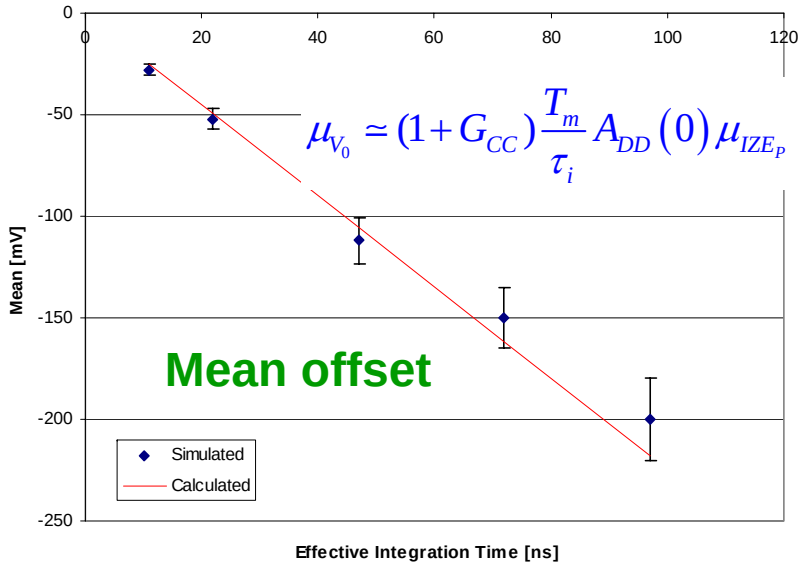
$$OZE(T_m) \simeq V_{OSI} \frac{T_m}{C_f R_E}$$

- Mismatch Monte Carlo simulations:
  - Compatible within statistical errors



Offset: full channel



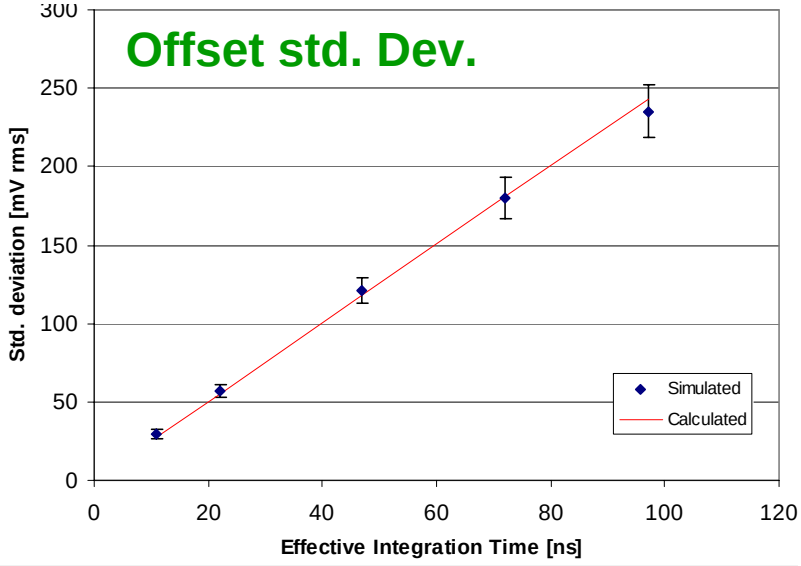


- For the full analogue chain the offset V_0 at the comparator input is:

$$V_0 = G_{0I1}\left[A_{DD}(0)\,IZE_P + IZE_{I1}\right] + G_{CC2}\left[G_{0I2}\left[A_{DD}(0)\,IZE_P + IZE_{I2}\right] + IZE_{TC2}\right] + IZE_{C1t} + IZE_{C1h} + IZE_{C1th}$$

  - IZE of all the blocks is comparable
  - Gain is concentrated on first stages
  - Uncorrelated sources

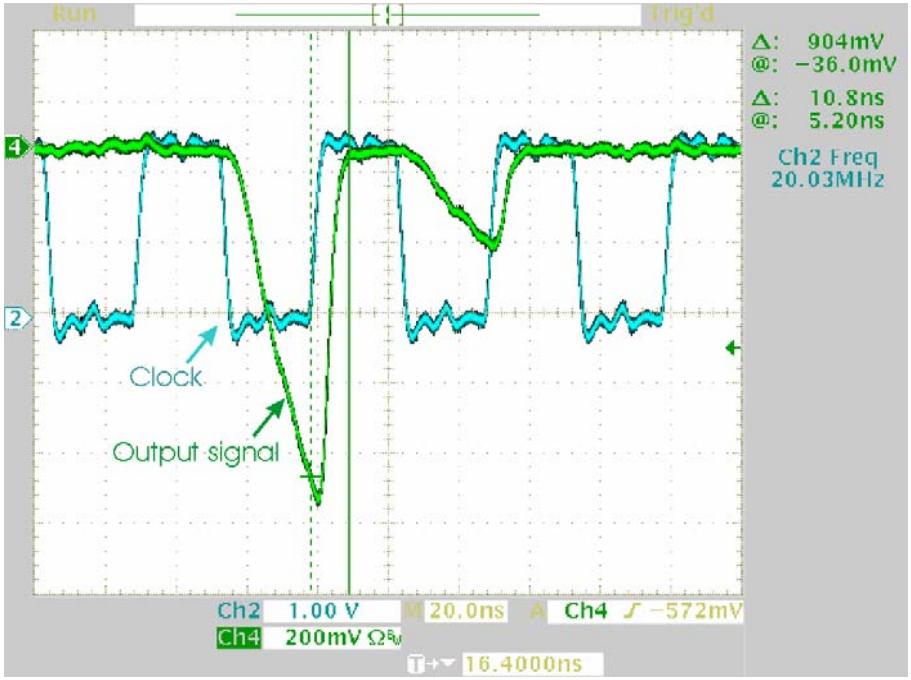
$$\sigma^2_{V_0} \simeq \left[G_{0I}(1+G_{CC})\right]^2\left[\sigma^2_{IZE_P}\left[A_{DD}(0)\right]^2 + \sigma^2_{IZE_I}\right]$$

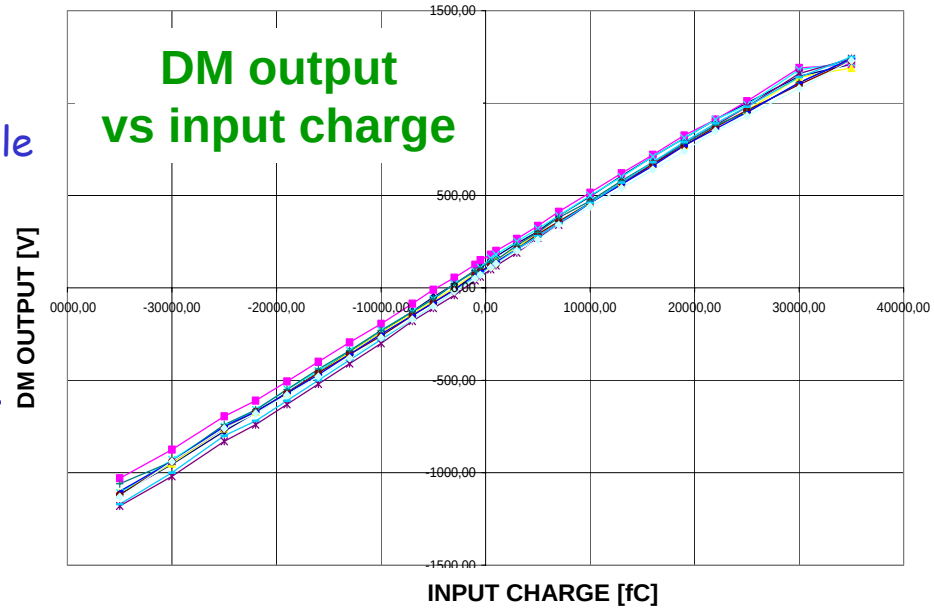


- Tail correction minimizes apparent offset:
  - Because G_{CC}<0.
- Calculations ok with Monte Carlo simulations.
- Temperature dependence: $\frac{\partial \mu_{V_0}}{\partial T} = -15\,\frac{\mu V}{K}$ $\frac{\partial \sigma_{V_0}}{\partial T} = 18\,\frac{\mu V}{K}$

Characterization of building blocks: integrator

- Good agreement except for mean offset.
- Post layout simulations including parasitic R and C do not show systematic offset.
- Offset measurement of the channel are compatible with some systematic offset, *but small*.
- Seems to be a true charge injection effect:
  - Clock or parasitic capacitance unbalance (channel).
  - Coupling at input pad (only block test circuit).
- Systematic injection: not a problem for resolution



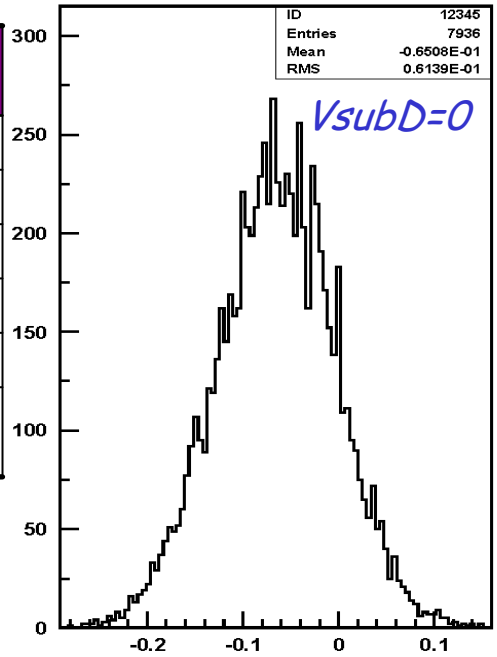


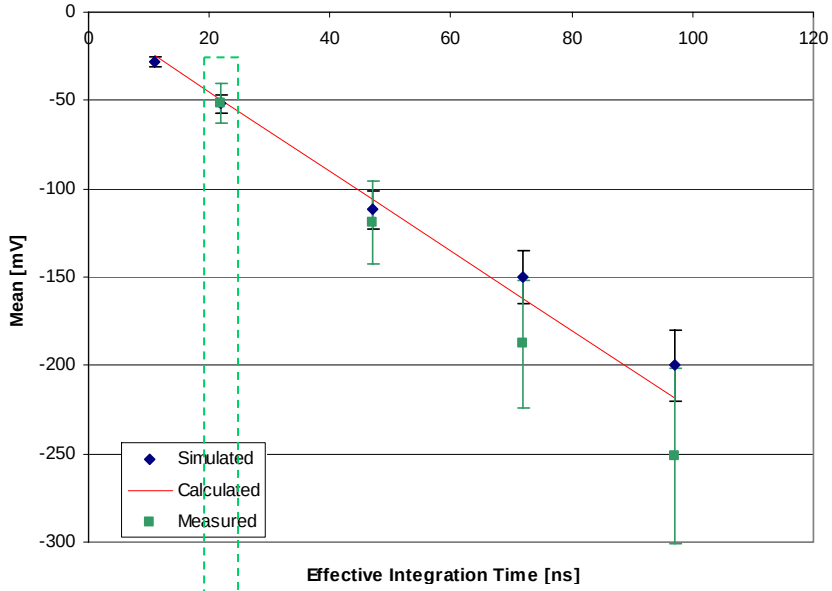
	Simulation / calculation	Measurement
Mean offset $\mu(v_{0SI})$	0	-1,3 mV
Std dev offset $\sigma(v_{0SI})$	1,2 mV rms	1,1 mV rms
Time constant ($R_E C_f$)	1,6 ns	1,6 ns
Reset time @ 1 V	< 10 ns	5 ns
Linearity error |VoD| < 300 mV	< 0,1 %	< 1 %
Temperature coefficient	- 150 ppm/C	- 200 ppm/C

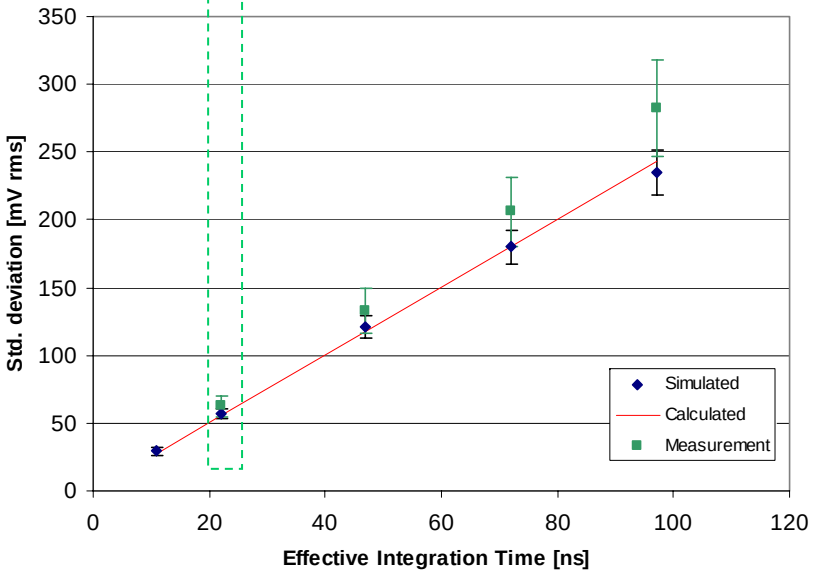
System performance: offset and yield

- Good agreement with calculations for chip soldered in VFE cards (perfect at T=25 ns).
- Discrepancies are higher for measurements in test socket (charge injection).
- A yield of 80 % is obtained.
- Less 1 % are rejected for high offset.

Total	1311	**100 %**
Digital Error	112	8,5 %
Bias problem	38	3 %
Gen. failure	29	2,2 %
Dead channel	73	5,6 %
High offset	9	0,7 %
Pass	1050	80 %



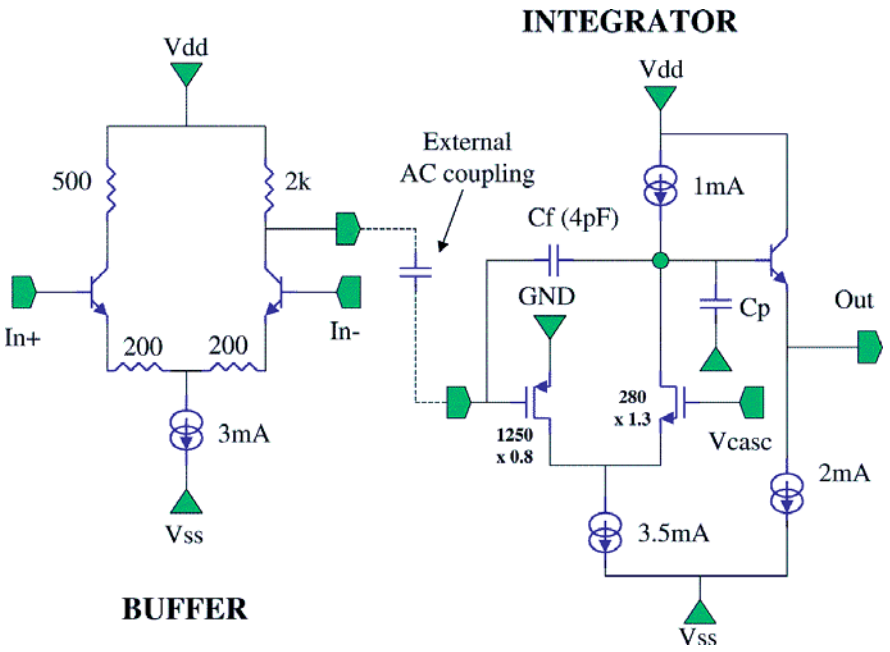


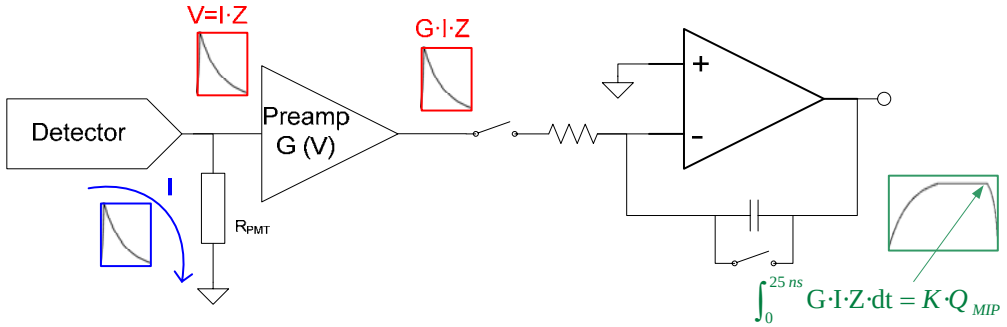


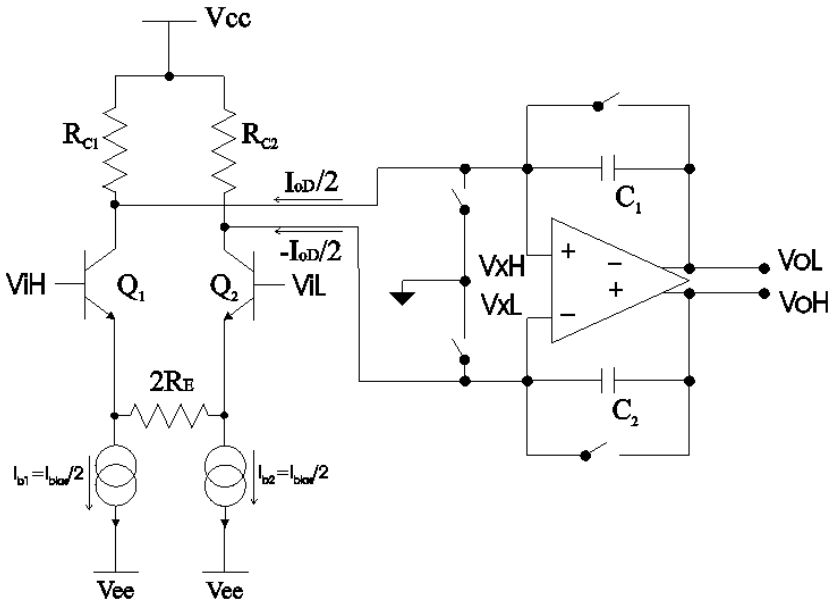
Extrapolation SPD to ECAL

- Gain: V (int. output) / Q

$$G_Q \equiv \frac{v_{oD}\left(t=T_m\right)}{-Q_{MIP}} \simeq R_{PMT} A \frac{1}{R_E C_f}\left(1-e^{-\frac{T_m}{\tau}}\right)_{T_m=25ns}$$







Conclusions

- Std deviation is about 55 mV rms
- Gain: V (int. output) / Q
  - 0,36 mV / ADC count
  - 5 fC / ADC count
  - 75 uV / fC: gain in charge is 16 higher in SPD
- Resistor converting PMT current to voltage is 470/50 = 9,4
- Voltage gain is only about factor 2 large in SPD
- Extrapolated "random" offset should be 27 mV rms!
  - It is probably smaller in PS
  - Improve by a factor 3 (technology, layout)
  - AC coupling, differentiator…
- Charge injection by switches is almost negligible
  - Thanks to differential circuitry and integration