On-Chip I-V Variability and Random Telegraph Noise Characterization in 28 nm CMOS

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Outline

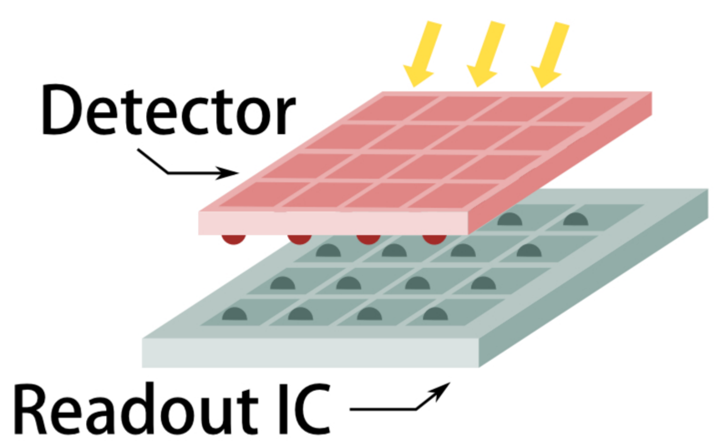
- Background & motivation
- Prior art comparison
- Proposed design
- Test chip results
- Conclusions

***This talk does not contain ITAR or EAR controlled information**

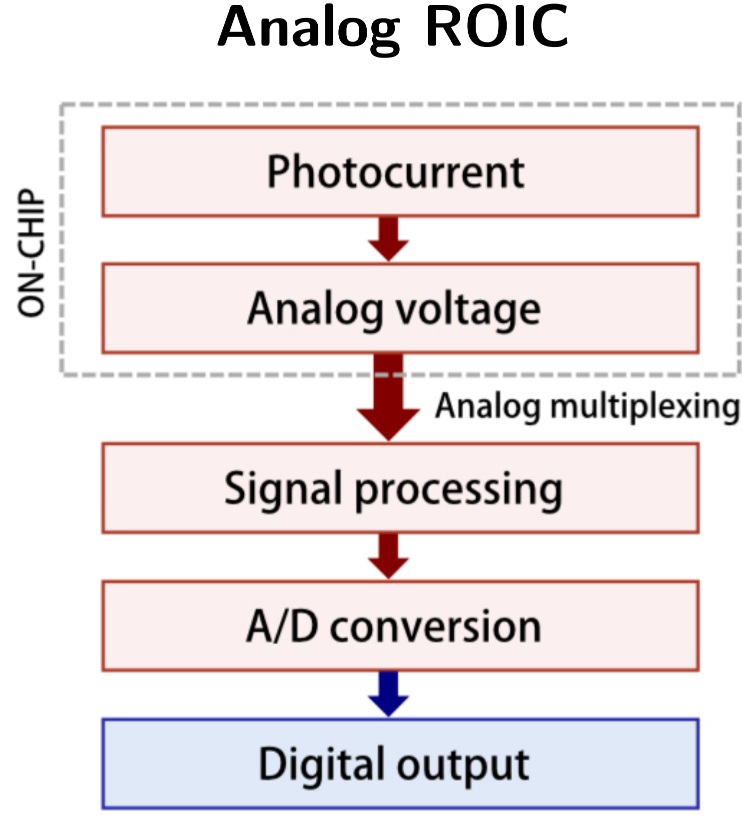
Outline

- **Background & motivation**
  - **Readout integrated circuits**
  - **Random telegraph noise (RTN)**
  - **RTN measurement challenges**
- Prior art comparison
- Proposed design
- Test chip results
- Conclusions

Readout Integrated Circuits (ROICs)



Infrared sensors use non-silicon detector arrays bonded to CMOS ROICs



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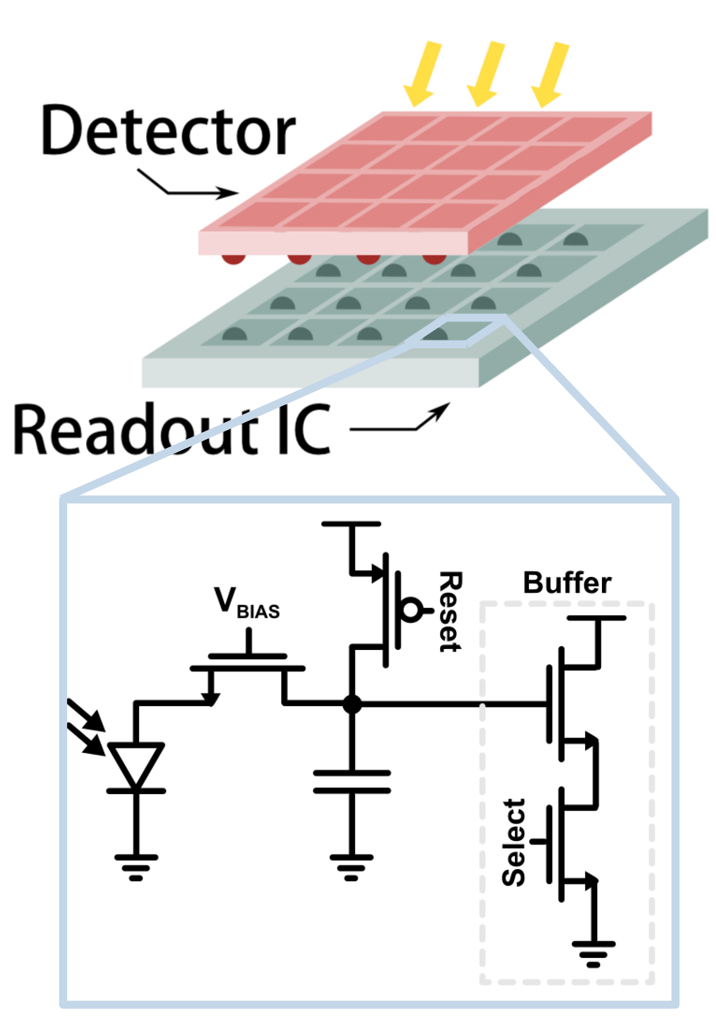
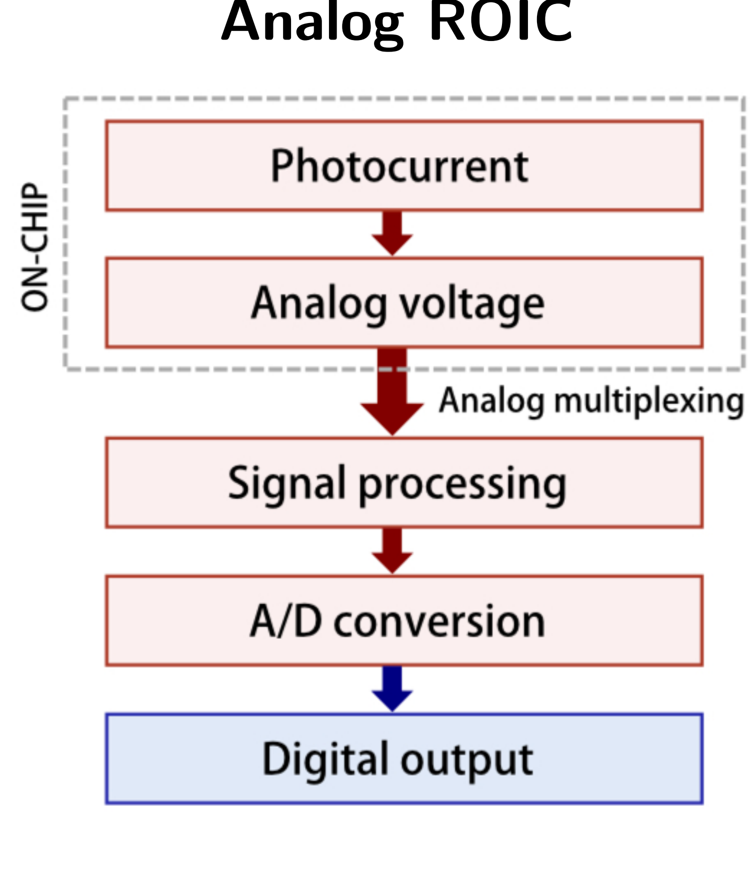
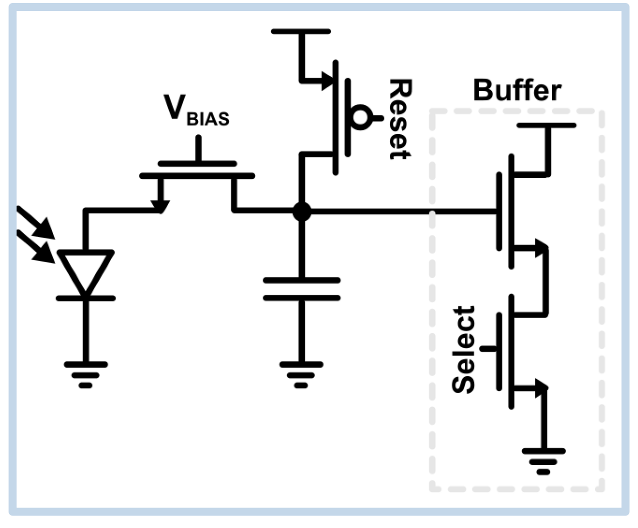


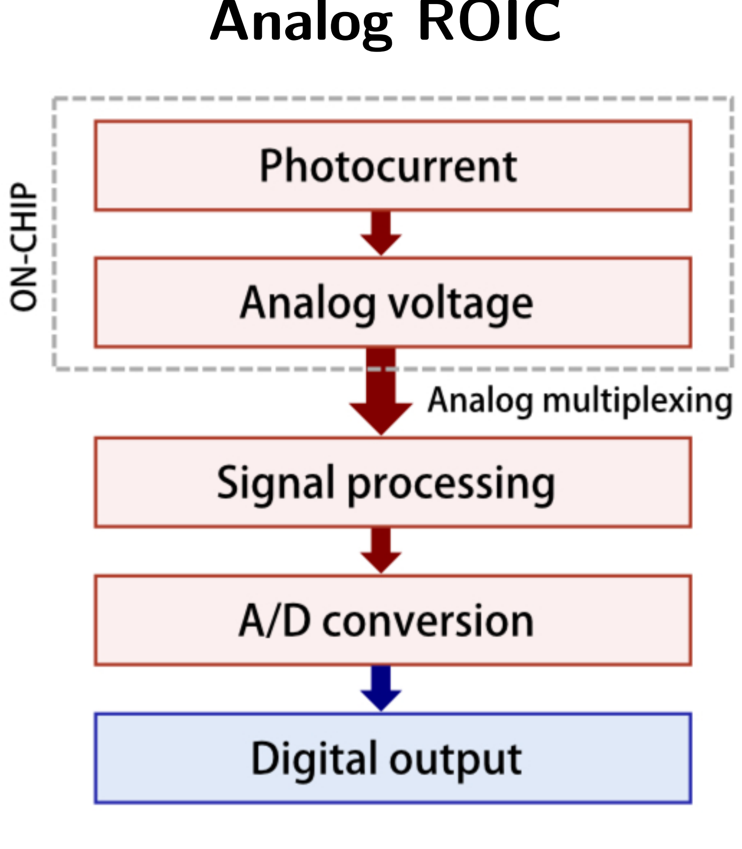


Readout Integrated Circuits (ROICs)

Maximum detectable signal set by $C_{int}V_{max}$

Reduces with technology node





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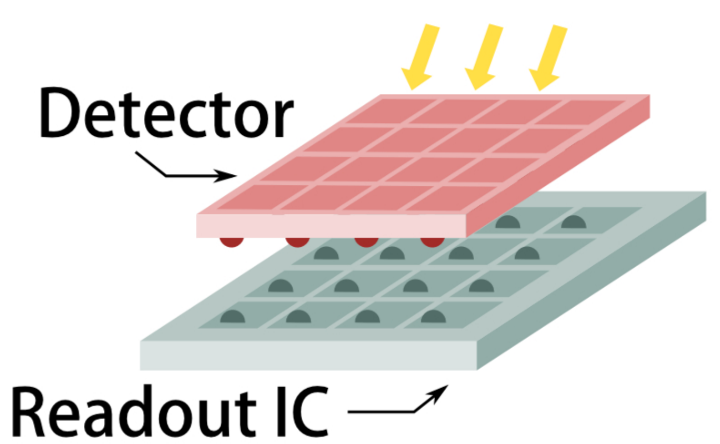
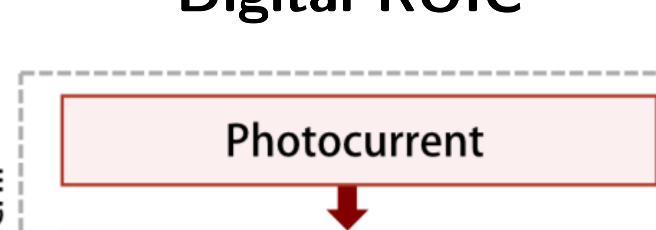
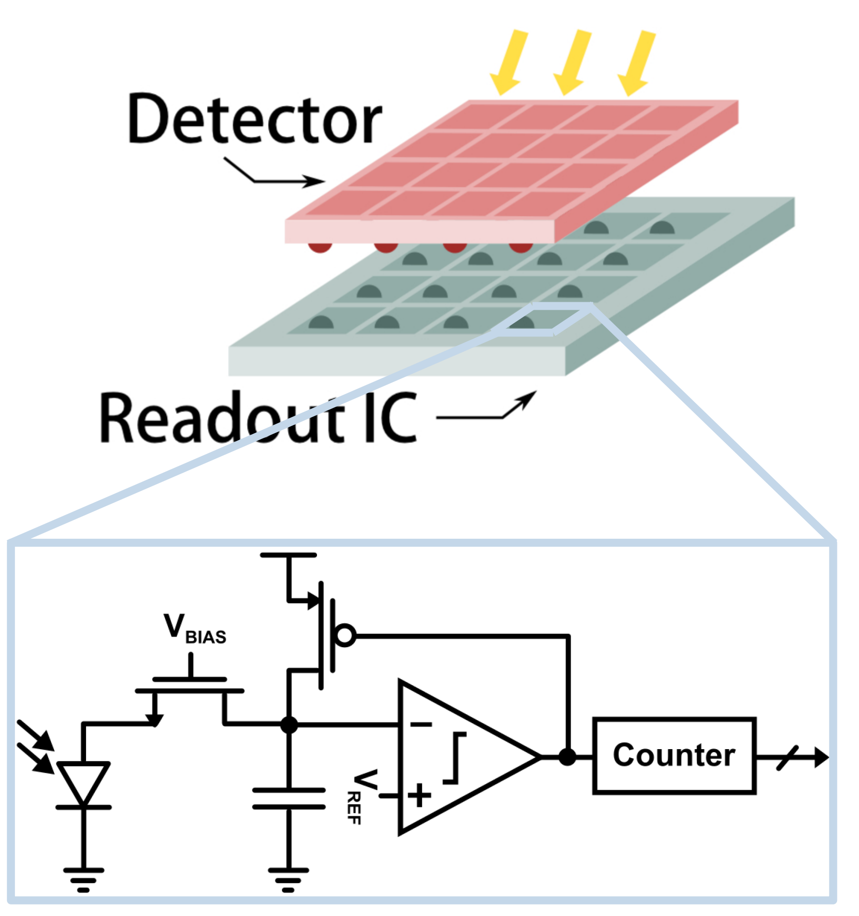


Digital ROIC



Higher integration levels allow for more compact sensors [1]

Readout Integrated Circuits (ROICs)



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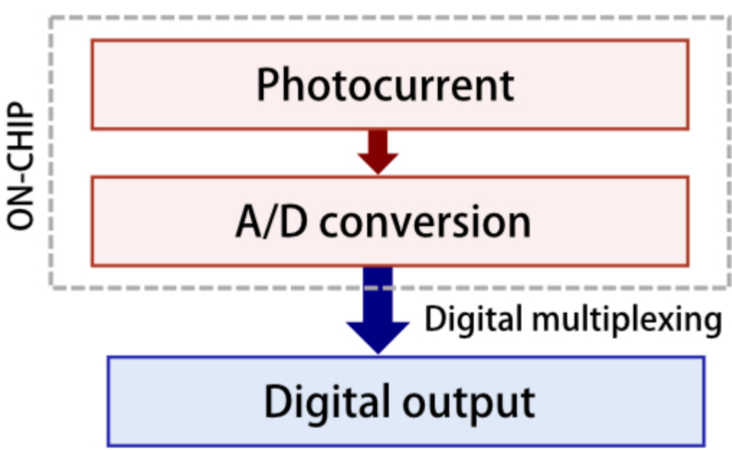

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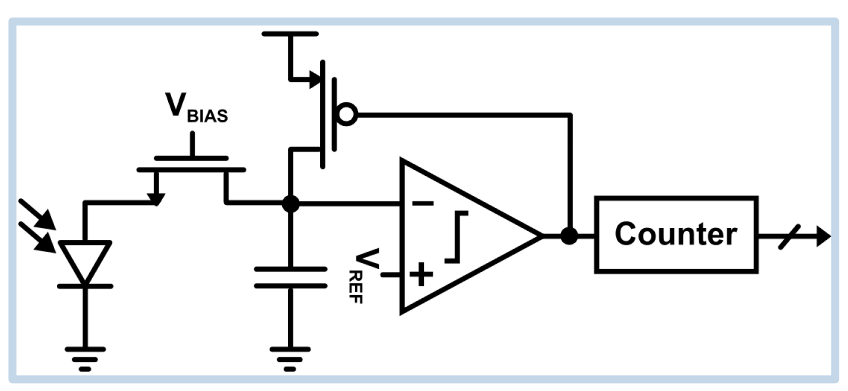
Readout Integrated Circuits (ROICs)

Maximum detectable signal set by counter size, t_{int}/t_{LSB}

Improves with technology node



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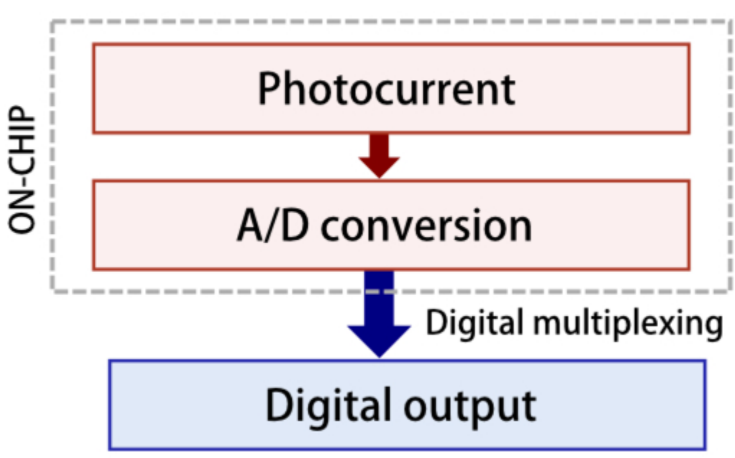
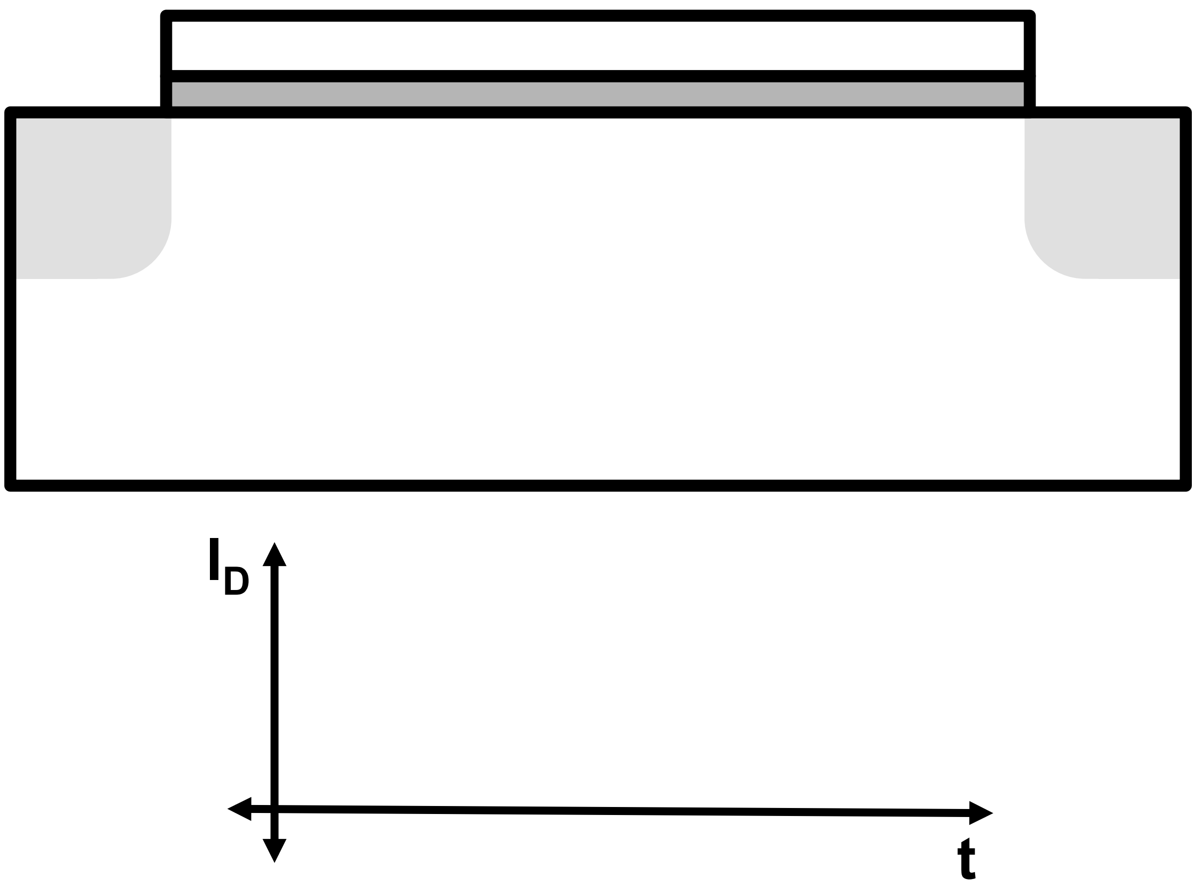


Higher integration levels allow for more compact sensors [1]

Technology Concerns in Imagers: Random Telegraph Noise (RTN)



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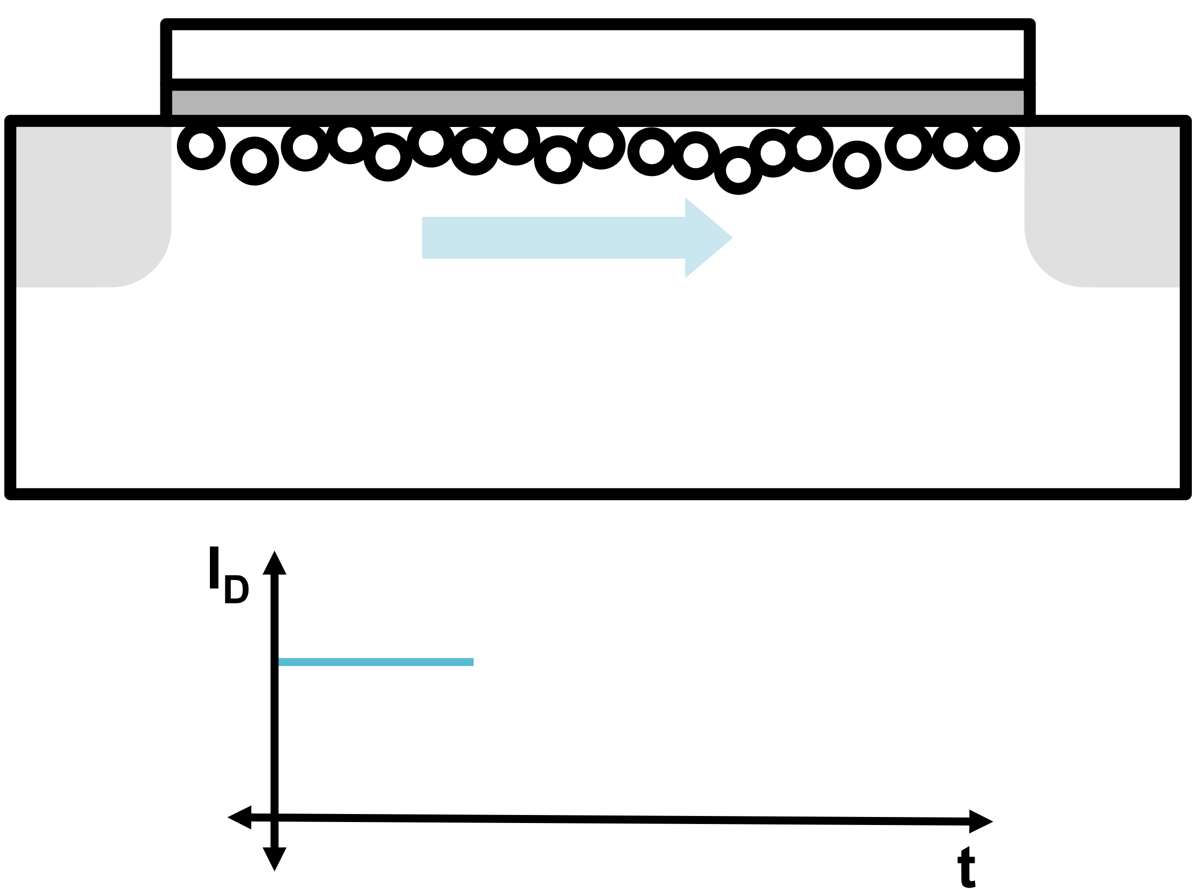

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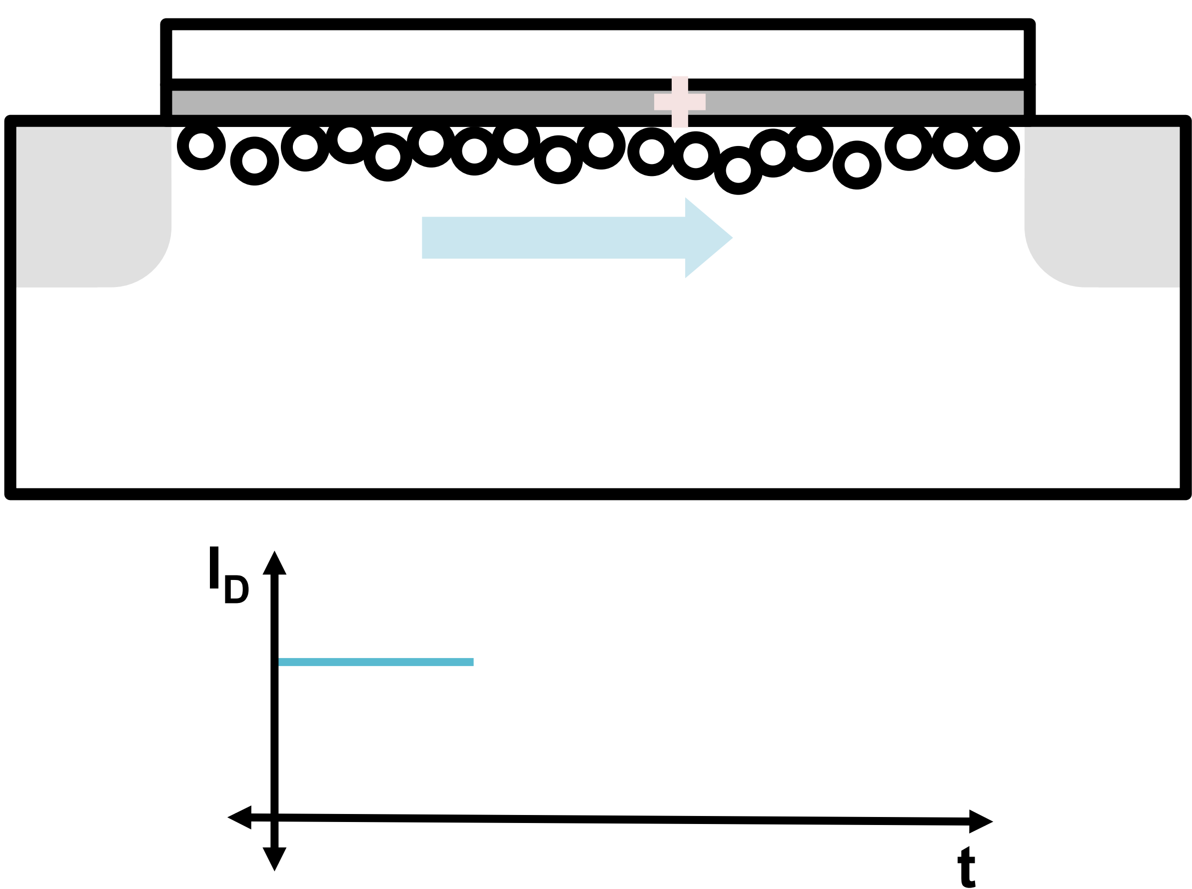

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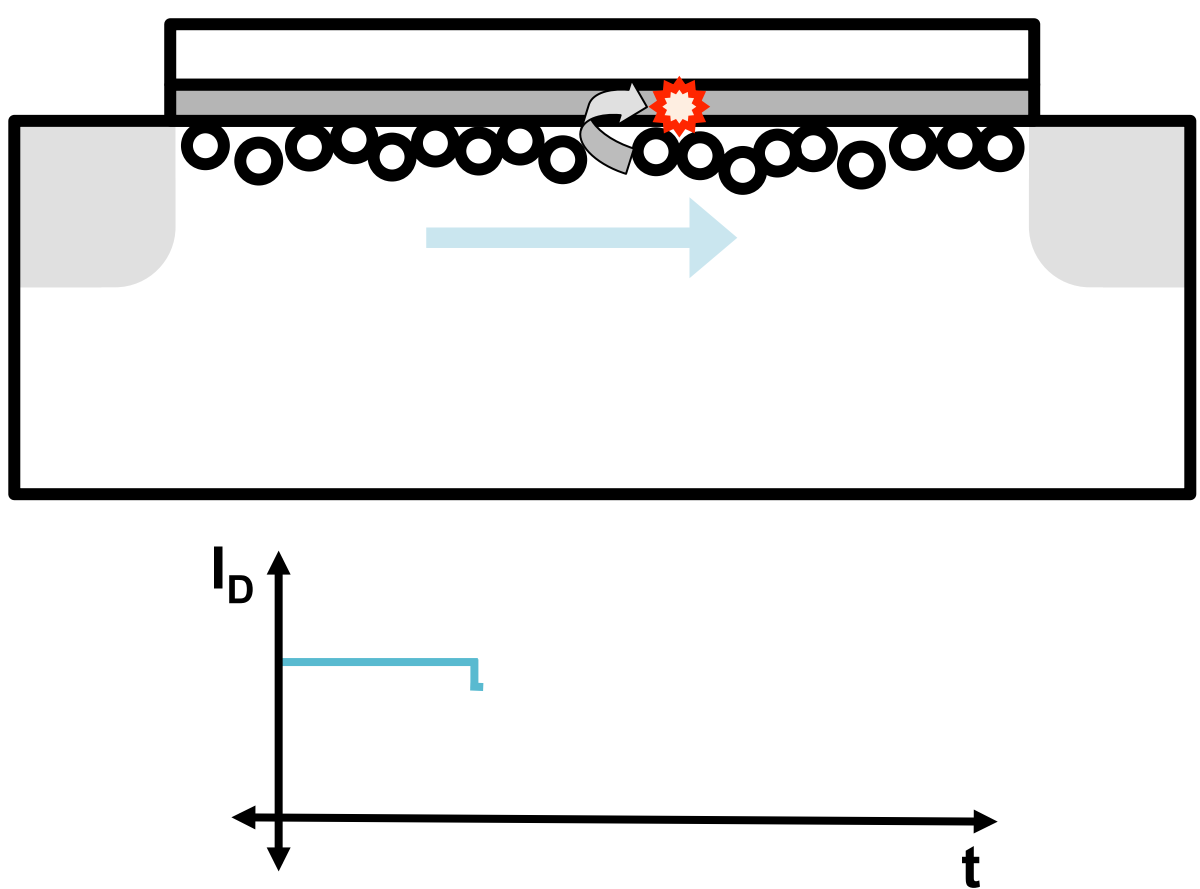

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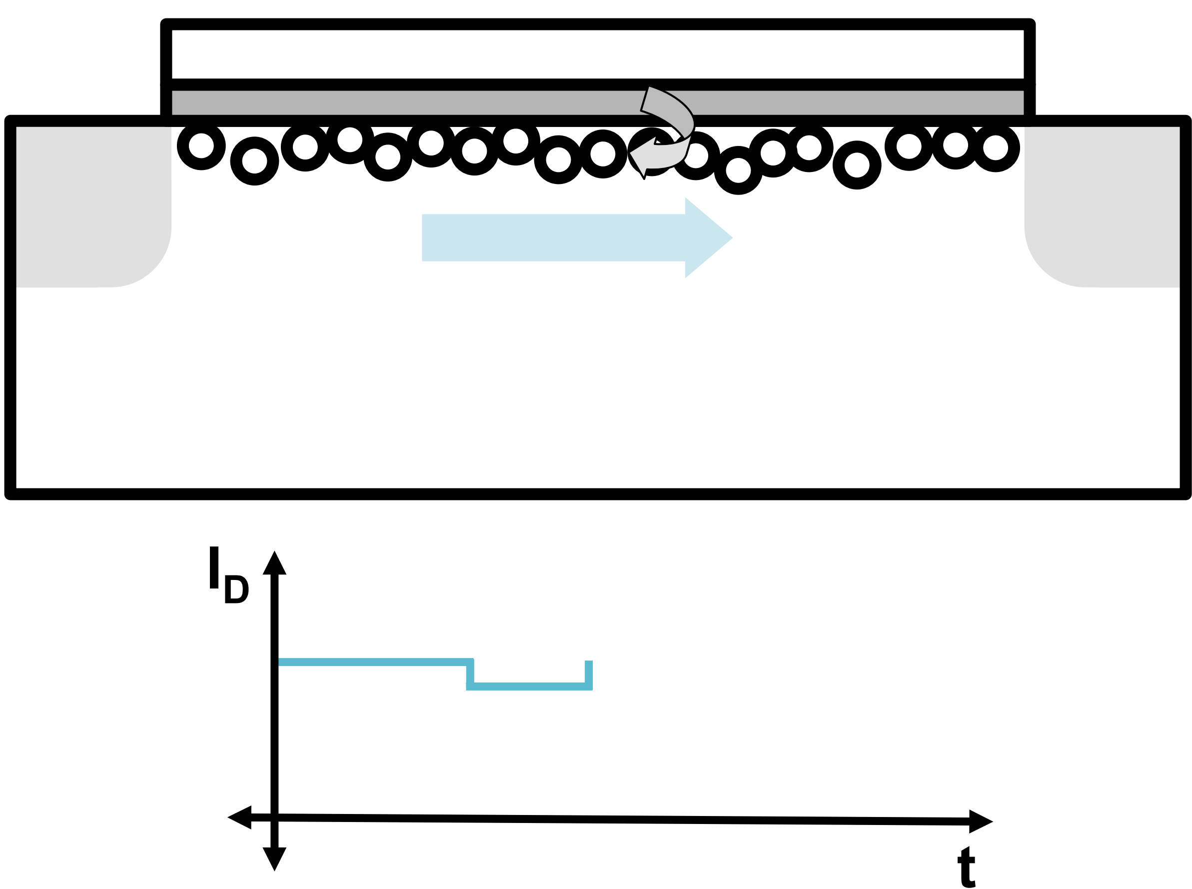

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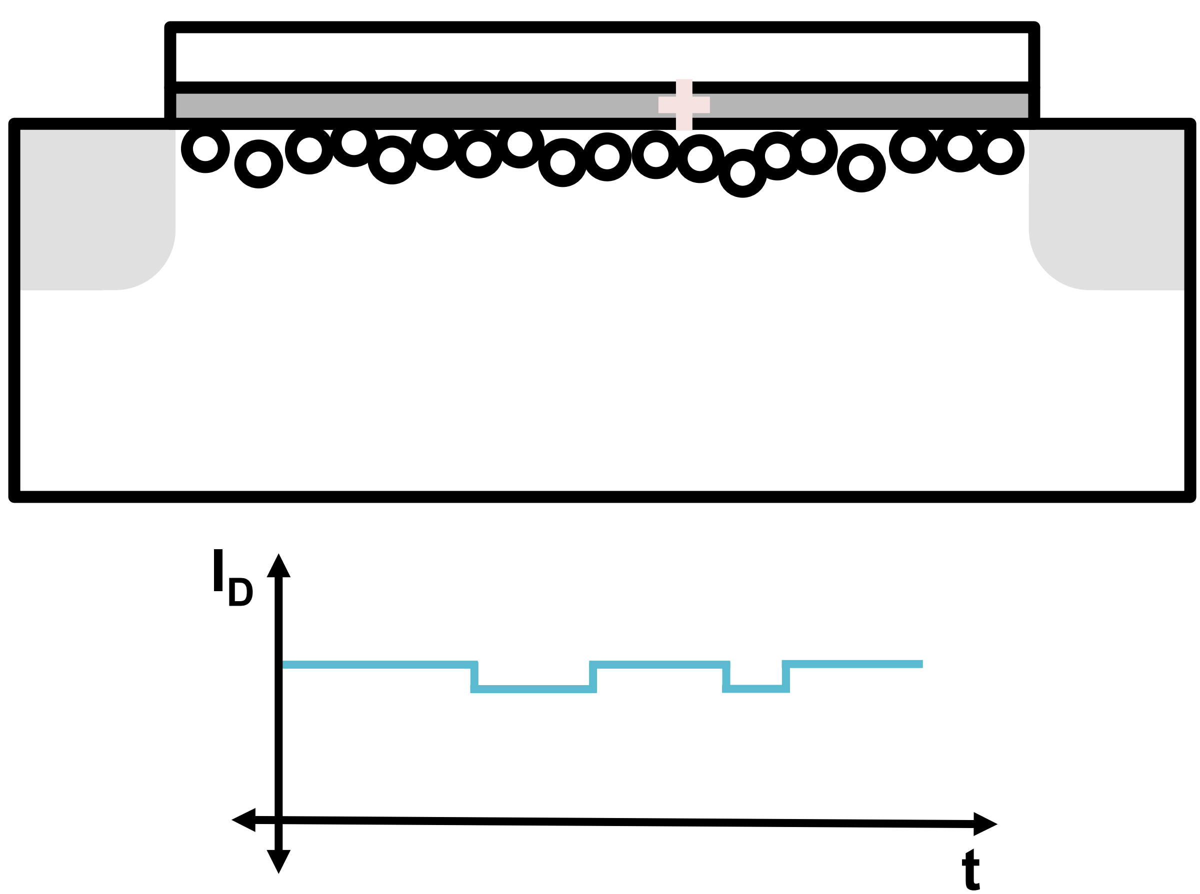

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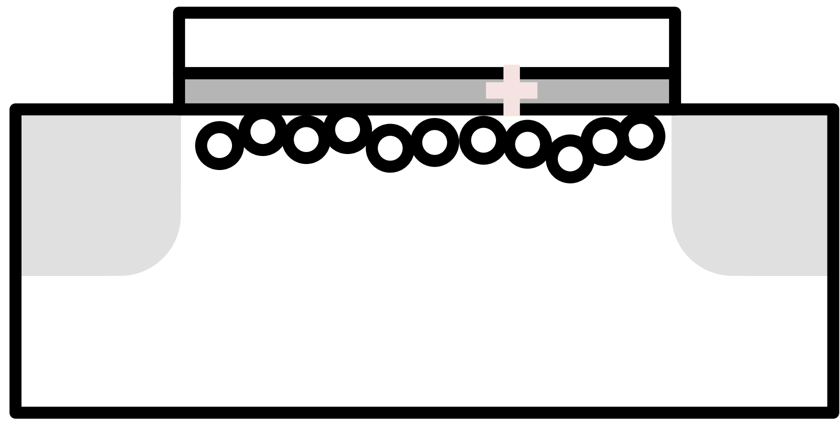

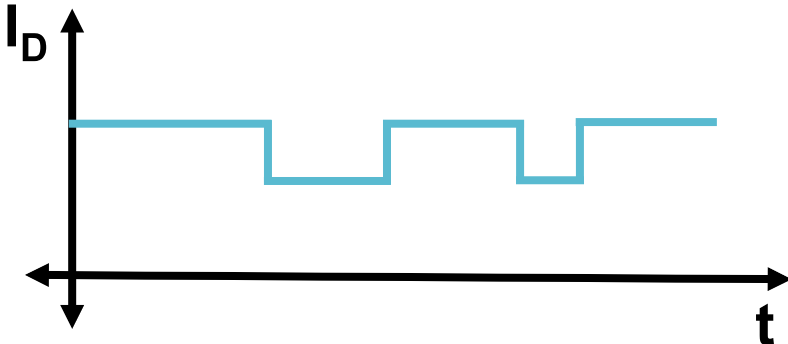

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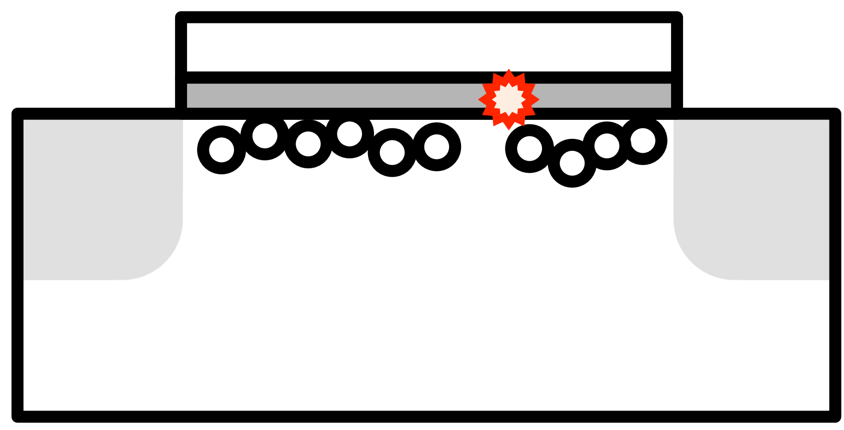
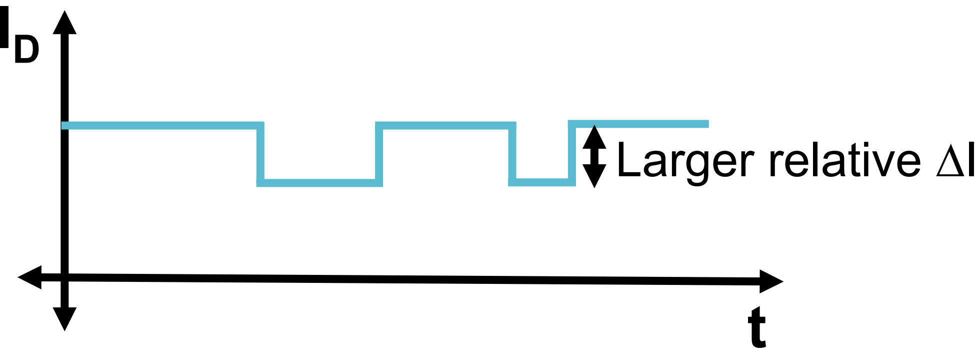
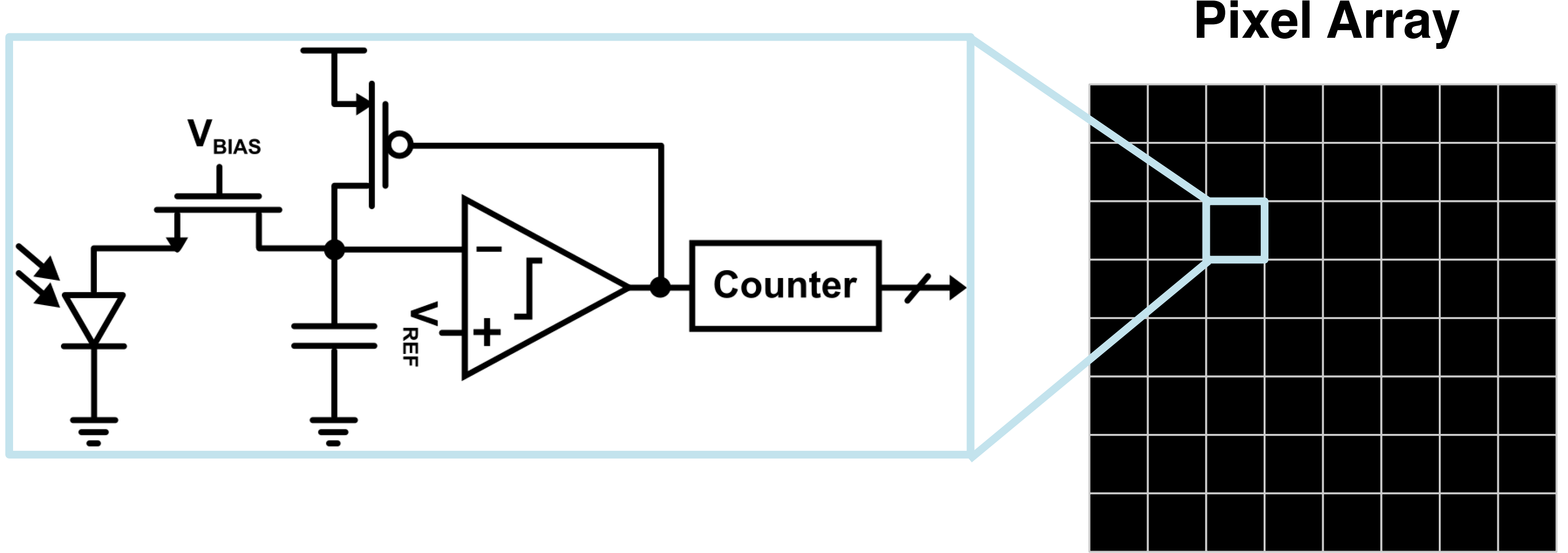




Random Telegraph Noise (RTN) Impact



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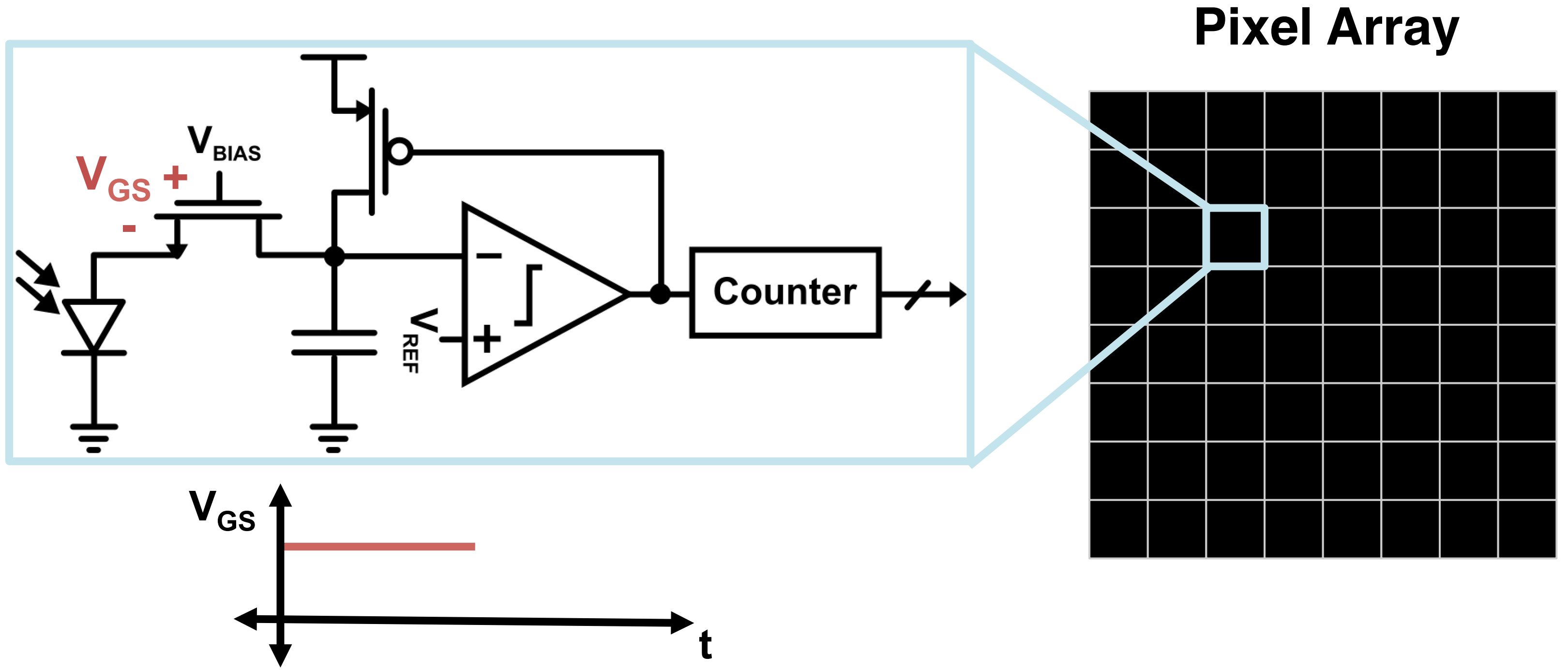
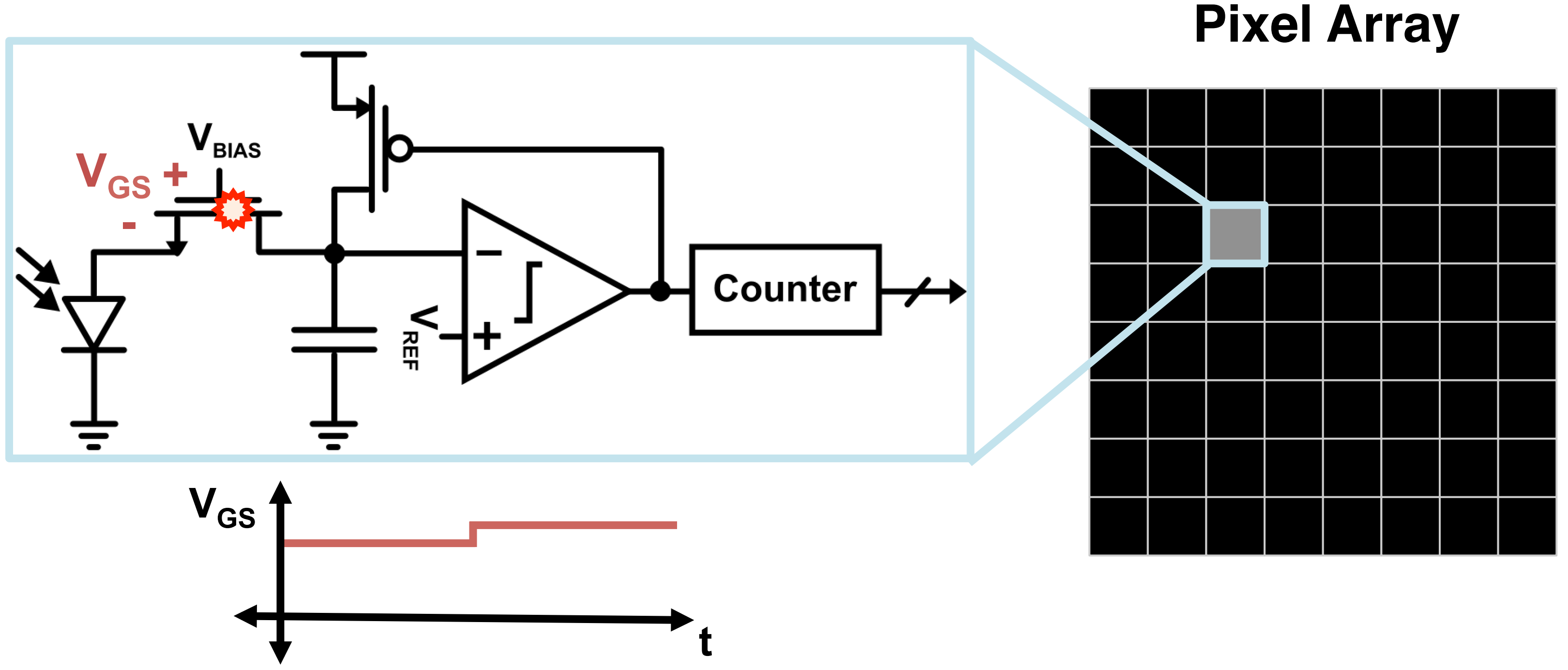


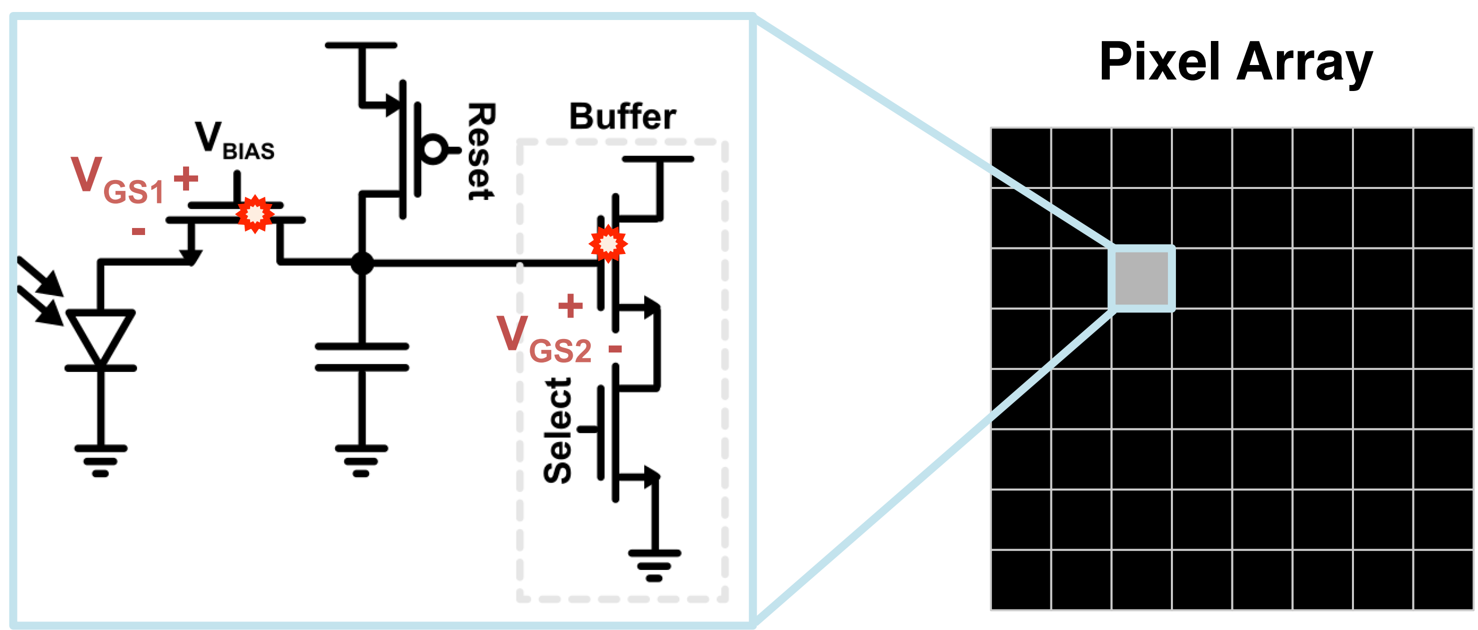
- Photodetector bias set by V_{GS} of direct injection transistor

Random Telegraph Noise (RTN) Impact



- Photodetector bias set by V_{GS} of direct injection transistor
- RTN will cause threshold voltage shifts that change V_{GS}, resulting in "blinking" pixels

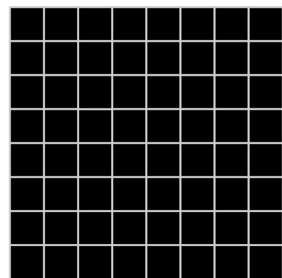
Random Telegraph Noise (RTN) Impact

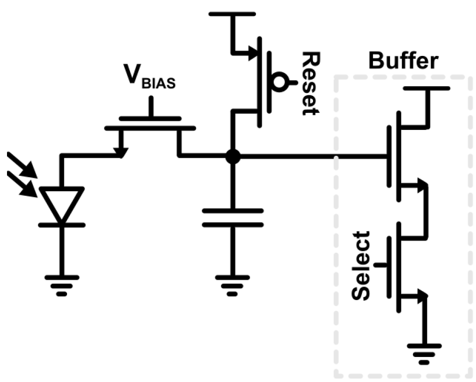


- Photodetector bias set by V_{GS} of direct injection transistor
  - Source follower output set by V_{GS} of buffer device
- RTN will cause threshold voltage shifts that change V_{GS}, resulting in "blinking" pixels

Random Telegraph Noise (RTN) Impact

Imaging Applications [2]

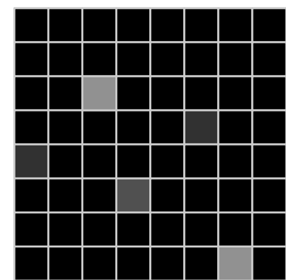


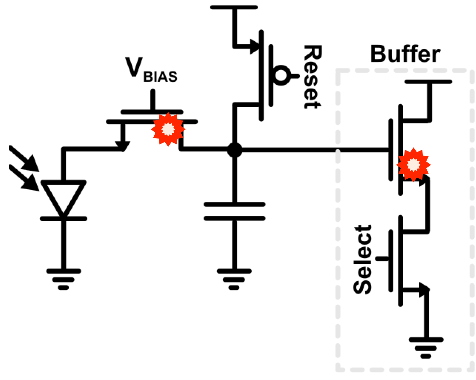


RTN is a growing problem in deeply scaled mixed-signal integrated circuit designs

Random Telegraph Noise (RTN) Impact

Imaging Applications [2]





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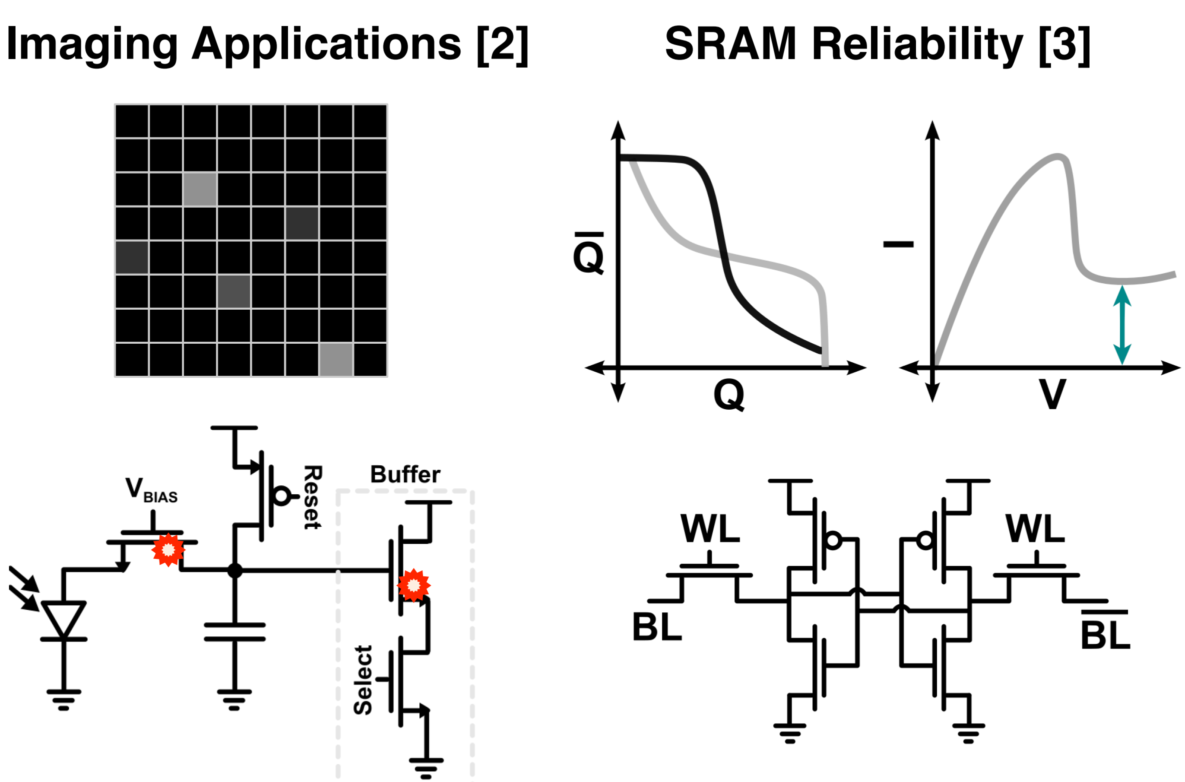

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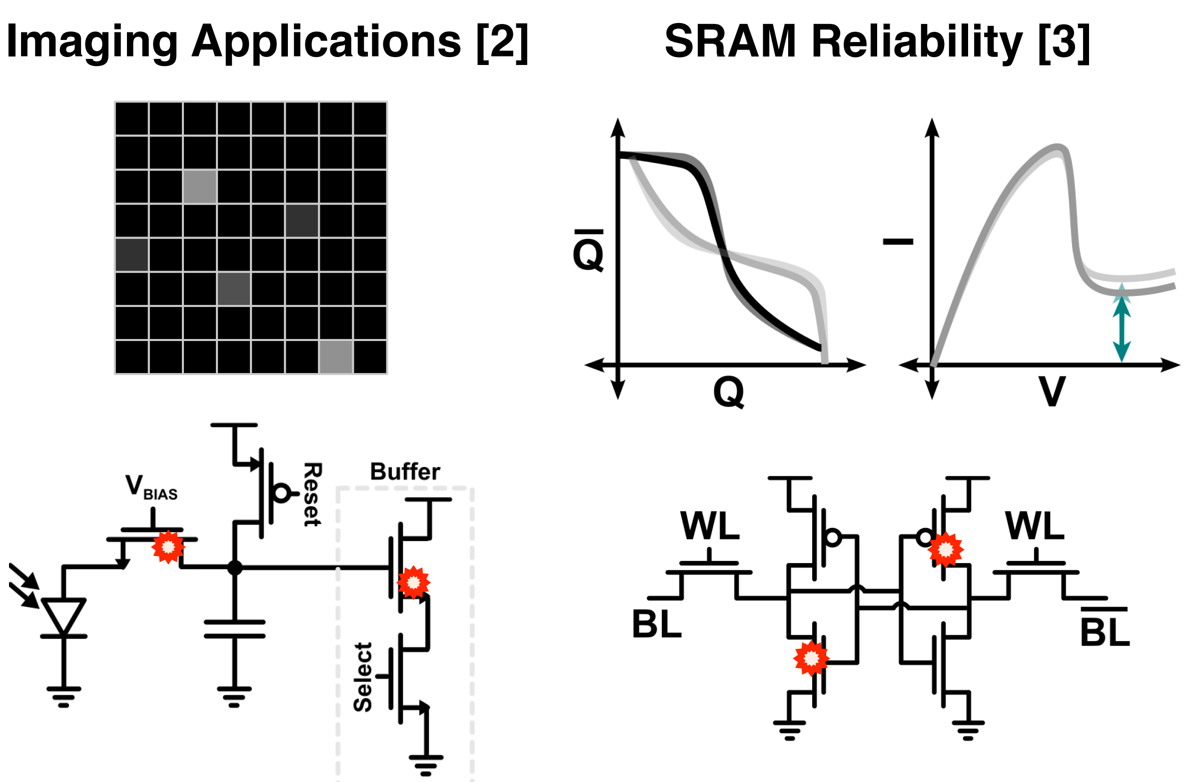

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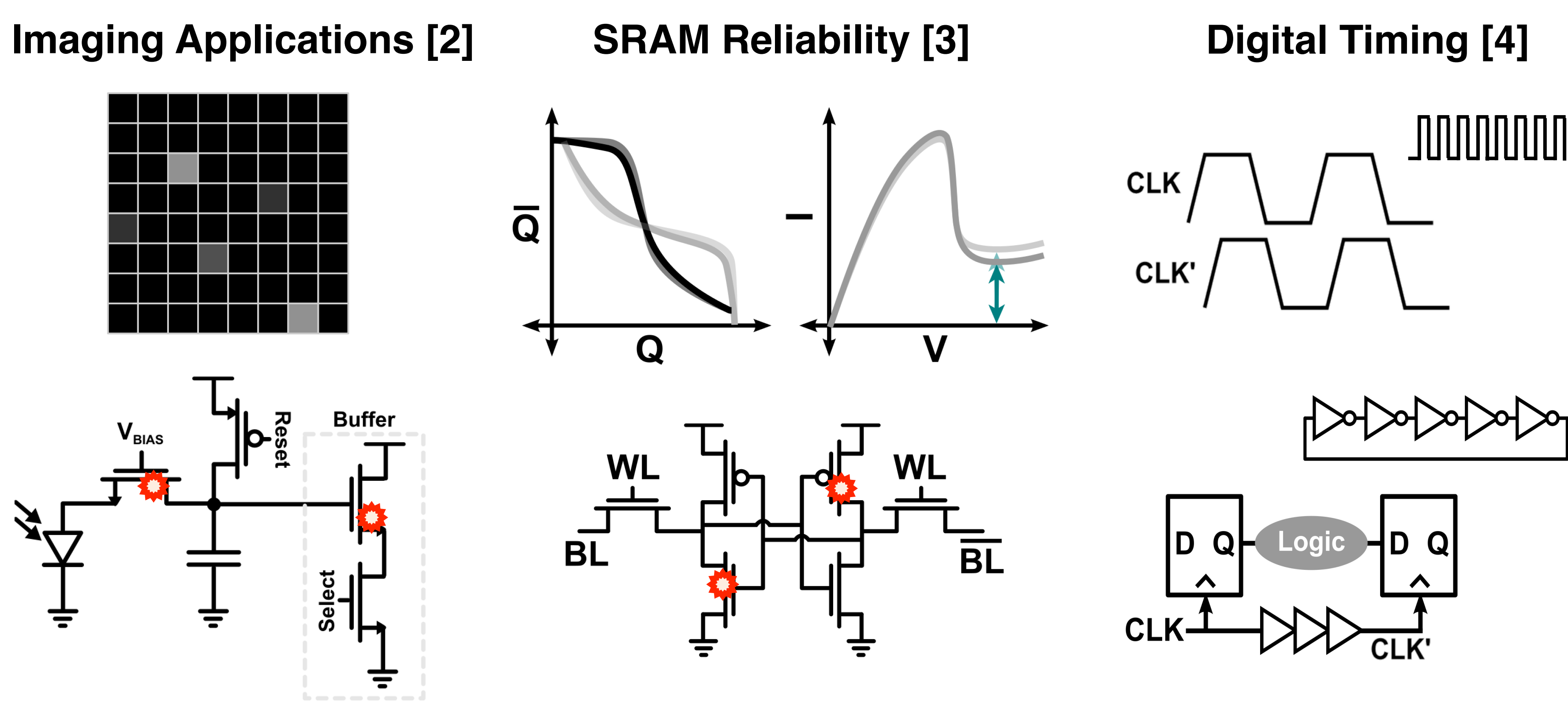

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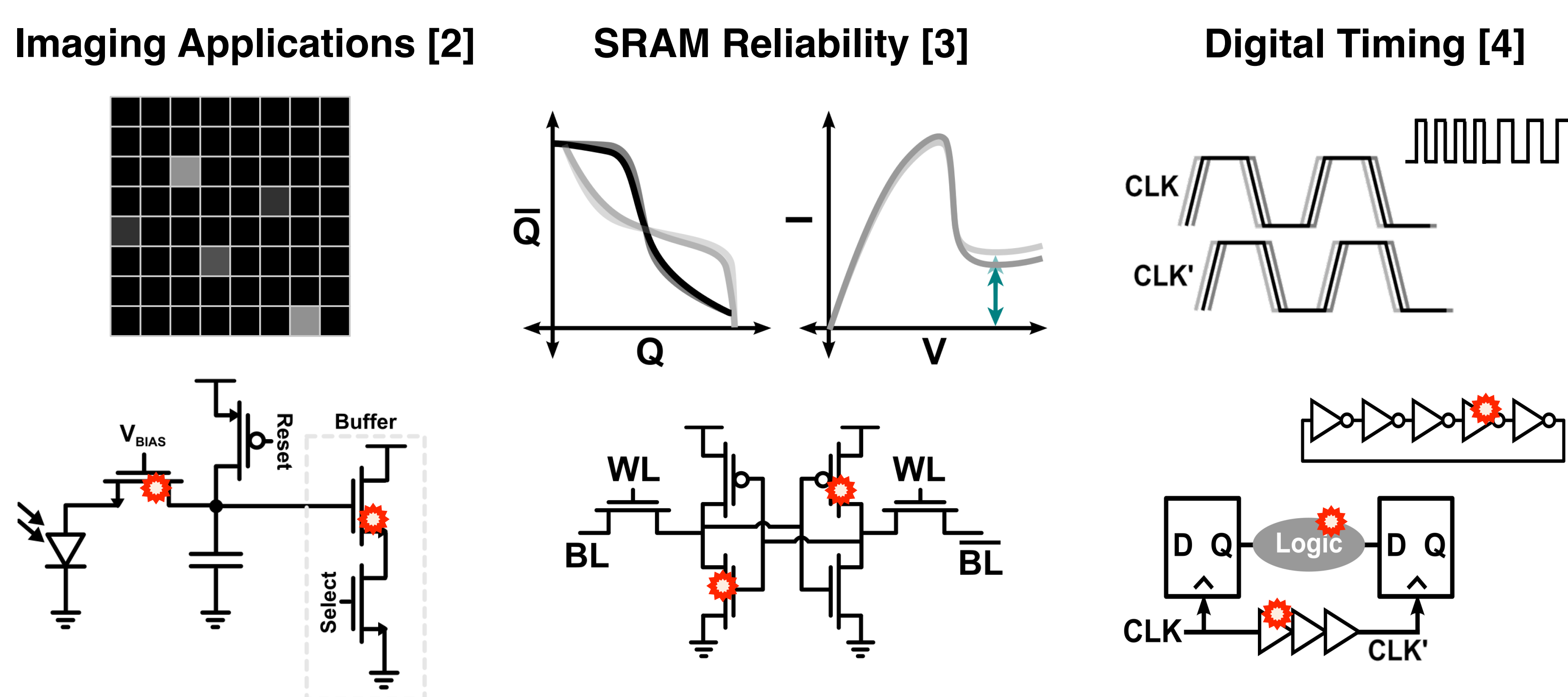

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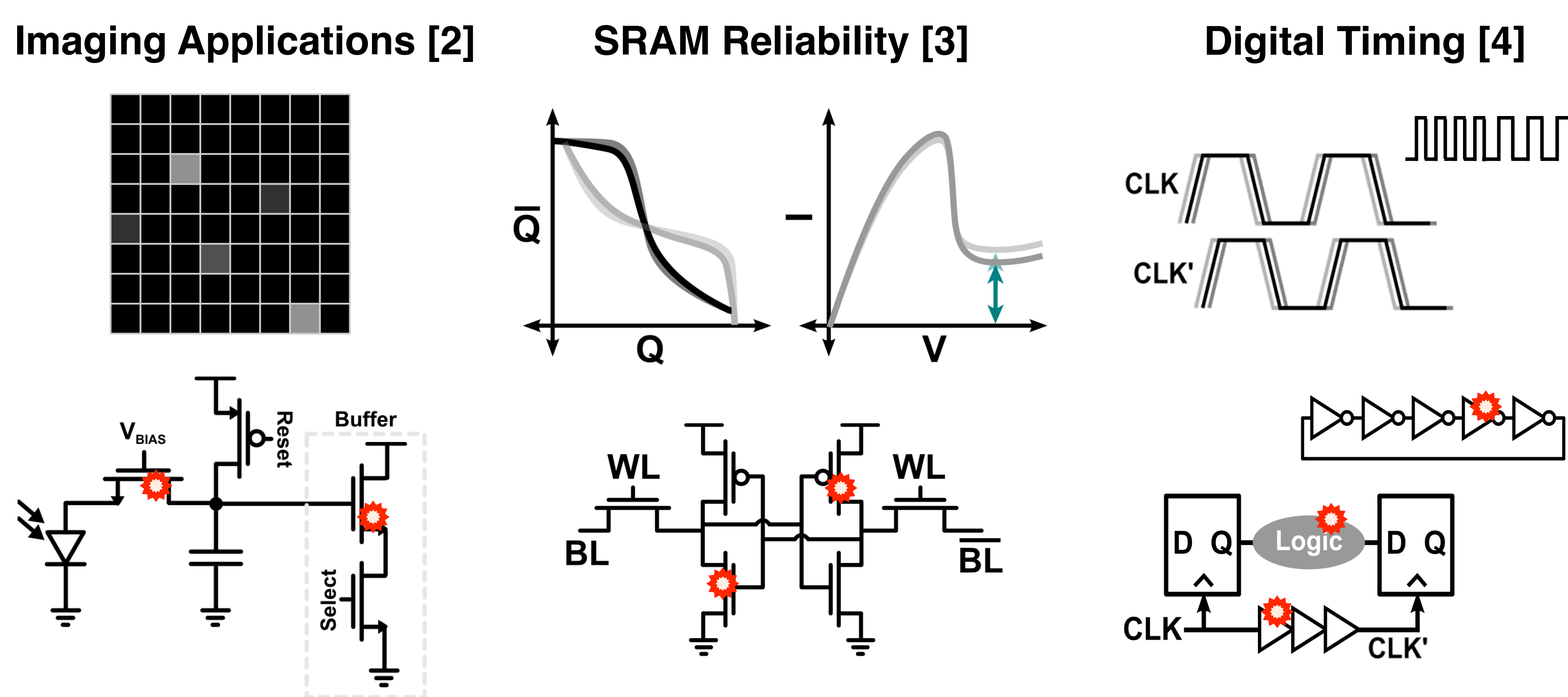
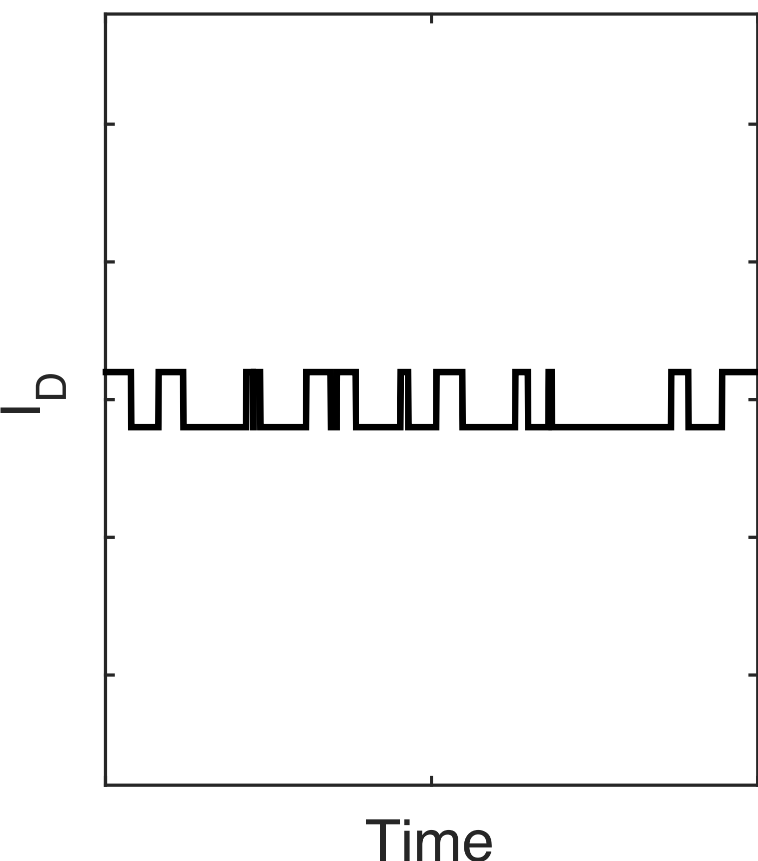


Large-scale RTN characterization is necessary to develop accurate circuit models

RTN Characterization Challenges



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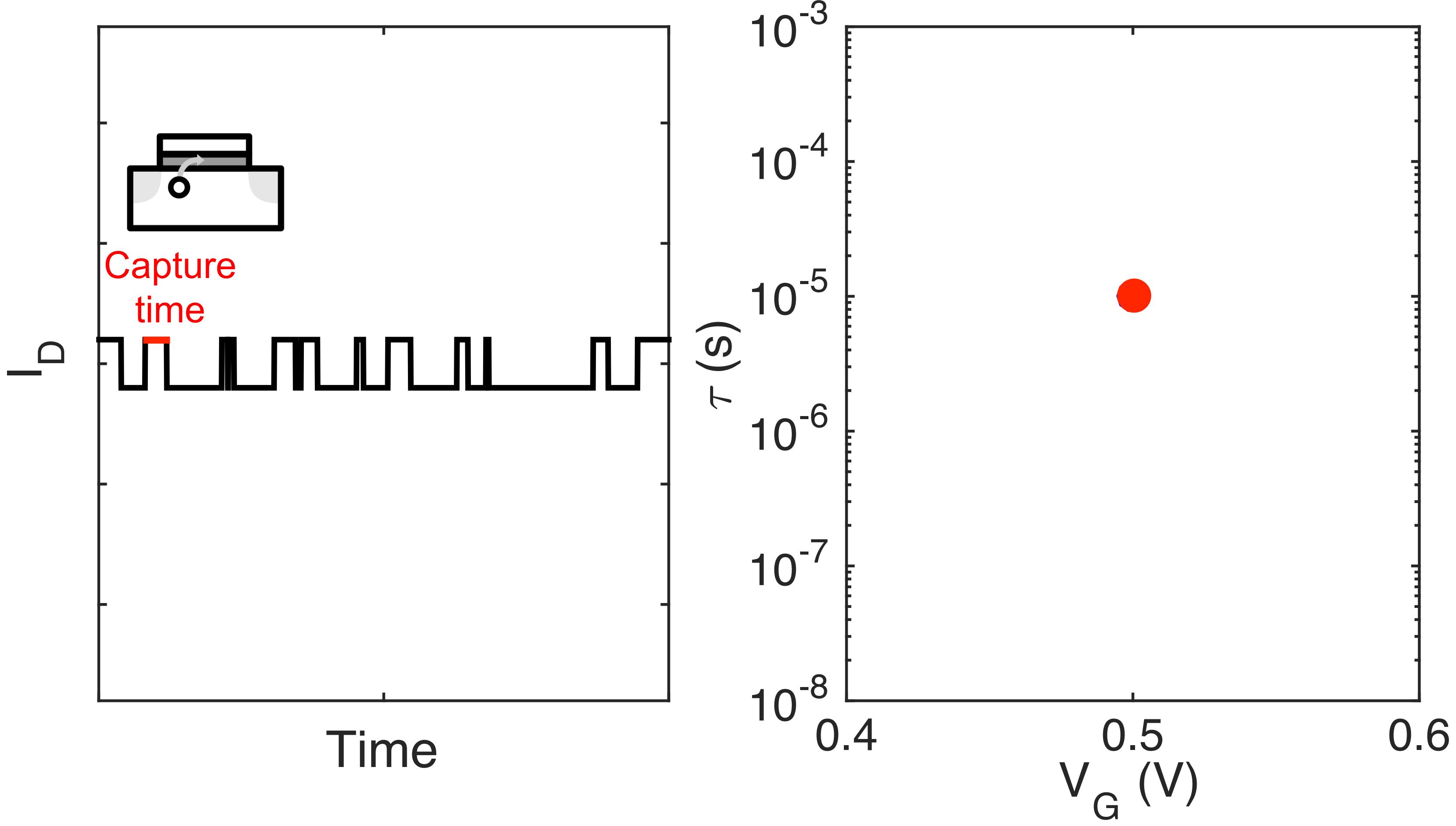

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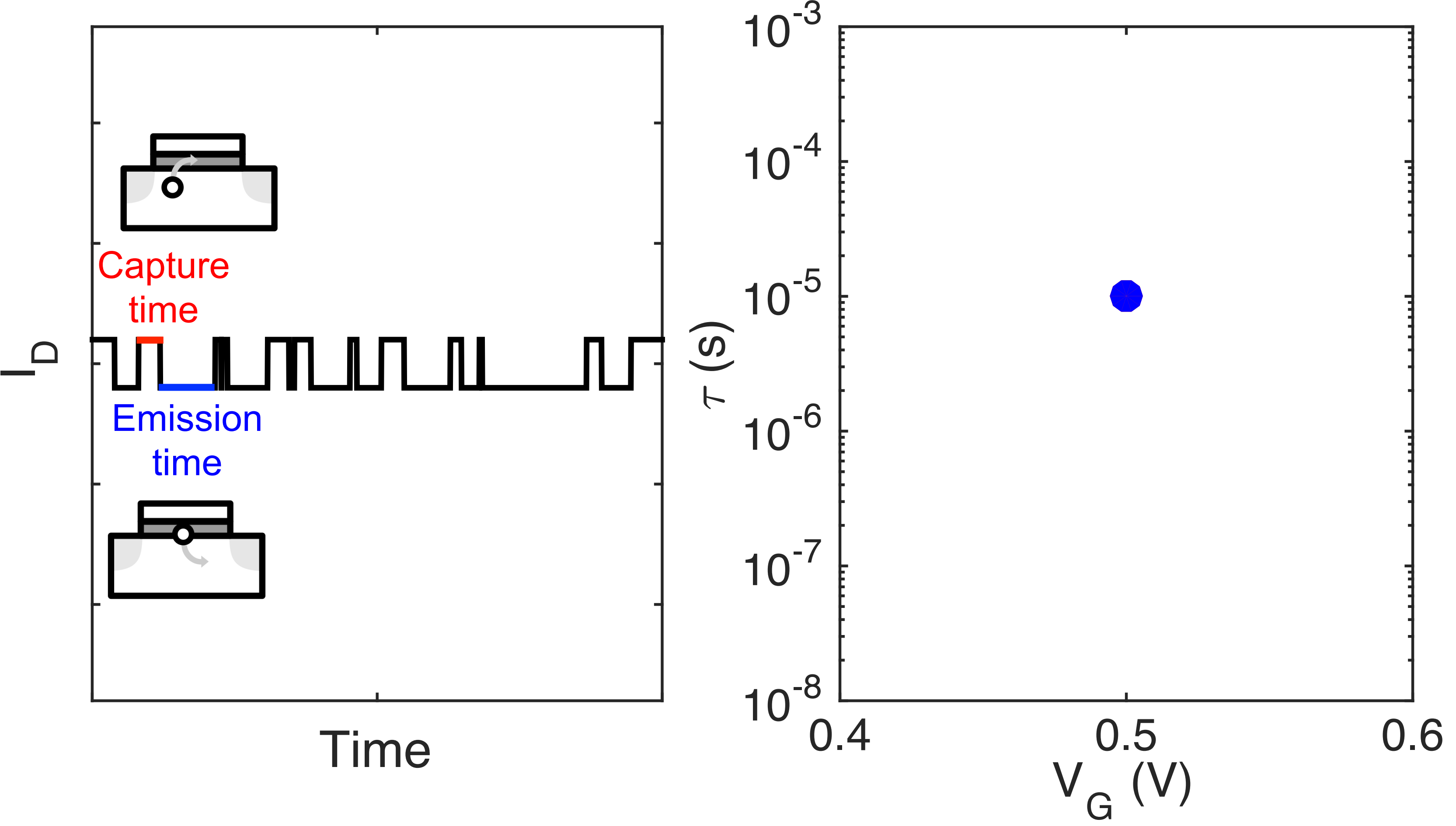

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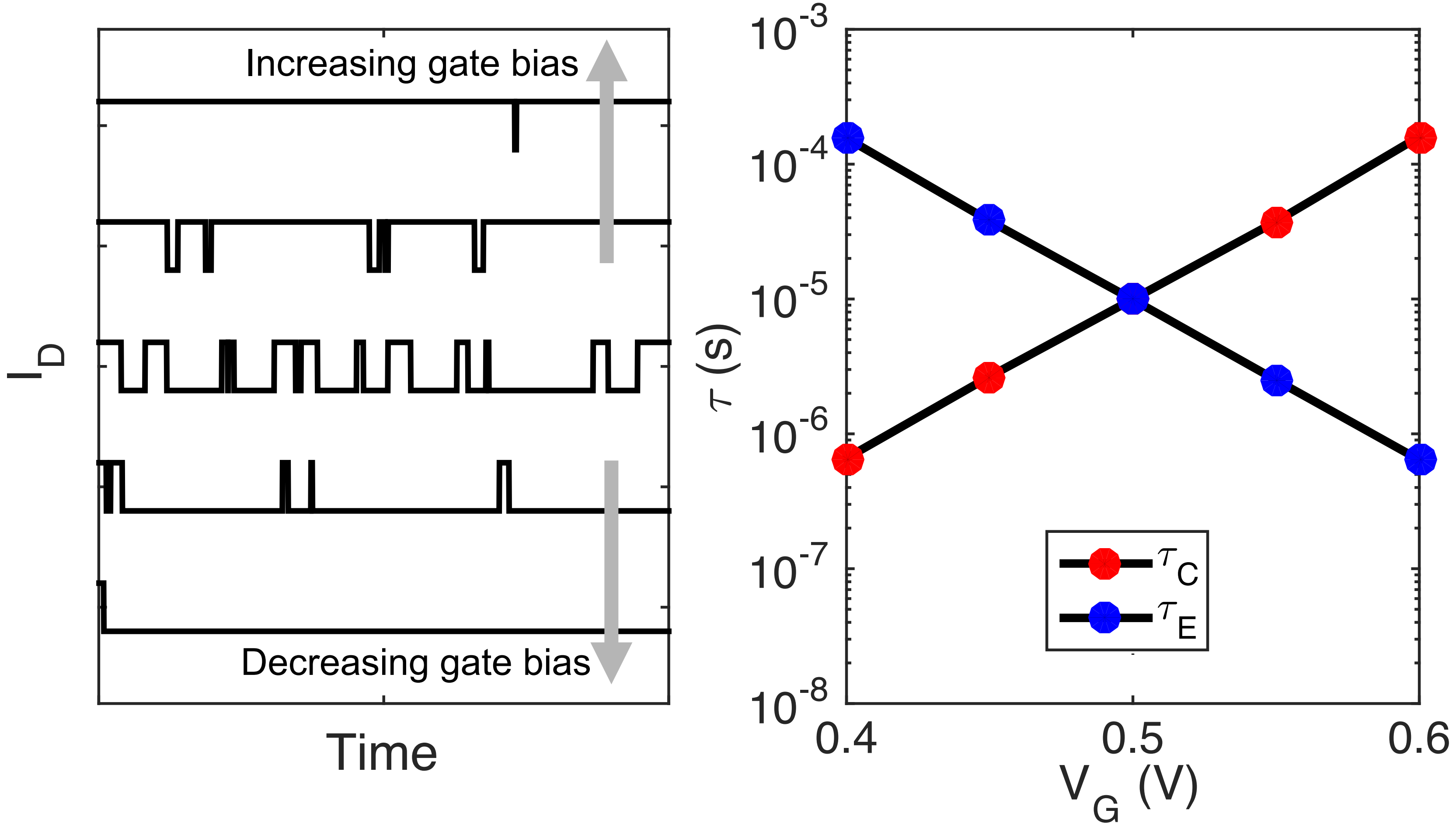

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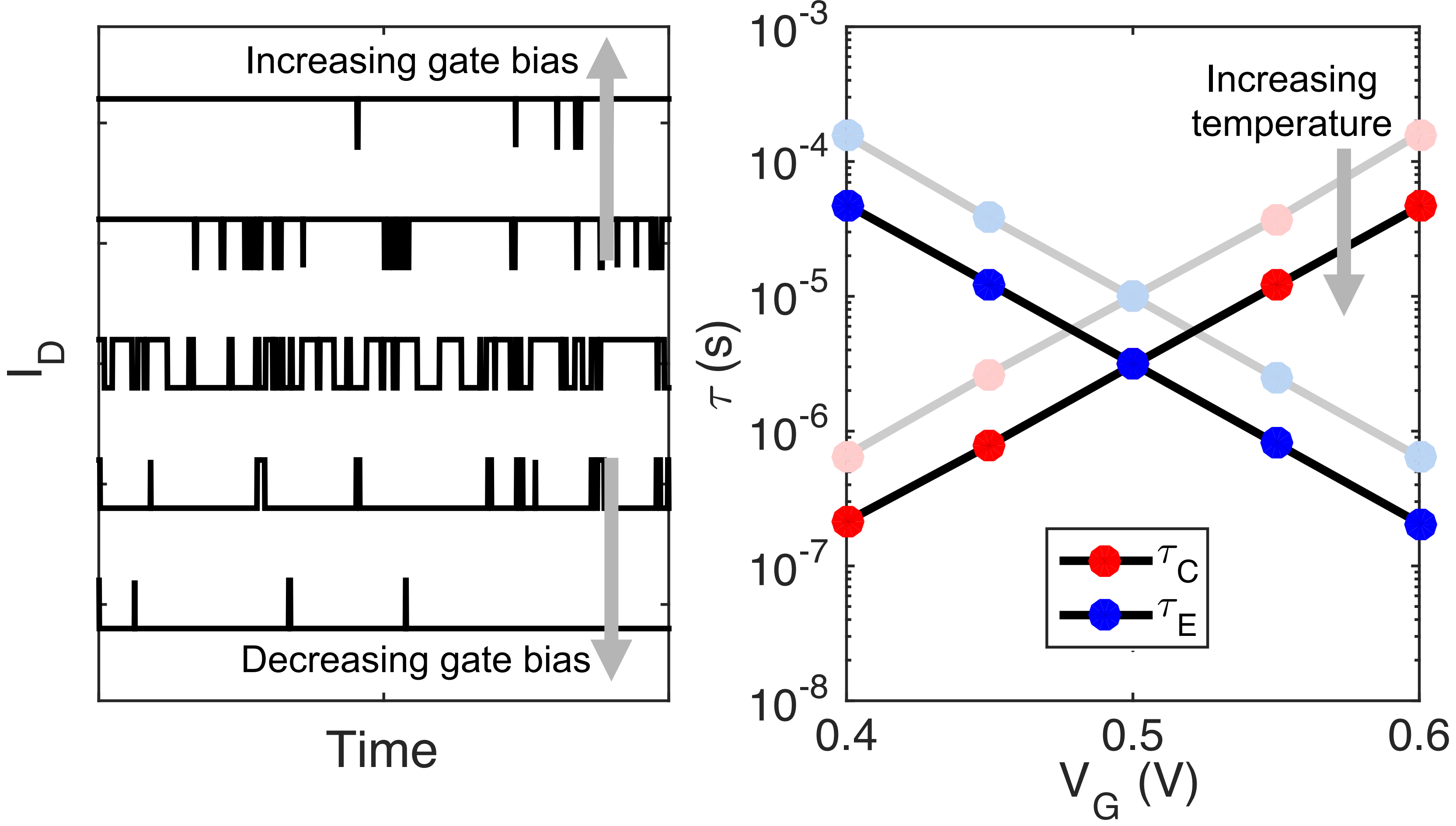

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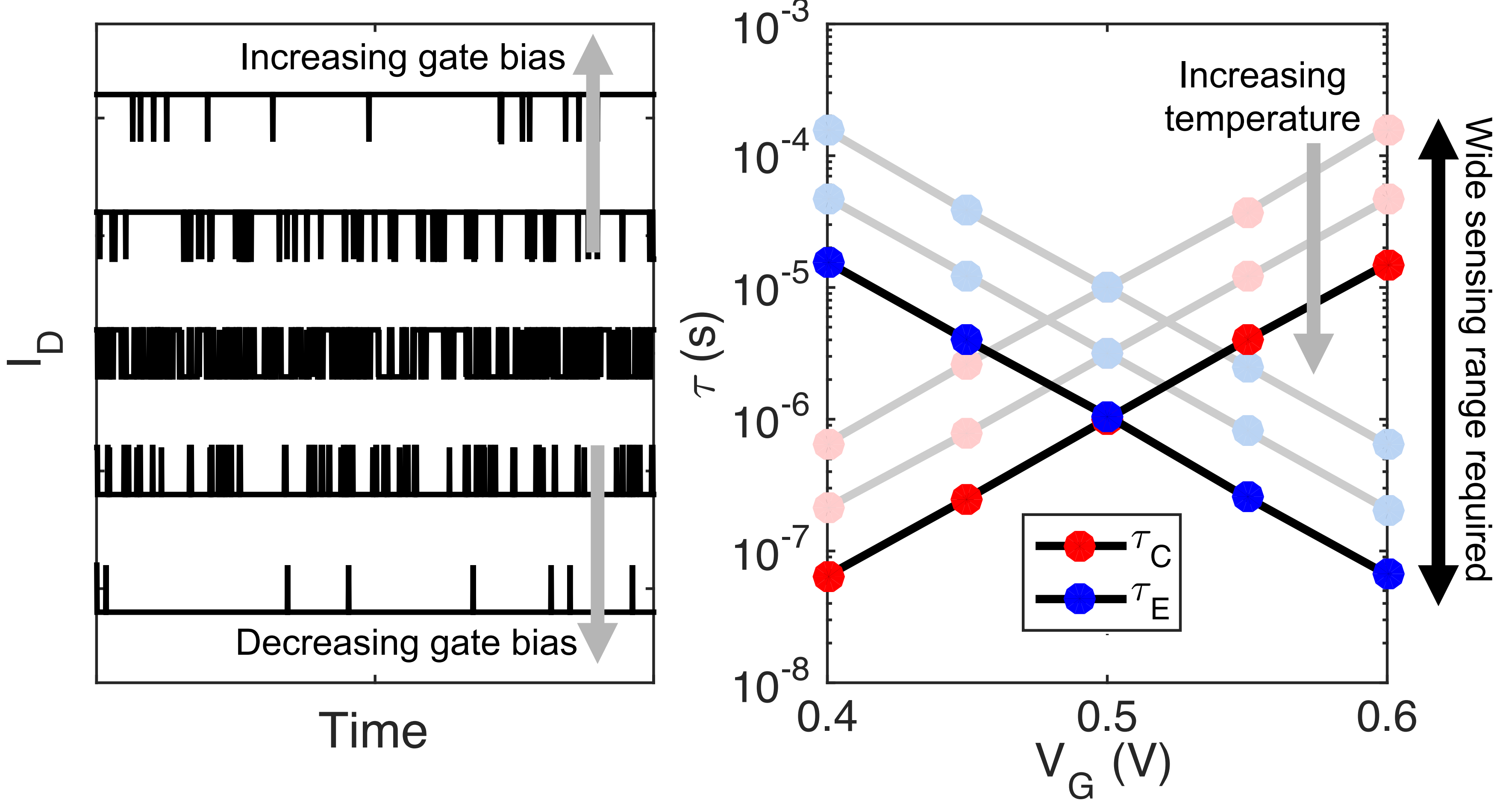

Understanding bias, temperature sensitivity of RTN requires long, fast sampling

Outline

- Background & motivation
- **Prior art comparison**
  - **General methodology comparison**
  - **Similar methods**
  - **This approach**
- Proposed design
- Test chip results
- Conclusions

RTN Characterization Array Comparison

	Concept	Testing time	Needed test equipment	Devices in test array
Standard	CHIP, SMU	$\frac{N \cdot k}{f_{samp}}$ Long	High-performance source/measure unit ✕✕	-

N = # of test devices; k = # data points; f_{samp} = sample rate

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On-chip DAC/ADC	CHIP, ADC	$\frac{N \cdot k}{f_{samp}}$ **Long**	**Digital interface board** ✓	45 nm CMOS ~4000 N/PFETs, 6 W/L ratios

Realov & Shepard, *TED* 2013.

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Analog array	CHIP, SHIFT REG, (Fast) ADC	$\frac{k}{f_{samp}}$ Short	Fast off-chip ADC + interface board ✗	0.18 µm / 0.22 µm CMOS 10^6 / 10^5 NFETs, 14 / 1 W/L ratio(s)	Abe et al., *VLSI Tech.* 2007 / Yonezawa et al., *IRPS* 2013.

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ADC array	CHIP, ADC	$\frac{k}{f_{samp}}$ Short	Digital interface board ✓	**28 nm** / 14 nm CMOS **~10^5** / 10^7 N/PFETs **2** / 1 W/L ratio(s) **3** / 1 V_{TH}	**This work** / Giles et al., *VLSI Tech.* 2015.

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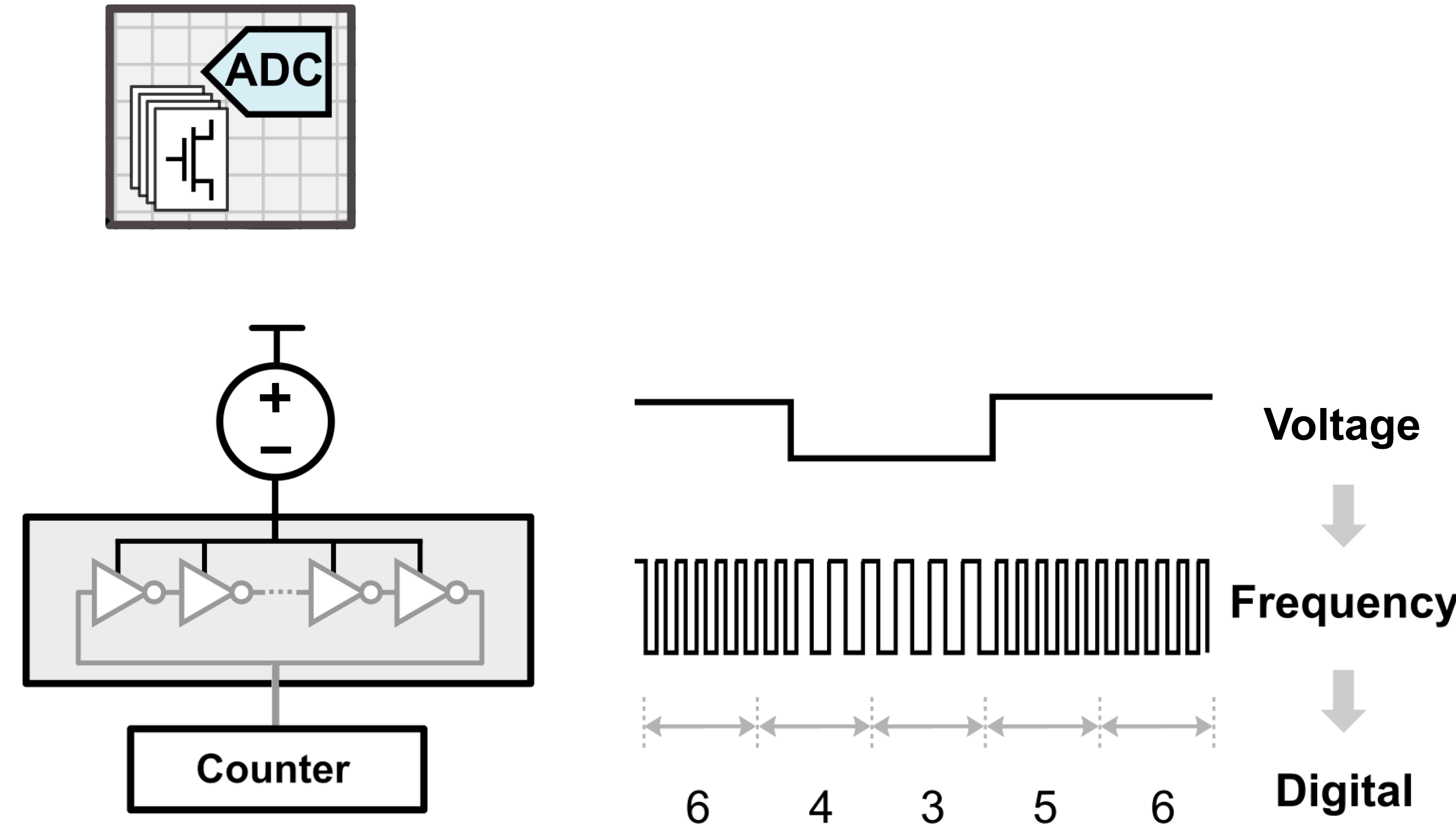
On-Chip ADC Implementation: Prior Work



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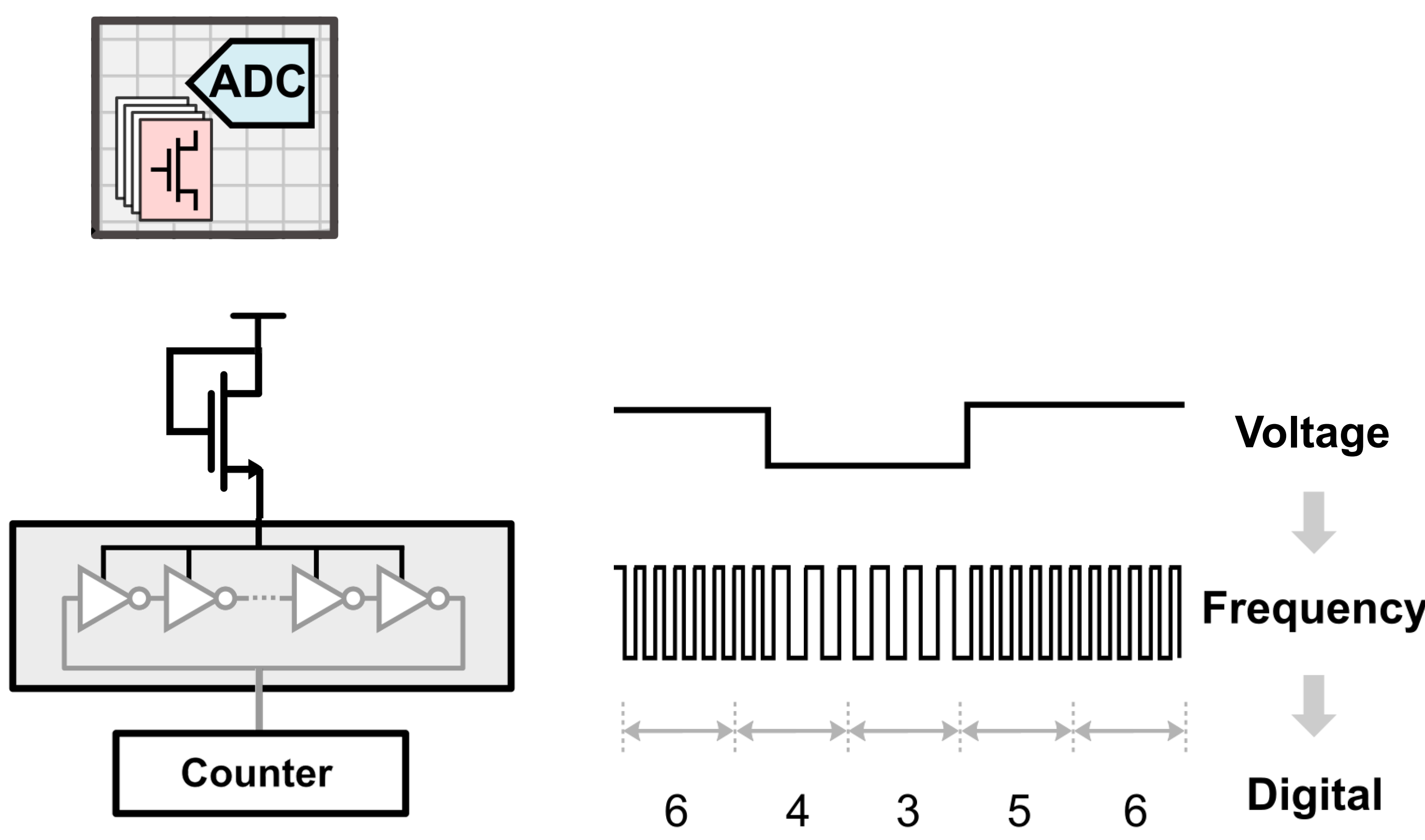

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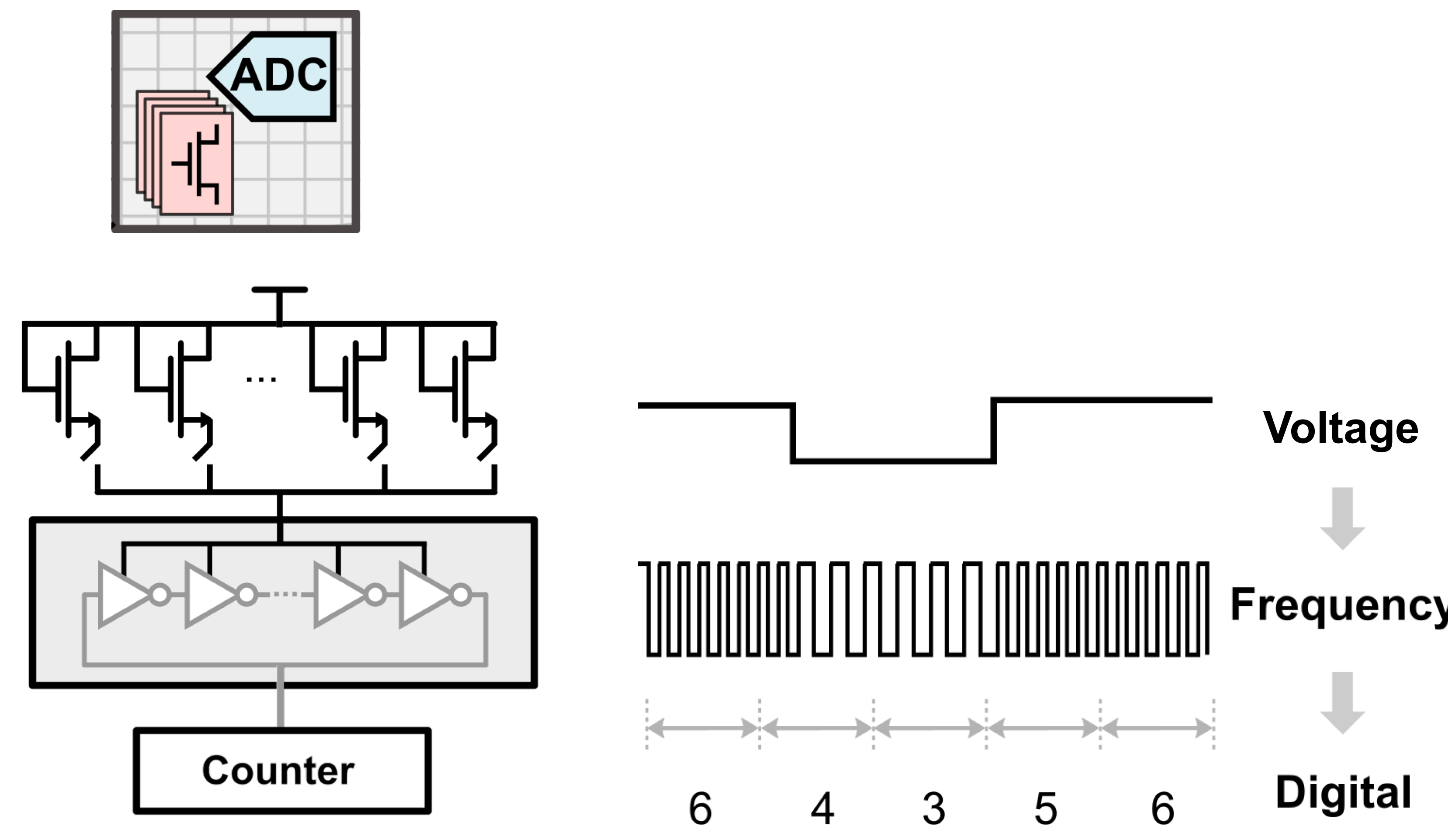

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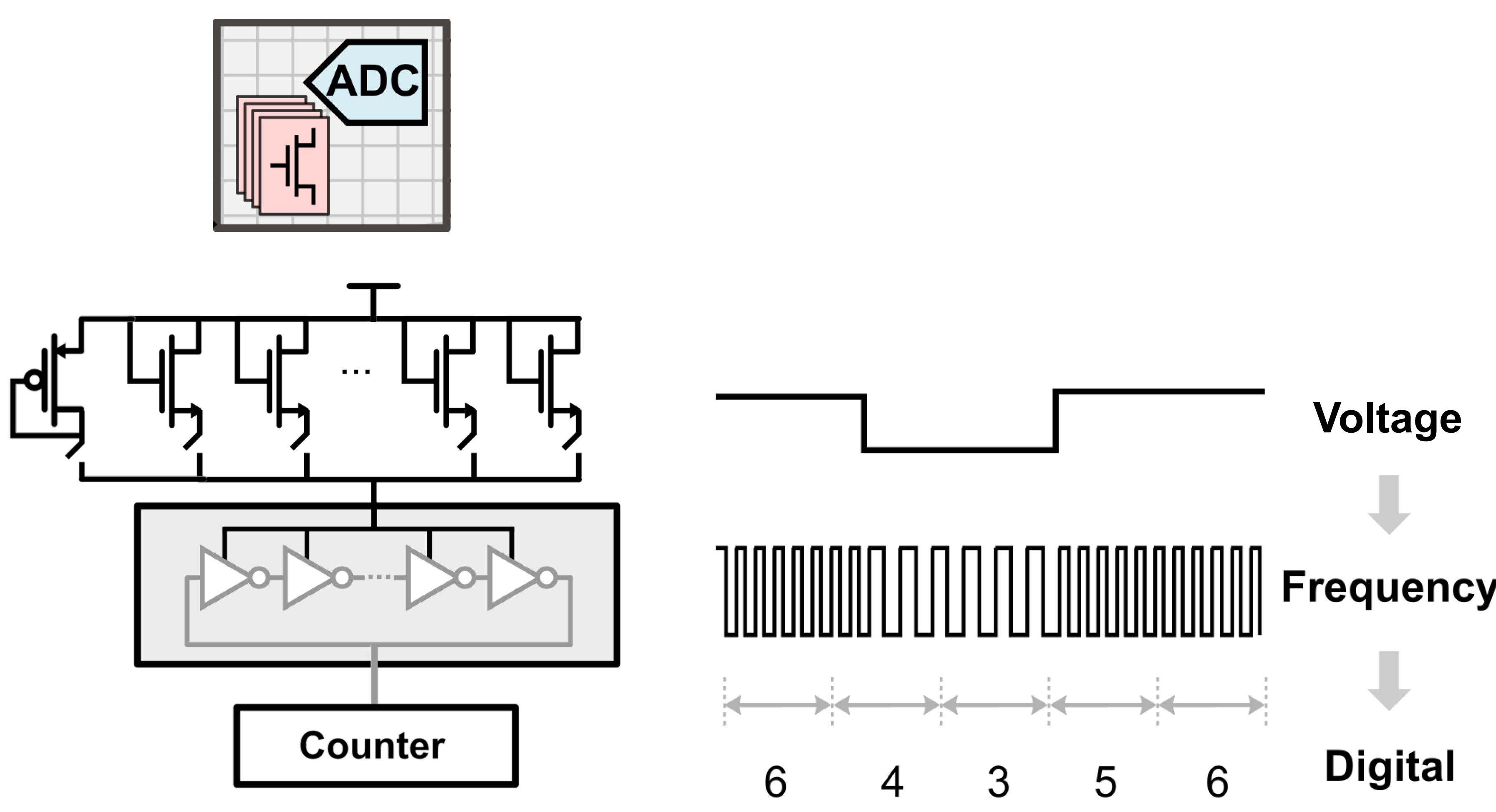

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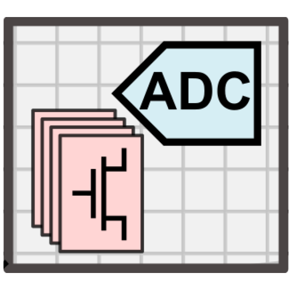
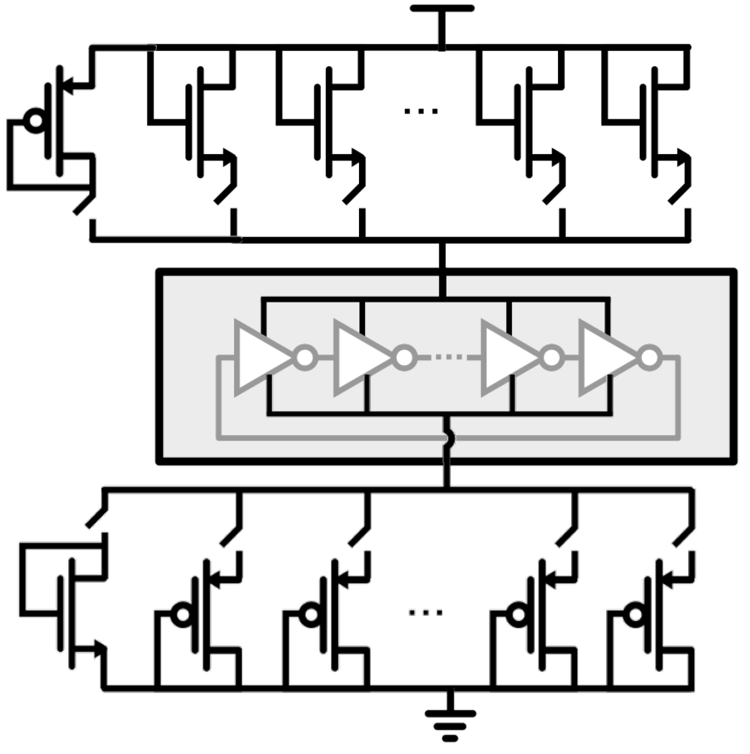
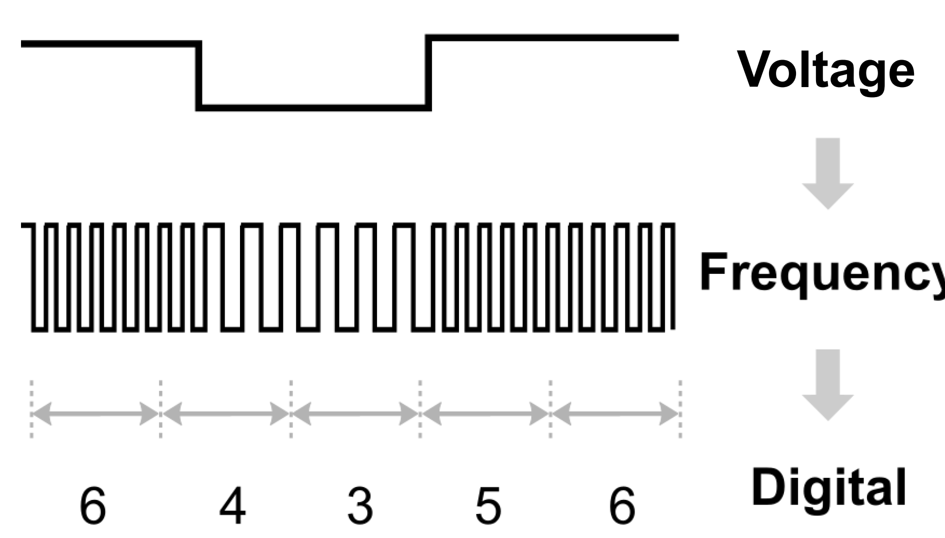


- No current measurements
- Limited bias sensitivity testing





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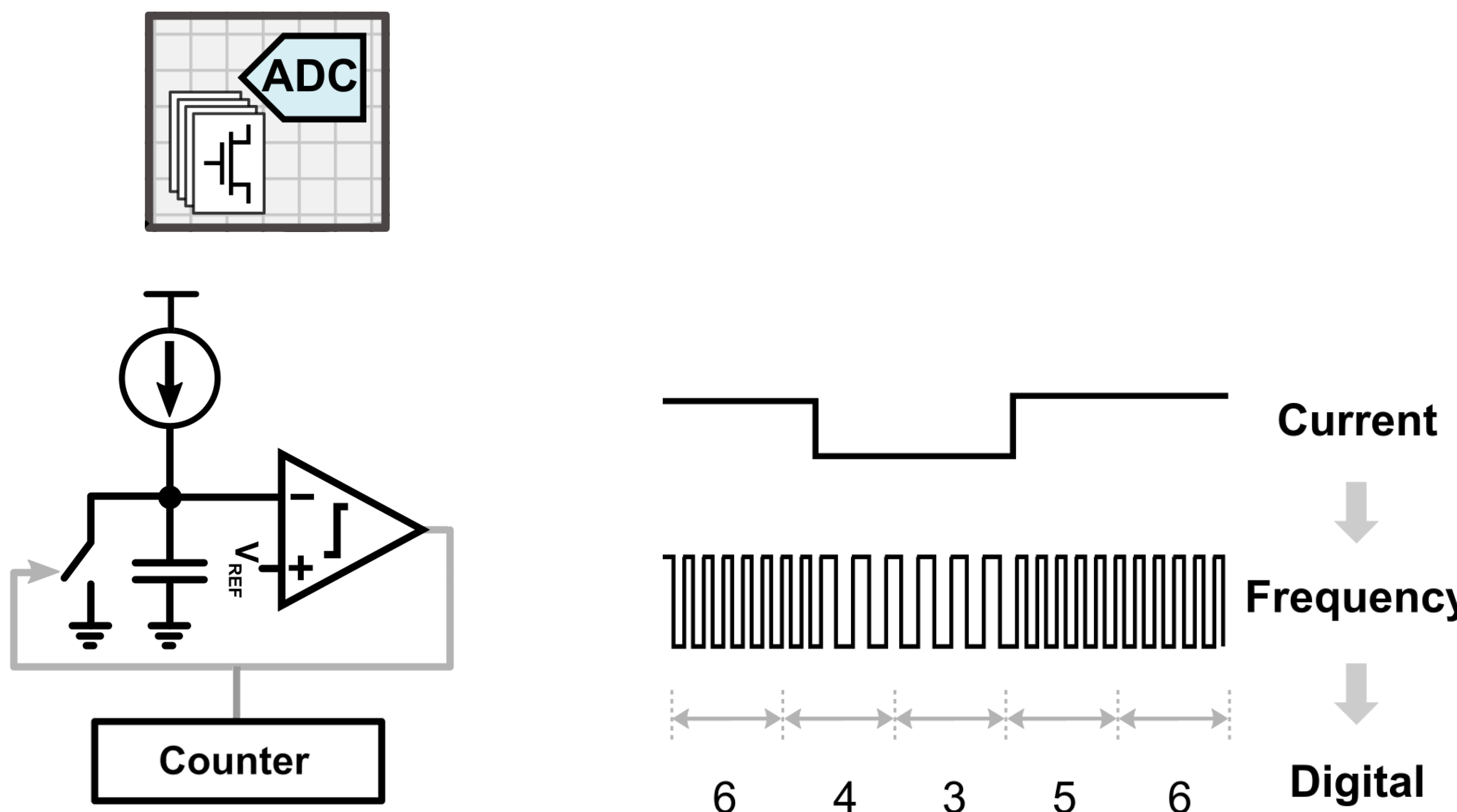

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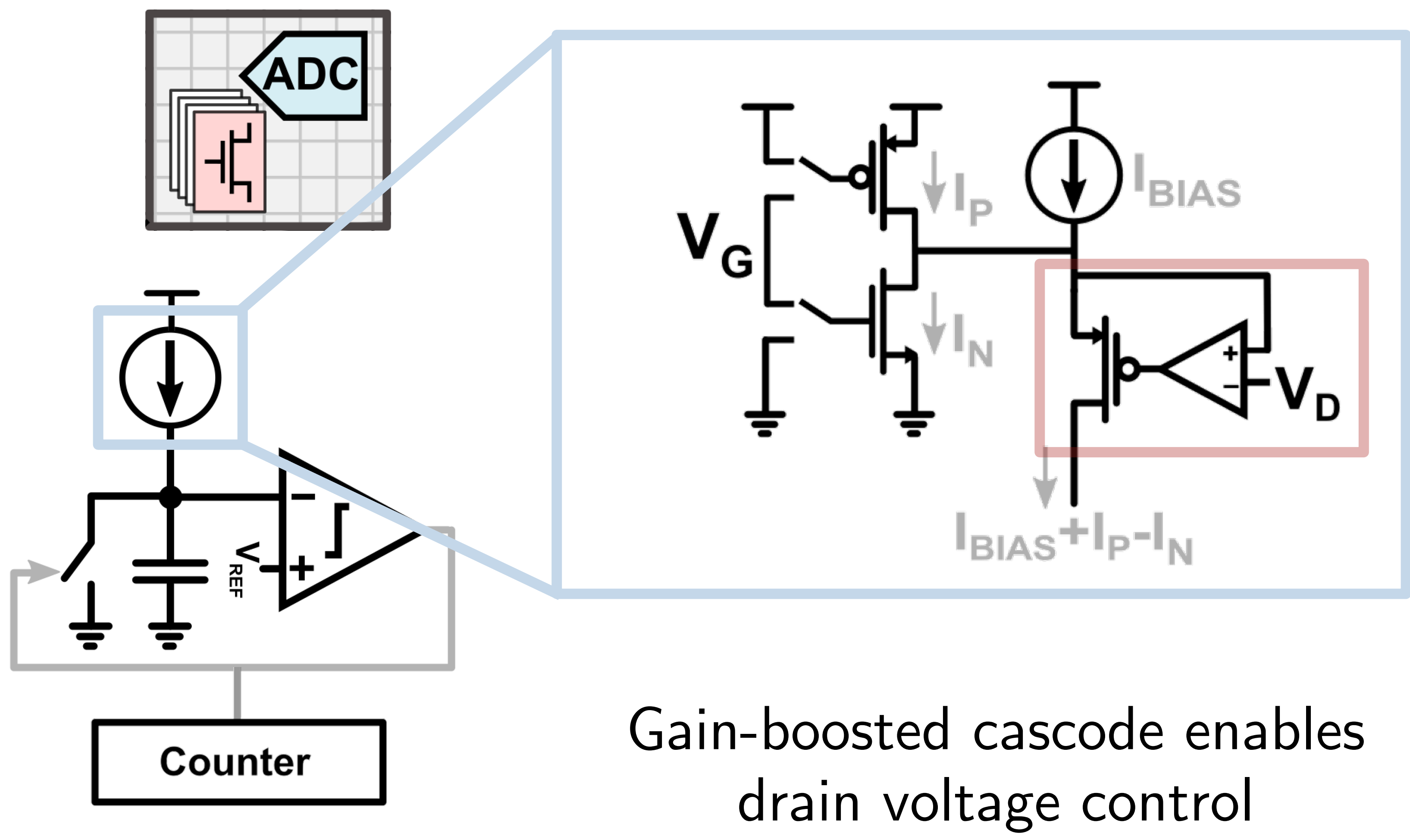
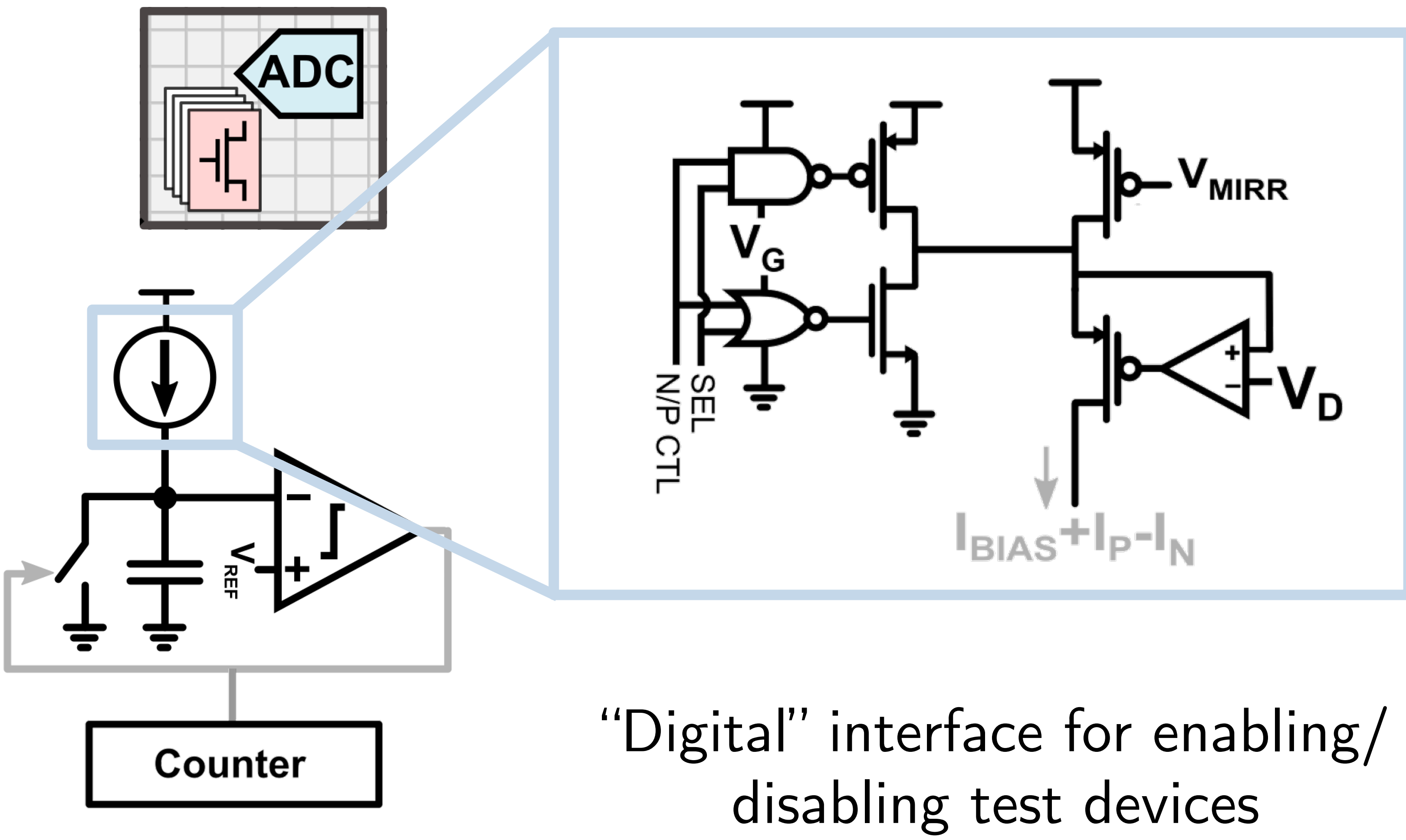


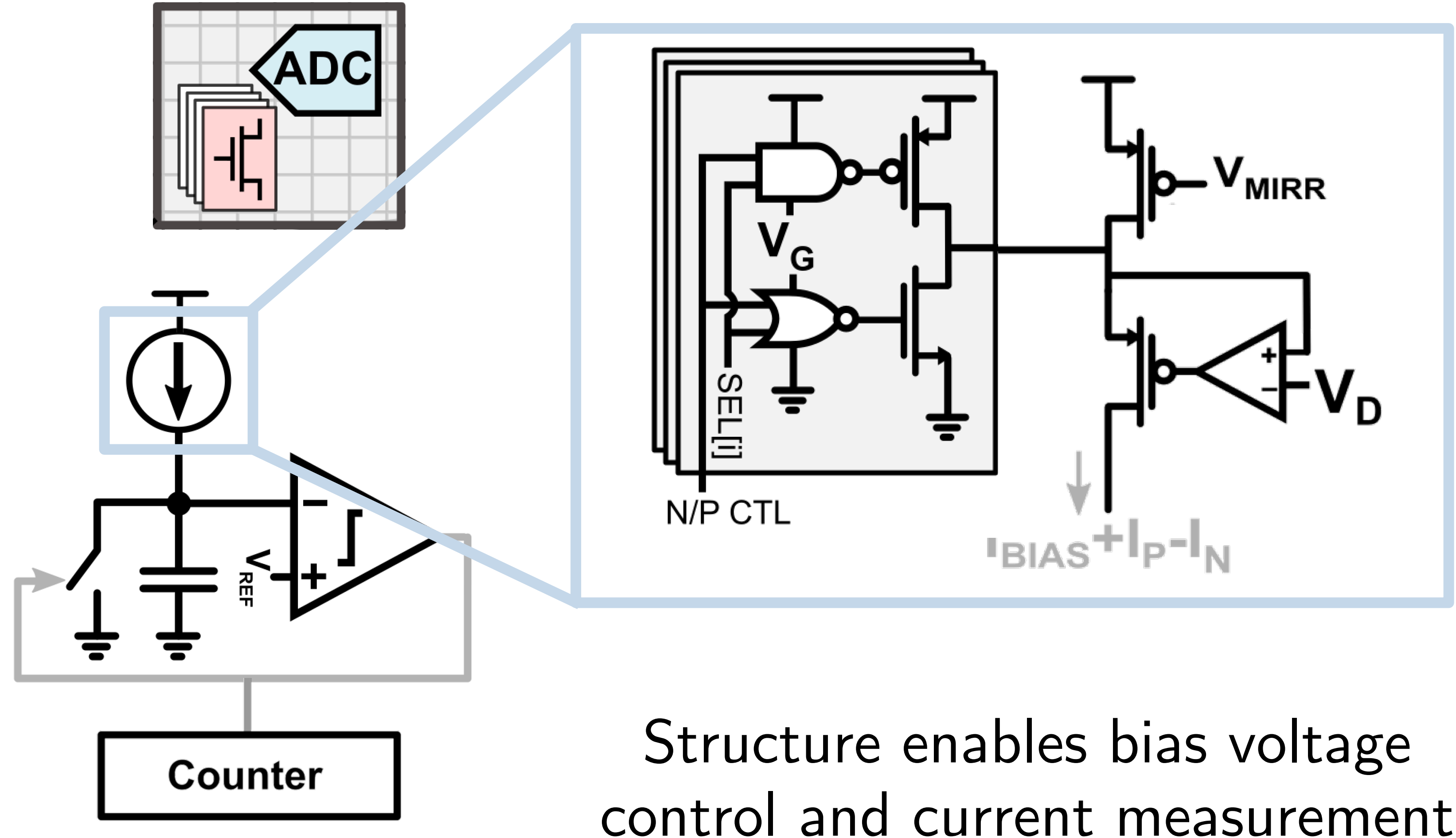
Gain-boosted cascode enables drain voltage control

On-Chip ADC Implementation: This Work



"Digital" interface for enabling/ disabling test devices

On-Chip ADC Implementation: This Work



Structure enables bias voltage control and current measurement

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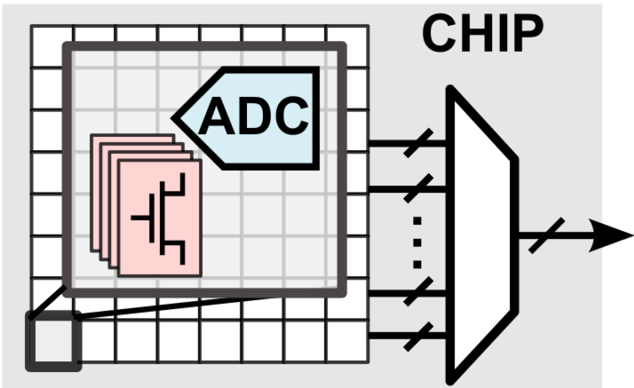
  - **Array implementation**
  - **Cell implementation**
- Test chip results
- Conclusions

Characterization Array Implementation



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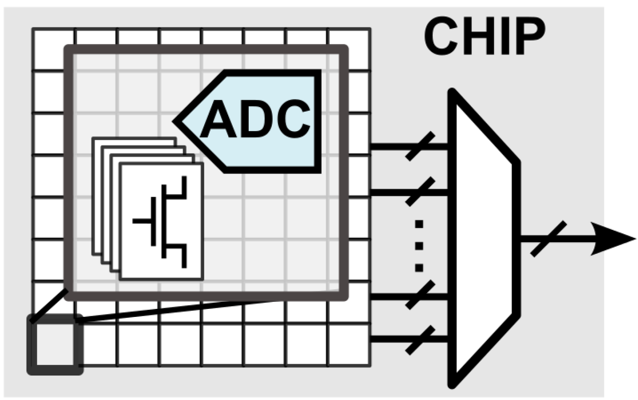
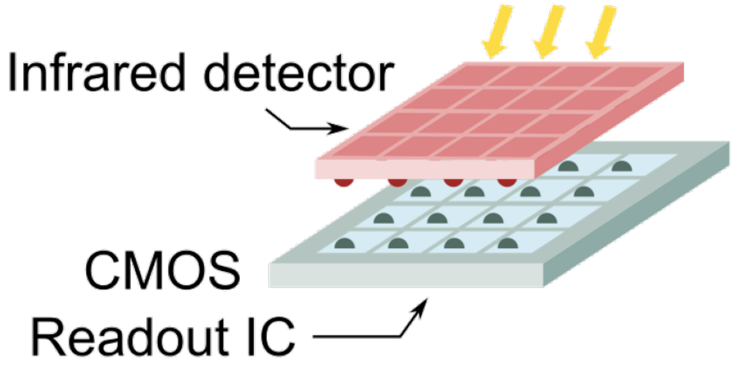
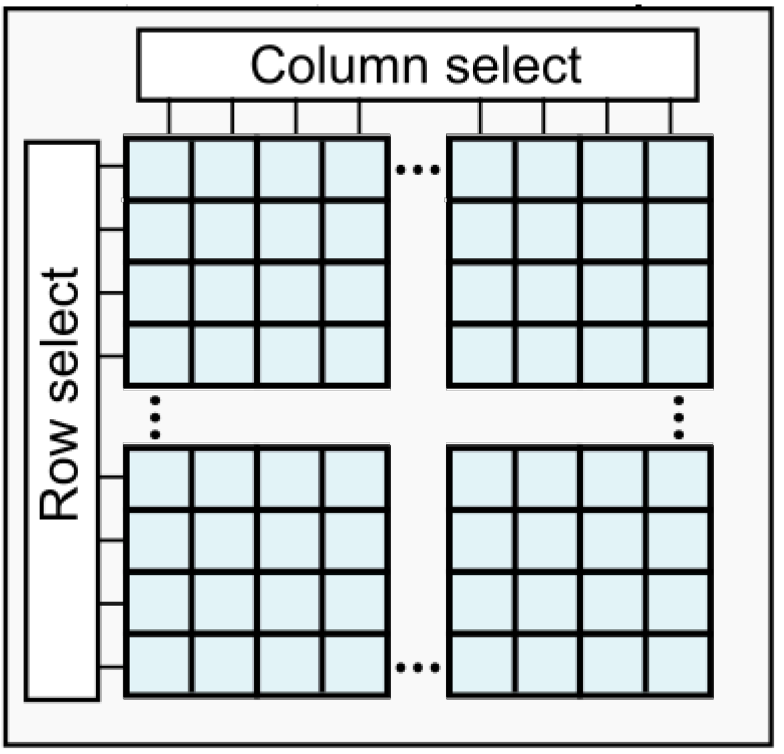
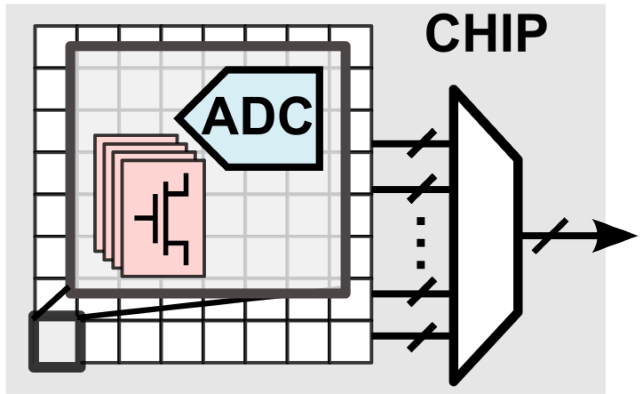


Typical detector array structure

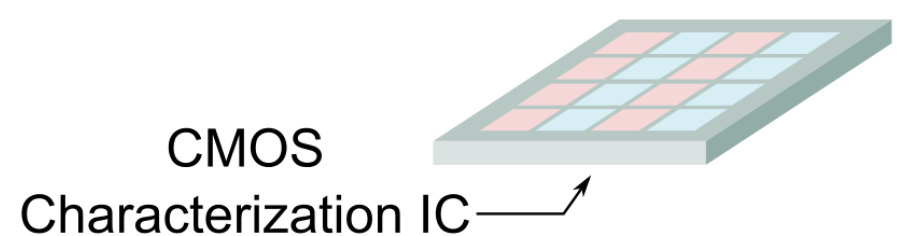


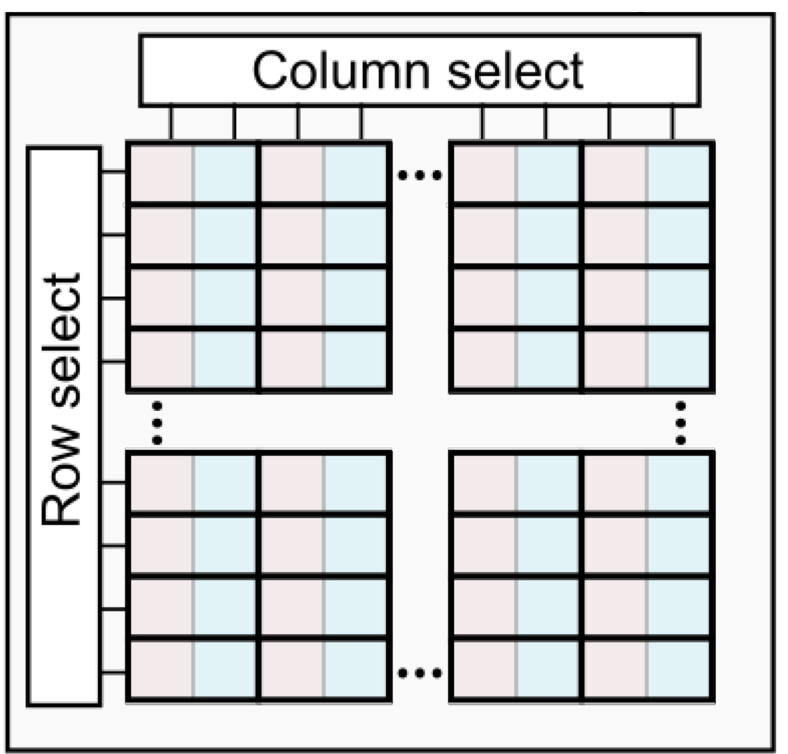


Characterization Array Implementation

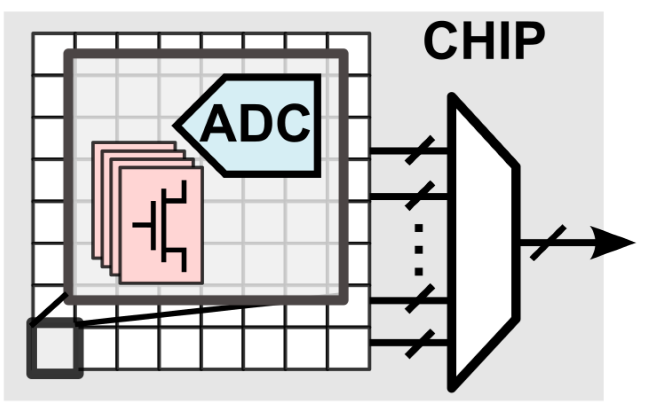


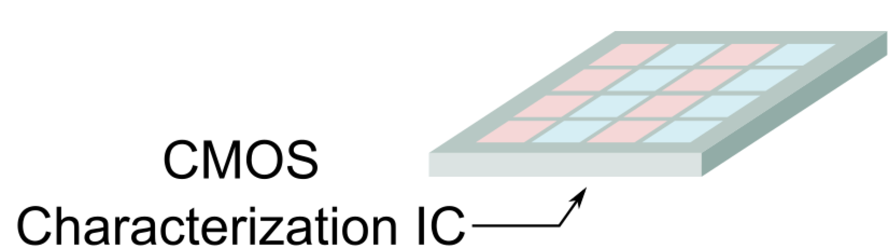
Characterization array +
Test current cells

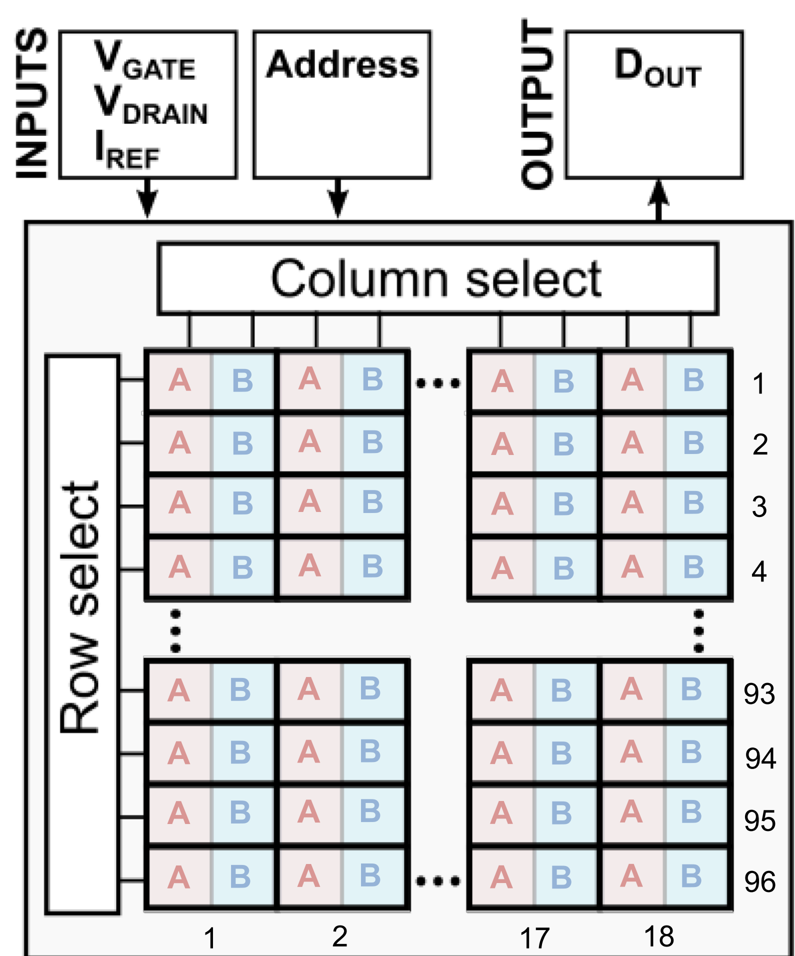




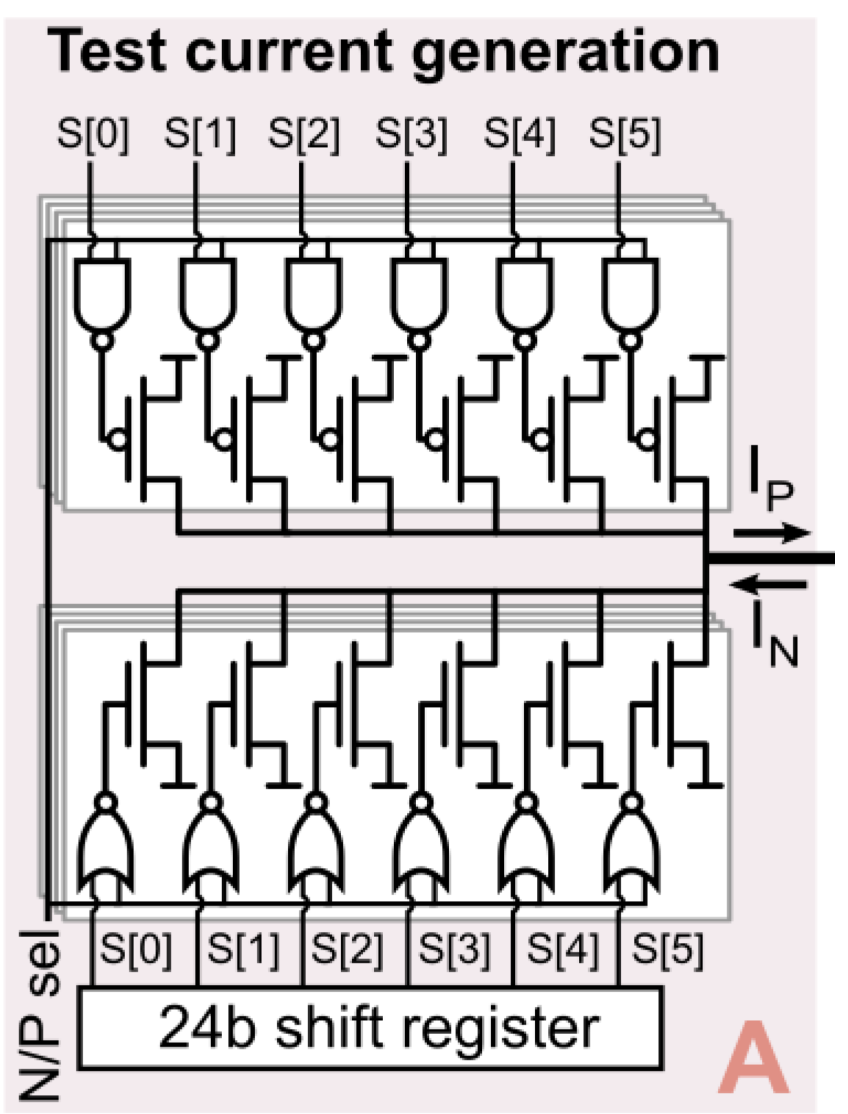
Characterization Array Implementation



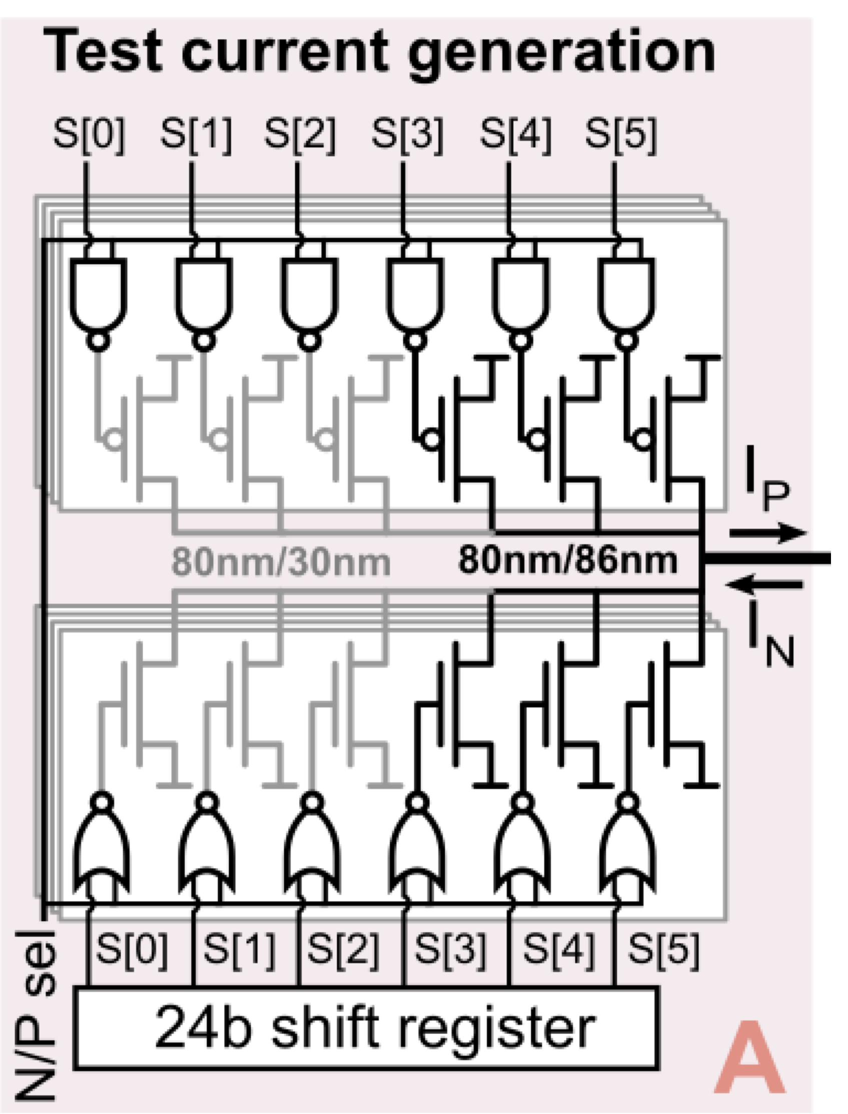




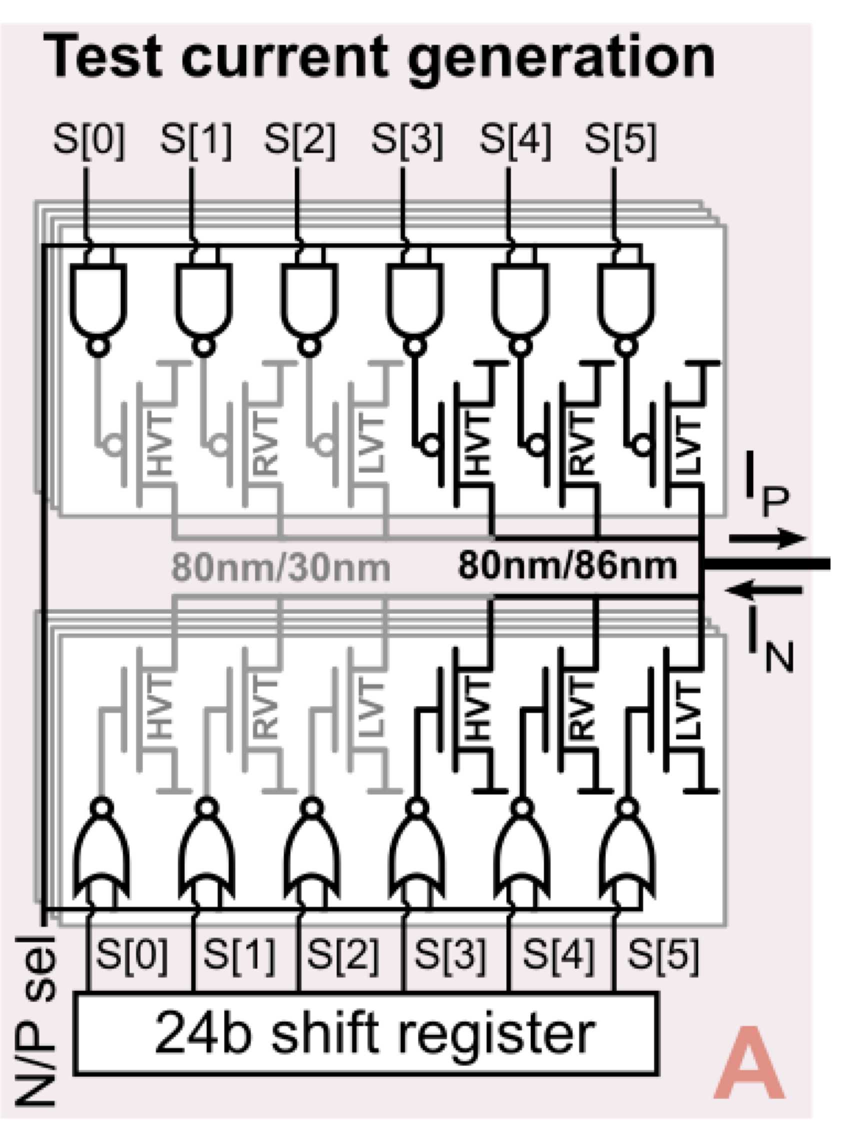
Device Under Test + Measurement Cells



Device Under Test + Measurement Cells

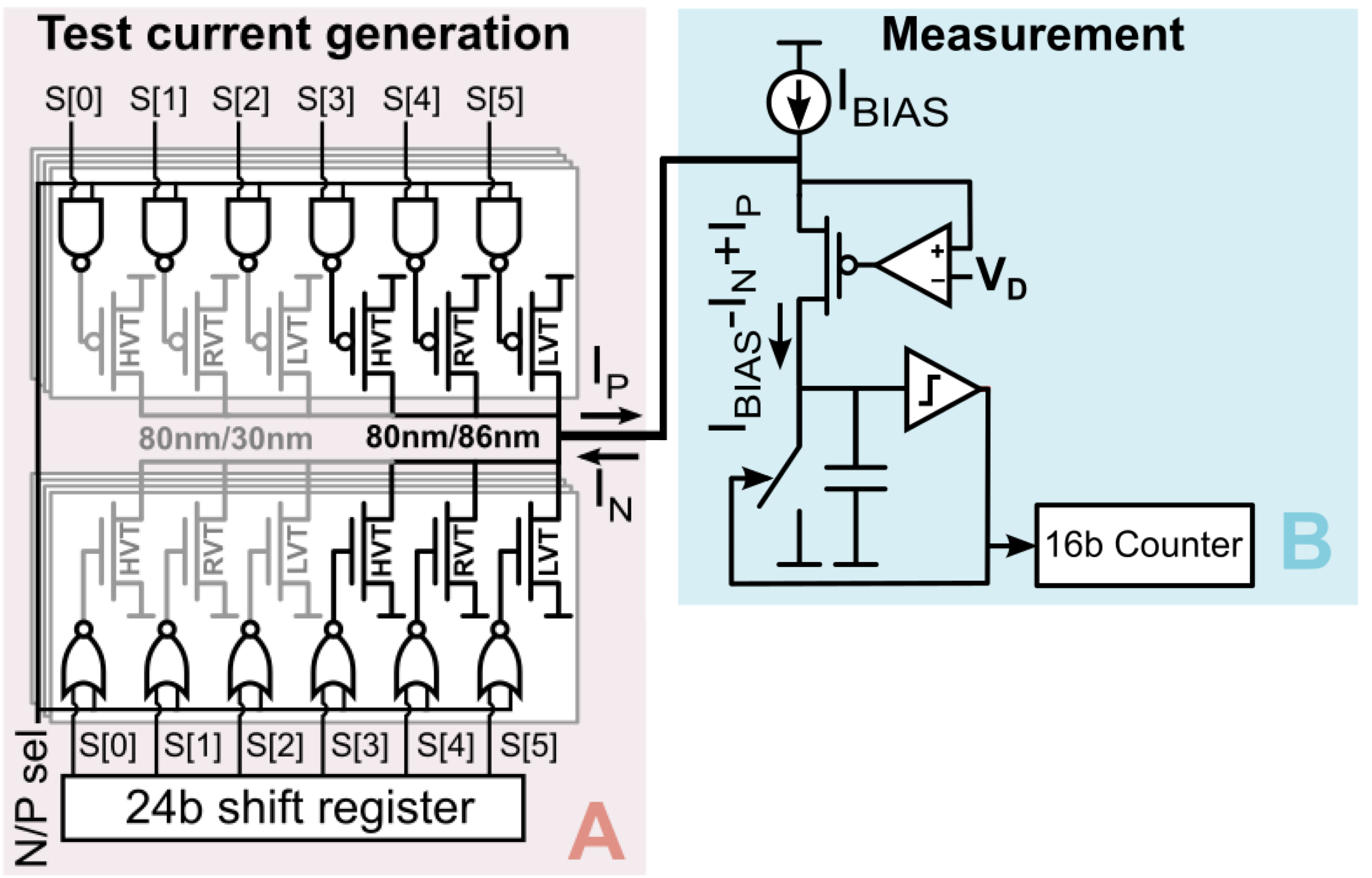


Device Under Test + Measurement Cells

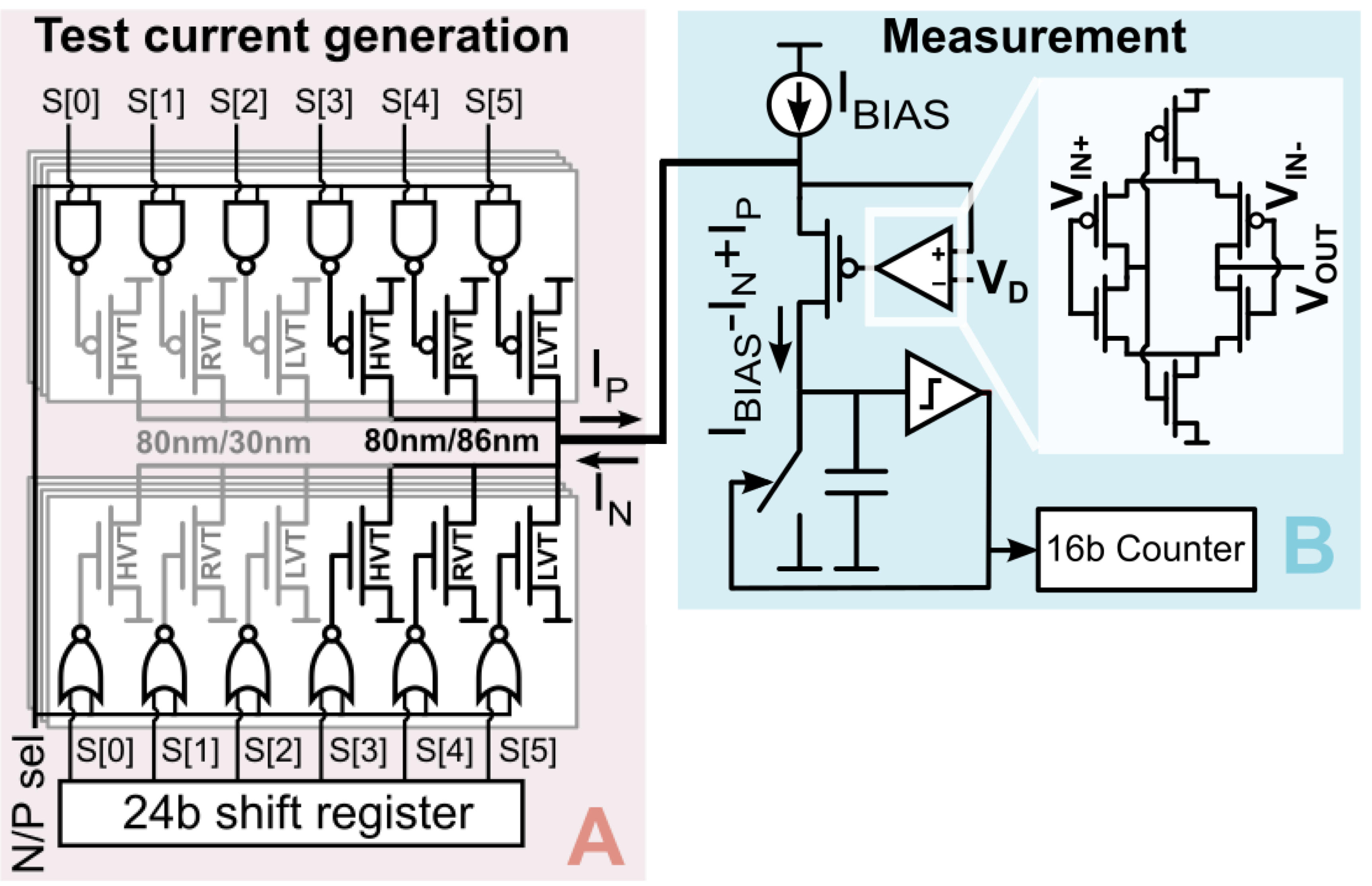


Test cells support multiple V_T, size characterization

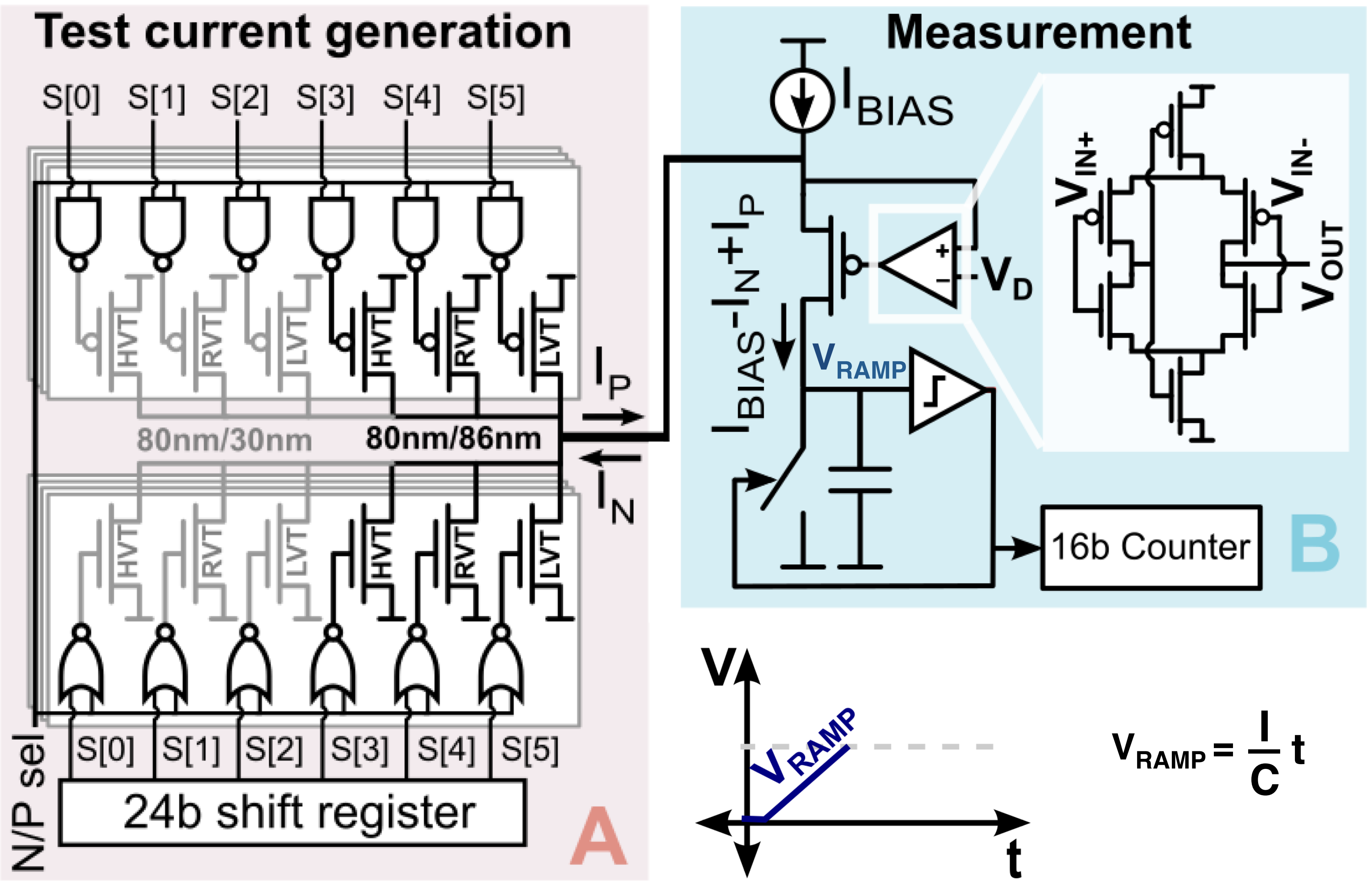
Device Under Test + Measurement Cells



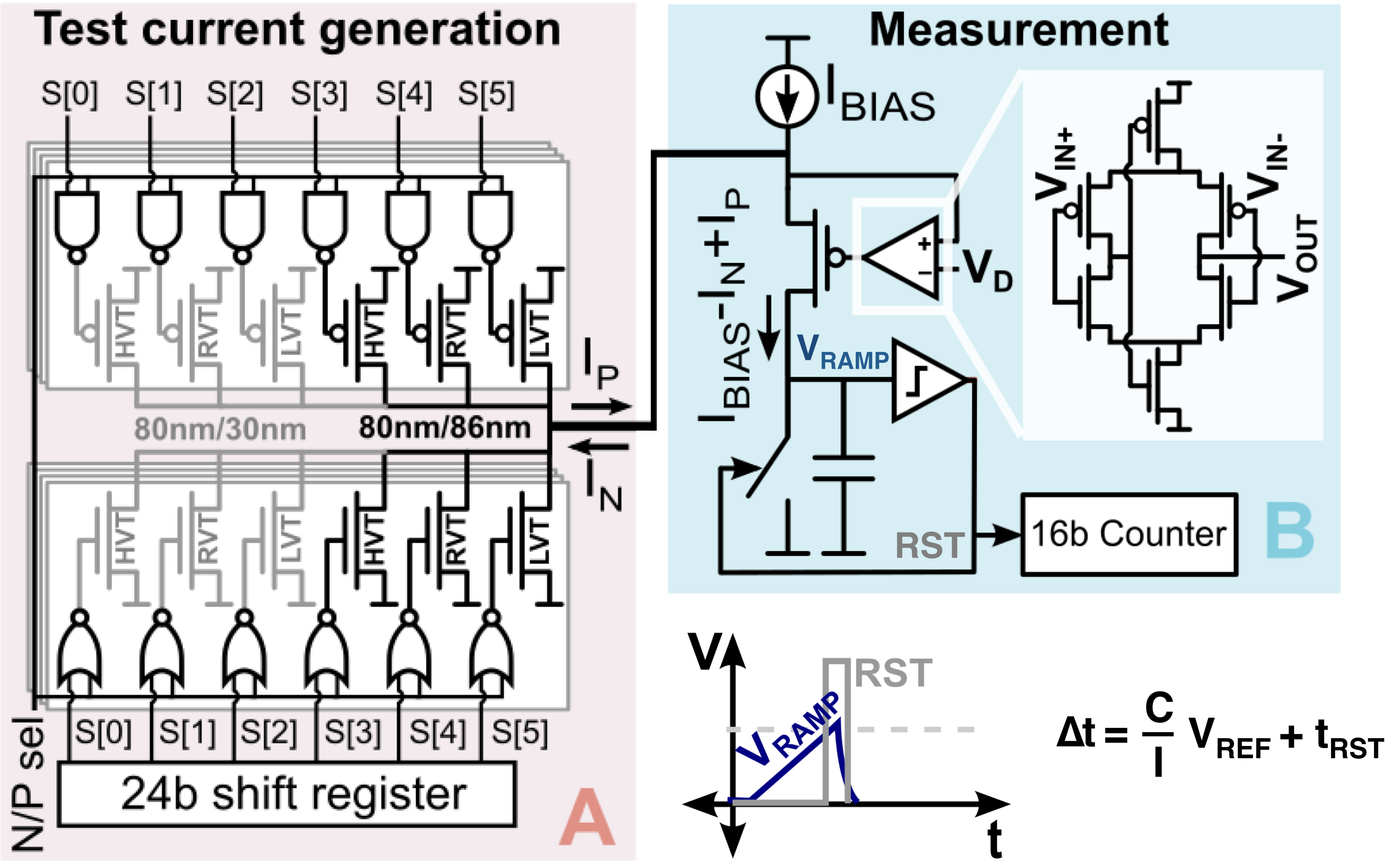
Device Under Test + Measurement Cells



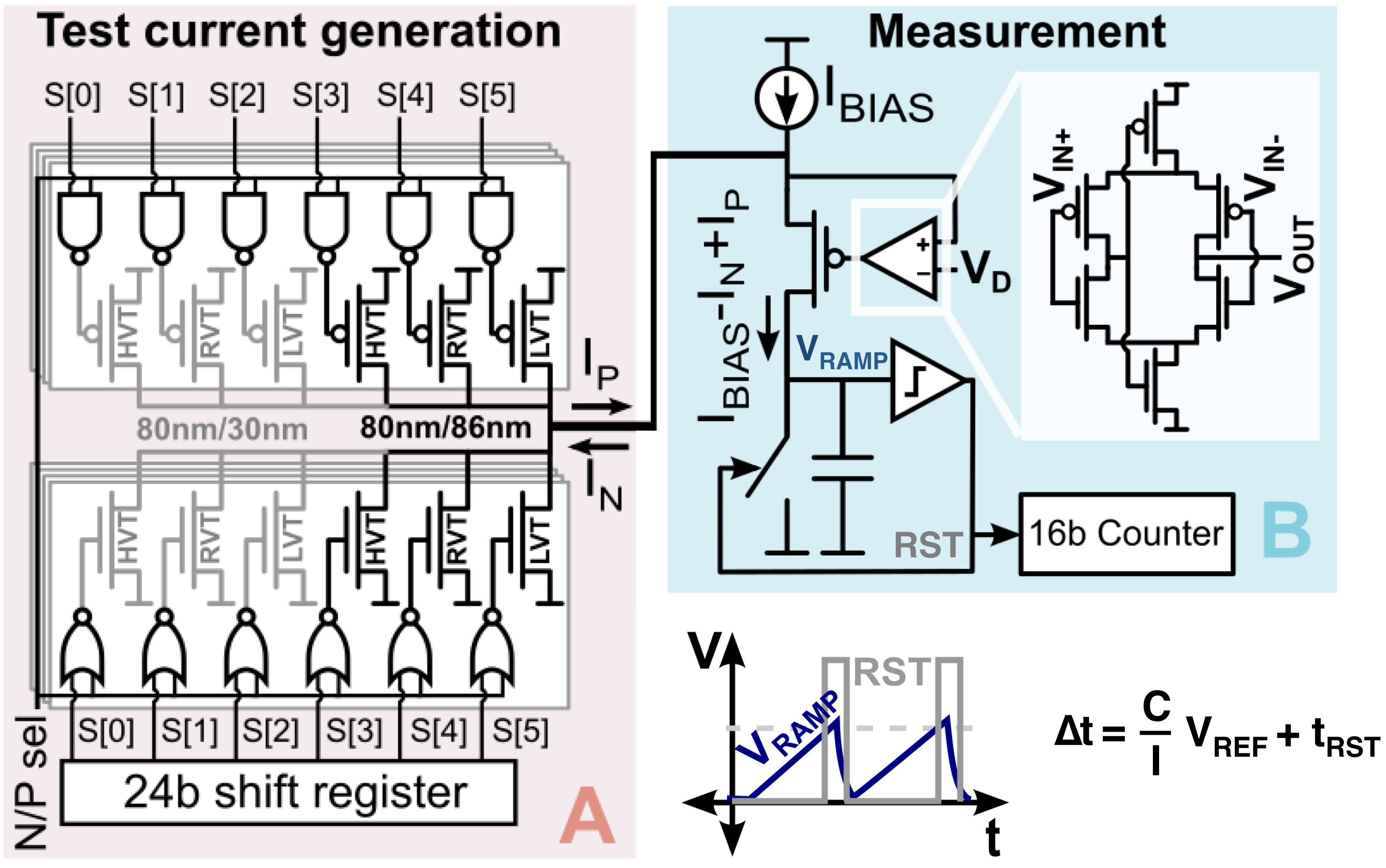
Device Under Test + Measurement Cells



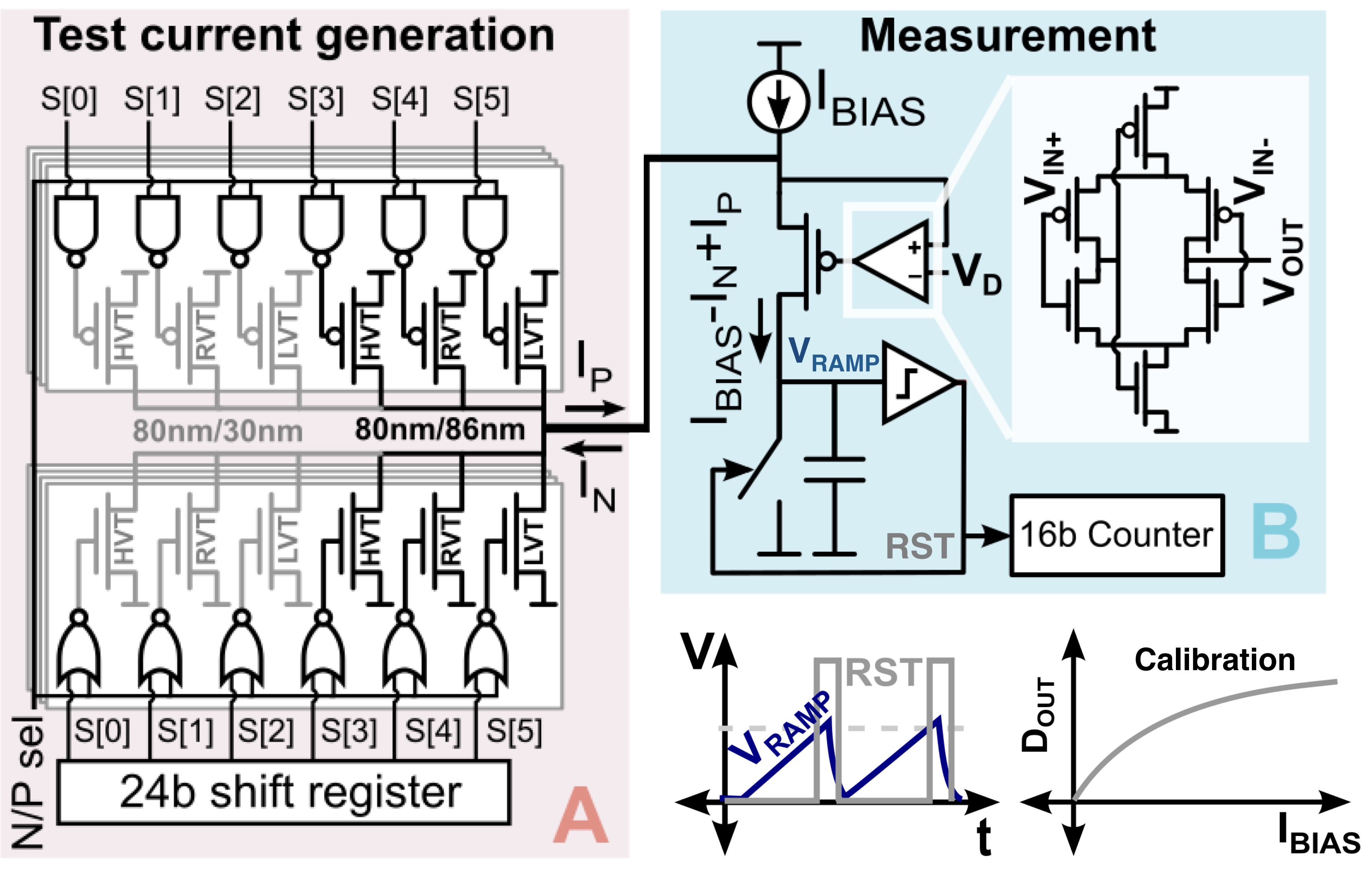
Device Under Test + Measurement Cells



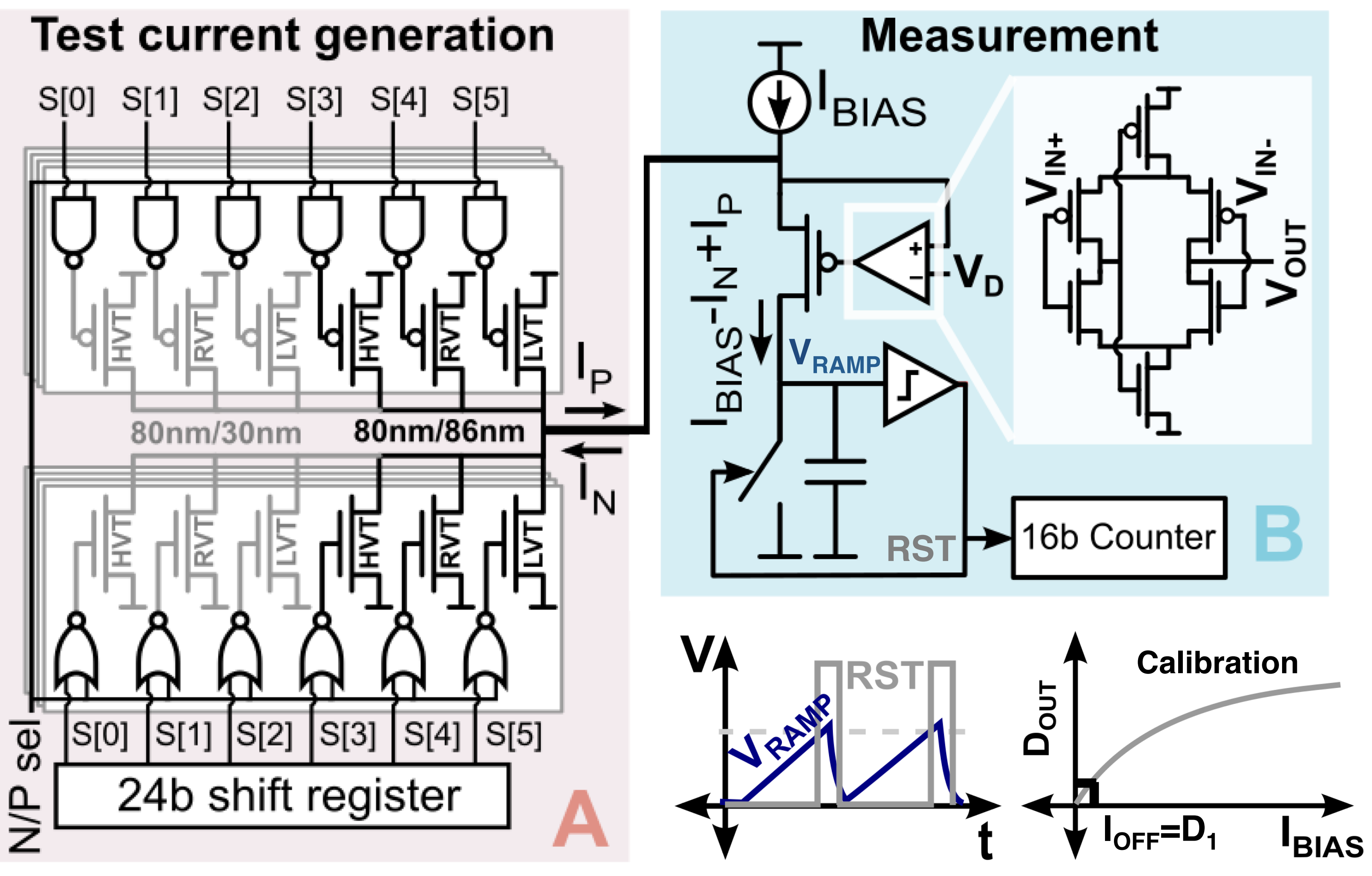
Device Under Test + Measurement Cells



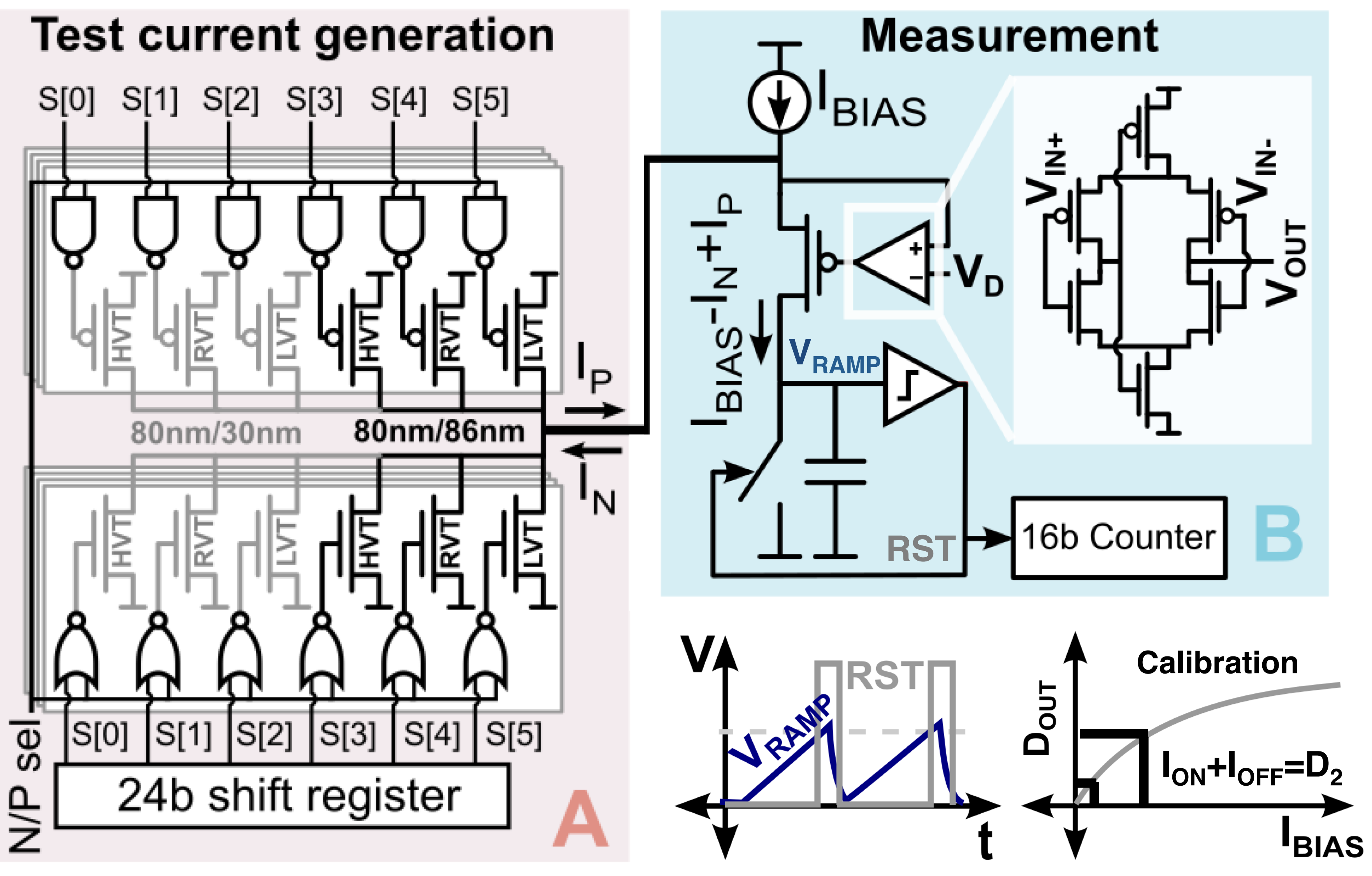
Device Under Test + Measurement Cells



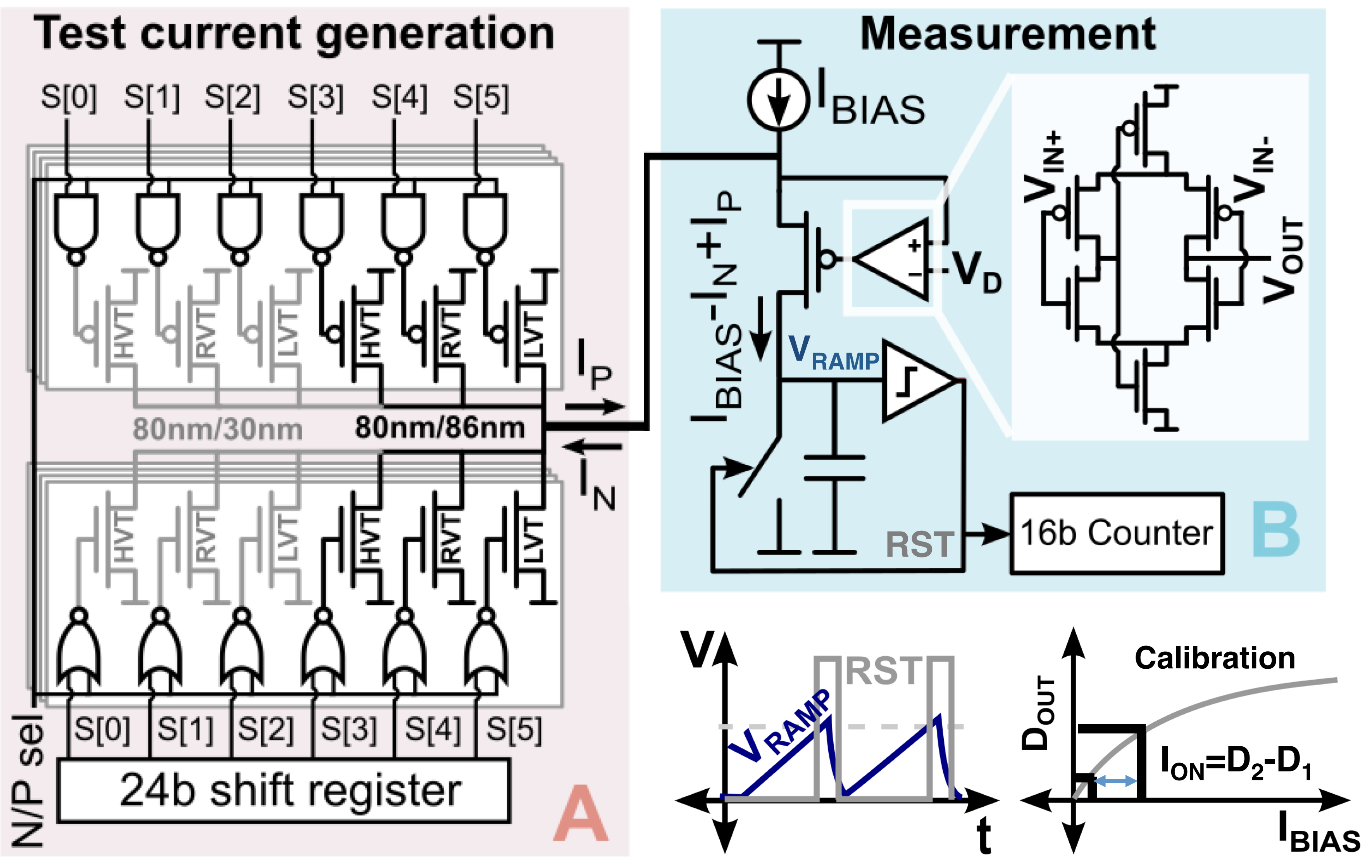
Device Under Test + Measurement Cells



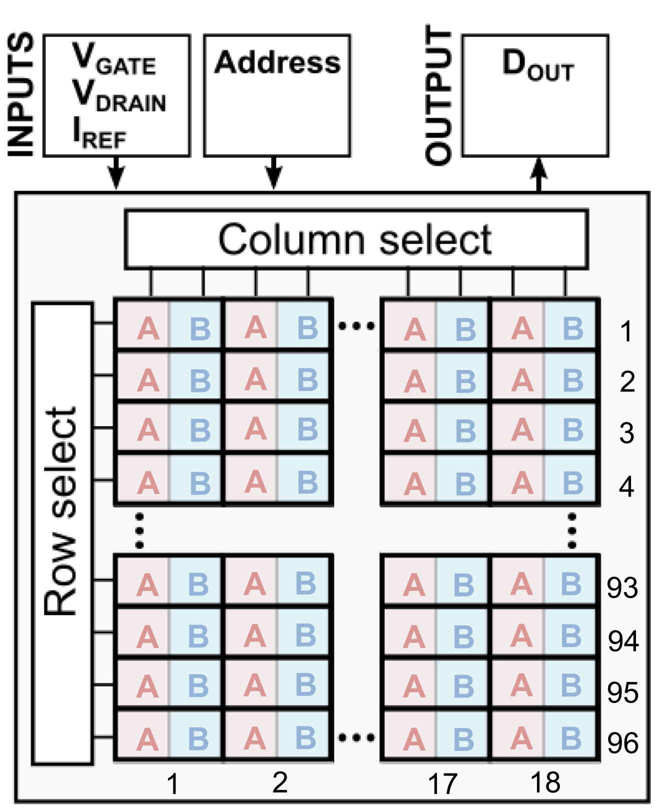
Device Under Test + Measurement Cells



Device Under Test + Measurement Cells

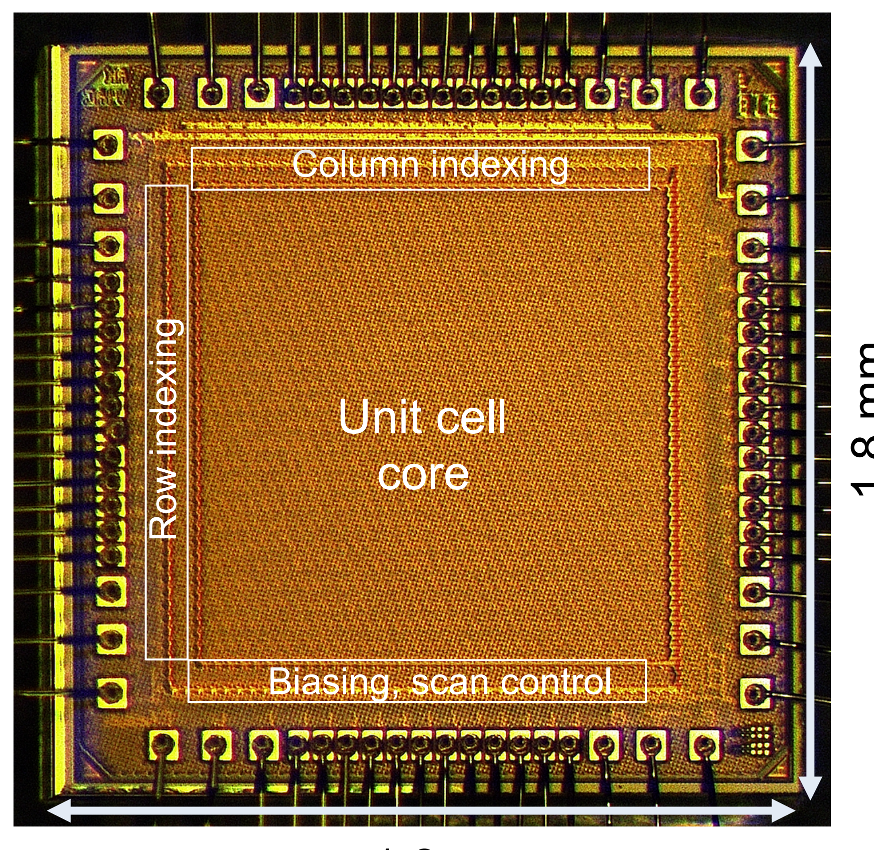


Characterization Array Implementation



A = Test current cell (48 devices/cell)
B = Measurement cell (16-bit ADC)

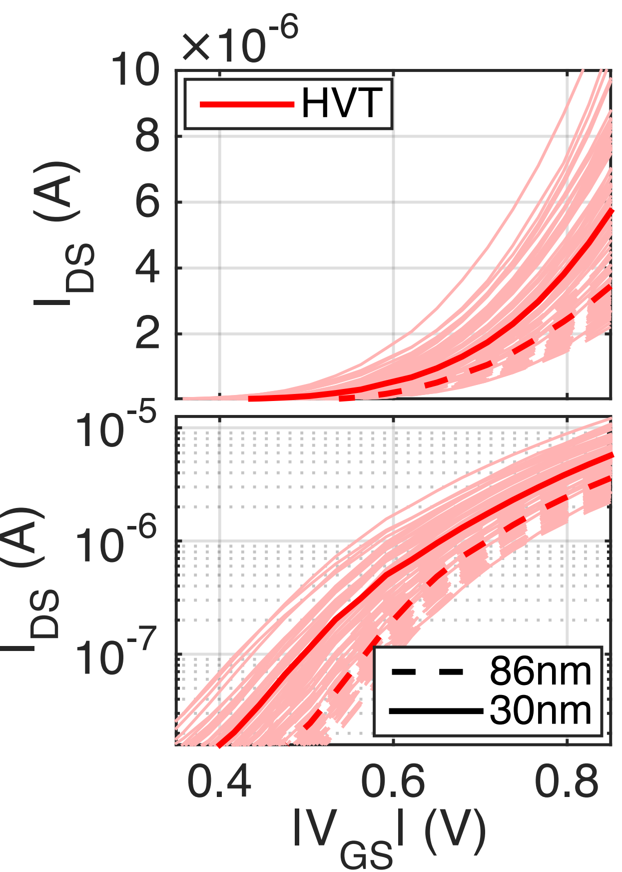
Fabricated in 28 nm bulk HKMG CMOS

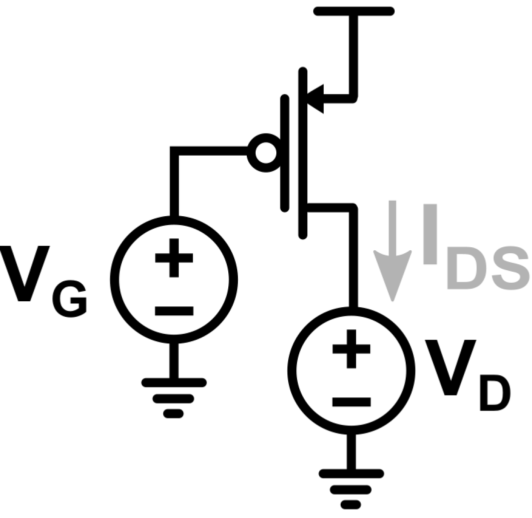


Outline

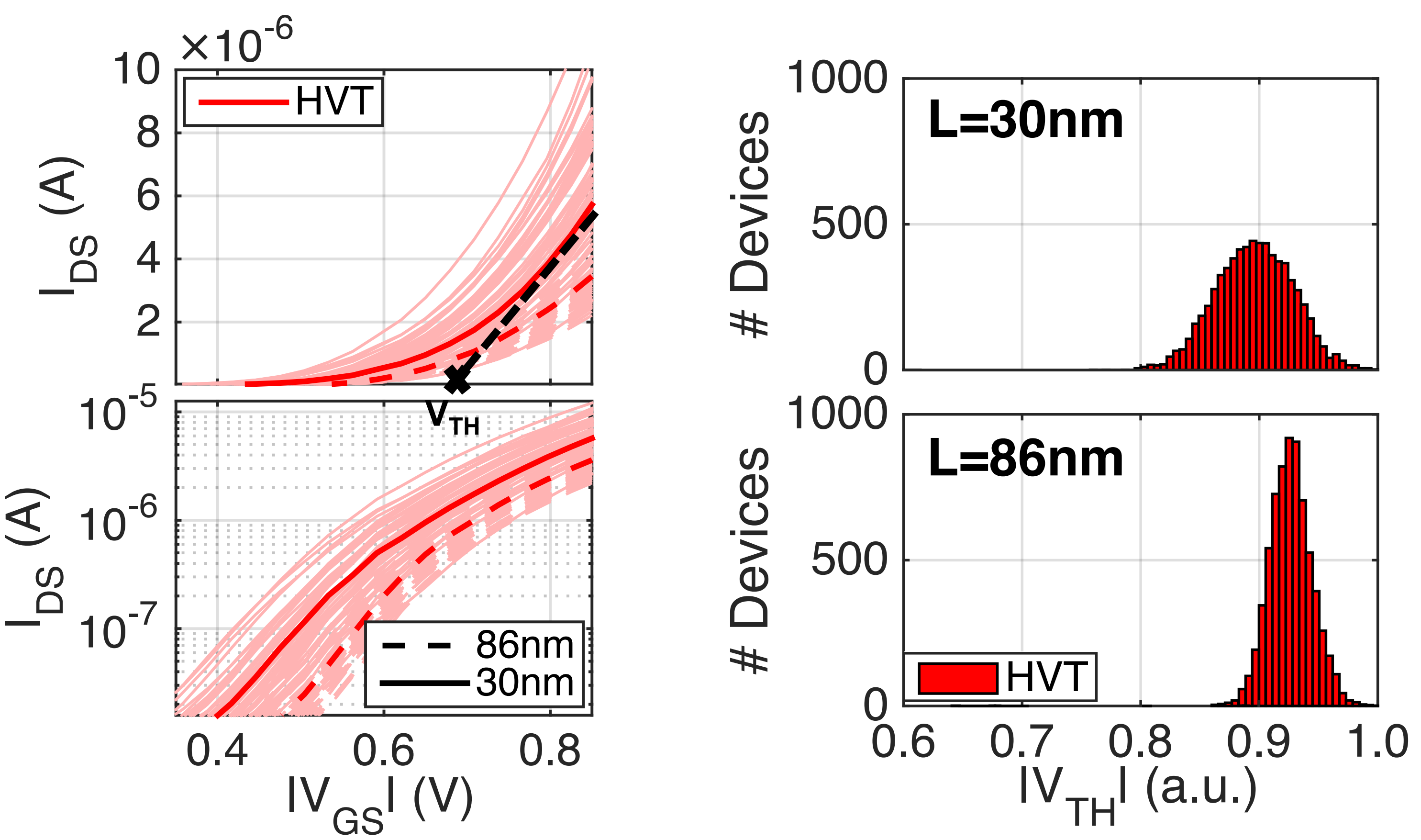
- Background & motivation
- Prior art comparison
- Proposed design
- **Test chip results**
  - **I-V measurements**
  - **RTN measurements**
- Conclusions

Results: I-V Characterization



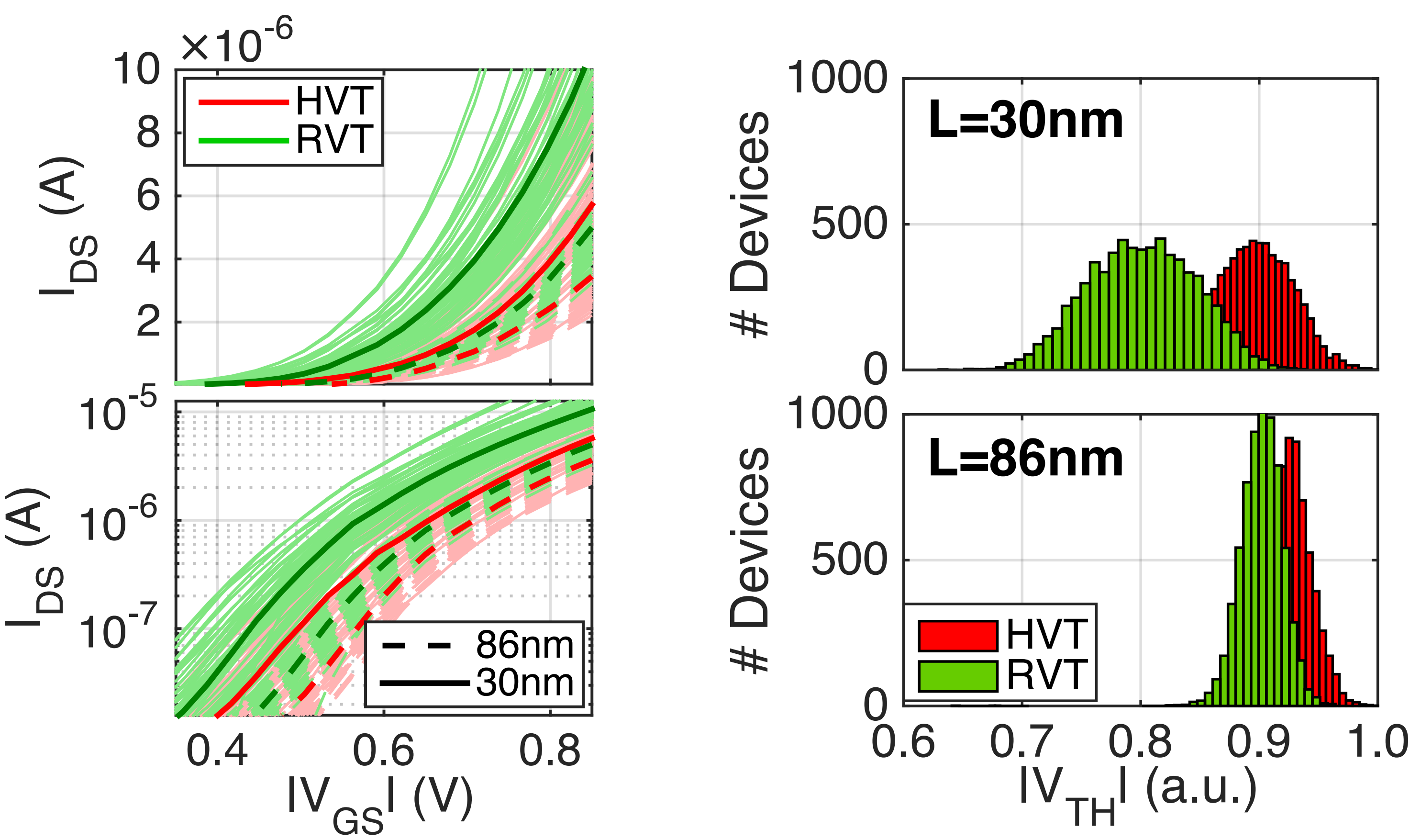


Results: I-V Characterization



Extracted threshold voltage follows expected trends

Results: I-V Characterization



Extracted threshold voltage follows expected trends

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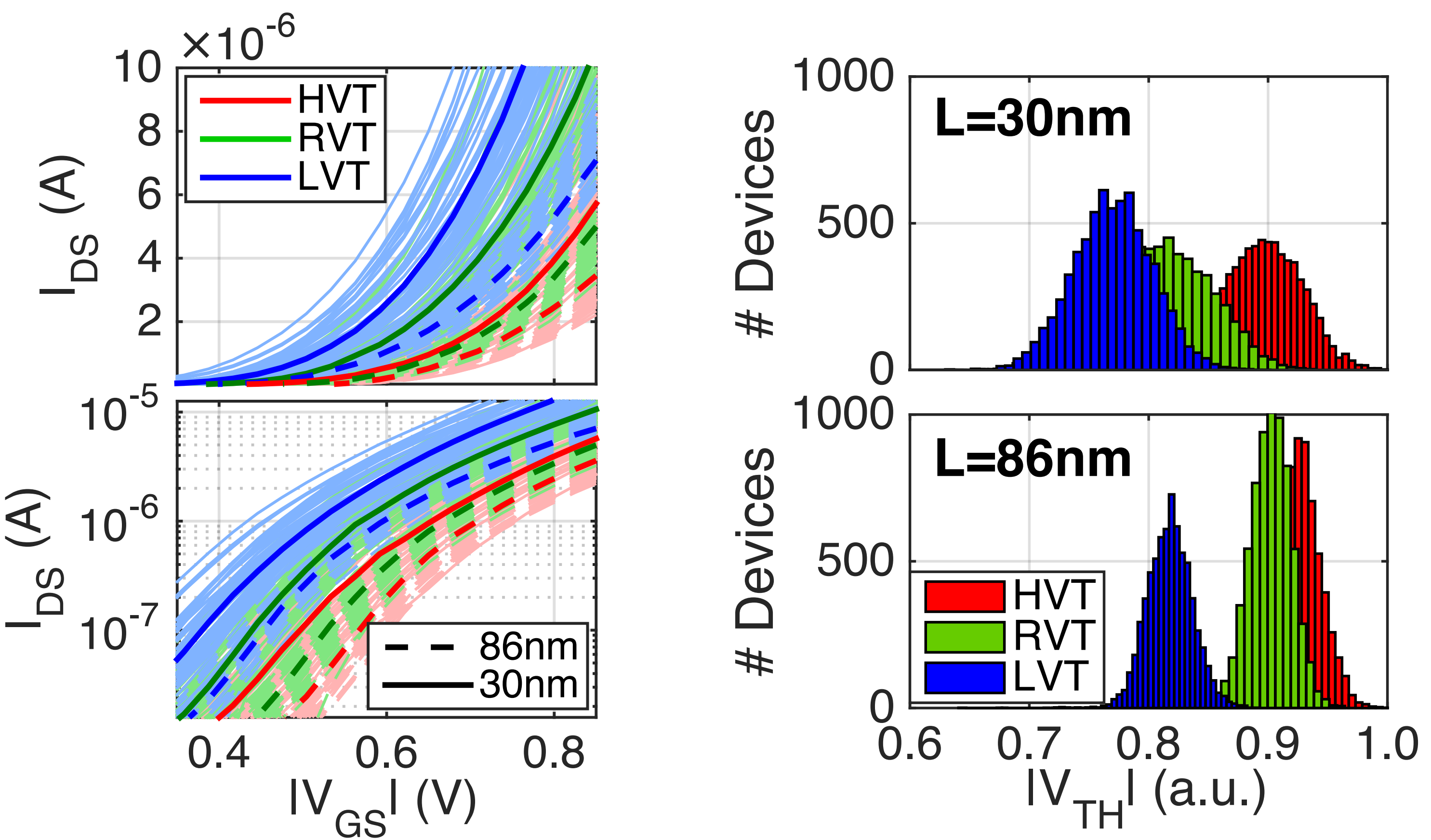

Extracted threshold voltage follows expected trends

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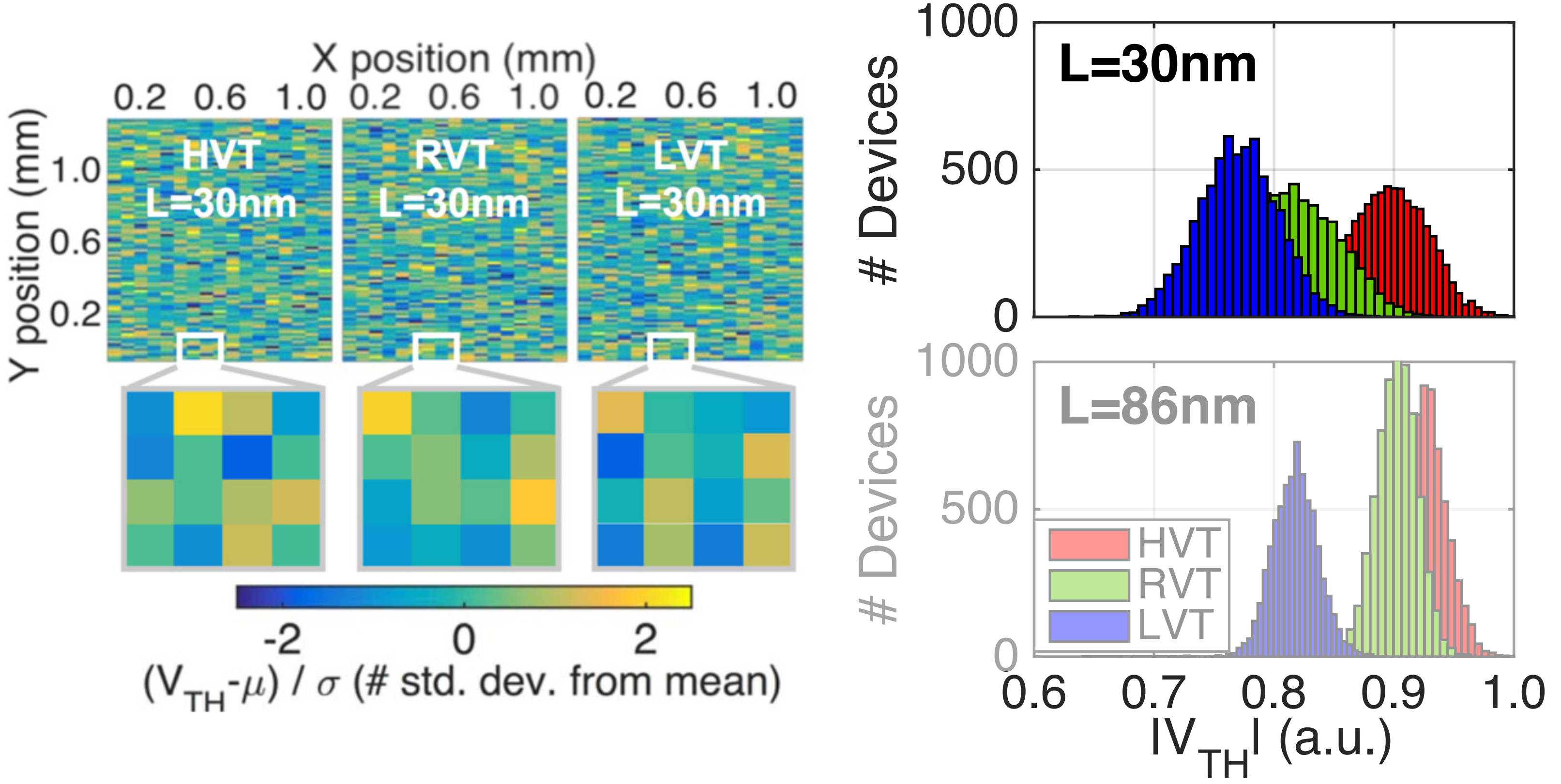
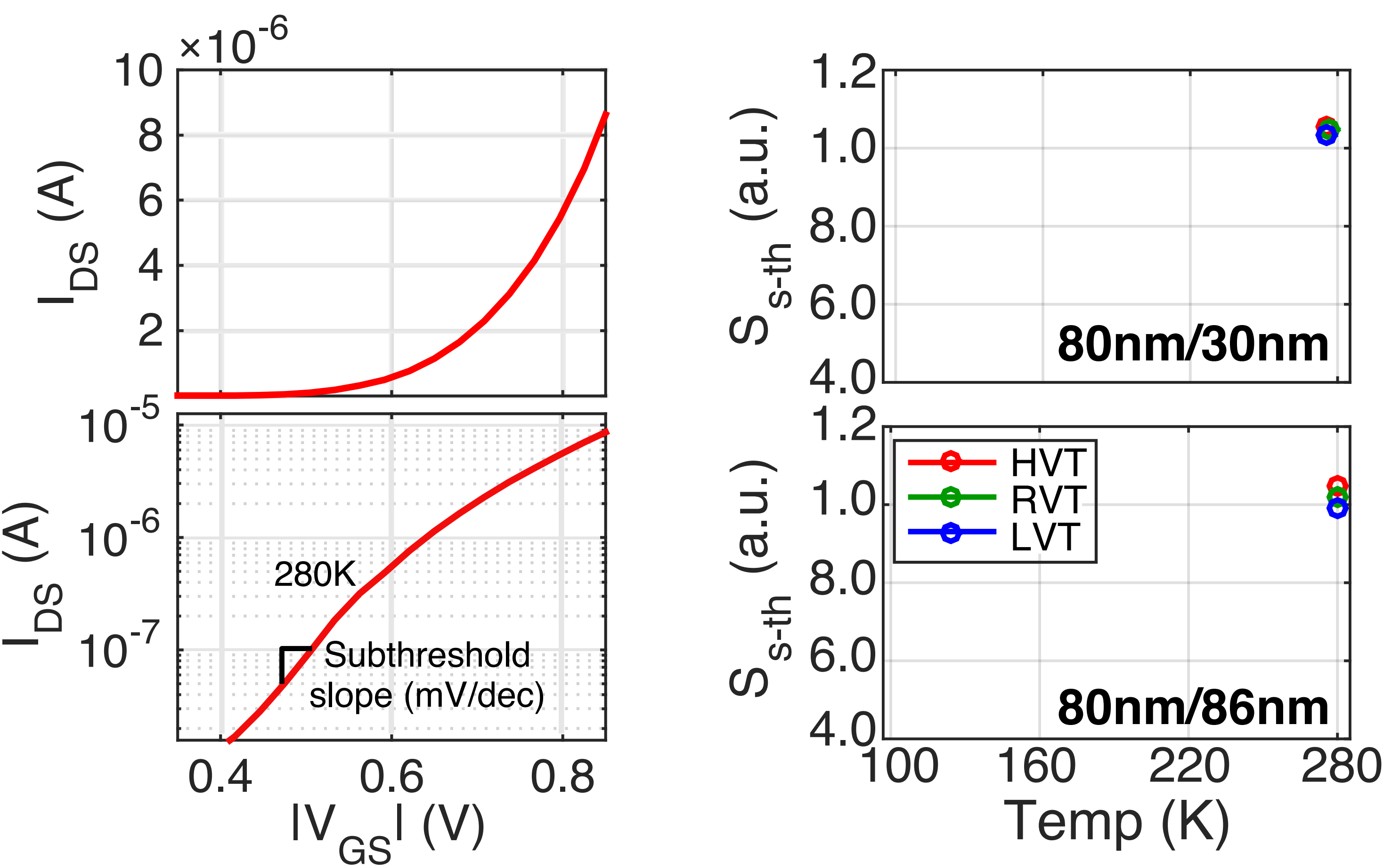


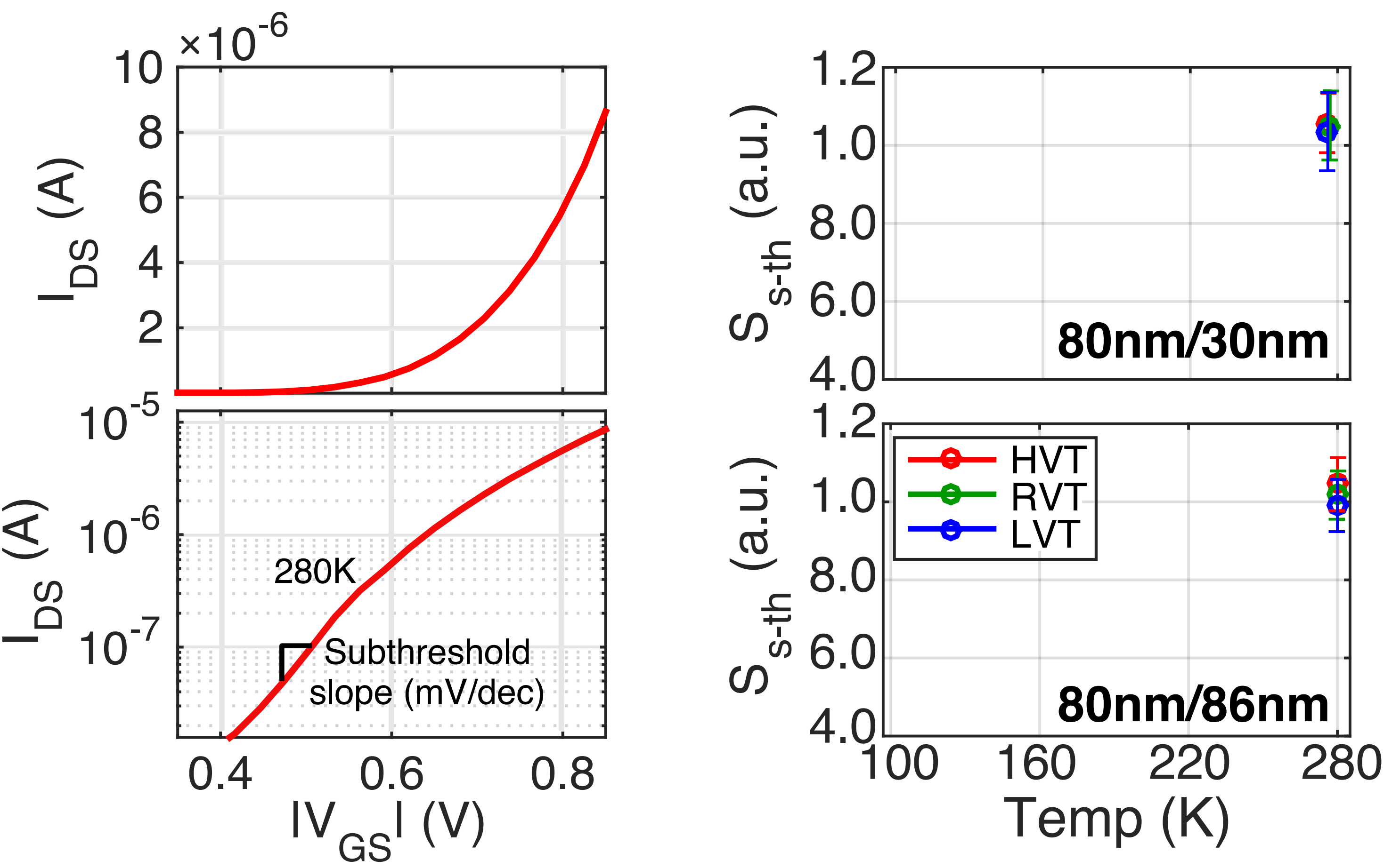
Random variation dominates spatial variation in 1 mm x 1 mm area

Results: I-V Characterization



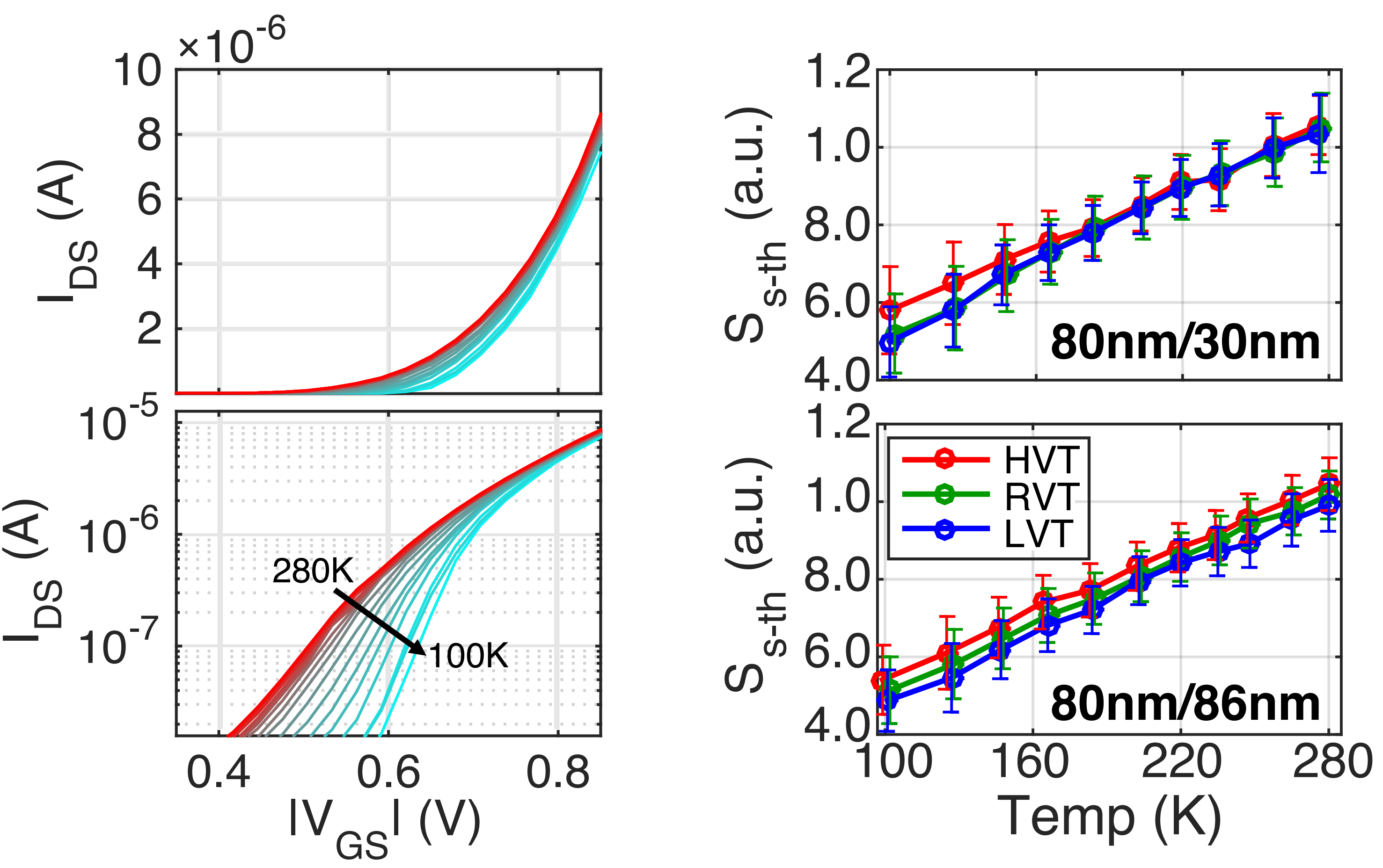
High dynamic range enables
subthreshold I-V characterization

Results: I-V Characterization



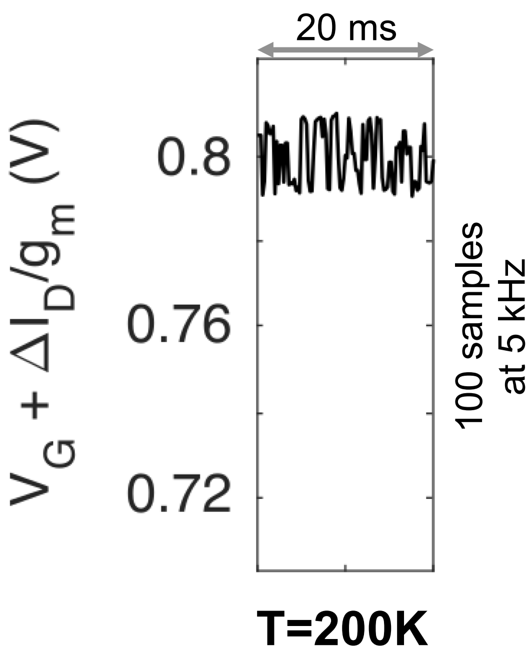
High dynamic range enables subthreshold I-V characterization

Results: I-V Characterization

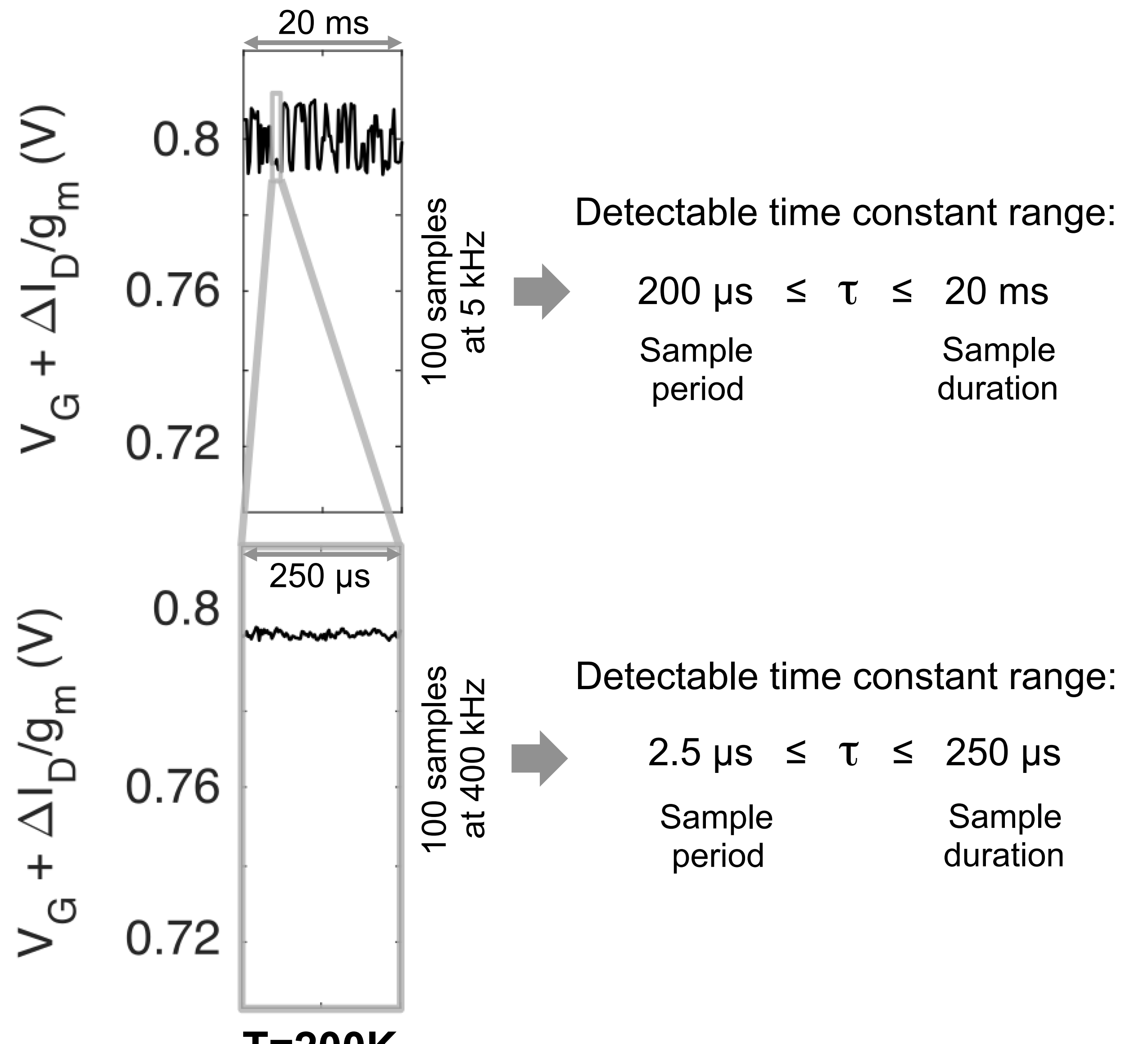


Relative variability in subthreshold slope decreases with temperature

Results: RTN Characterization



Results: RTN Characterization



Detectable time constant range:

$200\ \mu s \leq \tau \leq 20\ ms$

Sample period — Sample duration

Detectable time constant range:

$2.5\ \mu s \leq \tau \leq 250\ \mu s$

Sample period — Sample duration

Results: RTN Characterization

20 ms

$V_G + \Delta I_D/g_m$ (V)

0.8

0.76

0.72

100 samples at 5 kHz

250 µs

$V_G + \Delta I_D/g_m$ (V)

0.8

0.76

0.72

100 samples at 400 kHz

T=200K

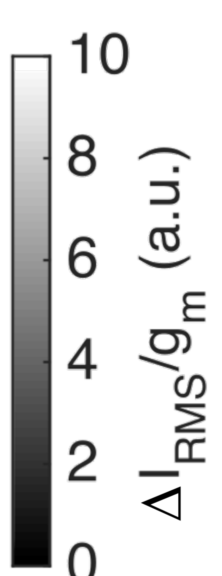
V_G=0.8V

V_G=0.72V

200K

V_G=0.8V

V_G=0.72V



Results: RTN Characterization

20 ms 20 ms

$V_G + \Delta I_D/g_m$ (V)

0.8

0.76

0.72

100 samples at 5 kHz

250 μs 250 μs

$V_G + \Delta I_D/g_m$ (V)

0.8

0.76

0.72

100 samples at 400 kHz

T=200K **T=220K**

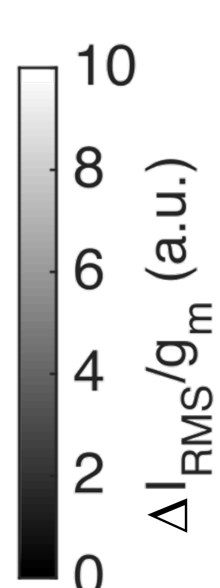
V_G=0.8V

V_G=0.72V

200K 220K

V_G=0.8V

V_G=0.72V



Results: RTN Characterization

20 ms 20 ms 20 ms

$V_G + \Delta I_D/g_m$ (V)

0.8
0.76
0.72

100 samples at 5 kHz

V_G=0.8V
V_G=0.72V

200K 220K 240K

250 µs 250 µs 250 µs

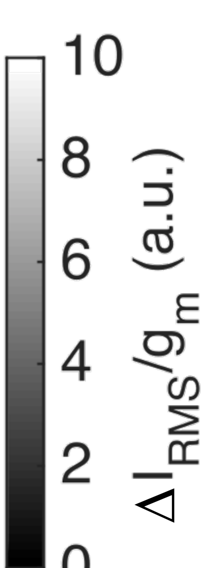
$V_G + \Delta I_D/g_m$ (V)

0.8
0.76
0.72

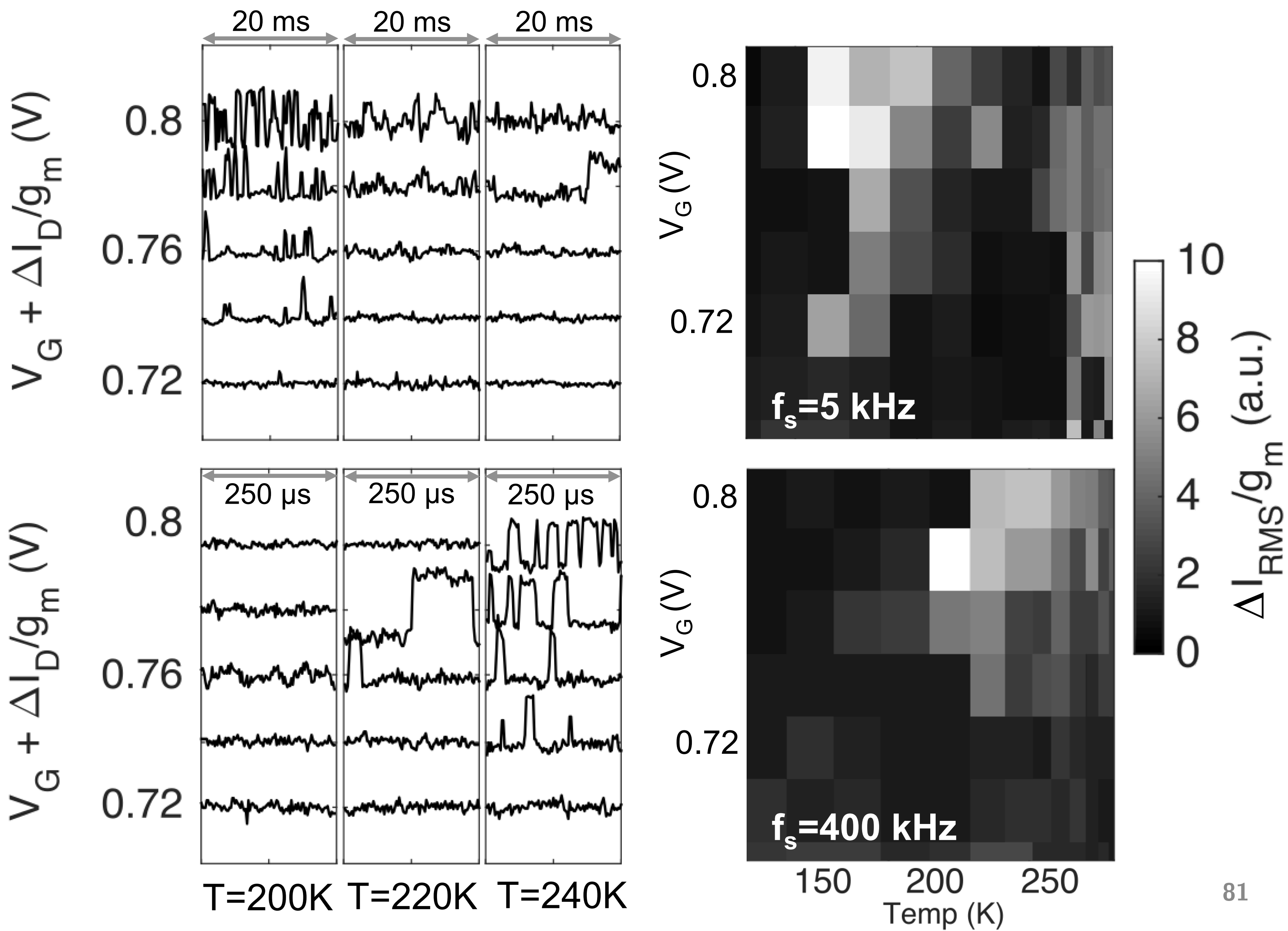
100 samples at 400 kHz

V_G=0.8V
V_G=0.72V

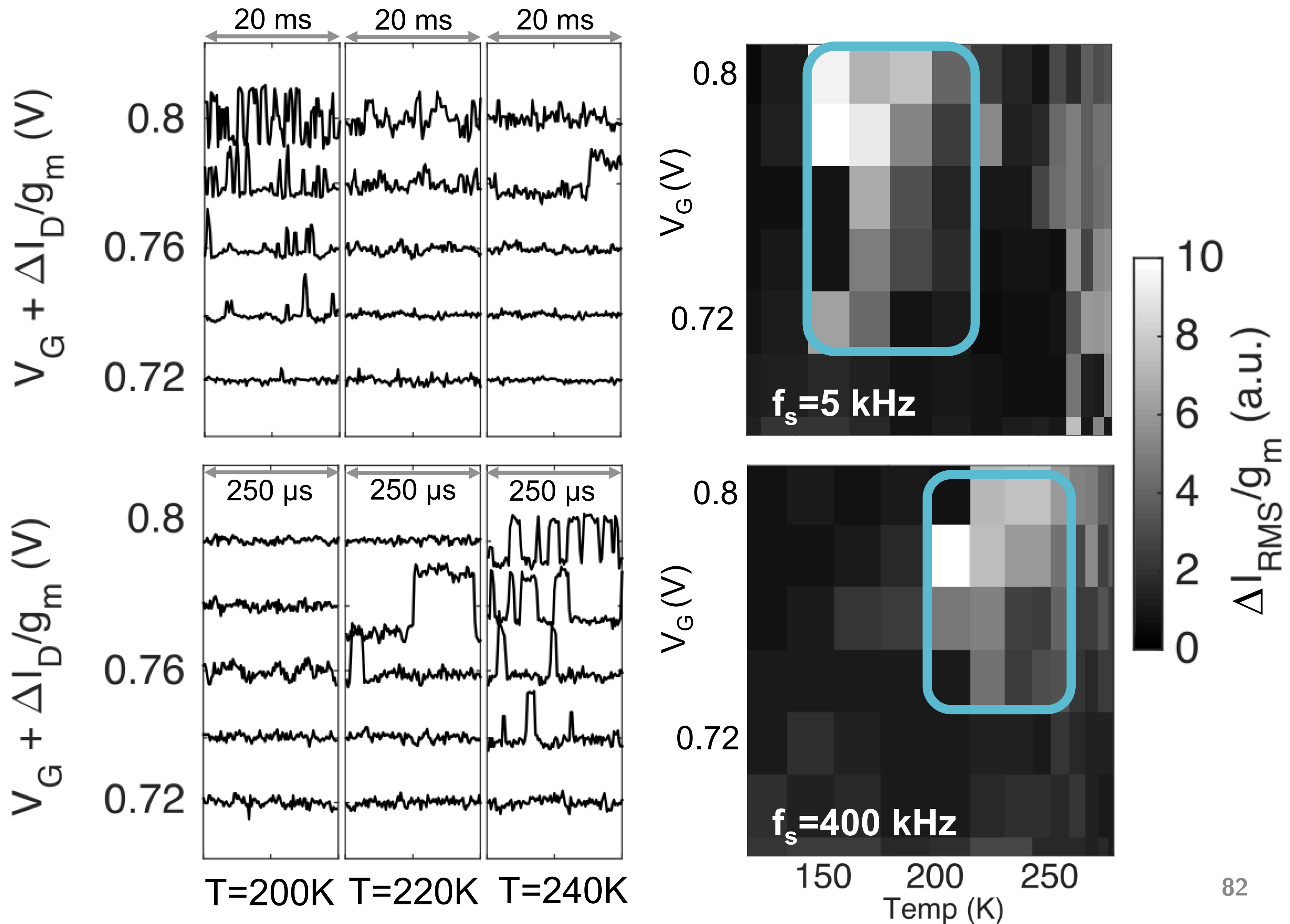
T=200K T=220K **T=240K**



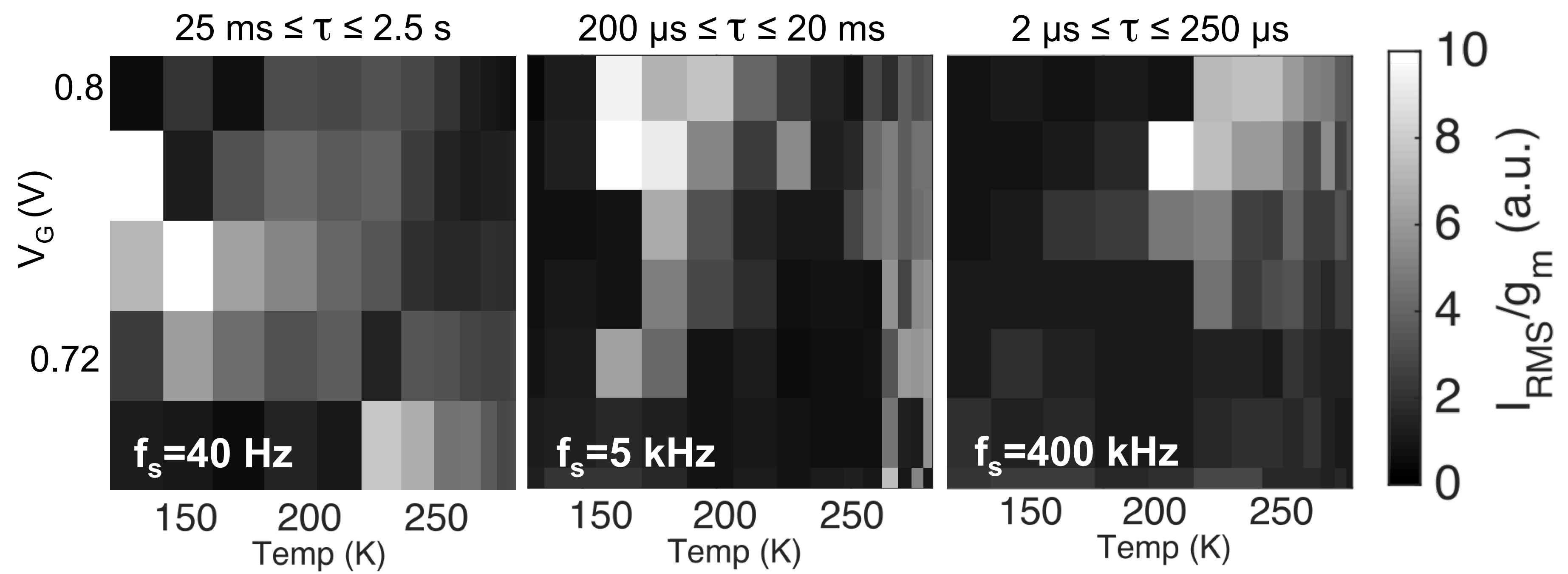
Results: RTN Characterization



Results: RTN Characterization

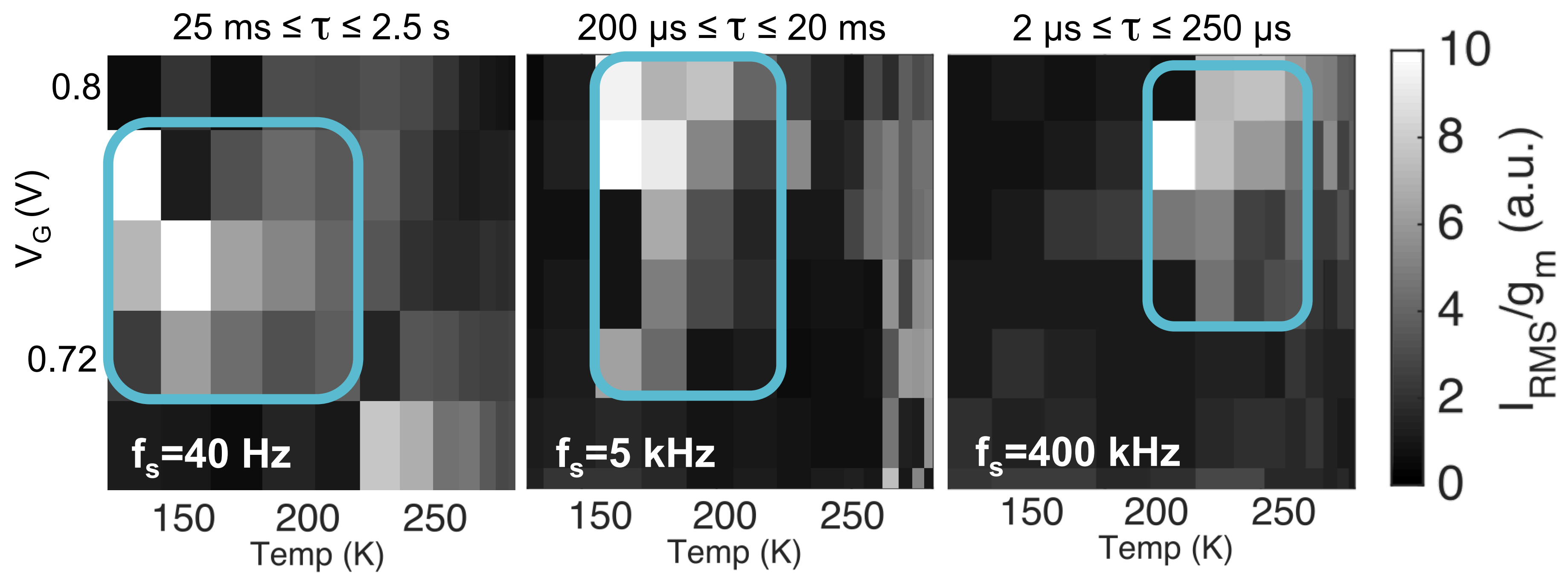


Results: RTN Characterization



Two RTN traps active at different biases and temperatures are evident

Results: RTN Characterization



Two RTN traps active at different biases
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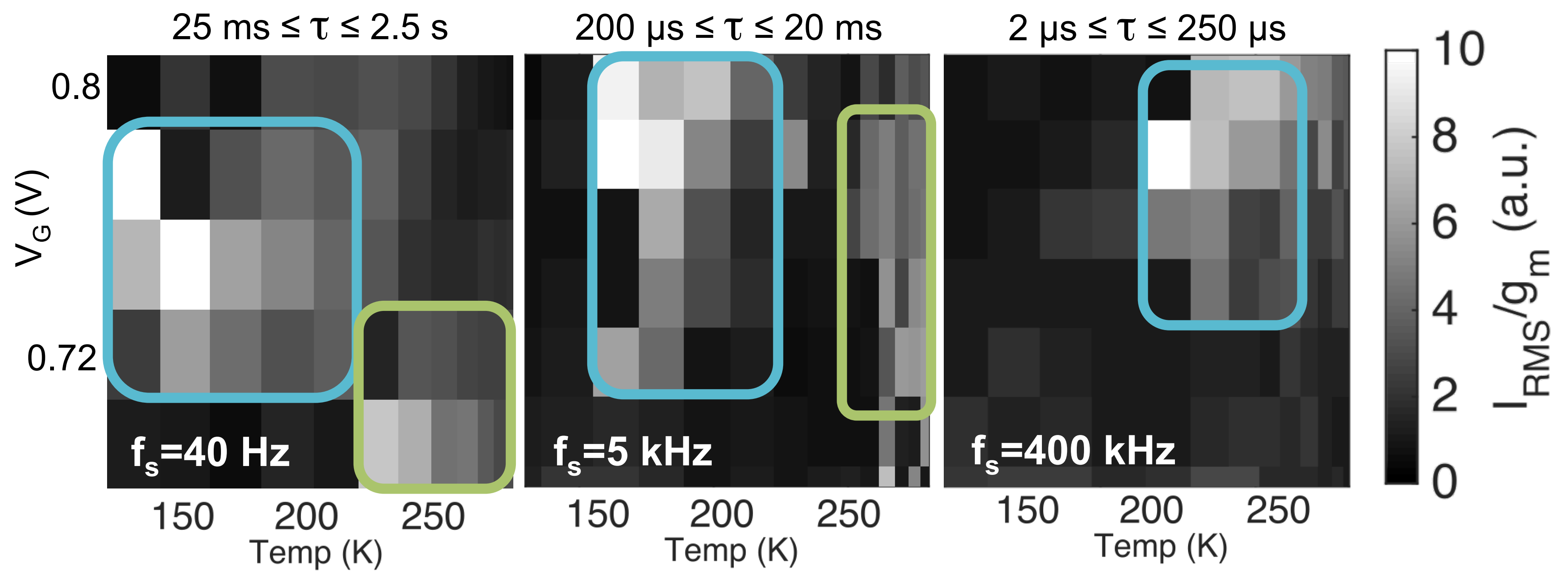
Results: RTN Characterization



Two RTN traps active at different biases and temperatures are evident

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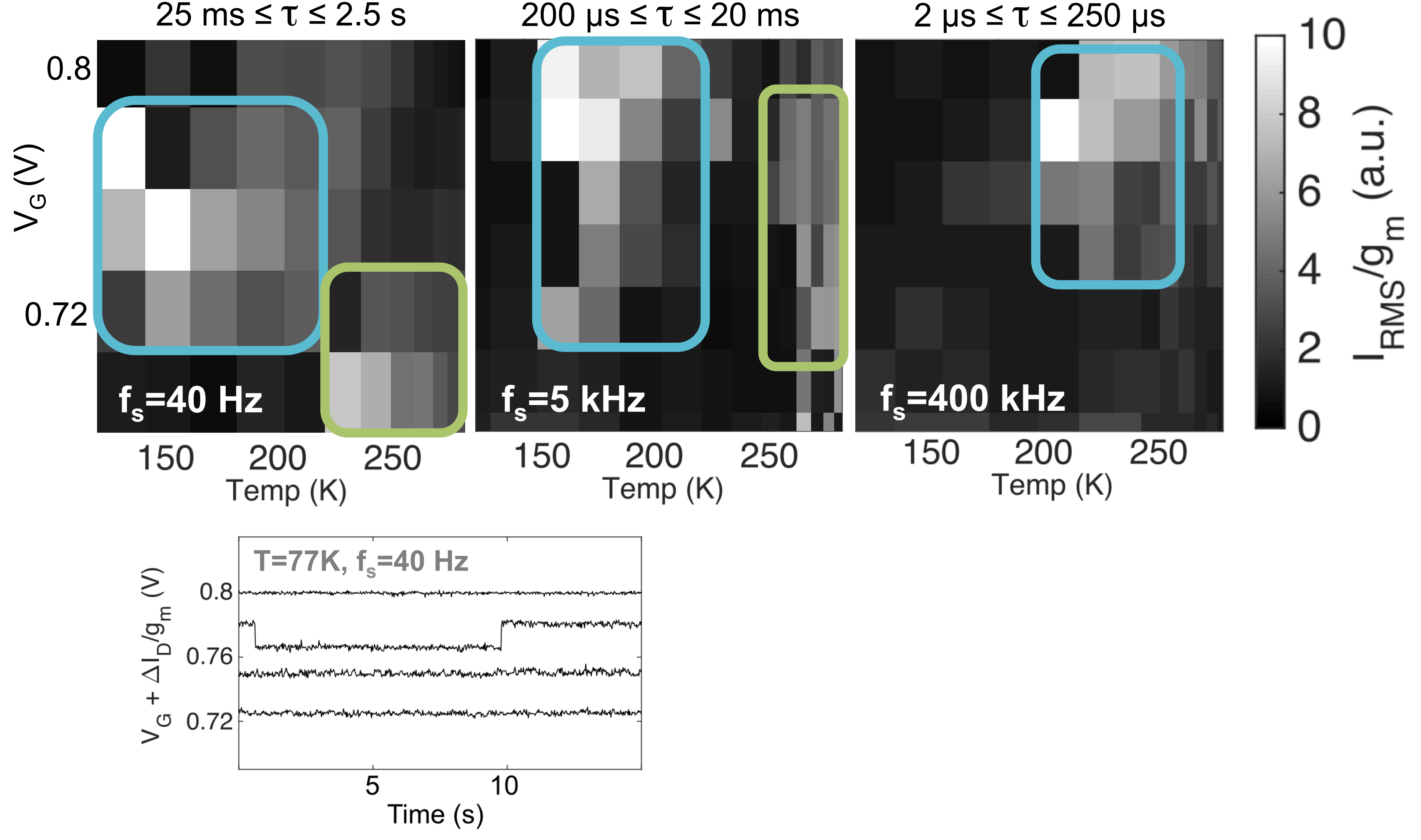
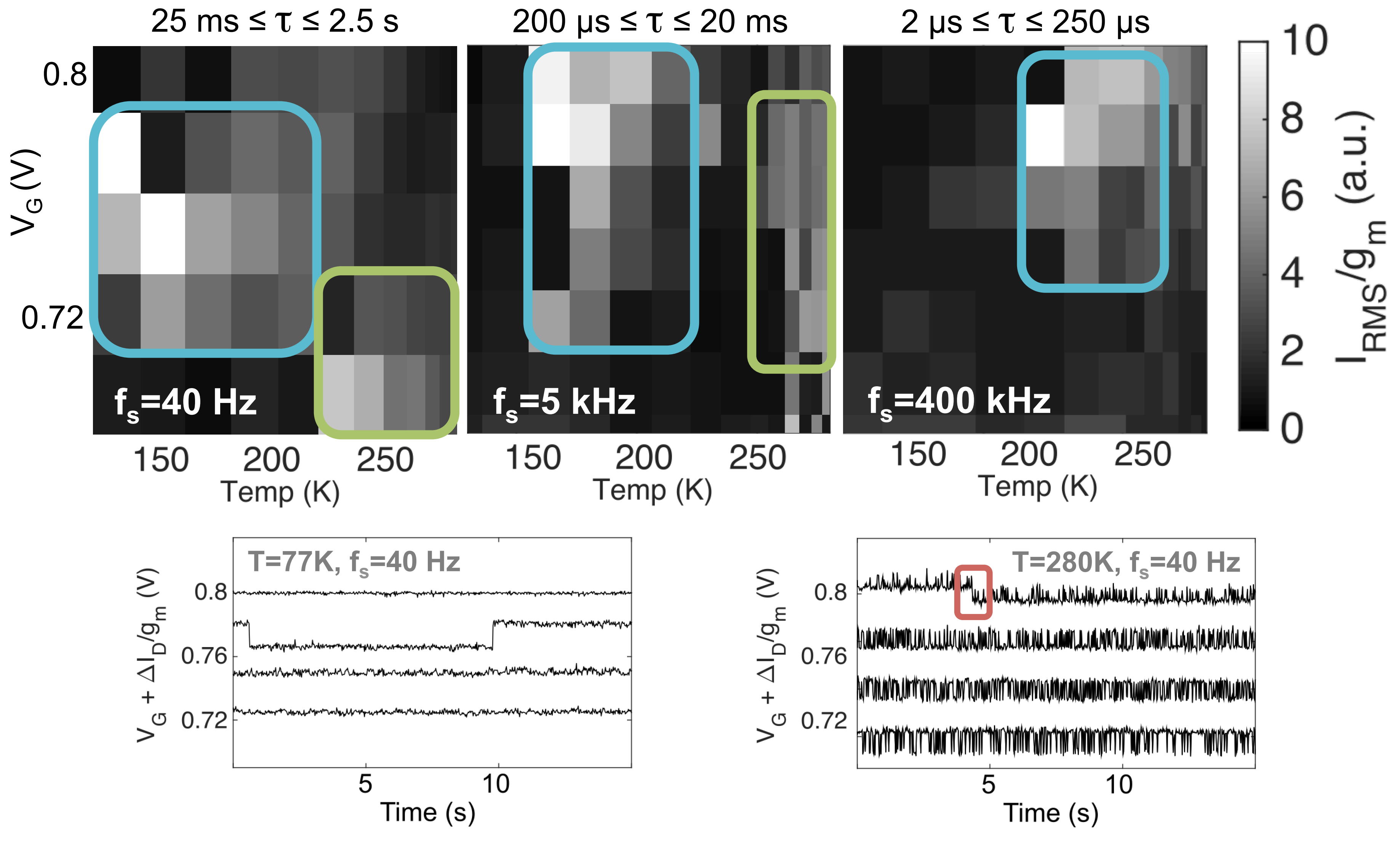


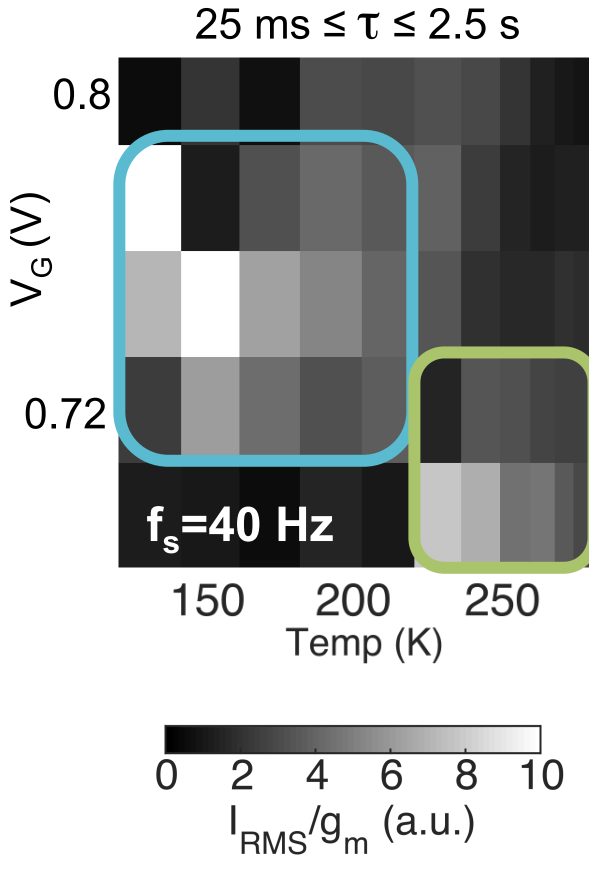
RTN is evident even at cryogenic temperatures

Results: RTN Characterization

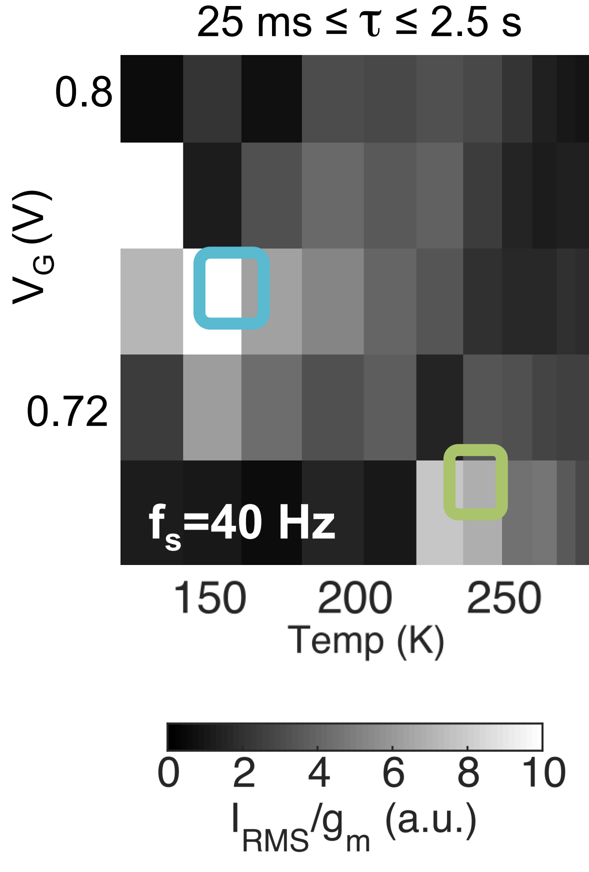


Longer 280 K sample shows third trap

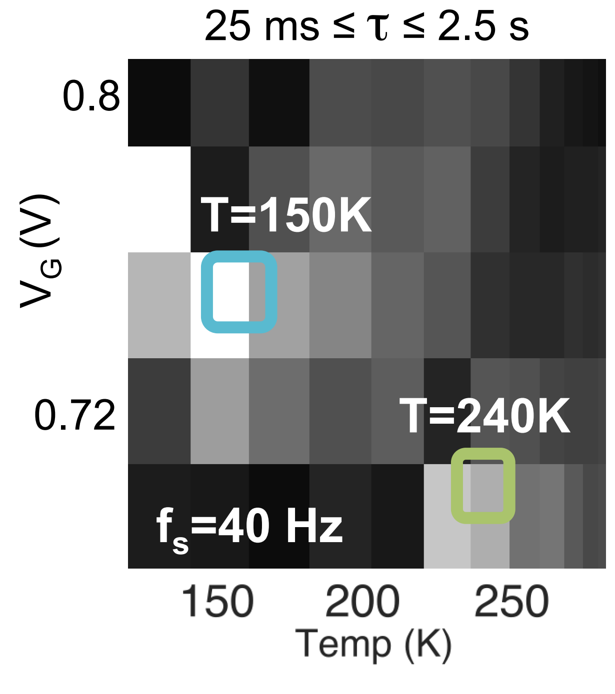
Results: RTN Characterization

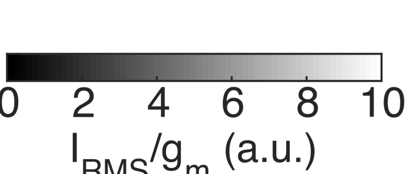


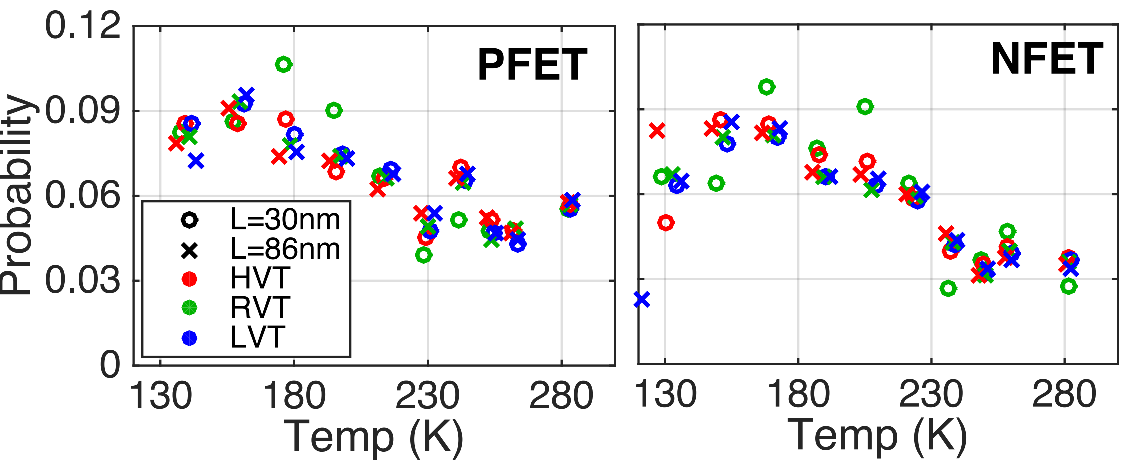
Results: RTN Characterization



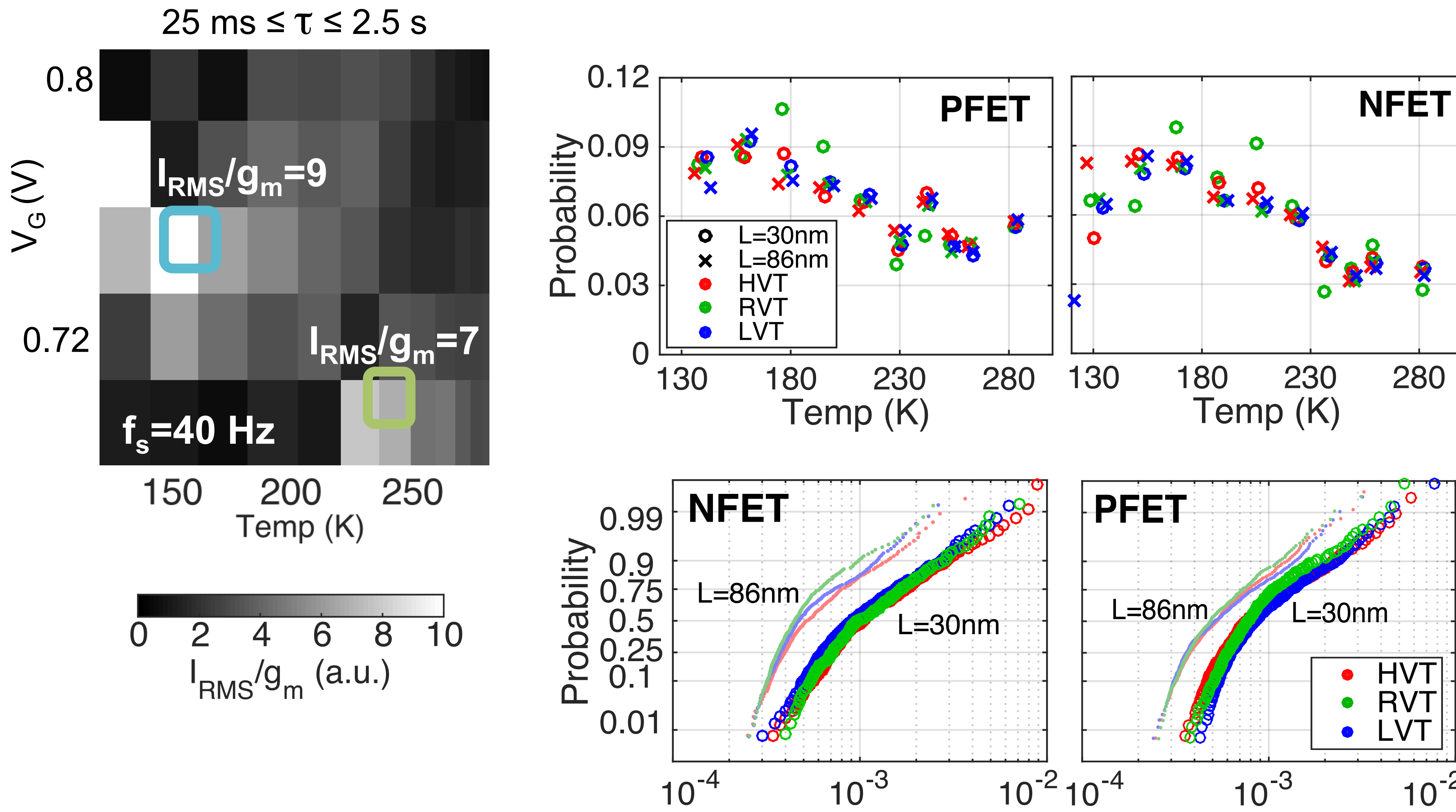
Results: RTN Characterization



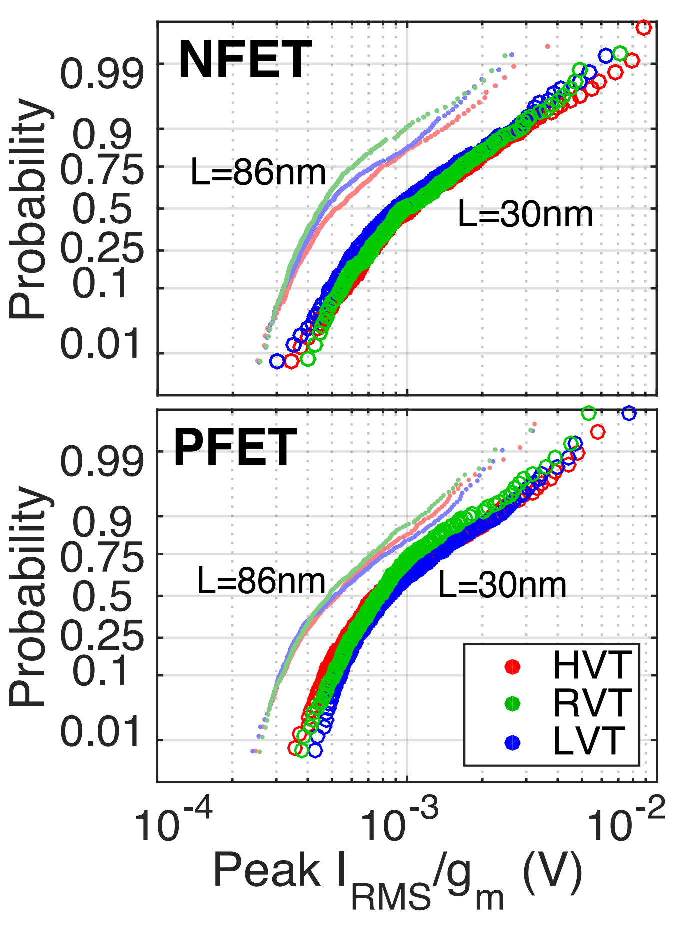




Results: RTN Characterization

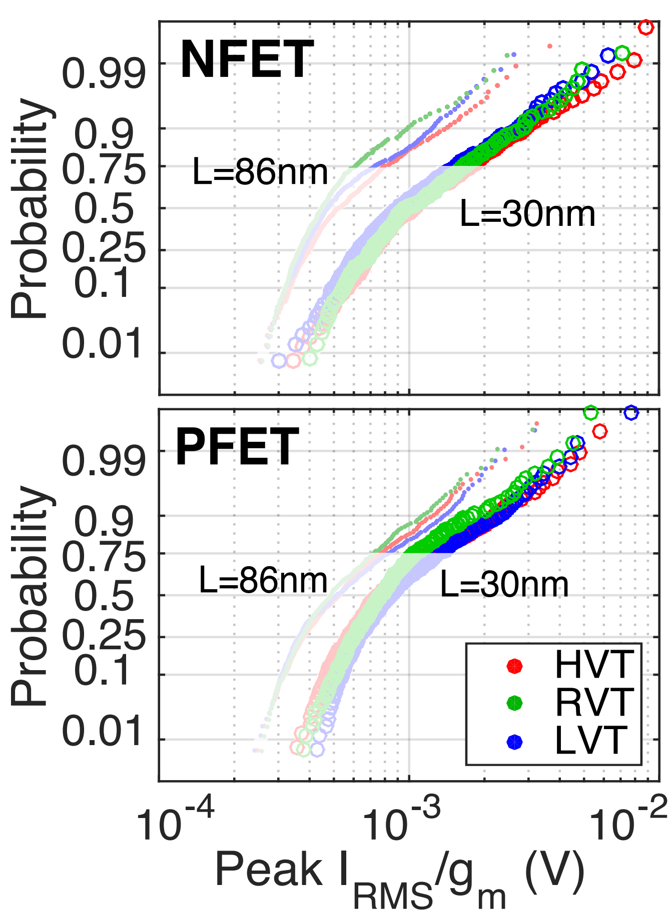


Results: RTN Characterization



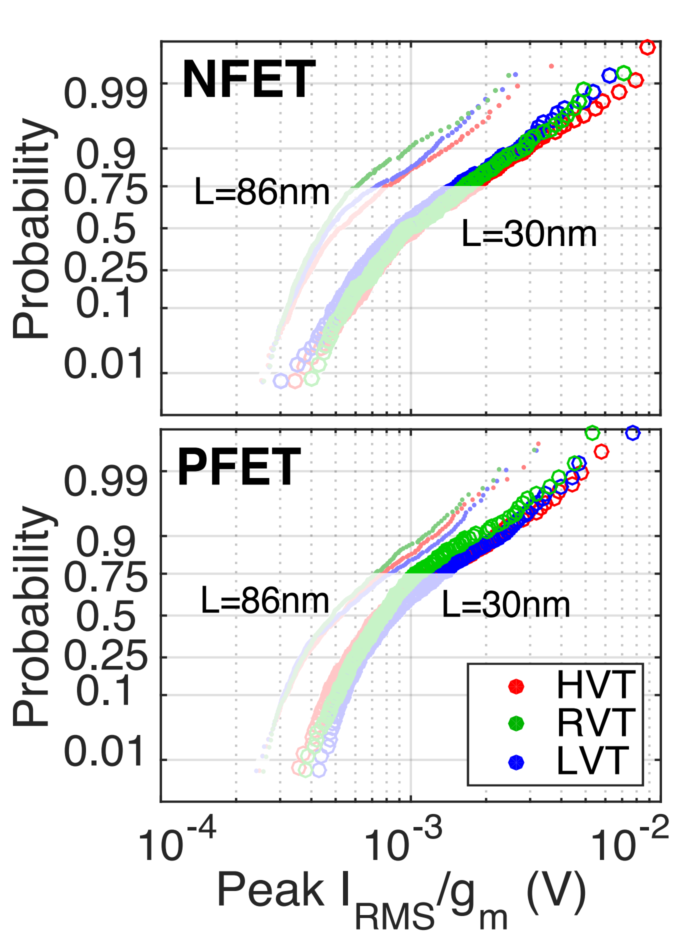
- Larger RTN with smaller channel length
- NFET RTN amplitudes are typically larger
- Doping level has little consistent effect

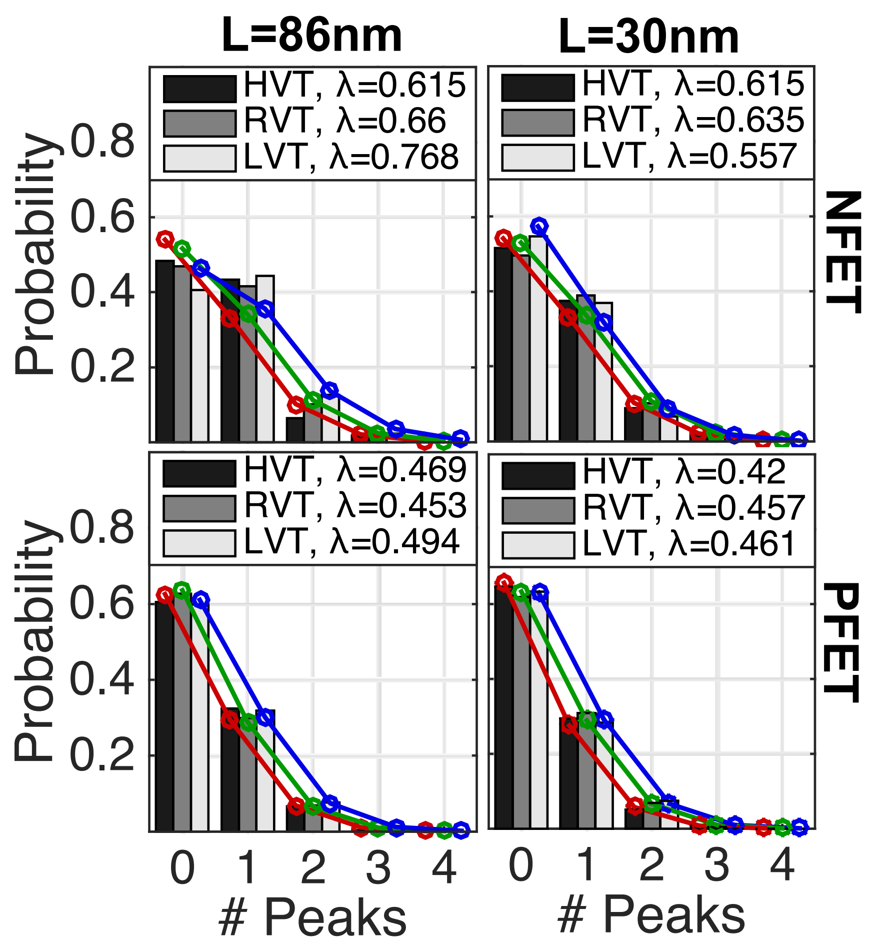
Results: RTN Characterization



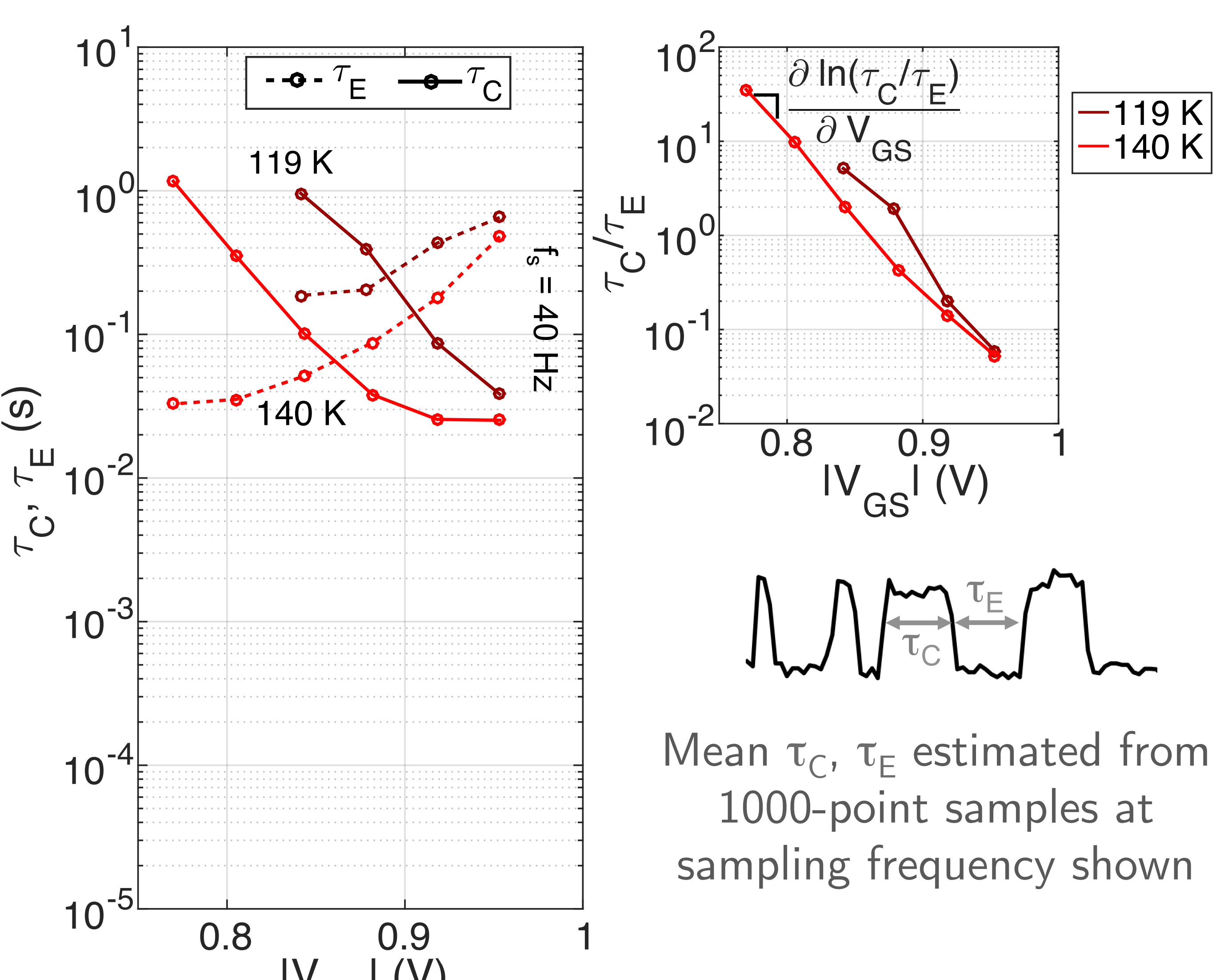
High I_{RMS}/g_m levels correspond to device RTN, not detector noise

Results: RTN Characterization



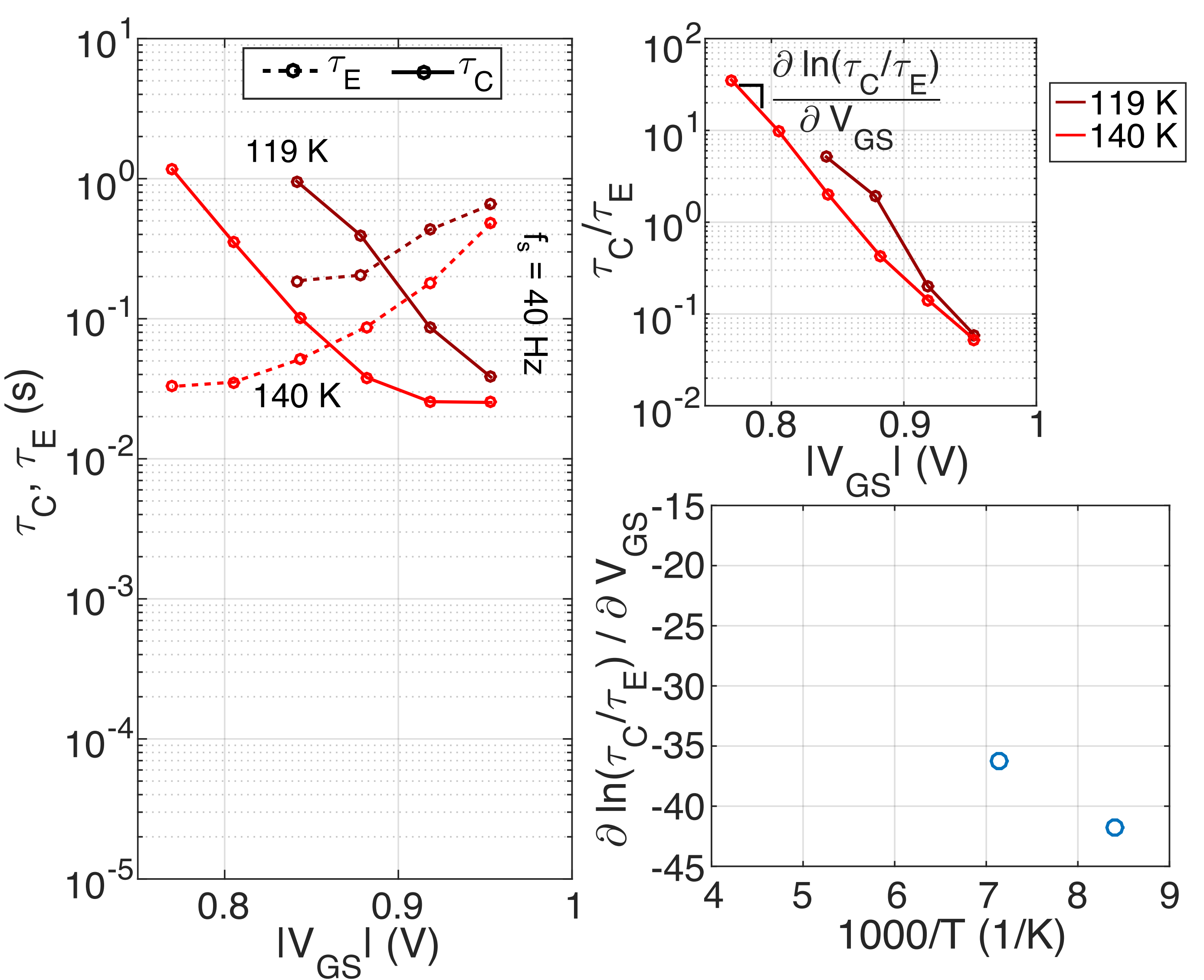


Results: RTN Characterization

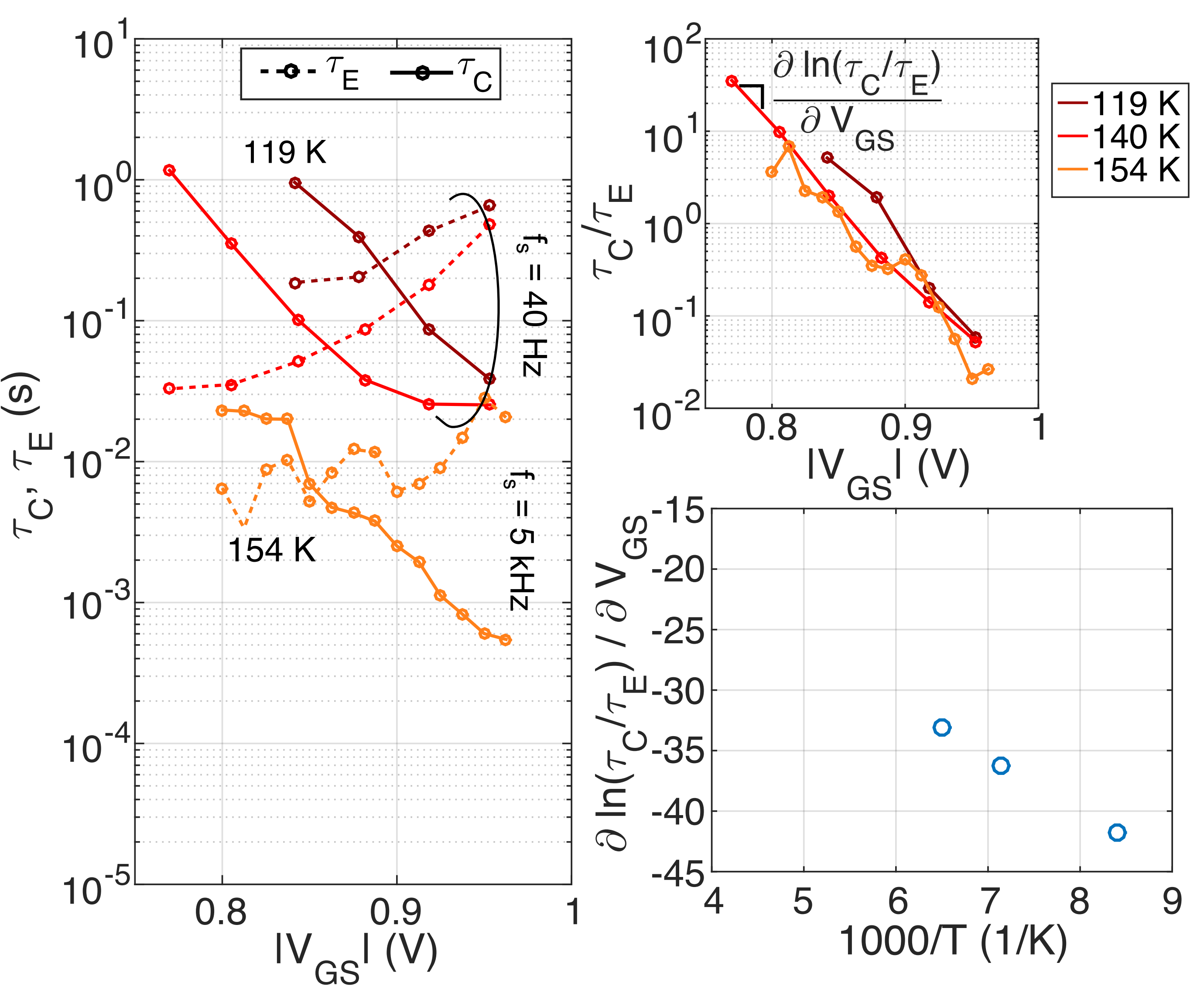


Mean τ_C, τ_E estimated from 1000-point samples at sampling frequency shown

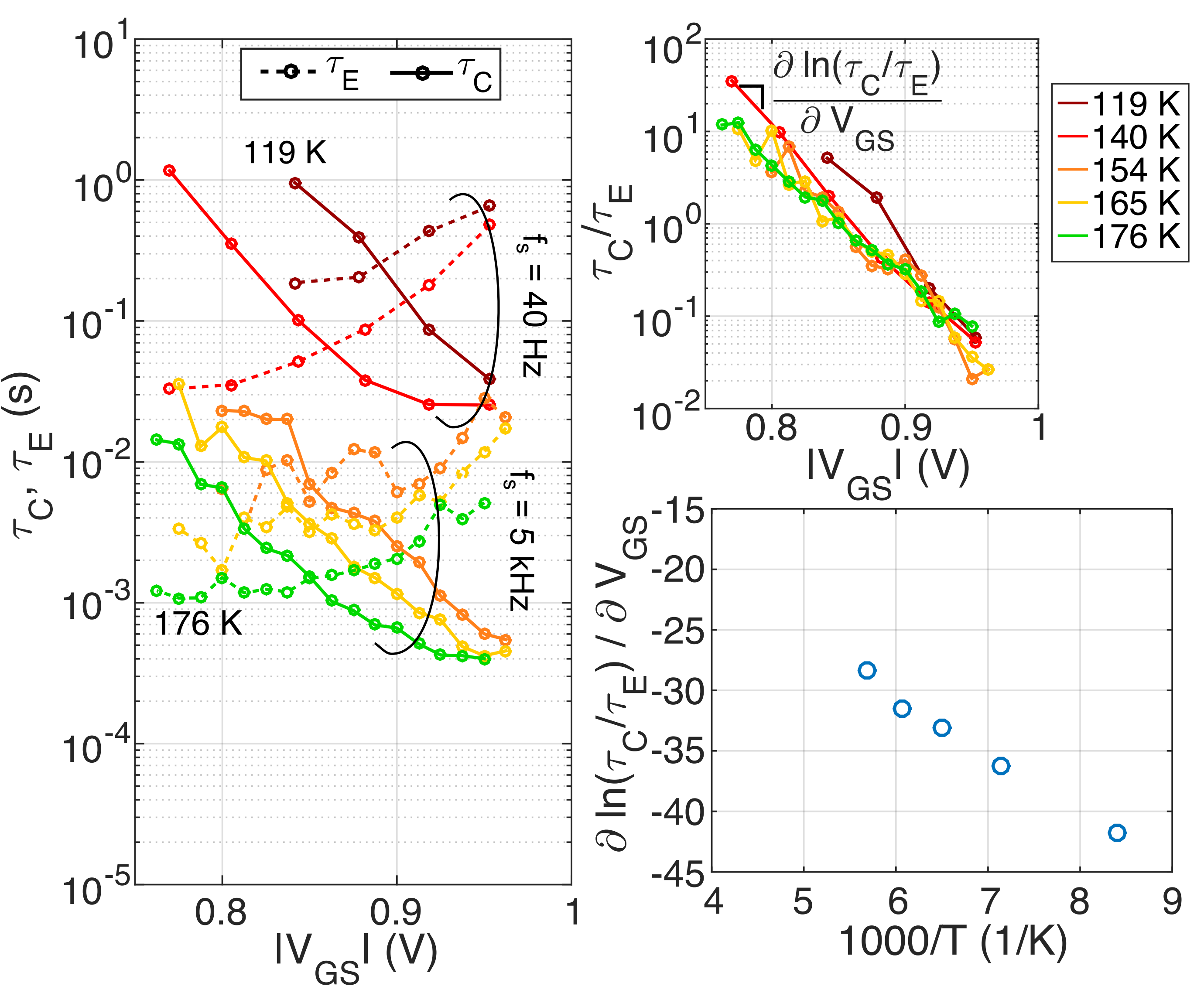
Results: RTN Characterization



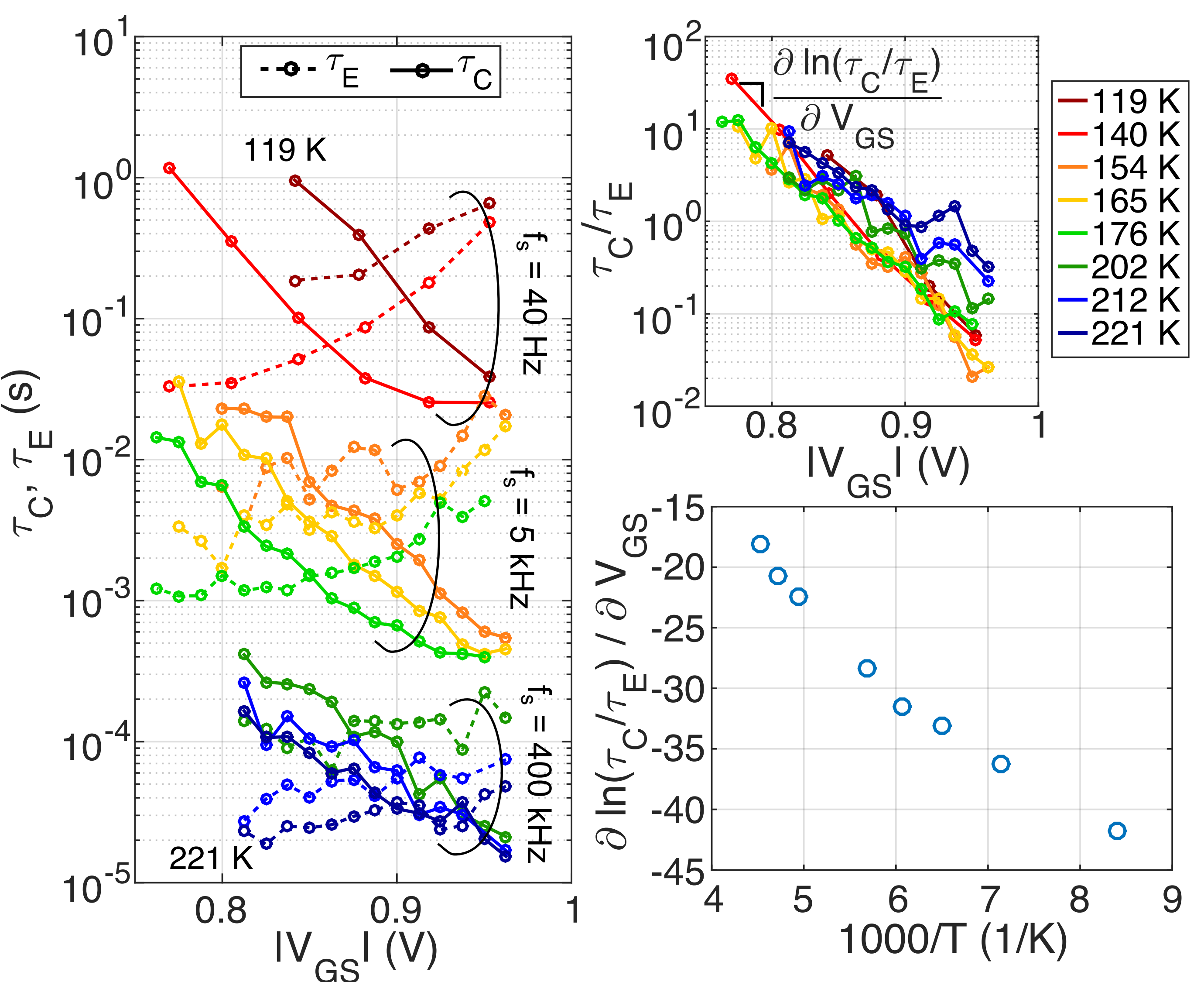
Results: RTN Characterization



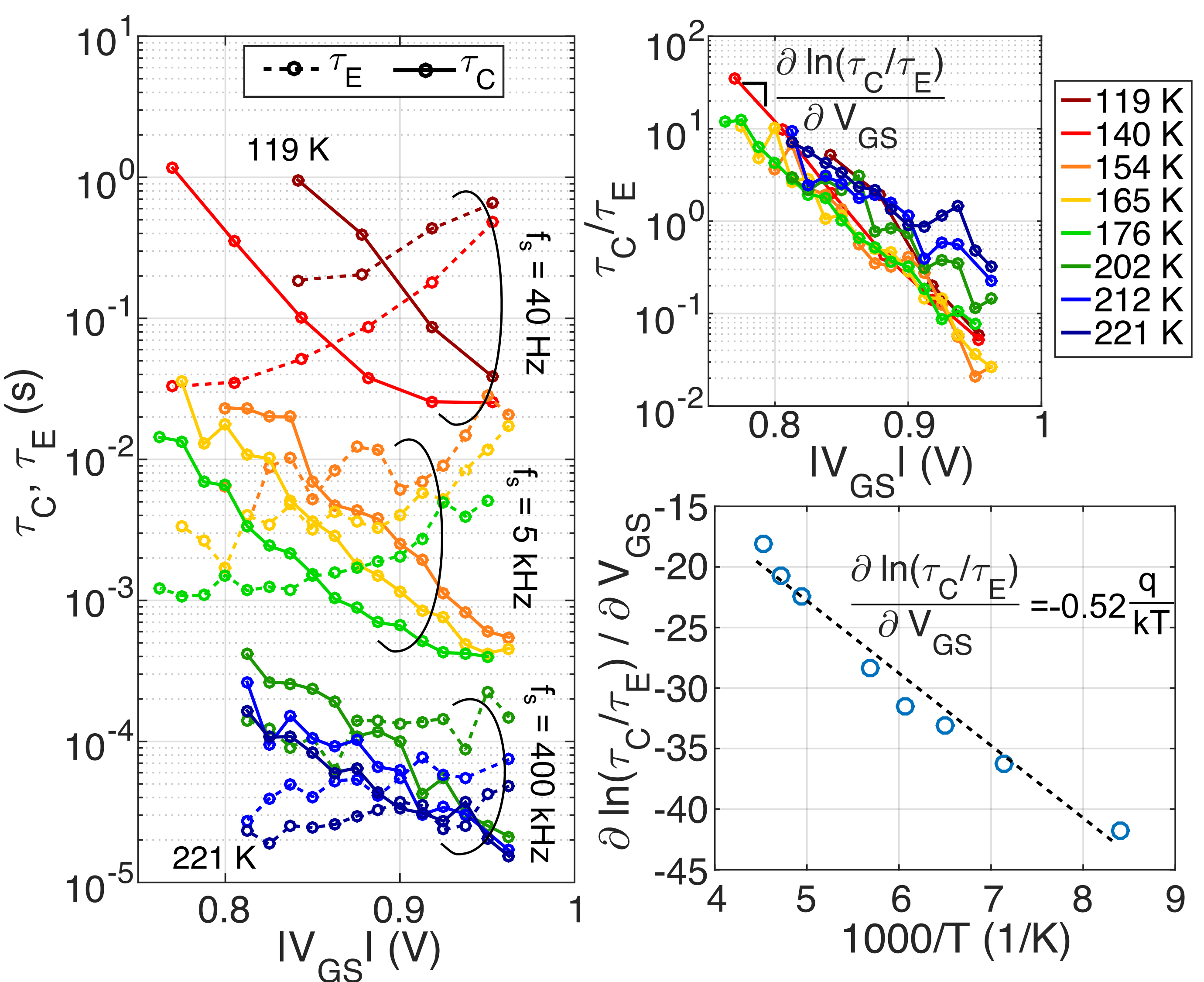
Results: RTN Characterization



Results: RTN Characterization



Results: RTN Characterization



Outline

- Background & motivation
- Prior art comparison
- Proposed design
- Test chip results
- **Conclusions**

Conclusions

- Conventional CMOS readout IC platform can be modified for device characterization purposes
- Compact array incorporates >80,000 HKMG test devices; subset of 6,000 devices measured across V_G down to cryogenic temperatures
- Measurements support previous studies of RTN bias and temperature dependence
- Complete RTN measurements require high dynamic range, fast sampling capabilities
- Array enables highly parallel subthreshold current detection and detects RTN time constants under 10 μs

Acknowledgements

- This work was supported in part by the Intelligence Advanced Research Projects Activity (IARPA) via the Space and Naval Warfare Systems Command (SPAWAR) contract number N66001-12-C-2010, the NDSEG fellowship, and the BWRC.
- The authors also thank Bruce Bozovich, Mike Jack, Dave Madajian, Eileen Herrin, Chris Tracy, Henry Lee, Roya Mokhtari, Adam Kennedy, Eric Beuville, Tsu-Jae Liu, Dan Connelly, Ana Arias' group, and the UCB Nanolab for support.

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[2] R. Kuroda et al., "A statistical evaluation of random telegraph noise of in-pixel source follower equivalent surface and buried channel transistors," *IEEE Trans. on Elec. Devices,* vol. 60, no. 10, pp. 3555-3561, Aug. 2013.

[3] H. Qiu et al., "Impact of random telegraph noise on write stability in Silicon-on-Thin-BOX (SOTB) SRAM cells at low supply voltage in sub-0.4V regime," *VLSI Technology*, June 2015.

[4] Q. Tang and C. Kim, "Assessing the impact of RTN on logic timing margin using a 32 nm dual ring oscillator array," *IEDM*, Dec. 2015.

[5] S. Realov and K. Shepard, "Analysis of random telegraph noise in 45-nm CMOS using on-chip characterization system," *IEEE Trans. on Elec. Devices*, vol. 60, no. 5, pp. 1716-1722, May 2013.

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[7] A. Yonezawa et al., "The study of time constant analysis in random telegraph noise at the subthreshold voltage region," *IRPS*, April 2013.

[8] M. Giles et al., "High sigma measurement of random threshold vatiation in 14nm logic FinFET technology," *VLSI Technology*, June 2015.