

Tracking and Vertexing Summary

A. Sugiyama (Saga Univ.)

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Vertex detectors
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Friday, March 10

Development of DEPFETs for the Vertex Detector

(Ladislav Andricek)

CMOS Monolithic Pixel R&D at LBNL

(Devis Contarato)

Monolithic CMOS Pixel Detectors for ILC Vertex Detection

(James Brau)

Development of CMOS sensors adapted to the vertex detector requirements

(Marc Winter)

Saturday, March 11

LCFI Status Report: Sensors for ILC Vertex Detector

(Konstantin Stefanov)

Investigation in the Properties of Charge Traps Created in CCD by Neutron and Electron Irradiation

(Nikolai Sinev)

Vertex Performance Study with a Realistic Pattern Recognition Algorithm

(Alexei Raspereza)

LCFI Vertex Detector Design Studies

(Andre SOPCZAK)

=====
Solid-state tracking
=====

Sunday, March 12

SiD Vertex Detector Mechanical Design

(Bill Cooper)

LCFI Status Report: Physics and Mechanics for ILC Vertex Detector

(Steve D. Worm)

Status on the development of FE and readout electronics for Large Silicon Trackers

(Jean-Francois Genat)

SiLC R&D present status and perspectives

(Aurore Savoy-Navarro)

Silicon Strip R&D Status in Korea

(Hwanbae Park)

5 sessions

10 talks for Vertex

3 talks for Si Tracker

8 talks for TPC

=====
Gaseous tracking
=====

Sunday, March 12

Large-Area Micromegas TPC R&D

(Michael T. Ronan)

Comparison between data and simulation for MT3

Studies on the Drift Properties and Spatial Resolution Using a

Micromegas-Equipped TPC

(Rosario L. Reserva)

A beam test of prototype TPCs using micro-pattern gas detectors at KEK

(Makoto Kobayashi)

Micromegas- and GEM-TPC resolution studies with charge

dispersion in a magnetic field in a test beam.

(Madhu Dixit)

Monday, March 13

ILC TPC R&D studies at DESY/U. Hamburg

(Katsumasa Ikematsu)

Developments for a digital TPC : the SiTPC project

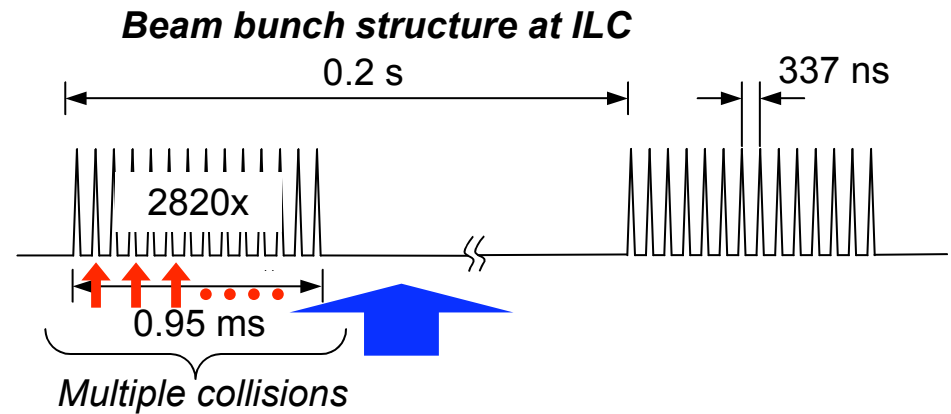
(Paul Colas)

TPC R&D Plans for the Large Prototype

(Ron Settles)

Brief Introduction of Vetex to "non-expert(myself)"

required point resolution ~ a few μm
low material < 0.5% X_0
Occupancy < 1%



Key issue of R&D

Bkg. hits exceed "occupancy limit"
after ~3000BX(1 train) w/ standard 20 μm pixel

- Solution: 1) read data before Occ. exceed limit (20 times/train)
can we read all data within 50 μs ? Column parallel CCD, CMOS, DEPFET
- 2) store data and reset sensor(20 depth in storage)
can we store data? read all data (within 199msec). ISIS, Macro/Micro
make pixel size small(20 times smaller in area; 5 μm pixel) can we make? FPCCD

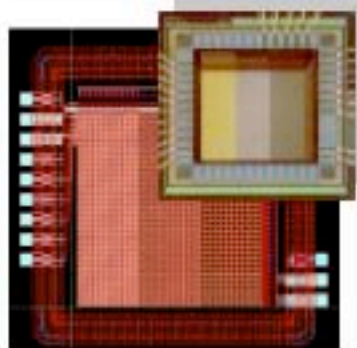
"Proof of Principle"

with reasonably low power dissipation,
high S/N,
low material (thinning) ,
tough rad. hardness
away from RF pick-up

many more things
mechanical design, support, cooling
Optimization under physics benchmark
Software development

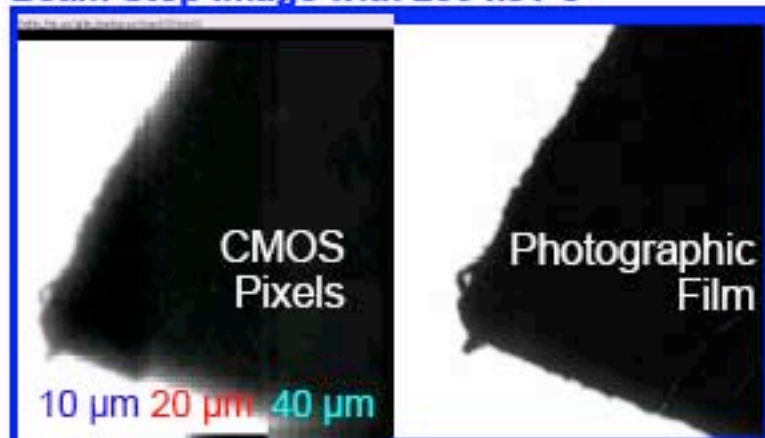
CMOS Monolithic Pixels R&D at LBNL

Devis Contarato

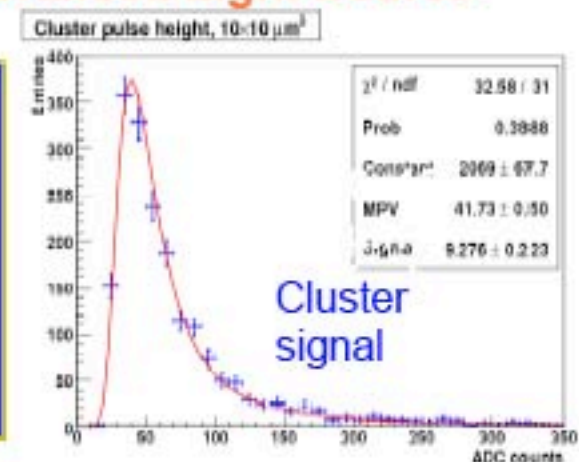
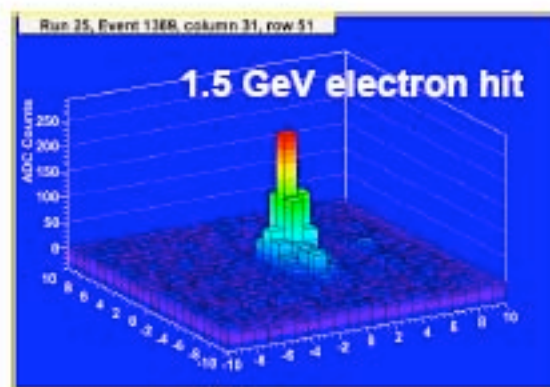


- Developed and characterized first CMOS pixel test structure in 0.35 μm OPTO AMS, with different pixel pitches (10, 20, 40 μm)
- Availability of facilities on-site: electron microscopy @ NCEM, beam-test with 1.5 GeV e^- at Advanced Light Source, 30 MeV proton irradiations at 88-inch Cyclotron
- Synergy with other on-going activities on CMOS pixels at LBNL

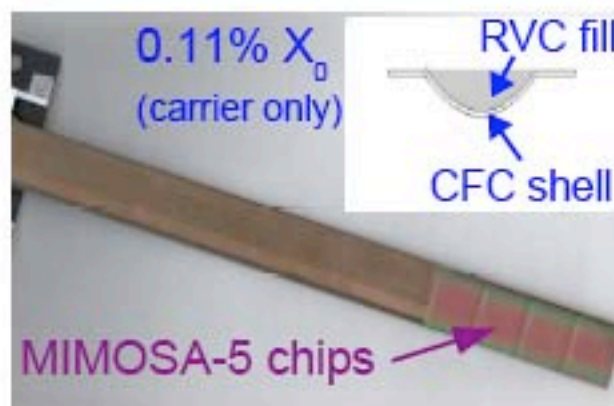
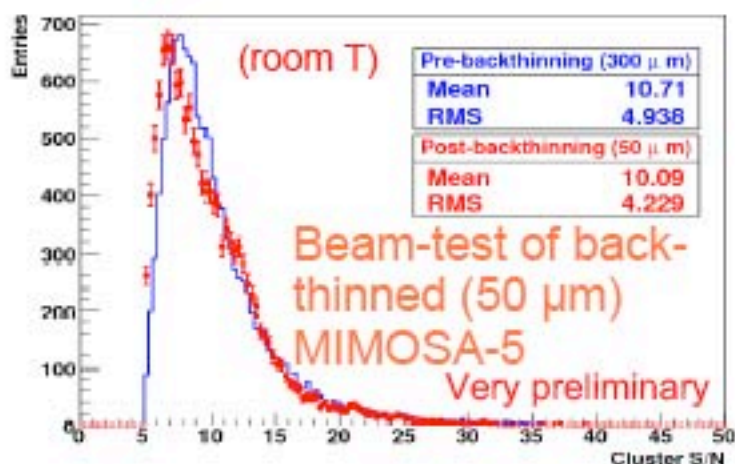
Beam Stop Image with 200 keV e^-



Beam-test at the Advanced Light Source



Cluster S/N comparison



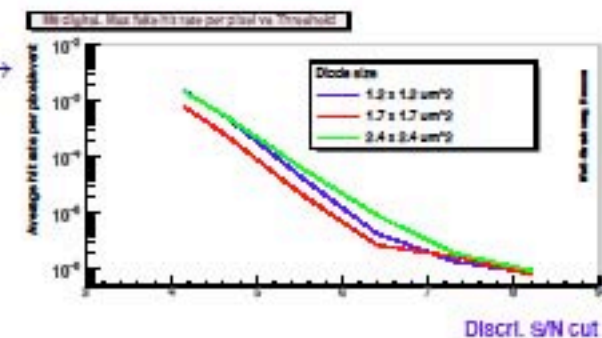
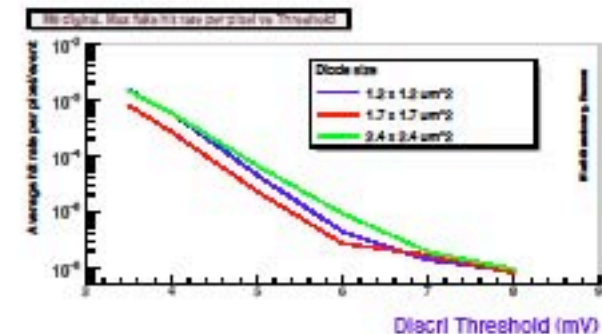
- Backthinning studies on MIMOSA-5 and pixel ladder prototype development (for STAR VXD upgrade)

2 sensor architectures developed:

- fast column parallel architecture for L1 ($25 \mu s$) and L2 ($50 \mu s$)
- multi-memory pixel architecture with delayed read-out (FAPS) for L3–5

Recent progress:

- prototype with integrated signal discrimination tested on beam (DESY):
 $50 \mu s$ read-out time, $N \lesssim 15 e^-$, detection eff. $\sim 99.3\%$, 10^{-3} fake hits \rightarrow
- prototype with radiation tolerant pixel validated at room temperature
 for doses up to 1 MRad (20 kRad/yr expected from e^{\pm}_{BS})



* Next important steps \rightarrow evolve the fast column parallel architecture:

- ◇ translate in micro-circuit technology offering high S/N
- ◇ improve speed
- ◇ make pixels radiation tolerant at room temperature
- ◇ replace discriminator by ADC

* Other on-going activities:

- ◇ try accommodating FAPS to L2
- ◇ try thinning to $\sim 35 \mu m$
- ◇ test 2 ladders equipped with prototype sensors in STAR DAQ
- ◇ design and fabricate sensors for STAR vertex detector upgrade and for equipping EUDET beam telescope

Monolithic CMOS pixel Detector for ILC Vertex

J. Brau

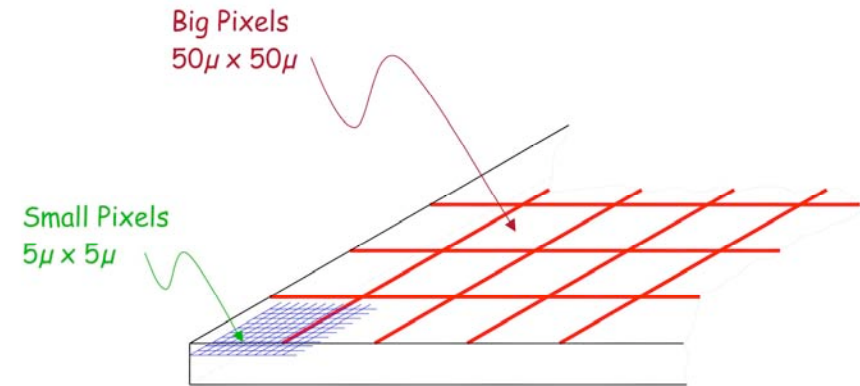
Monolithic CMOS Pixel Detectors

Macro	/	Micro
(50um pitch	/	5um pitch)
high speed(timing)	/	precise position

New approach

Macro only w/ 10-15 um pitch

much more tolerant to high background



Two active particle sensitive layers:

Big Pixels - High Speed Array	- Hit trigger, time of hit
Small Pixels - High Resolution Array	- Precise x,y position, intensity

Readout

22mmx 125mm chip

-> 176msec @50MHz

parallel readout ?

Read Noise

Signal to noise of 10 to 20

Power Consumption

~4mW/cm²

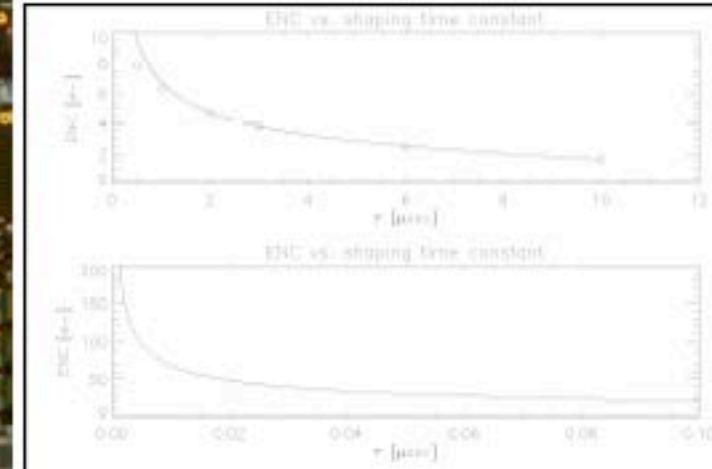
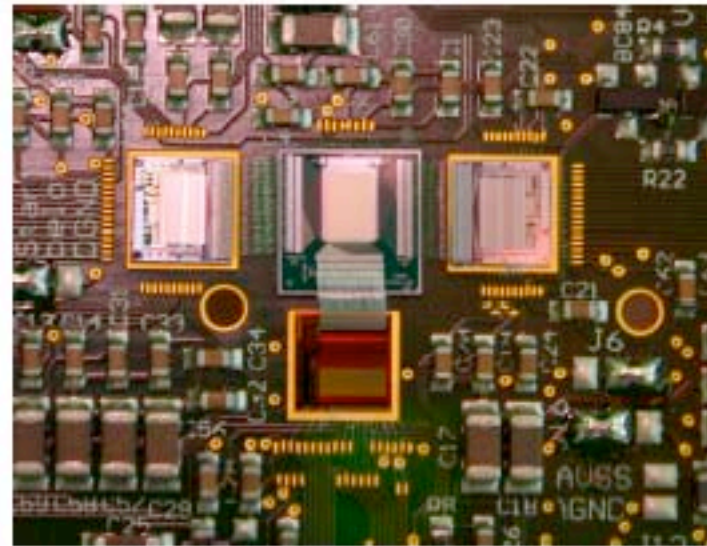
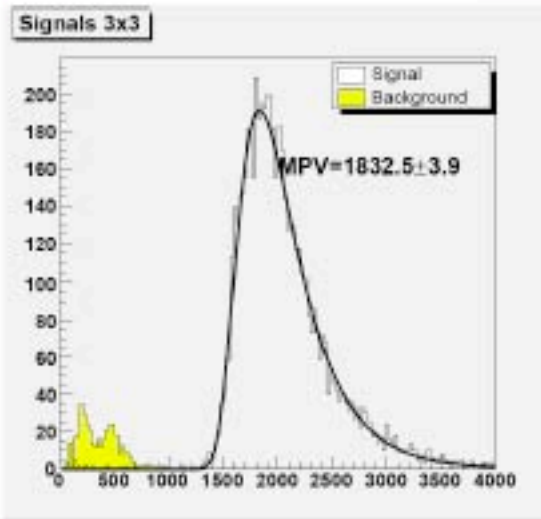
Macro pixel design is completed

DEPFET Development

Laci Andricek



64x128 pixel DEPFET matrix, cellsize 36 x 24 μm^2



New system in beam test at DESY:

- f/e Bandwidth and Clock: 50 Mhz
 - $\sim 6 \mu\text{s}/\text{row}$ with full data transf. to PC
 - Sample-clear-sample: $\sim 240 \text{ ns}$
 - Clear duration 20 ns
- $S/N \approx 111$ for 450 μm sensor

Single pixel tests pre and post irradi.

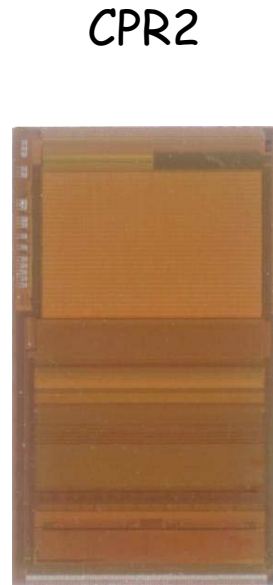
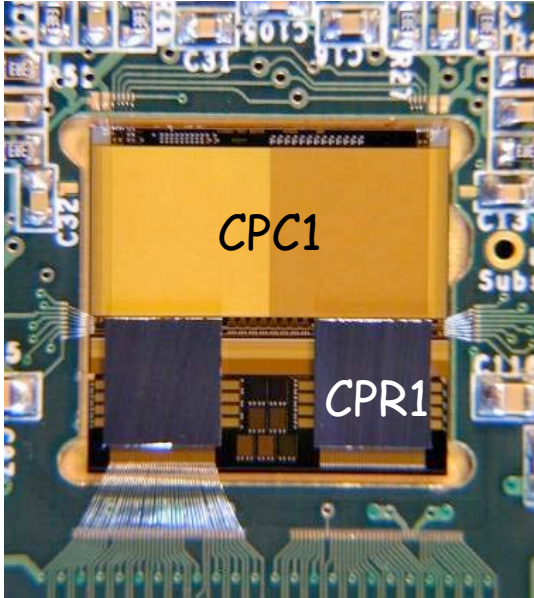
with 1 Mrad:

→ DEPFET noise in the 50 MHz range: ENC ≈ 50 electrons

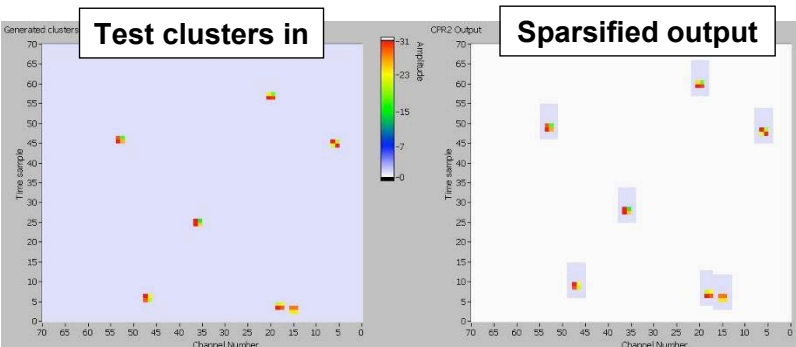
2006: new sensor production, new submissions for r/o chip CURO and SWITCHER

LCFI Status Report: Sensors for the ILC Konstantin Stefanov

Column Parallel CCD + CMOS readout
CPC1(400x750: 20um) CPR1



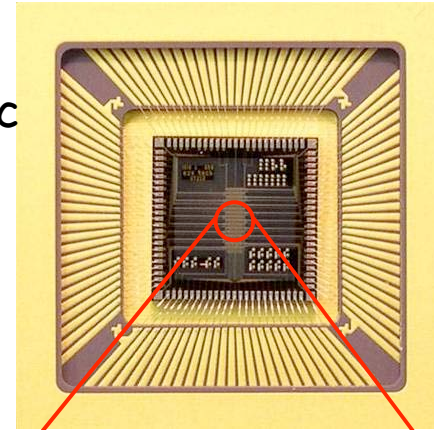
CPR1 +
Cluster Finding
Sparse Readout



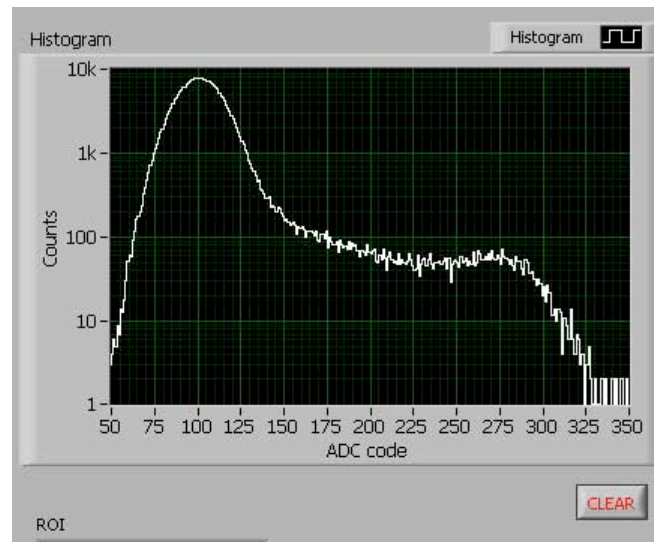
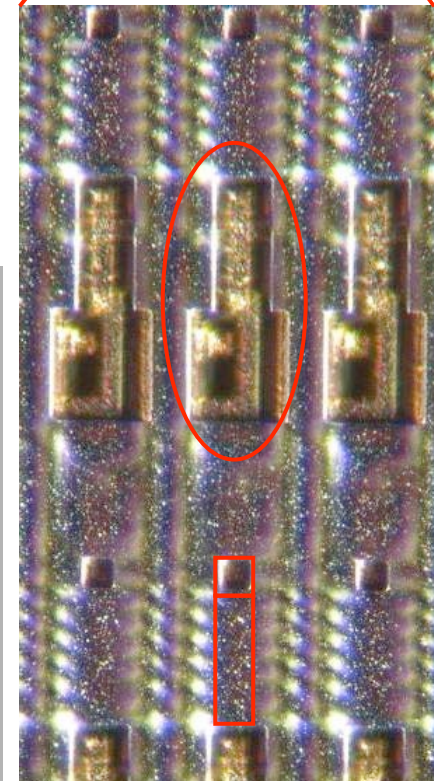
ISIS(In-situ Storage Image Sensor)
charges are stored in 20-pixel storage

1MHz column parallel ro
is enough within 200msec

RF pickup is avoidable



Source Test w/ Fe55



Investigation into properties of neutron and electron irradiated CCD

Charge traps are produced by neutron irradiation

Study of traps

charge retention time by traps

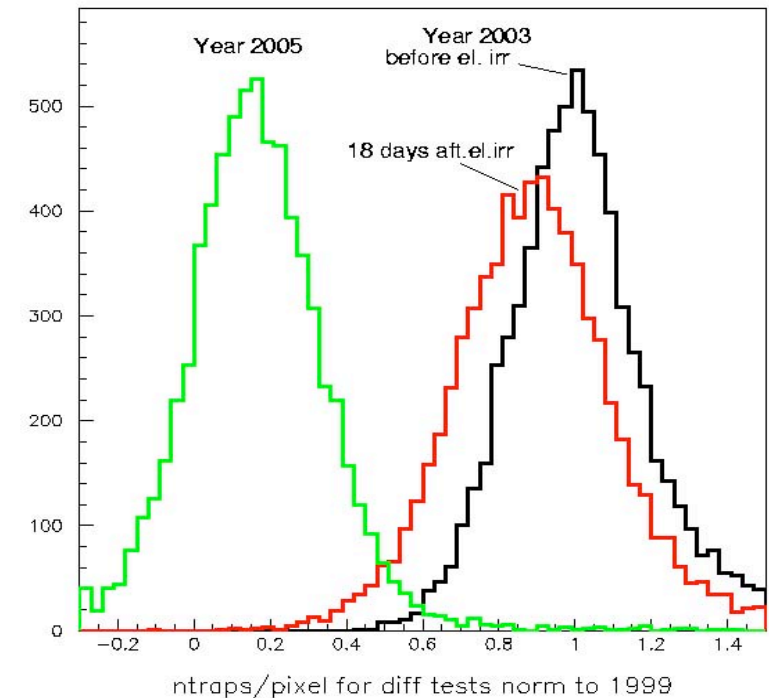
annealing

Charge Transfer Inefficiency

PUZZLE

electron capture to traps takes long $O(\text{msec})$
though $O(\text{nsec})$ is expected.

After irradiation of electrons
all traps disappeared



Alexei Raspereza

Simulation Studies of VXD Performance

Detector optimization has been started using
full simulator and realistic reconstruction program.

Mokka

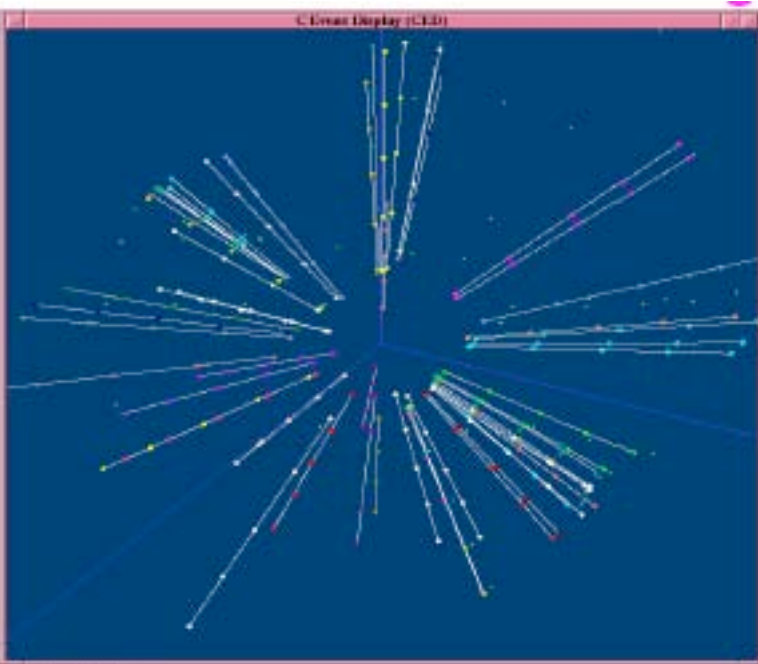
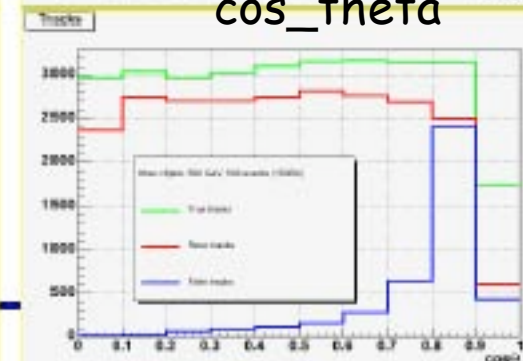
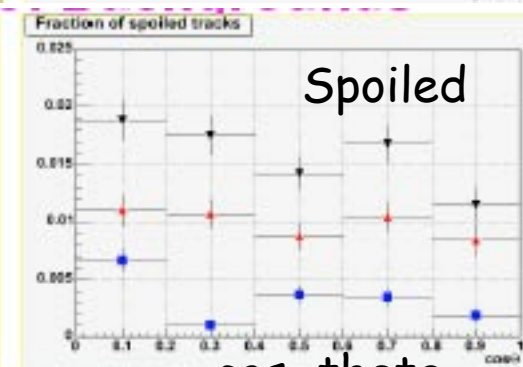
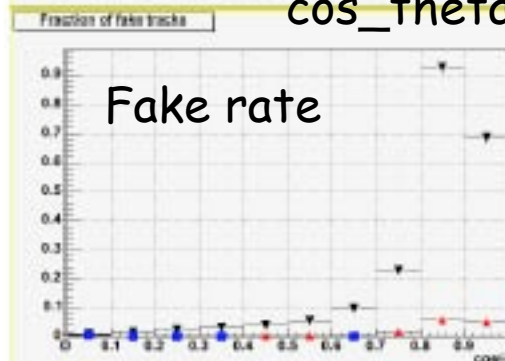
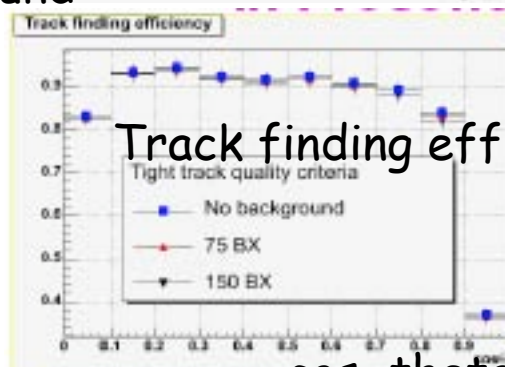
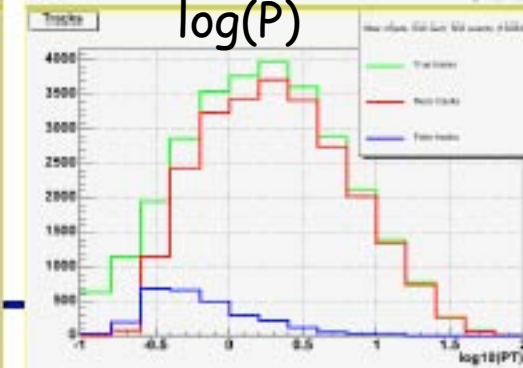
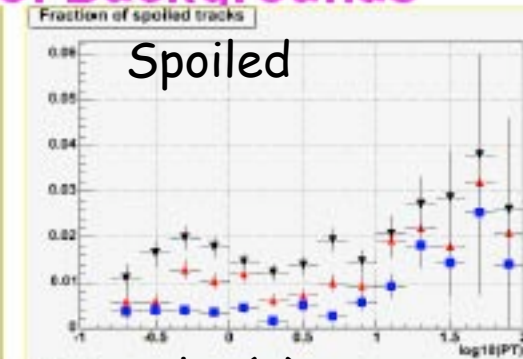
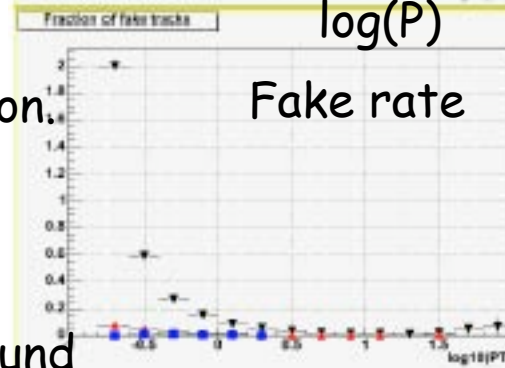
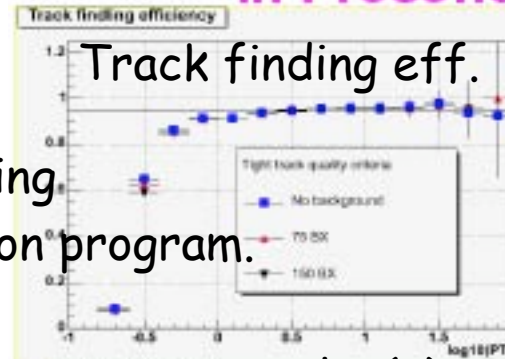
MARLIN

w/VXD,TPC,FT
Ecal, Hcal, Fcal

implement VXD
digitization + recon.

$t\bar{t} \rightarrow 6\text{jets}$ @500GeV with beam background

Pattern Recognition Performance in Presence of Backgrounds



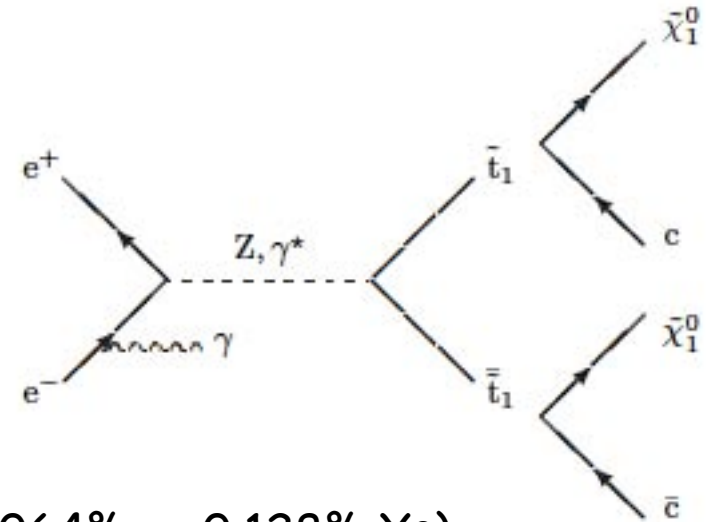
Scalar Top Study: Detector Optimization

Andre Sopczak

Cold Dark Matter can be a neutralino

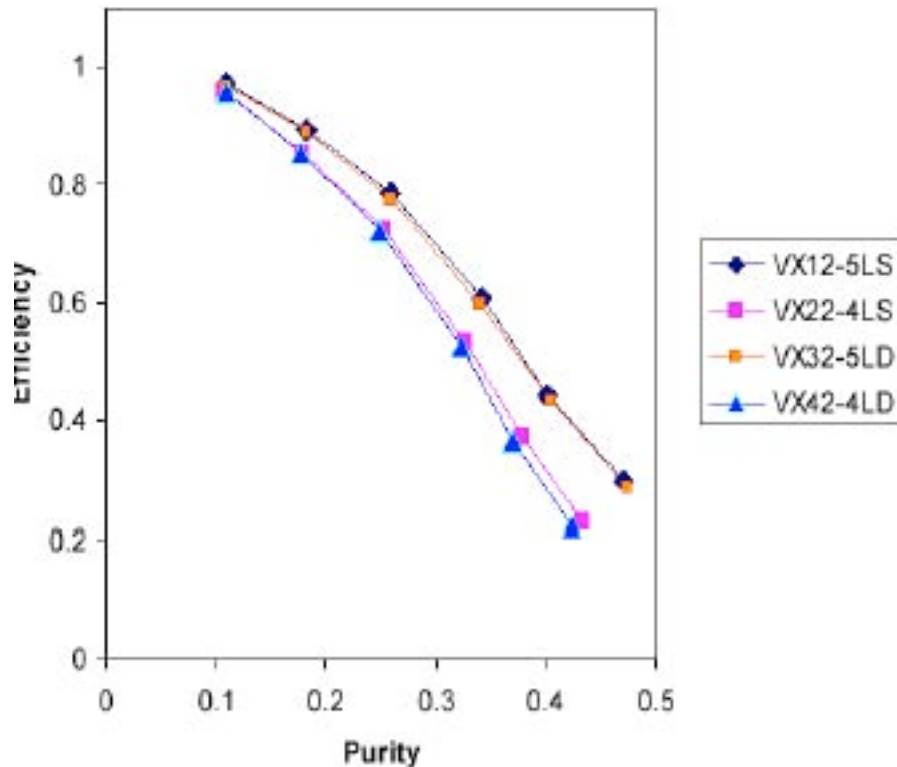
Amount of CDM is depend on
the mass difference to stop or stau

We ν is the dominant background.



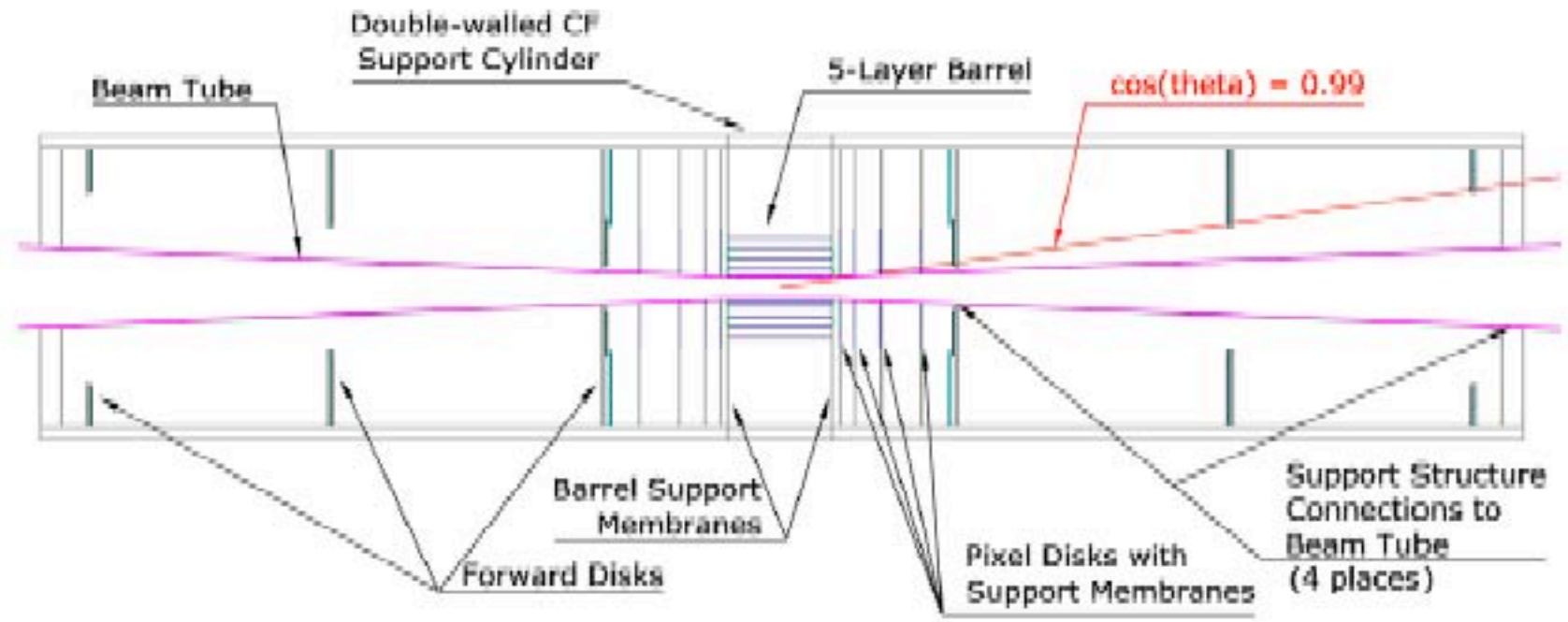
VTX configuration (5 or 4 layers) x (material 0.064% or 0.128% X₀)

reduce the innermost layer

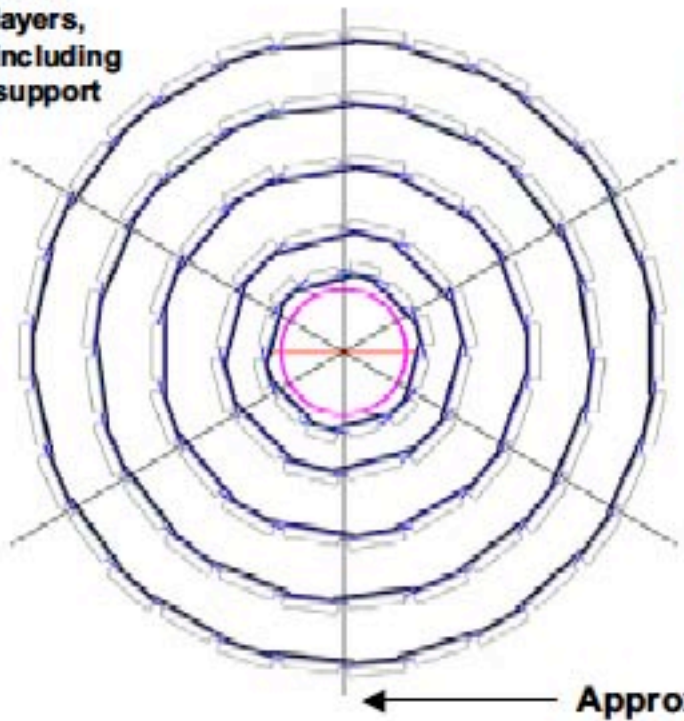


Large effect whether Layer 0 exist or not

Doubling material doesn't change results.



~1.6% RL at normal incidence for all 5 barrel layers, including support

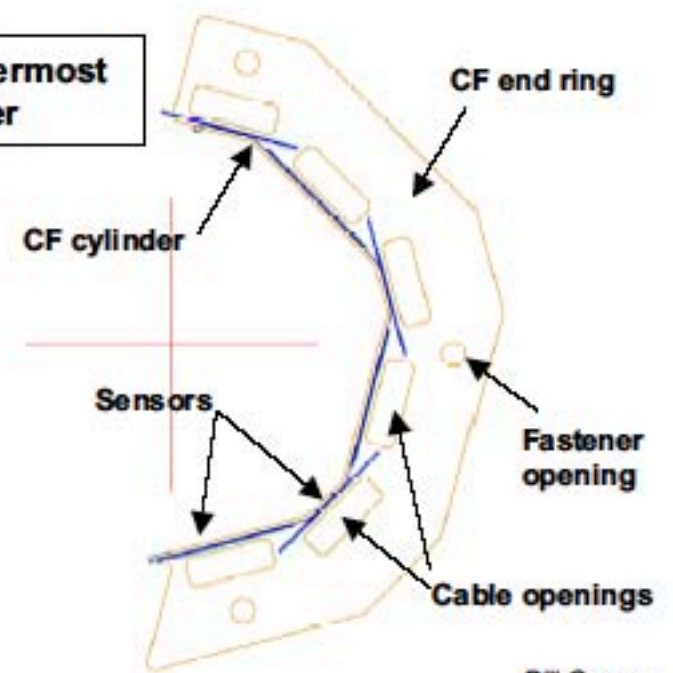


Sensors:
 IR_A = 14, 22, 35, 47.6, 60 mm
 IR_B = 15.15, 23.13, 35.89, 48.41, 60.77 mm
 Active widths: 9.1, 13.3 mm
 Cut widths: 9.6, 13.8 mm
 Beam pipe IR: 12 mm
 Beam pipe OR: 12.4 mm
 March 3, 2006

Oblong boxes are openings in end rings and end membranes for cables, optical fibers, and air flow.

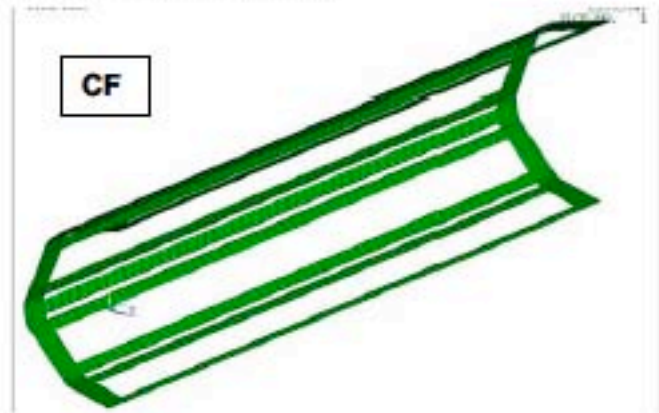
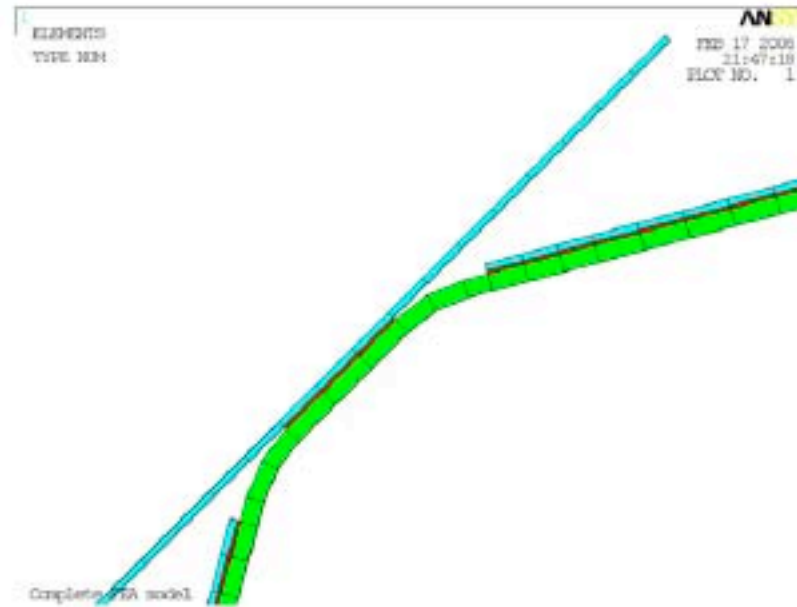
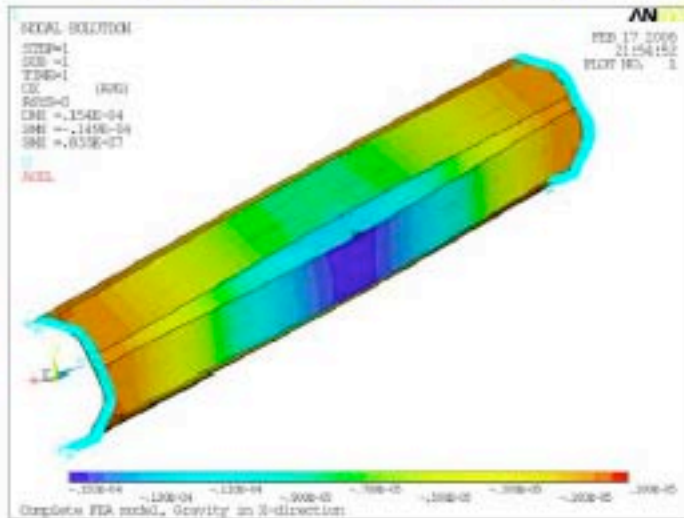
Splitting into two halves allows assembly about the beam pipe.

Innermost layer

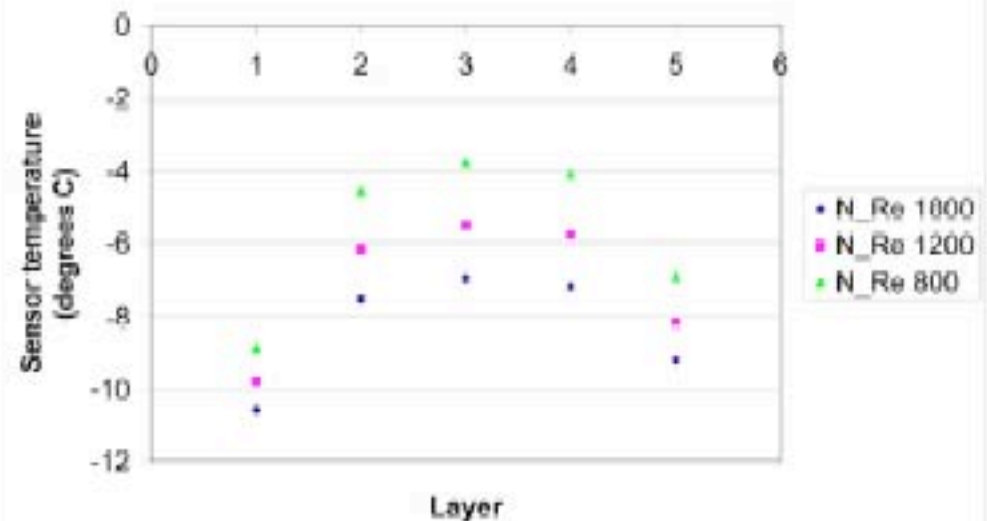


VXD: FEA & Cooling

- FEA of innermost layer gives 15 μm gravitational deflection (5 μm for a length of 125 mm)



Average Sensor Temperature for 20 Watts,
-15 C Air Supply



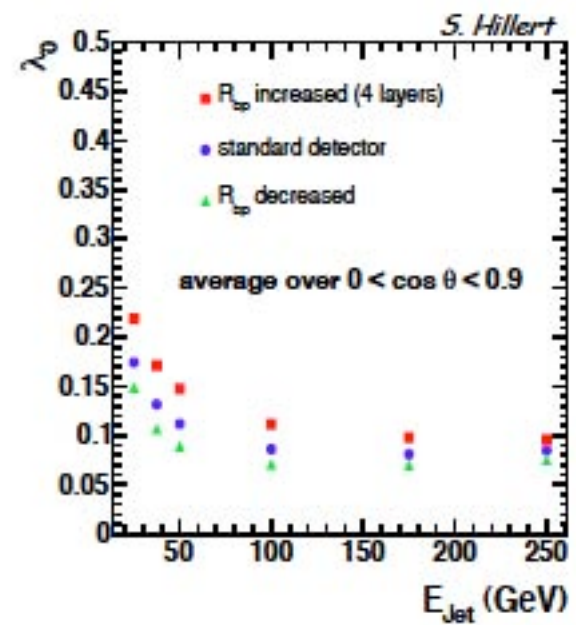
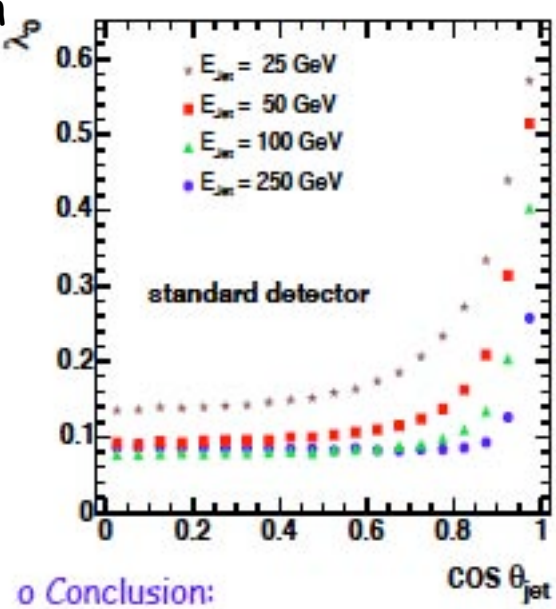
- Study of air cooling gives sensor temperatures $\sim -4^{\circ}\text{C}$ to -10°C for -15°C supply

LCFI status report: Physics & Mechanical for ILC VTX Steve Worm

Software tool for detector optimization
realistic recon. program is necessary

C++ based Vertex package:
ZVTOP, Flavor Tag, Vertex Charge

probability of reconstructing neutral hadron as charged (λ_0)

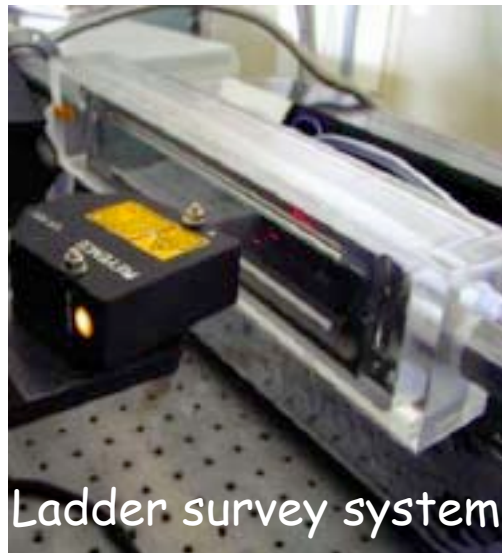


o Conclusion:

vertex charge performance strongly depends on low momentum tracks
→ differences between designs most pronounced for low jet energy and large $\cos \theta_{jet}$

Mechanical studies

Ladder mechanics

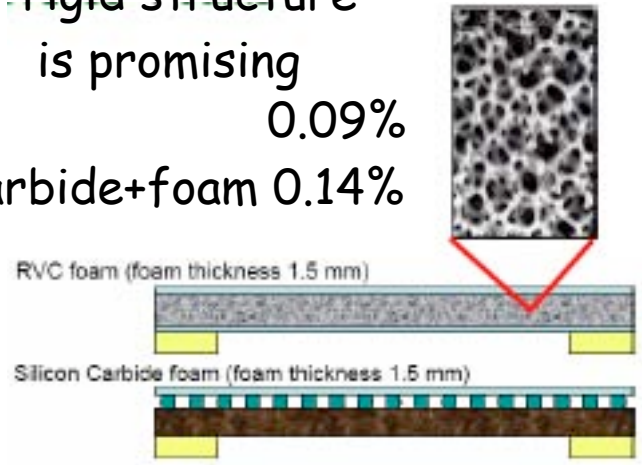


Ladder survey system

practical ladder design

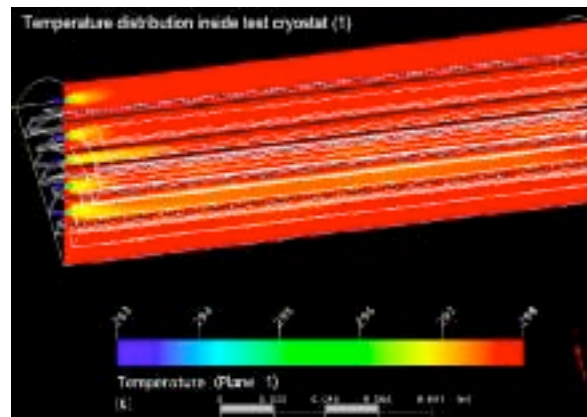
- rigid structure
- is promising

RVC 0.09%
SiCarbide+foam 0.14%



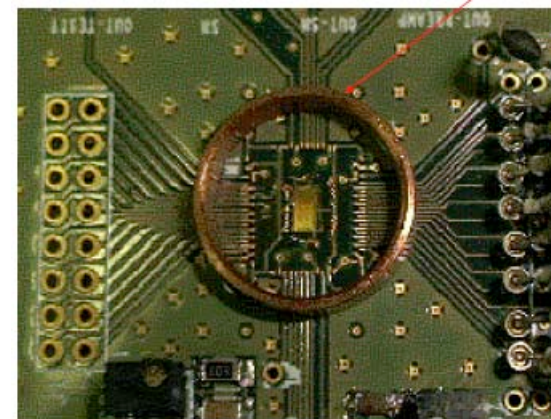
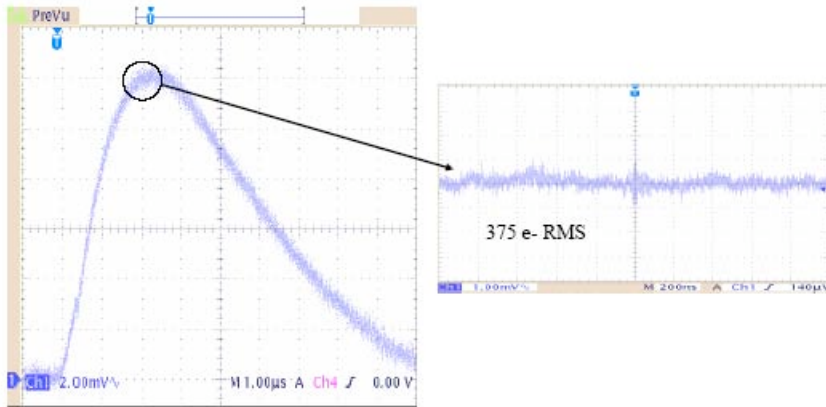
cooling

Gas cooling



Electronics for Large Silicon Trackers

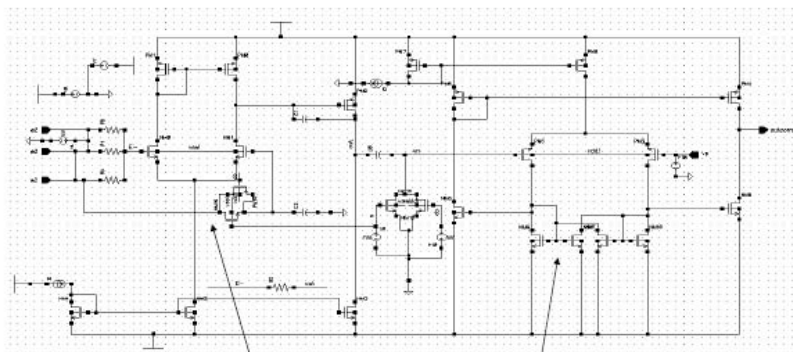
Final results from the first prototype FE chip in 180 nm: Very encouraging



375 e- input noise with chip-on-board wire-bonding (against 280 simulated)

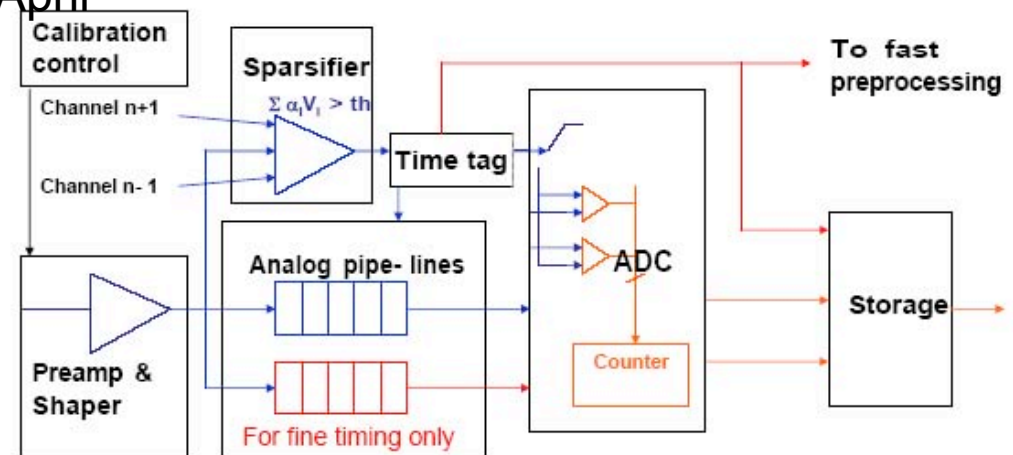
Second prototype underway in 130nm and full electronic chain (A/D and power cycling included), to be submitted end April

130nm Sparsifier



- Sum of adjacent channels
- Offset cancelled Threshold detection

Front-end architecture



Charge 1- 40 MIP, S/N~ 15- 20, Time resolutions: BC tagging, fine: ~ 2ns

Present technologies - Deep Sub-Micron CMOS
UMC 0.18 μm , 0.13 μm

Time-stamping on all layers
fine time resolution
on some layers

SiLC R&D collaboration objectives

Europe

Asia

USA

U. of Michigan, Ann Arbor
SCIPP & UCSC Santa Cruz

IMB-CNM Barcelona, Sp
HIP, Uni of Helsinki, FI
IEKP, Karlsruhe U., Ge
Uni of Liverpool, UK
Moscow State Uni, Ru
Obninsk State Uni, Ru
LPNHE, CNRS-IN2P3, Fr
Charles Uni, Prague, Cz
IFCA U. of Cantabria, Sp
University of Torino, It
IFIC-CSIC, Valencia, Sp
IHEP, Ac. Sc. Vienna, Au

Kyungpook U. Taegu, Ko
Yonsei U., Seoul, Ko
Korea U. Seoul, Ko
Seoul Nat. U., Seoul, Ko
SungKyunKwan U. Seoul
Tokyo U. (Japan)
HAMAMATSU (Japan)

Industrial firms
(in progress)

Close contacts with:
FNAL Si Lab team
SLAC SID Team
CERN LHC & Microelectronics teams

R&D Objectives:

- ▶ R&D on sensors
- ▶ R&D on associated electronics
- ▶ R&D on Mechanics
- and developing the needed tools:
 - Laboratory test benches
 - Alignment and position monitoring
 - Simulations
 - Cooling and other related integration tools

Synergy with the LHC present construction and future upgrades

EUDET testbeam Roadmap



Sept. 2006:
DESY 5 GeV e-beam, S/N with:
130nm chip (1st vers), medium & long strips ladder

Fall'07: CERN (FNAL)
First combined tests
(small calo, and TPC)
within B field
with Si prototypes
and 128 ch chips

Spring'09: CERN
Combined test with
final protos of Si
tracker, calo and TPC,
within B field
second foundry FE
chips, cooling and
alignment protos

2006

2007

2008

2009

Preparation test beam 07:
128ch chips & detector protos

Preparation test beam 09:
new chips & new detector protos,
cooling & alignment

▶ Preliminary measured pulse velocity on Lab test bench: 22ns/m

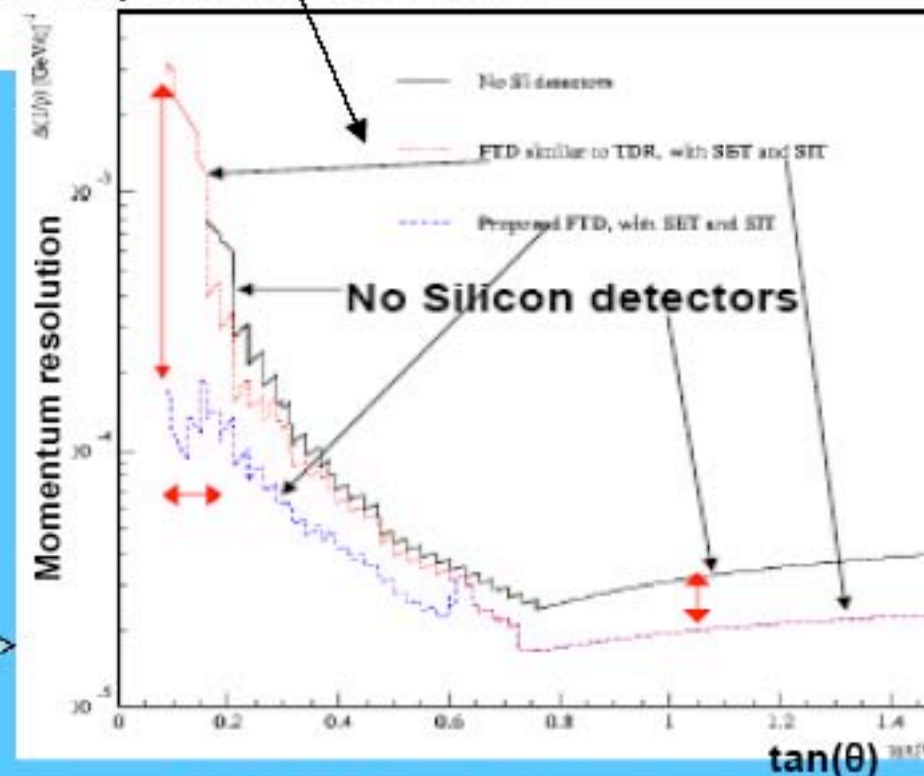
Applying constant fraction threshold gives of the order 5 cm spatial resolution and few ns time resolution.

▶ Elementary module revisited:
FE electronics on sensors using flip chip bump bonding

▶ Full chain F.E readout chip in UMC 130nm to be sent by April 24.

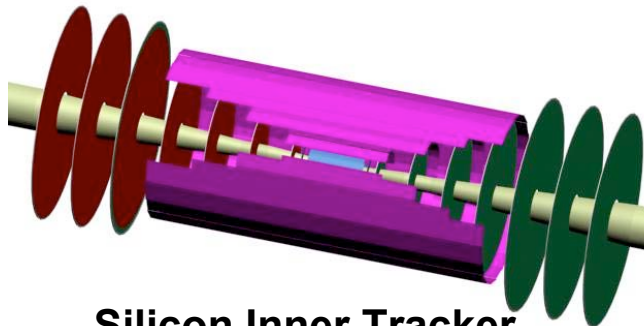
▶ Improvements of tracking performances with Silicon components added to TPC

Some novelties



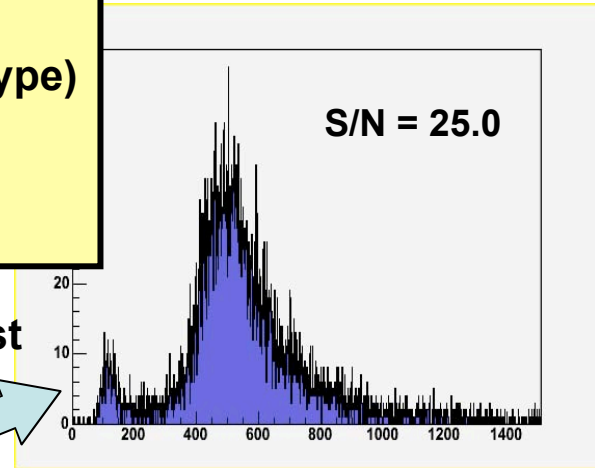
Only TPC (no Silicon trackers)
FTD as TESLA TDR + SIT & SET
FTD new + SIT + SET

Silicon R&D in Korea



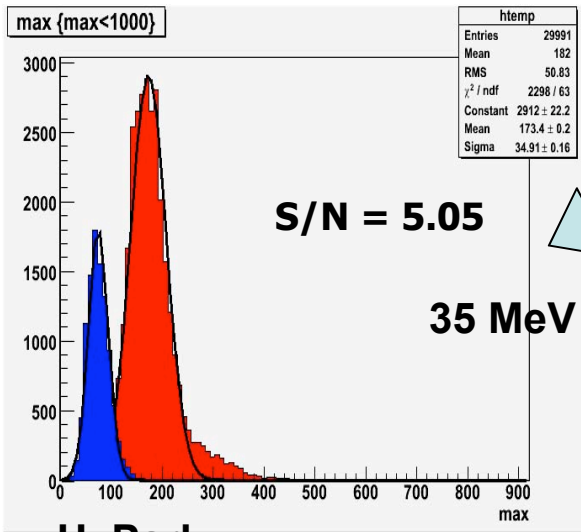
Silicon Inner Tracker

- Aiming
 - silicon sensor (DC- and AC-type) on large wafer
 - thinning
 - relatively cheap price



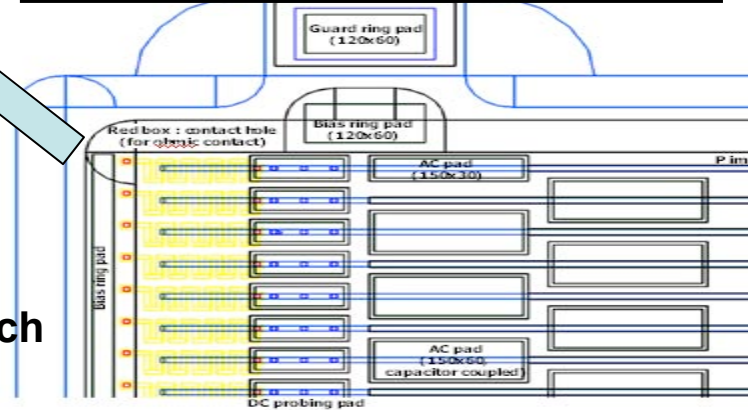
⁹⁰Sr Source Test

- DC-sensor fabrication and test
 - DSSD, SSD, Si diode
- AC-sensor is being fabricated
 - SSD



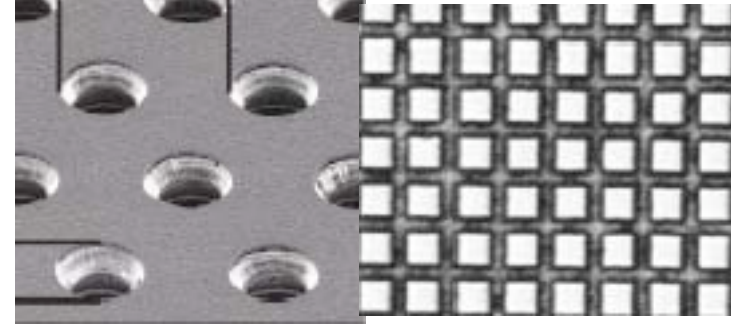
35 MeV proton beam test

mask design on 7inch



Brief Introduction of TPC

Required position resolution $\sim 100\text{-}120\mu\text{m}$ $\square_{P/P} \sim 10^{-4}P$
 Good two track separation



Key Issue

Can we achieve this resolution @ 2.5m drift ?

High B field suppress transverse diffusion.

MPGD (GEM, Micromegas) -TPC is a candidate as it is free from ExB effect.

Many groups have been studied performances using small prototype.

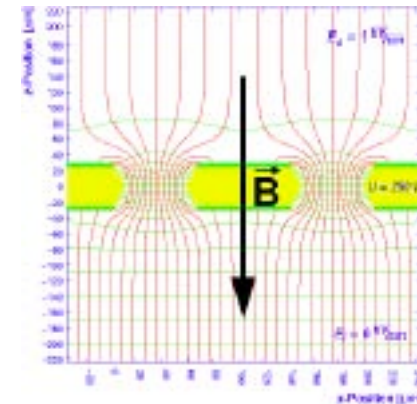
R&D towards TDR

phase I
 "Demonstration"
 Small Prototype

We are here

↓ phase II (~3years)
 "Consolidation"
 Large Prototype

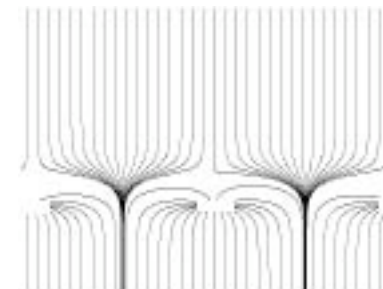
phase III
 "Design"



besides the resolution

gas study
 ion backdrift
 neutron background
 non-uniform B/E field
 software

Readout method
 standard pad readout
 std+charge dispersion
 advanced pixel readout
 electronics
 material budget at endplate



Point resolution vs. Drift distance

Mike Ronan

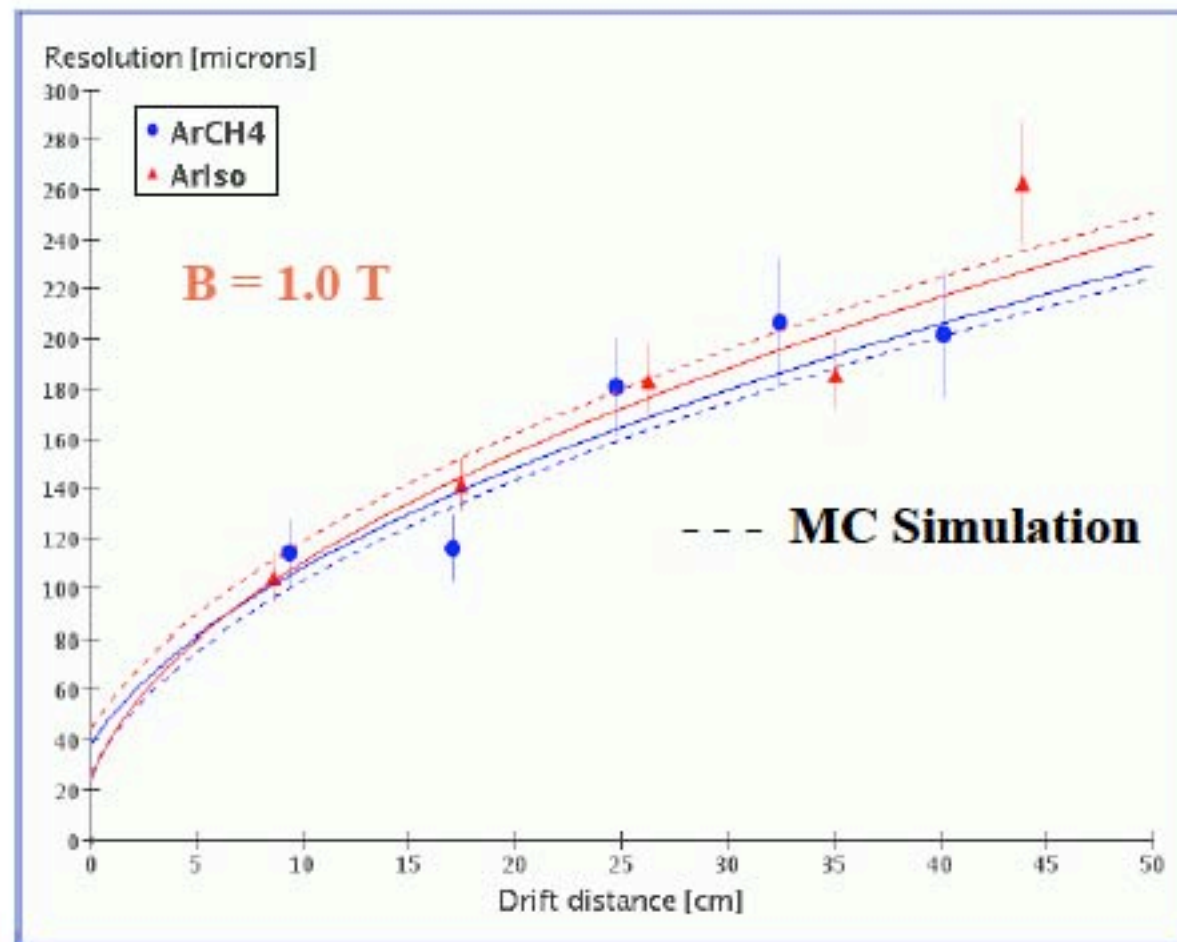
Similar point resolution results were obtained for both **Ar-Methane: 10% (P10)** and **Ar-Isobutane: 5%**. The larger diffusion in Ar-Isobutane is compensated by a larger number of effective electrons.

We find

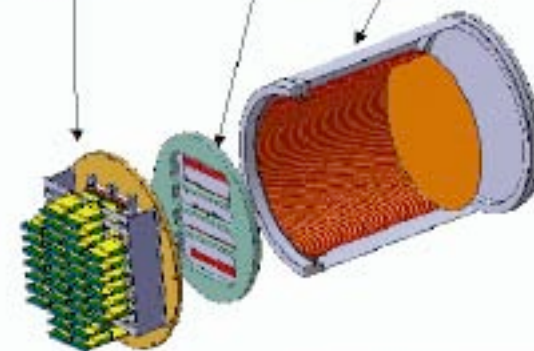
	Data	Monte Carlo
Ar CH4	19.1 +/- 4.6	19.4 +/- 0.5
Ar Isobutane	32.1 +/- 4.8	30.8 +/- 1.3

The extrapolated point resolution at zero drift is at or below 50 microns for both gases.

However, Ar-CF4 is quite different.



Measured Micromegas TPC points: **Berkeley**, **Saclay**, **Orsay**
 Argon-Methane: 10% (P10)
 magnetic field of 1. tesla. A Monte Carlo simulation of ionization, electron drift and avalanche formation is to be in excellent agreement with the data.



MT3/MPT collaboration

Multi Technologies testing TPC
Multi Prototype TPC

test MWPC, GEM & Micromegas

MWPC, GEM

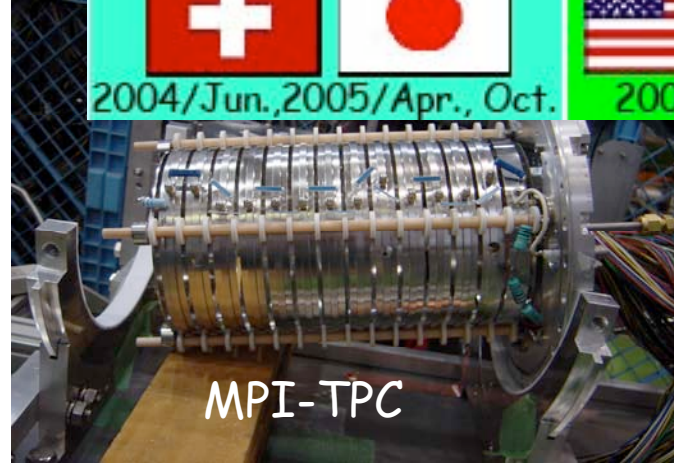
2004/Jun., 2005/Apr., Oct.

MicroMegas

2005/Jun.

Charge Dispersion Readout

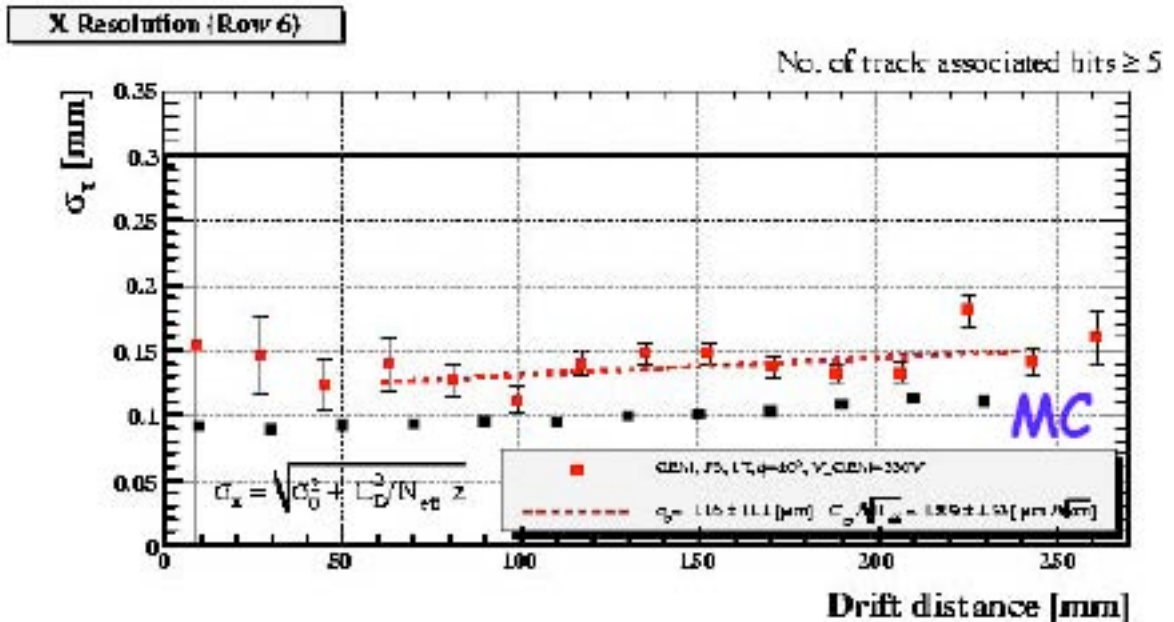
2005/Oct.



GEM with 1.27mm staggered pad
in P5 gas under 1T B field

Oct. P5 50V/cm

$$\sigma_x = \sqrt{\sigma_0^2 + \frac{C_D^2}{N_{eff}} z}$$

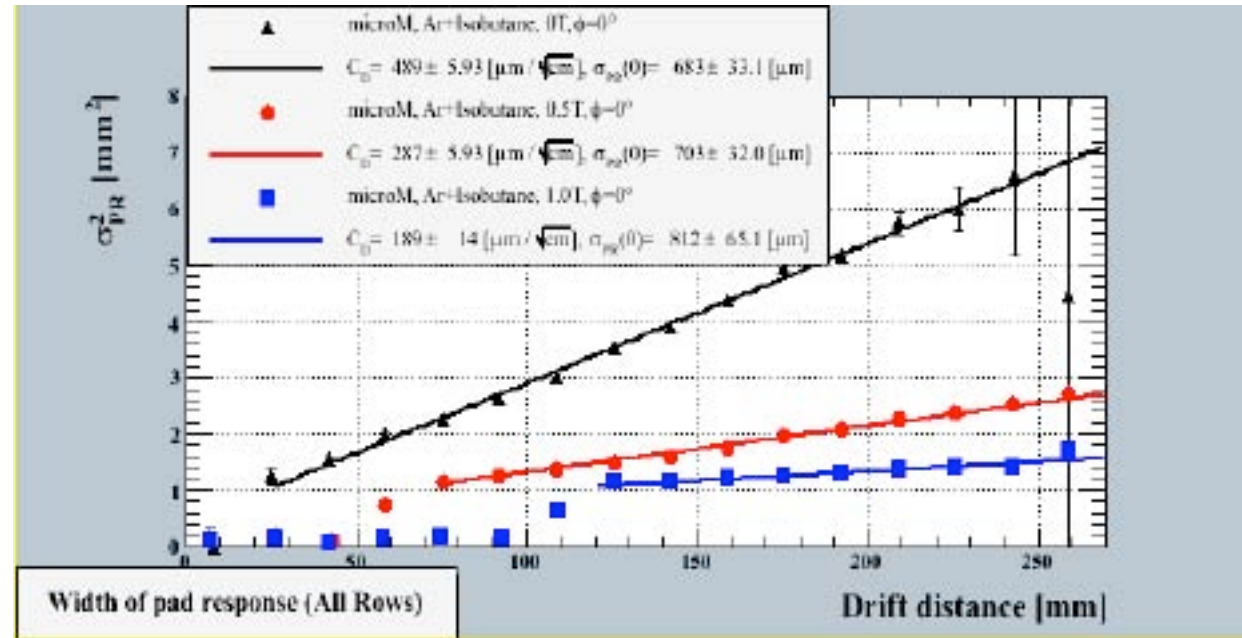


Ar:isoC4H10

2.3mm pad

CD measurement

$$\sigma_{PR} = \sqrt{\sigma_{PR}^0{}^2 + C_D^2 \times z}$$



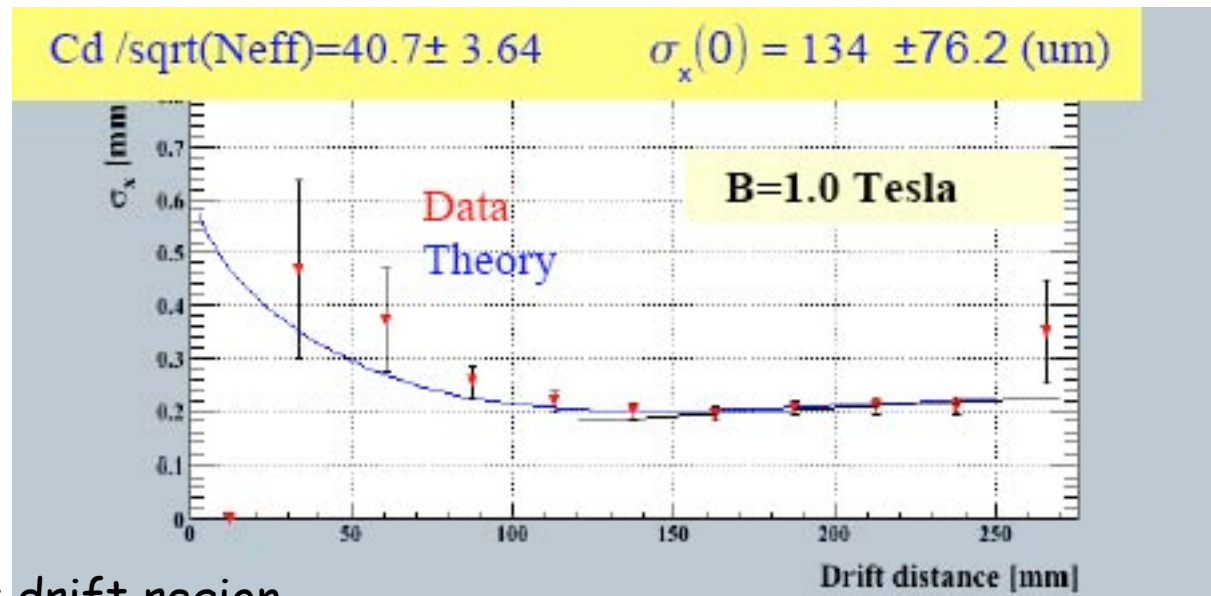
Resolution

not behave like this

$$\sigma_x = \sqrt{\sigma_0^2 + \frac{C_D^2}{N_{eff}} z}$$

Pad size is too wide comparing to the narrow MM signal.

It dominates the resolution at short drift region



Formulation of Spatial Resolution

for tracks perpendicular to the pad row

$$\sigma_X^2 = \int_{-\frac{w}{2}}^{+\frac{w}{2}} d\left(\frac{x^*}{w}\right) \left[\text{[i]} + \frac{1}{N_{\text{eff}}} \text{[ii]} + \text{[III]} \right]$$

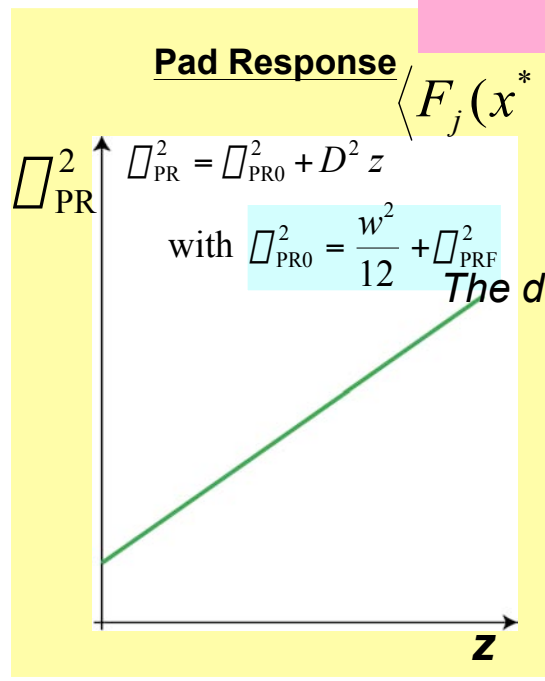
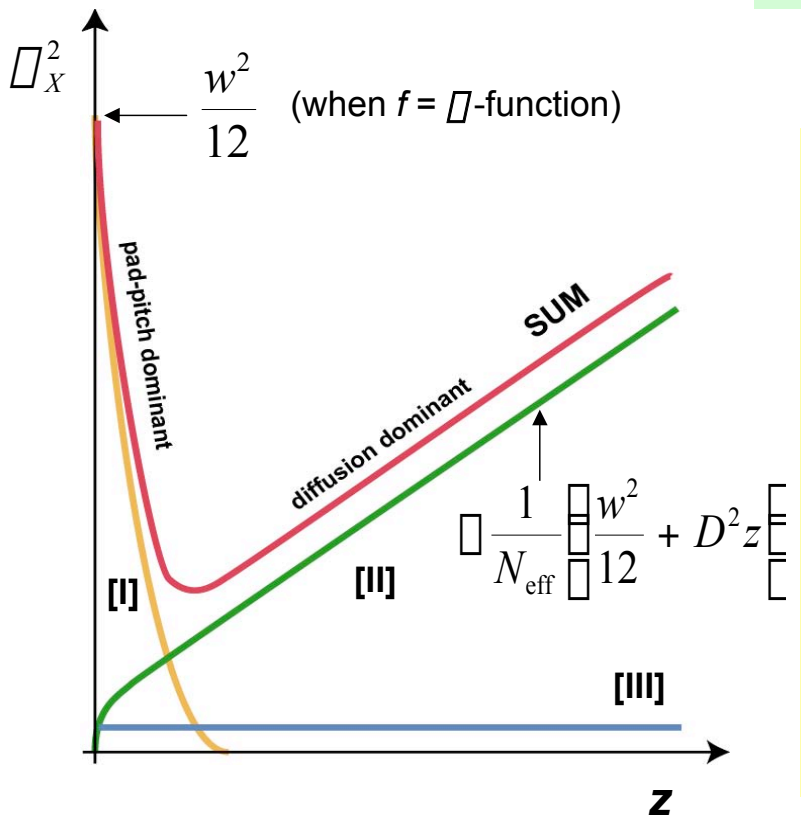
$$\text{[i]} \equiv \int_j (jw) \langle F_j(x^* + \Delta x) \rangle \Delta x^2$$

$$\text{[ii]} \equiv \int_{i,k} jkw^2 \langle F_j(x^* + \Delta x) F_k(x^* + \Delta x) \rangle \int_j jw \langle F_j(x^* + \Delta x) \rangle$$

$$\text{[III]} \equiv \frac{\langle (\Delta q)^2 \rangle}{\langle Q \rangle^2} \left\langle \frac{1}{N^2} \right\rangle \int_j (jw)^2 \quad (\Delta q : \text{ electric noise charge on a pad})$$

where $N_{\text{eff}} \equiv \left\langle \frac{1}{N} \right\rangle \frac{\langle Q^2 \rangle}{\langle Q \rangle^2}$ and

When pad response is narrow (like Micromegas) resolution can be described analytically.



$$\langle F_j(x^* + \Delta x) \rangle \equiv \int_{-\frac{w}{2}}^{+\frac{w}{2}} d(\Delta x) P_D F_j(x^* + \Delta x)$$

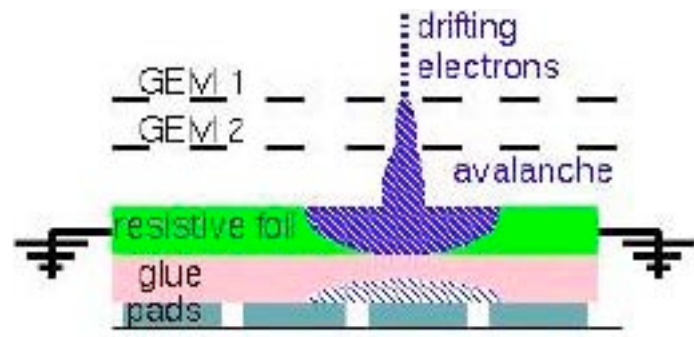
with $P_D \equiv \frac{1}{\sqrt{2\pi}D} \exp\left[-\frac{(\Delta x)^2}{2D^2}\right]$

The definition is similar for $\langle F_j \cdot F_k \rangle$.

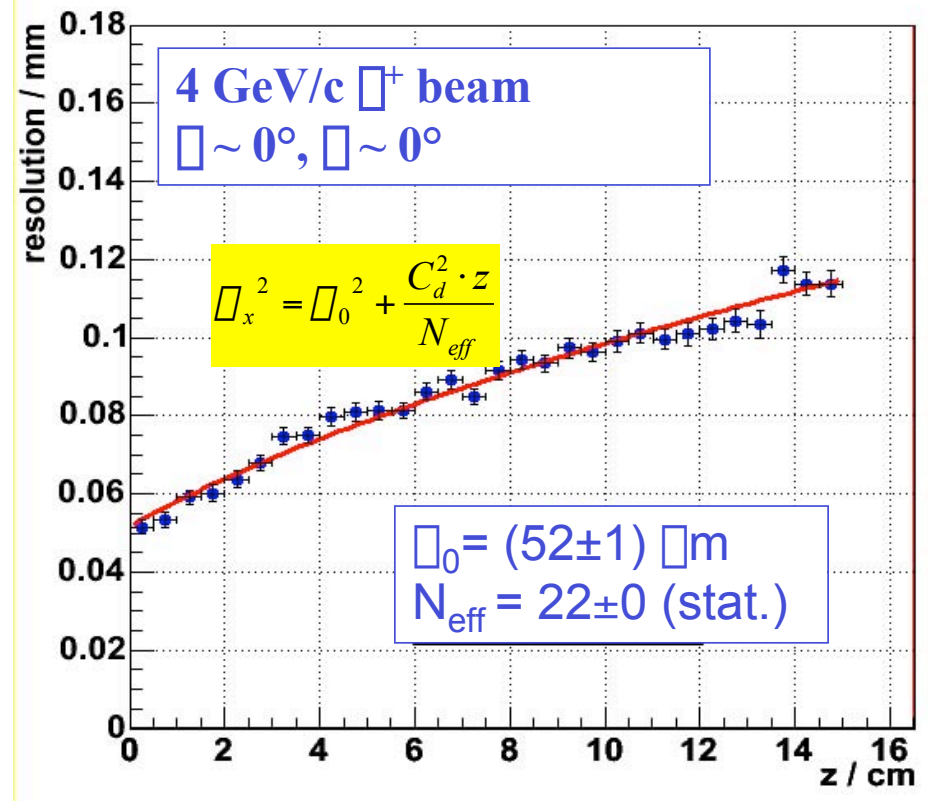
narrow pad is necessary or..



Micromegas



Charge dispersion readout endplate



- Significant suppression of transverse diffusion at 4 T.
- Example gases:
 $D_{Tr} \sim 32 \mu\text{m}/\text{cm}$ (P10)
 $\sim 20\text{-}30 \mu\text{m}/\text{cm}$ (Ar/CF4 mixtures)

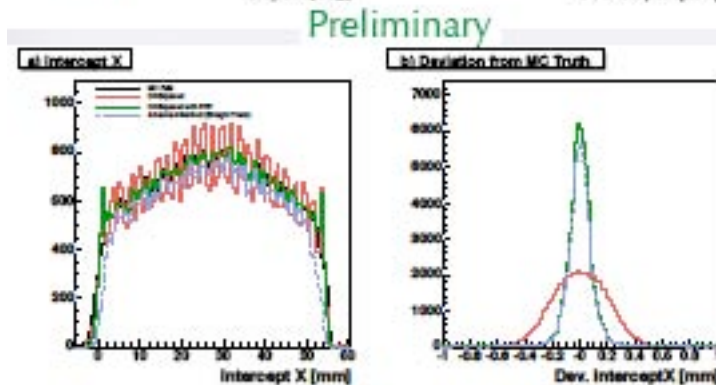
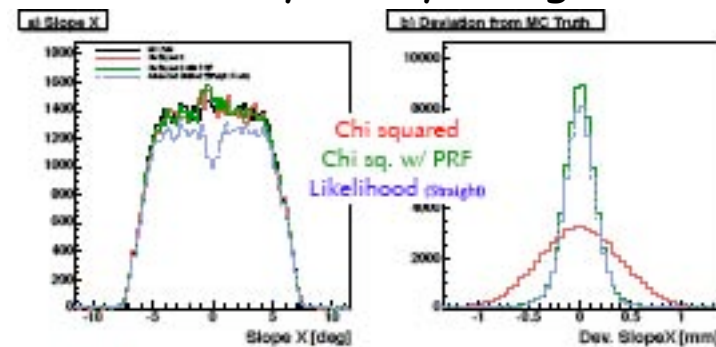
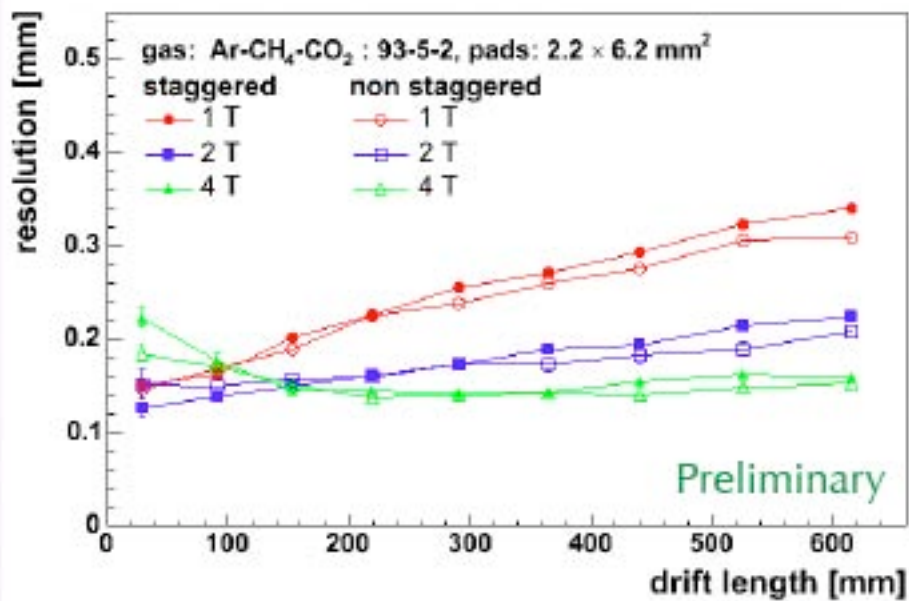
Extrapolate from present data to B = 4T
Use $D_{Tr} = 32 \mu\text{m}/\text{cm}$
Resolution (2 mm pads)
 $\sigma_{Tr} \approx 100 \mu\text{m}$ (2 m drift)

ILC TPC R&D studies at DESY/U. Hamburg

Katsumasa Ikematsu

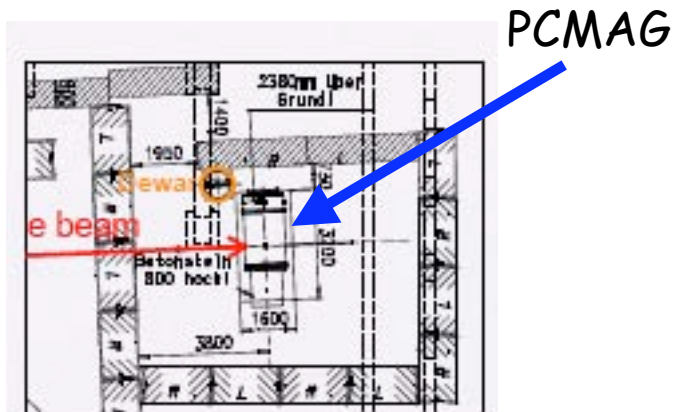
Efficiency study using MC

resolution study using several fitting methods

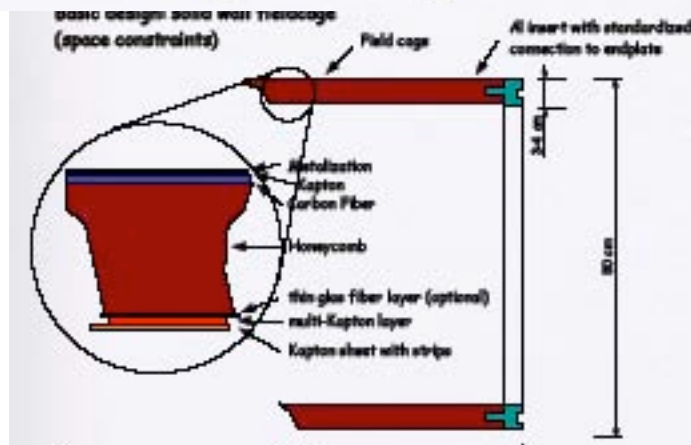


Effort to EUDET & Large Prototype TPC

Preparation of test beam



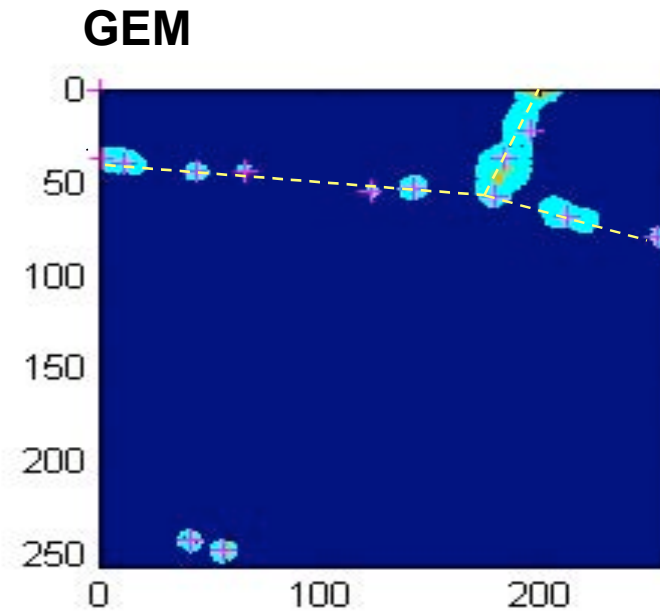
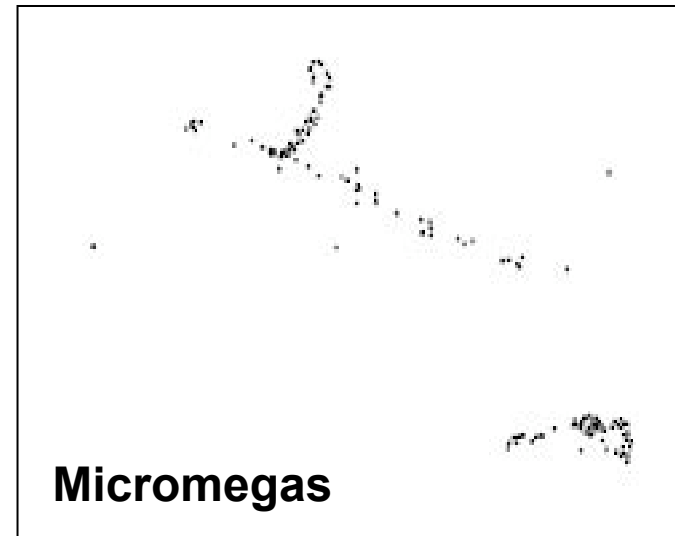
Field cage design



SiTPC : digital TPC

- Readout a TPC with CMOS VLSI chips
- Tracks seen, single-e or single-clusters, with Micromegas or GEM amplification
- MC and theoretical studies show ultimate resolution

Paul Colas

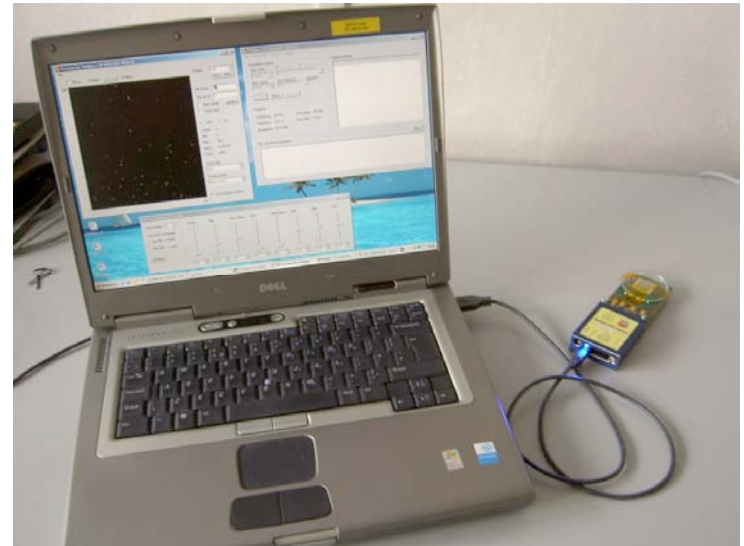
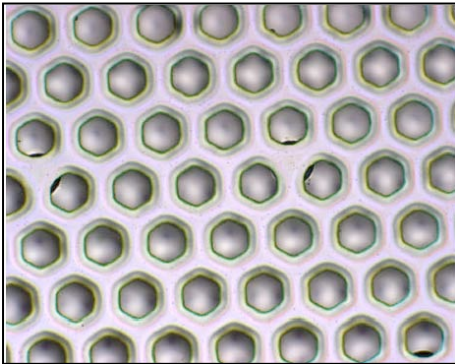


Developments in progress

USB pluggable readout, new Medipix2 chip

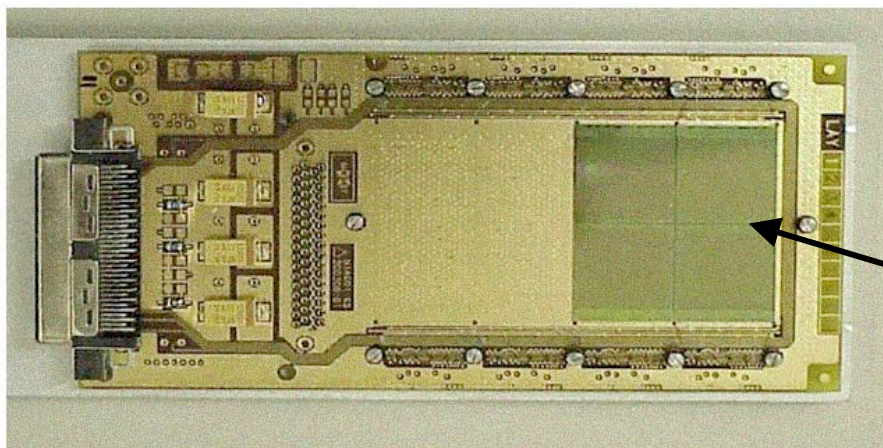
Noise under study

Integrate Micromesh onto the chip by post-processing (InGrid)



Add a protective layer

Provide time measurement
(switchable with time over
threshold) -> TimePix



Tile-up chips and speed-up
readout (RELAXD project)

TPC milestones

- 2006 Continue LC-TPC R&D via small-prototype tests, organize work for Large Prototype
- 2007-2009 Test Large Prototype, decide technology
- 2010 Final design of LC TPC
- 2014 Four years construction
- 2015 Commission/Install TPC in LC Detector

