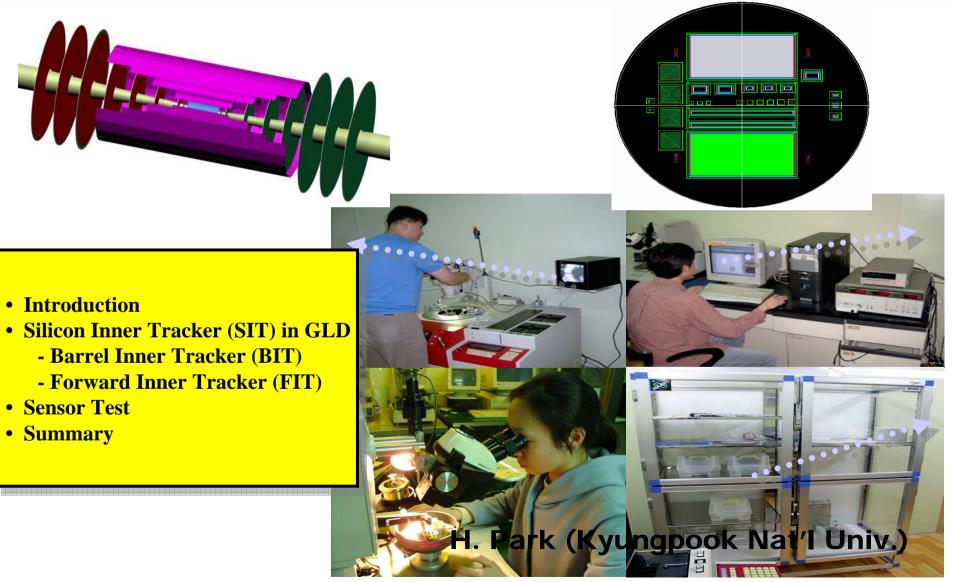
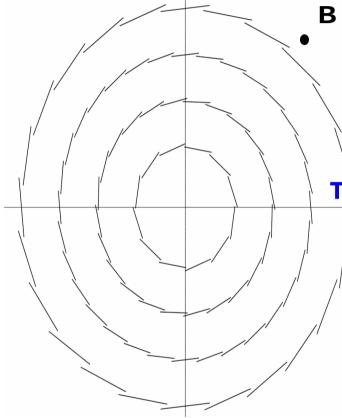
Silicon Inner Tracker R&D Status in Korea



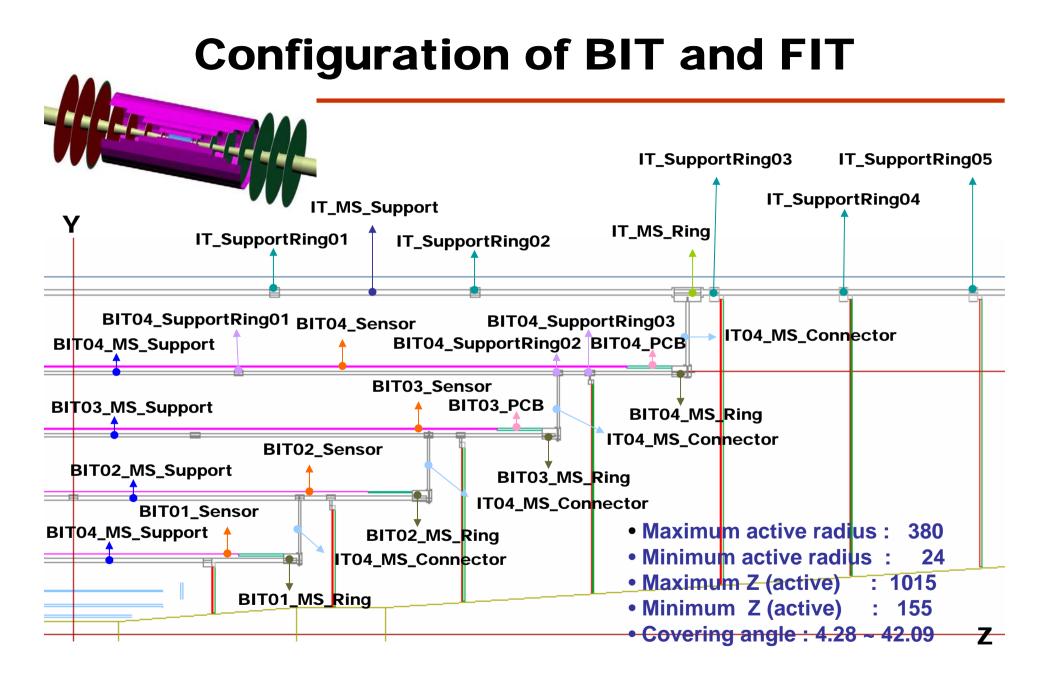
Barrel Inner Tracker Configuration



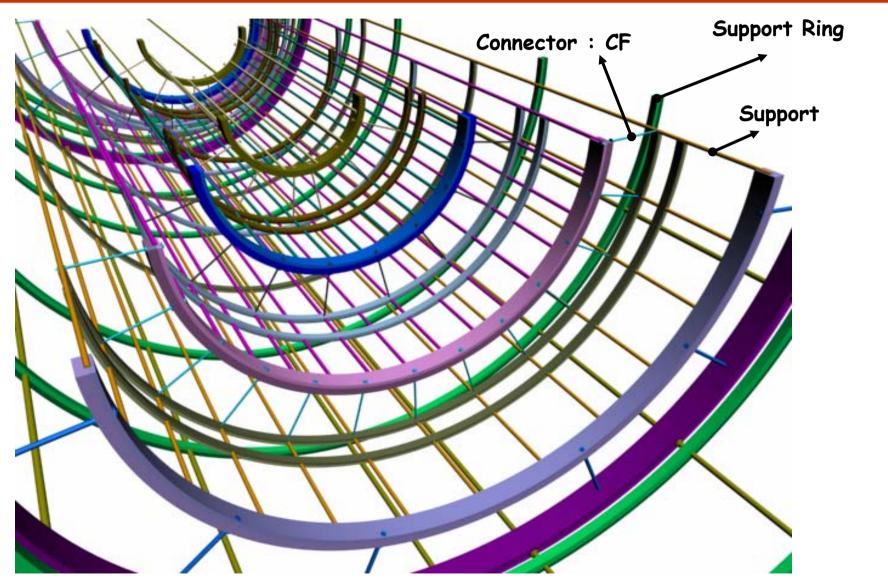
BIT	Half Z	Real Z(o 1.6 mm)	R	sensor type	
layer 1	185	195.2	90	50 X 50	5.76°
layer 2	330	340.4	160	50 X 50	5.76°
layer 3	475	485.6	230	50 X 50	5.76°
layer 4	620	620.4	300	90 X 90	5.76°

To make dead region free, module has 1.6 mm overlap

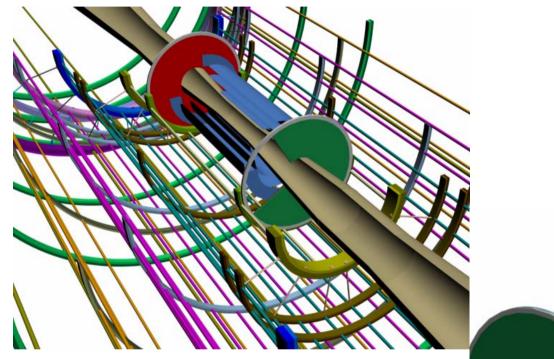
BIT	sensor area	# sensor of a module (o 1.6)	# module	# sensor	total area
layer 1	50 X 50	4	24	96	240000 MM2
layer 2	50 X 50	7	48	336	840000 MM2
layer 3	50 X 50	10	64	640	1600000 MM ²
layer 4	90 X 90	7	24	168	1360800 MM ²

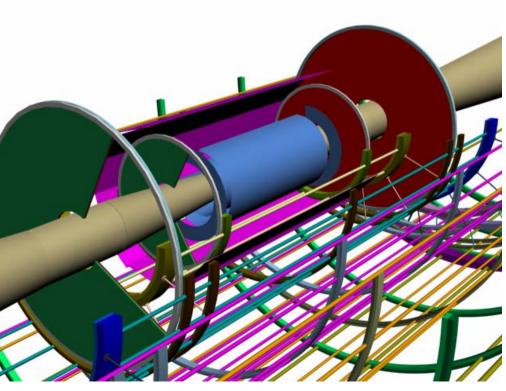


SIT Mechanical Structure

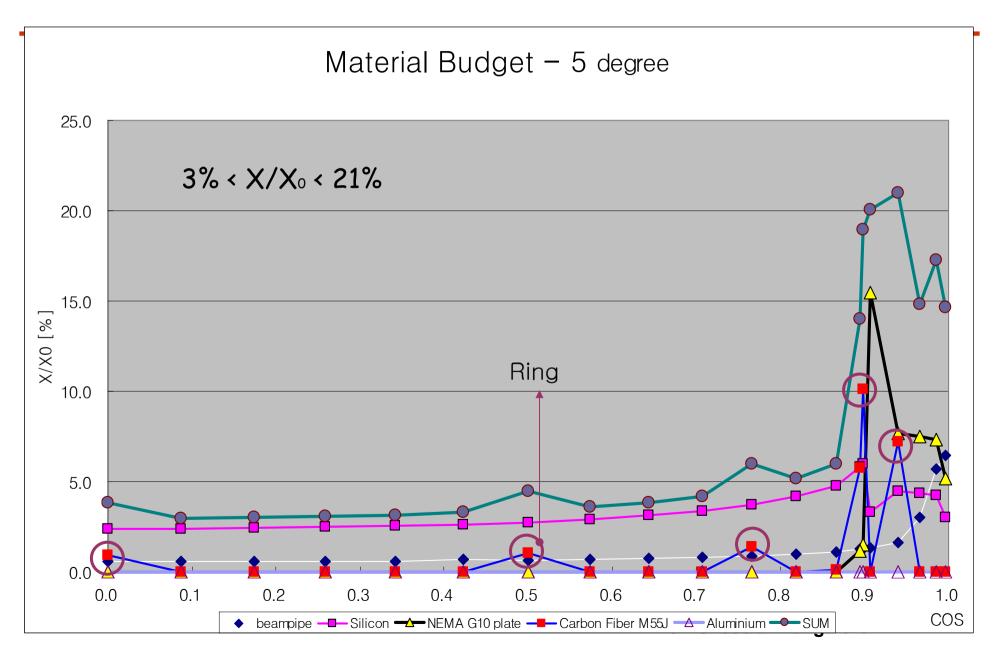


IT Mechanical Structure

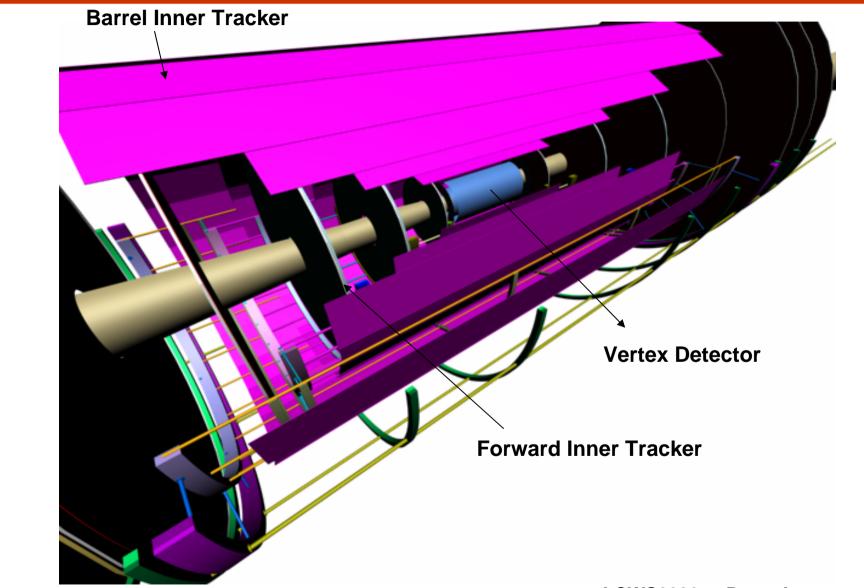




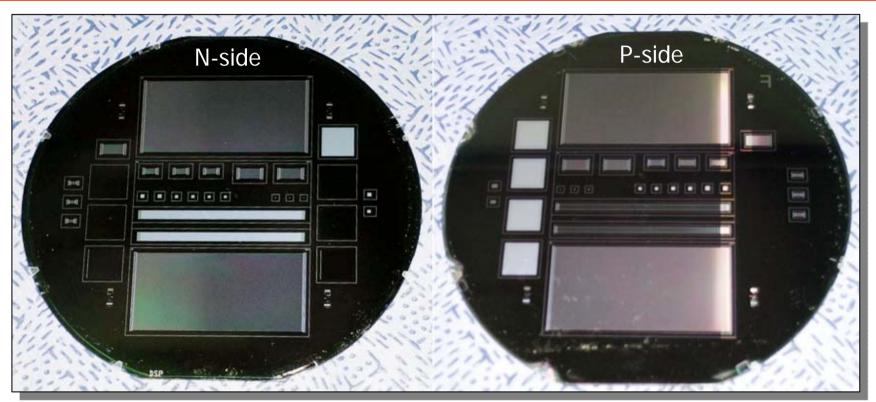
Material Budget



IT Mechanical Structure

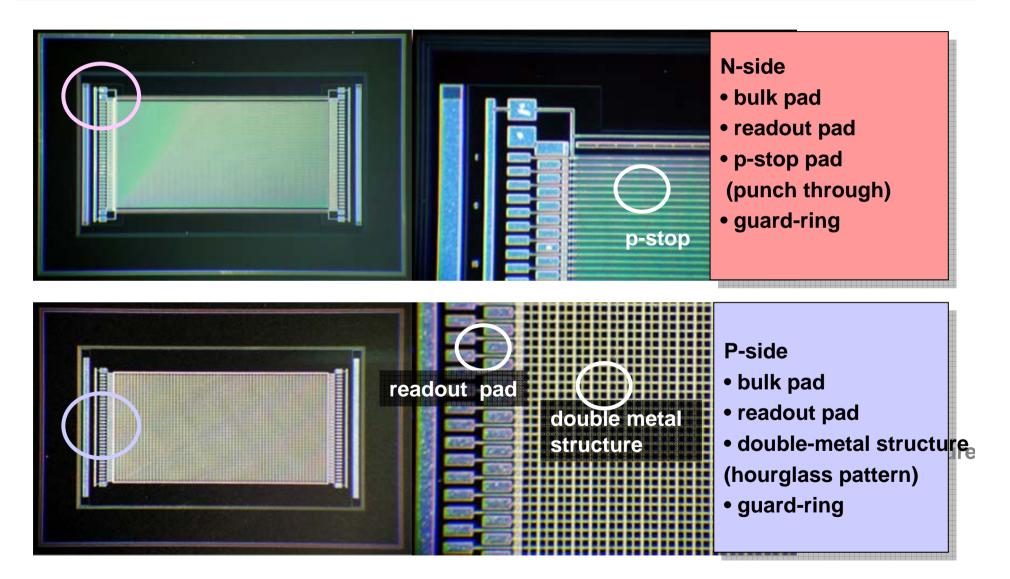


Prototype

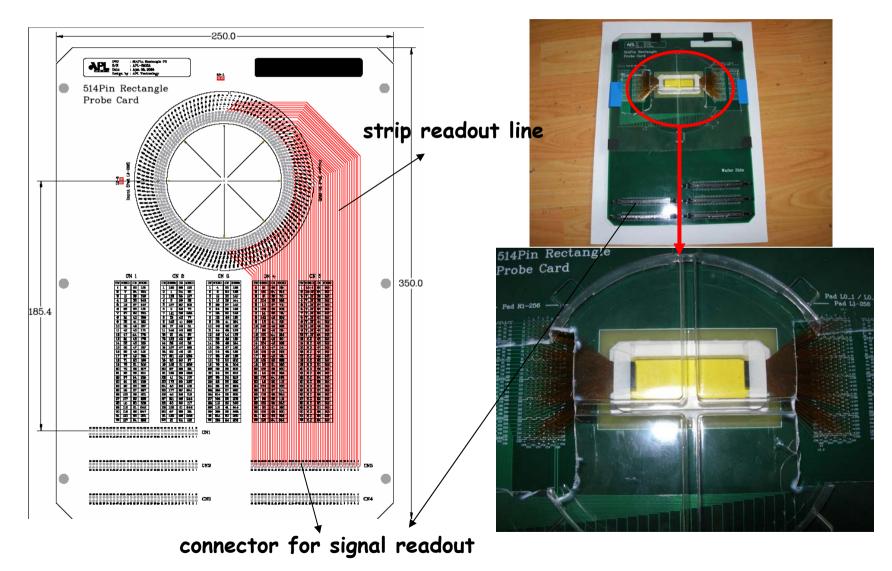


	TOPSIL	strip width	9 µ m
wafer	(5inch, high resistivity, (100), FZ, DSP)	strip pitch	50(100) µ m
thickness	380 µ m	readout pitch	50 µ m
size	51 x 26 mm ²	readout channel	512(512) Bangalore

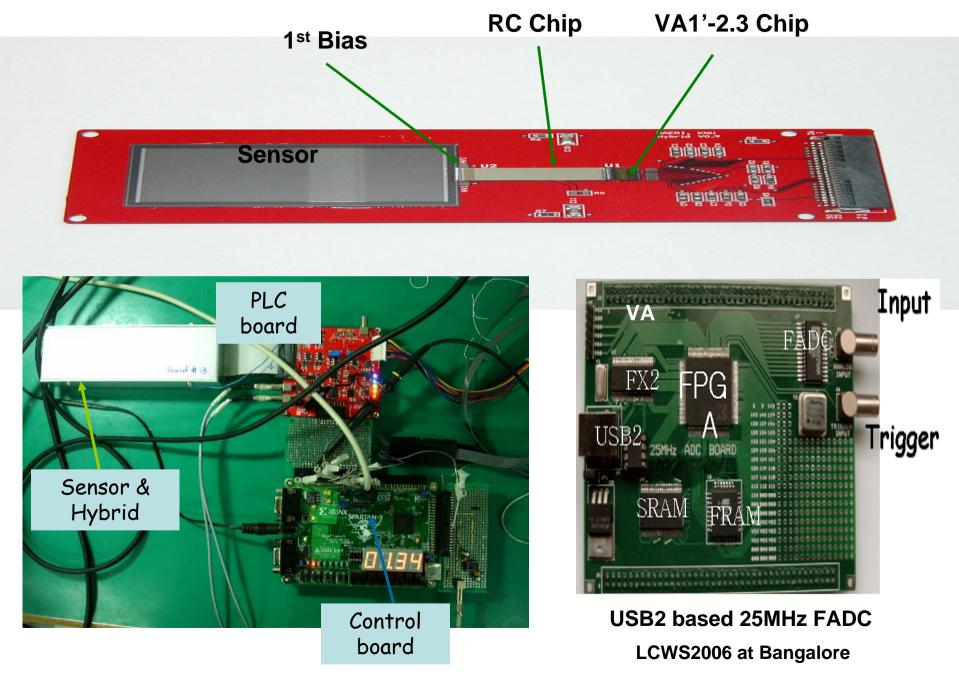
DDDS Prototype



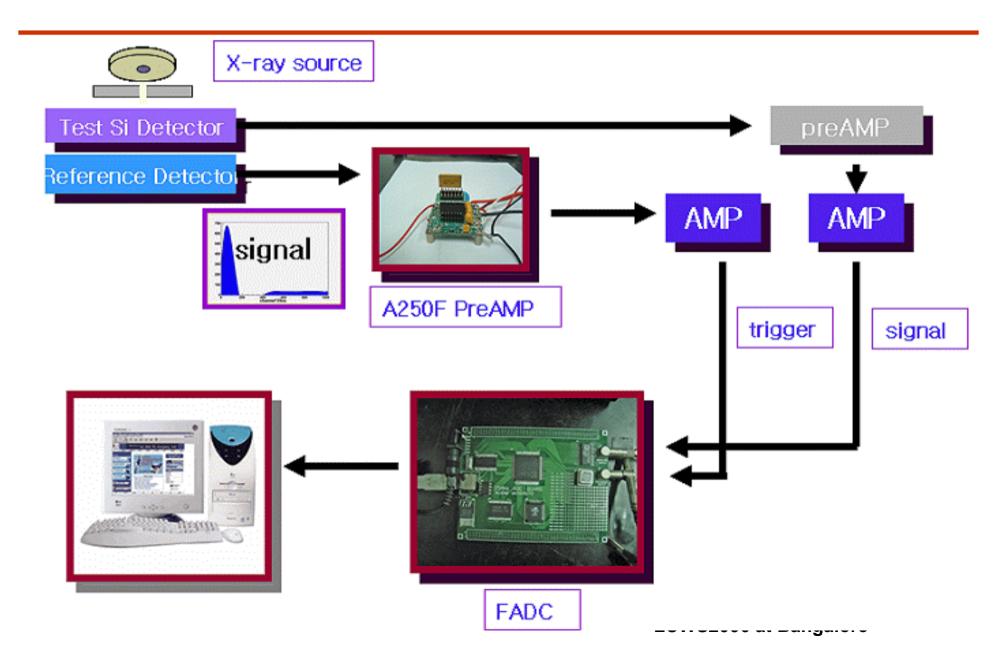
Probe Card for Strip Measurement



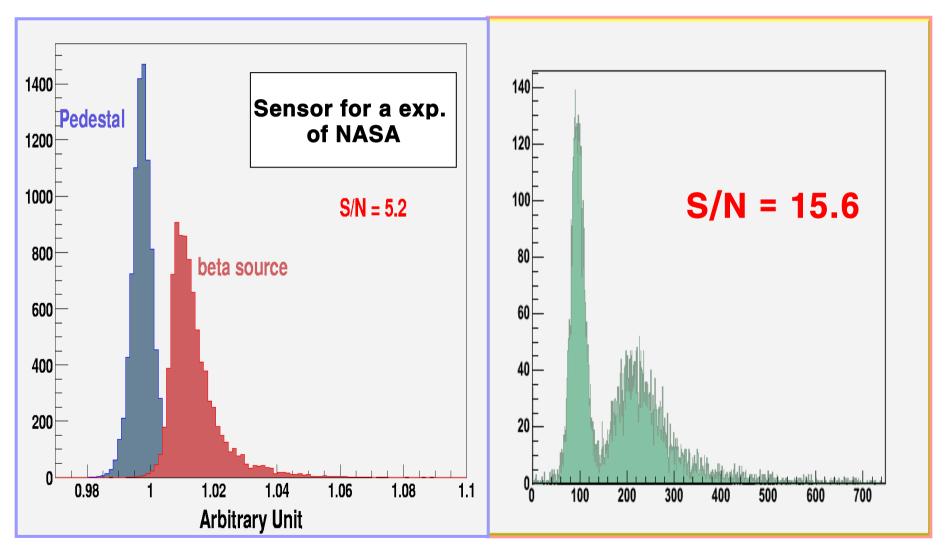
Sensor Signal Readout



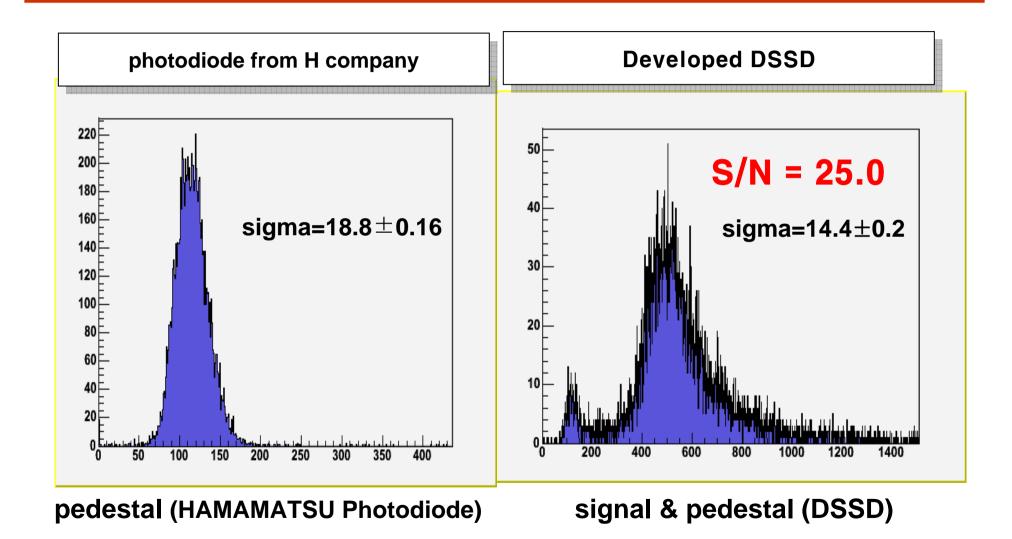
For S/N Measurement

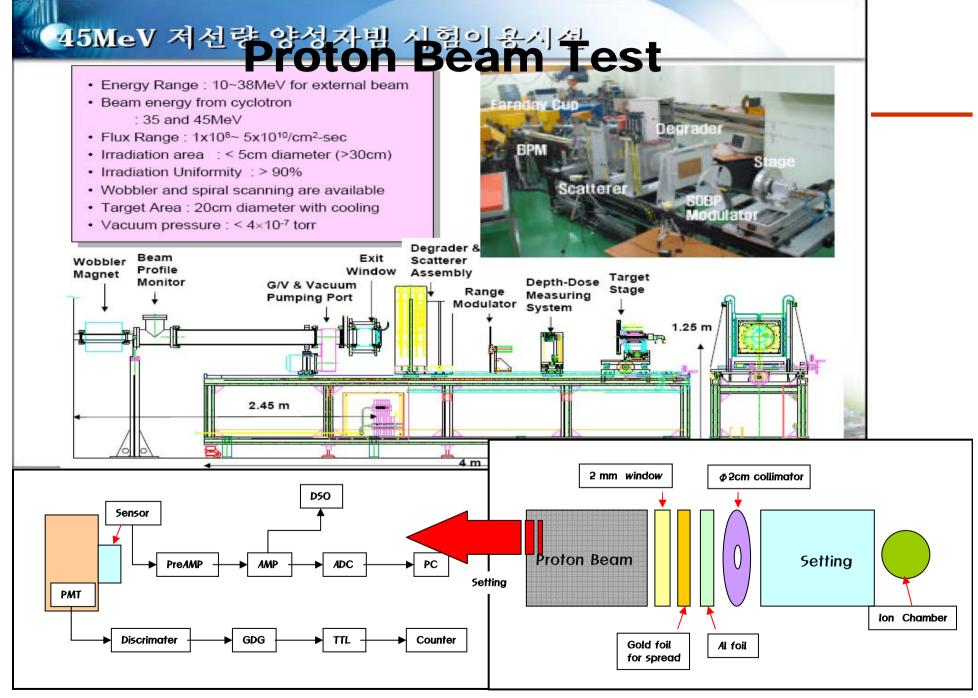


S/N Measurement Result

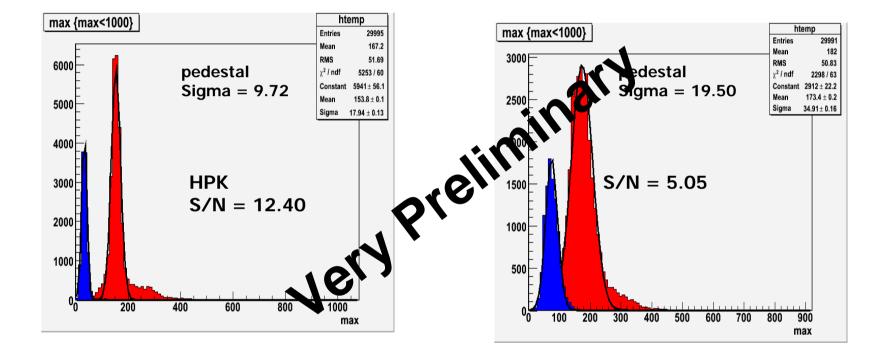


S/N Measurement Result

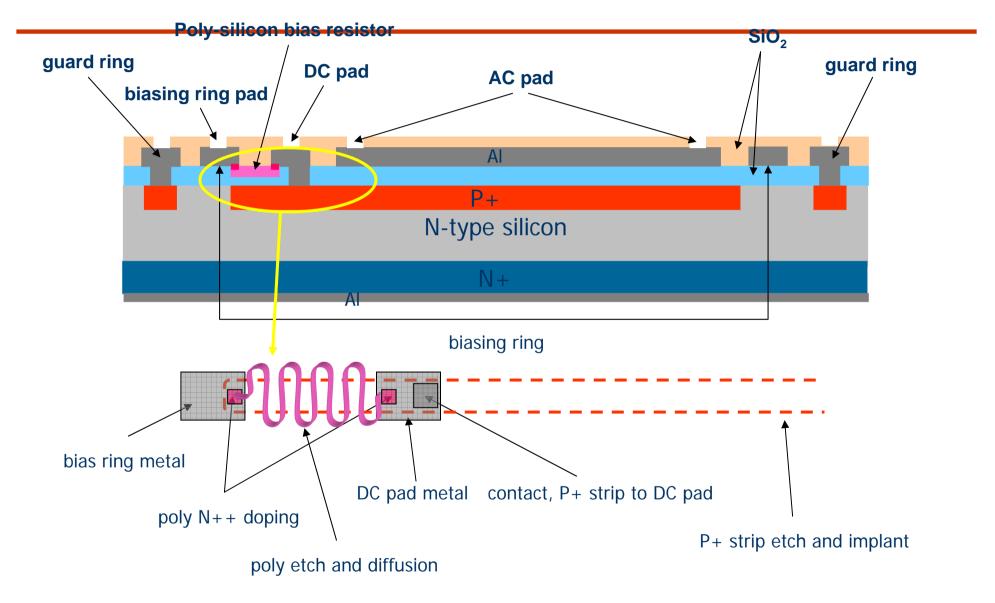




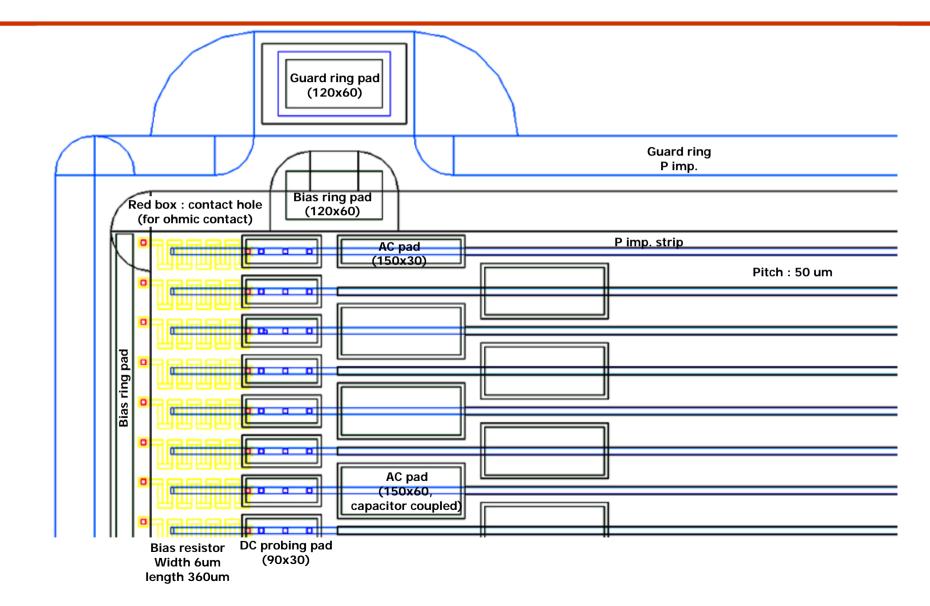
Proton Beam Test



AC-Type SSSD



Mask Design of SSSD



Summary

- Baseline design of silicon inner tracker $\sqrt{4}$ layers of barrel inner tracker with 1.6 mm overlap
 - $\sqrt{7}$ 7 layers of forward inner tracker
 - $\sqrt{}$ mechanical structures of BIT and FIT
 - $\sqrt{}$ readout electronics
- Sensor development and performance test
 - $\sqrt{}$ sensor fabrication and test for DC-DSSD, DC-SSD, DC-PAD
 - $\sqrt{}$ sensor on batch for AC-SSD in progress