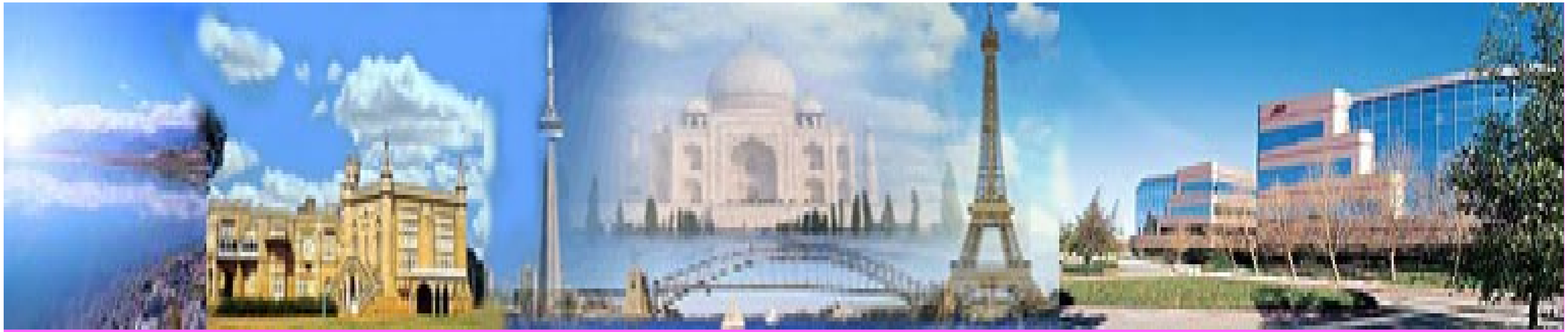
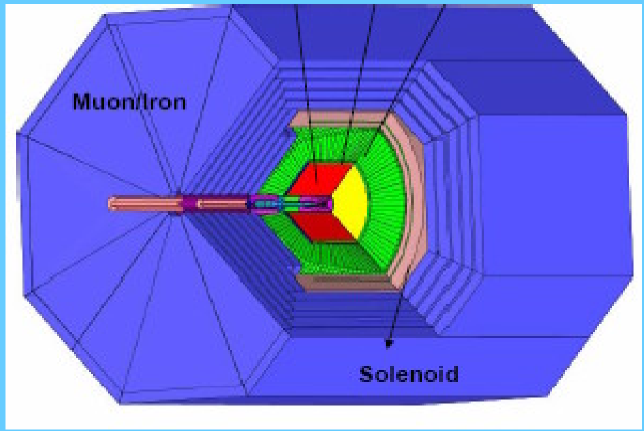
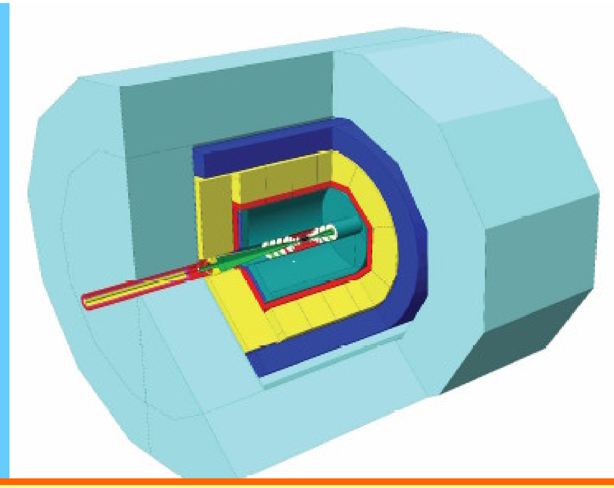


SiLC: present status & perspectives

Aurore Savoy-Navarro
LPNHE-Universités de Paris 6 et 7/CNRS-IN2P3
On behalf of the SiLC R&D Collaboration

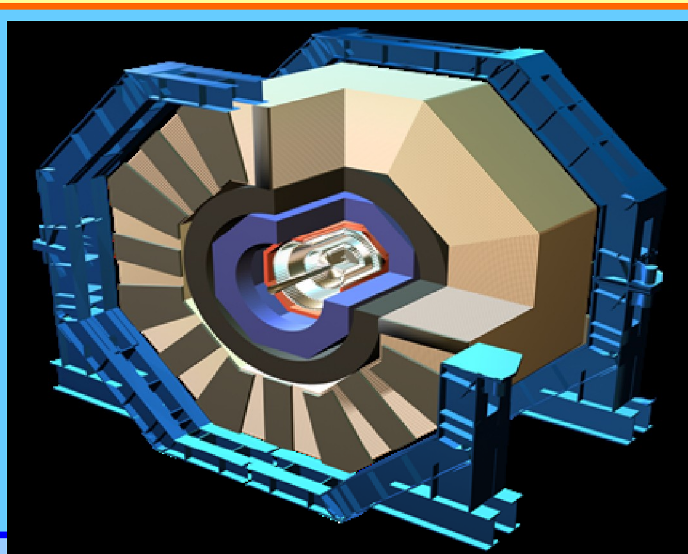
LCWS06, Bangalore, March 9 to 13, 2006





SiLC IS A GENERIC R&D COLLABORATION AIMING TO DEVELOP THE NEXT GENERATION OF LARGE AREA Si TRACKERS

It applies to ALL 3 detector concepts



- ***Main difference between the detector concepts = tracking system***
- ***SILC R&D offers a unique framework to compare their tracking performances***

SiLC R&D collaboration objectives

Europe

IMB-CNM Barcelona, Sp
HIP, Uni of Helsinki, Fi
IEKP, Karlsruhe U., Ge
Uni of Liverpool, UK
Moscow State Uni, Ru
Obnisnk State Uni. Ru
LPNHE, CNRS-IN2P3, Fr
Charles Uni, Prague, Cz
IFCA U. of Cantabria, Sp
University of Torino, It
IFIC-CSIC, Valencia, Sp
IHEP, Ac Sc. Vienna, Au

USA

U. Of Michigan, Ann Arbor
SCIPP & UCSC Santa Cruz

Asia

Kyungpook U. Taegu, Ko
Yonsei U., Seoul, Ko
Korea U. Seoul, Ko
Seoul Nat. U., Seoul, Ko
SungKyunKwan U. Seoul
Tokyo U. (Japan)
HAMAMATSU (Japan)

Close contacts with:
FNAL Si Lab team
SLAC SiD Team
CERN LHC & Microelectronics teams

Industrial firms (in progress)

R&D Objectives:

- R&D on sensors
- R&D on associated electronics
- R&D on Mechanics

and developing the needed tools:

- Laboratory test benches
- Alignment and position monitoring
- Simulations
- Cooling and other related integration tools

Synergy with the LHC present construction and future upgrades

R&D on sensors

HIP Helsinki & VTT, IMB-CNM/CSIC, SiLAB-Moscow State U., ETRI (Korea) , Hamamatsu Japan, (UK & Italy ?)

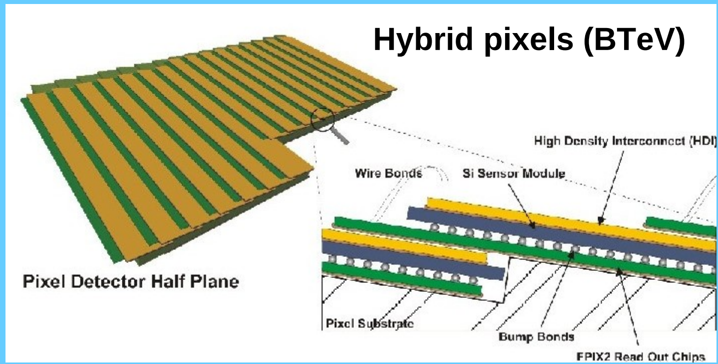
SENSOR TECHNOLOGIES:
Silicon strips are the baseline with:
Larger size wafers, single sided, thinner/thinning
New technos in some regions (pixelization)
New Hybrid Pixels, DEPFET, MAPS/FAPS, SOI

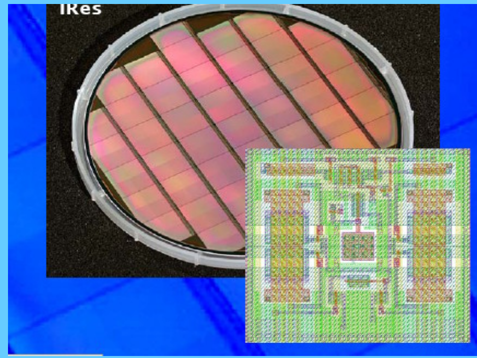
STRATEGY:
The research Labs develop & test new ideas
Transfer to small Fabs for reduced production
Large production, high quality and reliability:
HAMAMATSU Monopoly
But attempt to create alternative

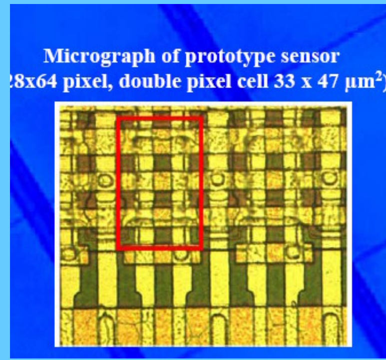
SiLC will make use as much as possible of the new sensors for constructing the Si tracking prototypes for test beam

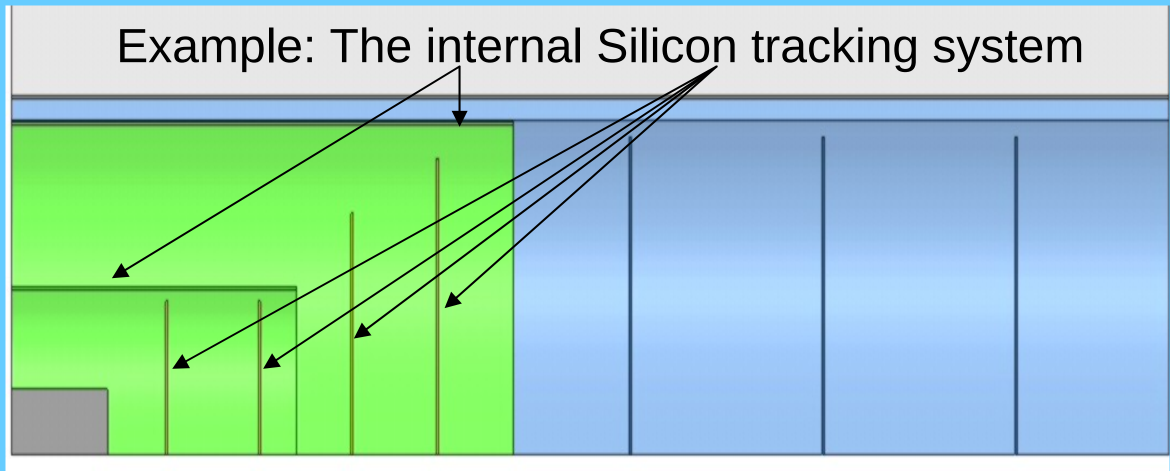
USE of PIXELS

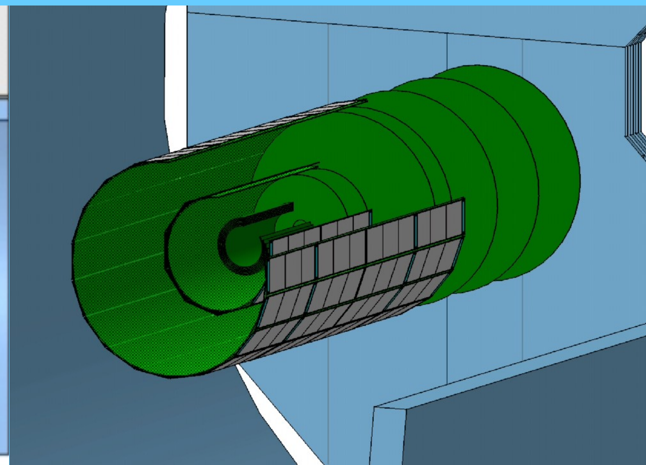
IFIC-Valencia, HIP Helsinki, Liverpool, MPI Munich









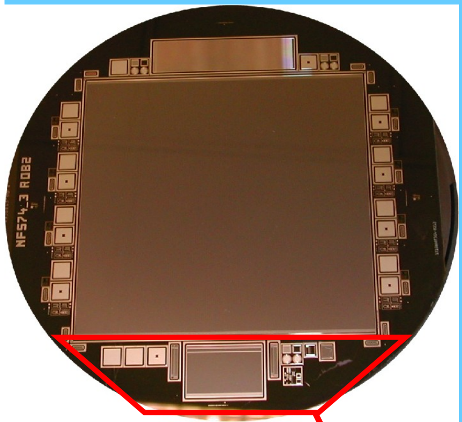


Small prototypes with different pixel technologies will be tested for the EUDET project

R&D on sensors cont'd

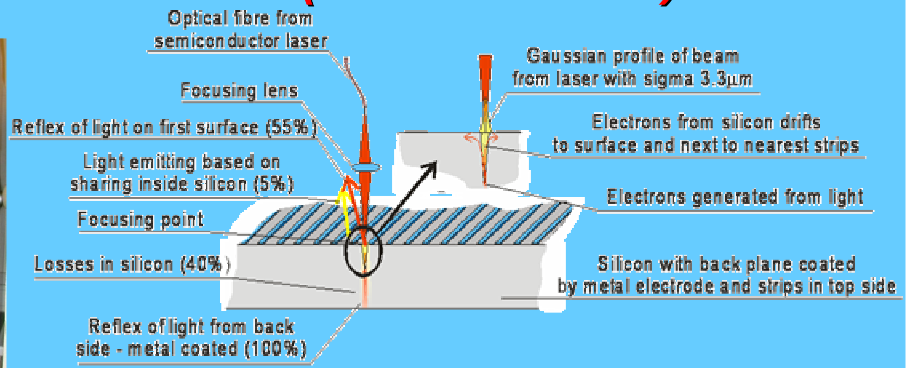
- **Test Quality Control of fab. Line**

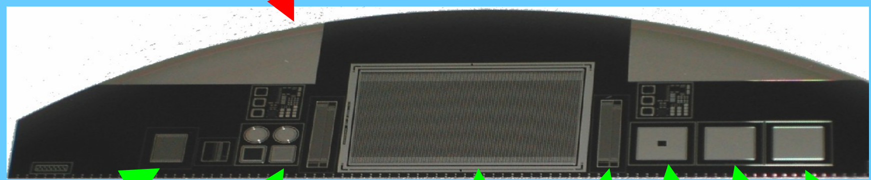
(IEKP Karlsruhe, IHEP Vienna + others)



- **Sensor characterization with LD1050**

(most SiLC teams)

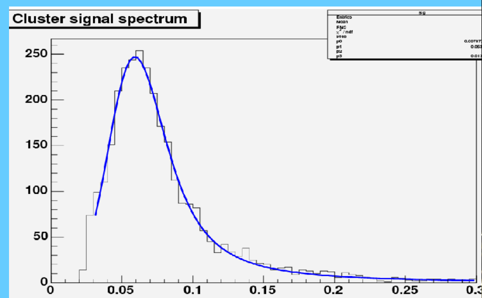


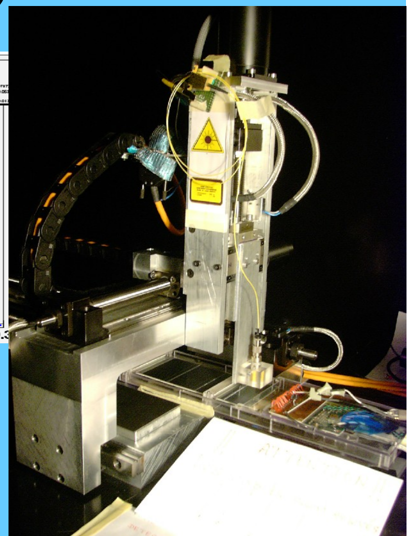


TS-CAP | sheet | GCD | CAP-TS-AC | baby | CAP-TS-AC | diode | MOS in | MOS out

Detailed test structures allowing full characterization & quality test of the production line.

- **Sensor characterization with radioactive sources** ***(Prague, Paris, HIP & many others)***





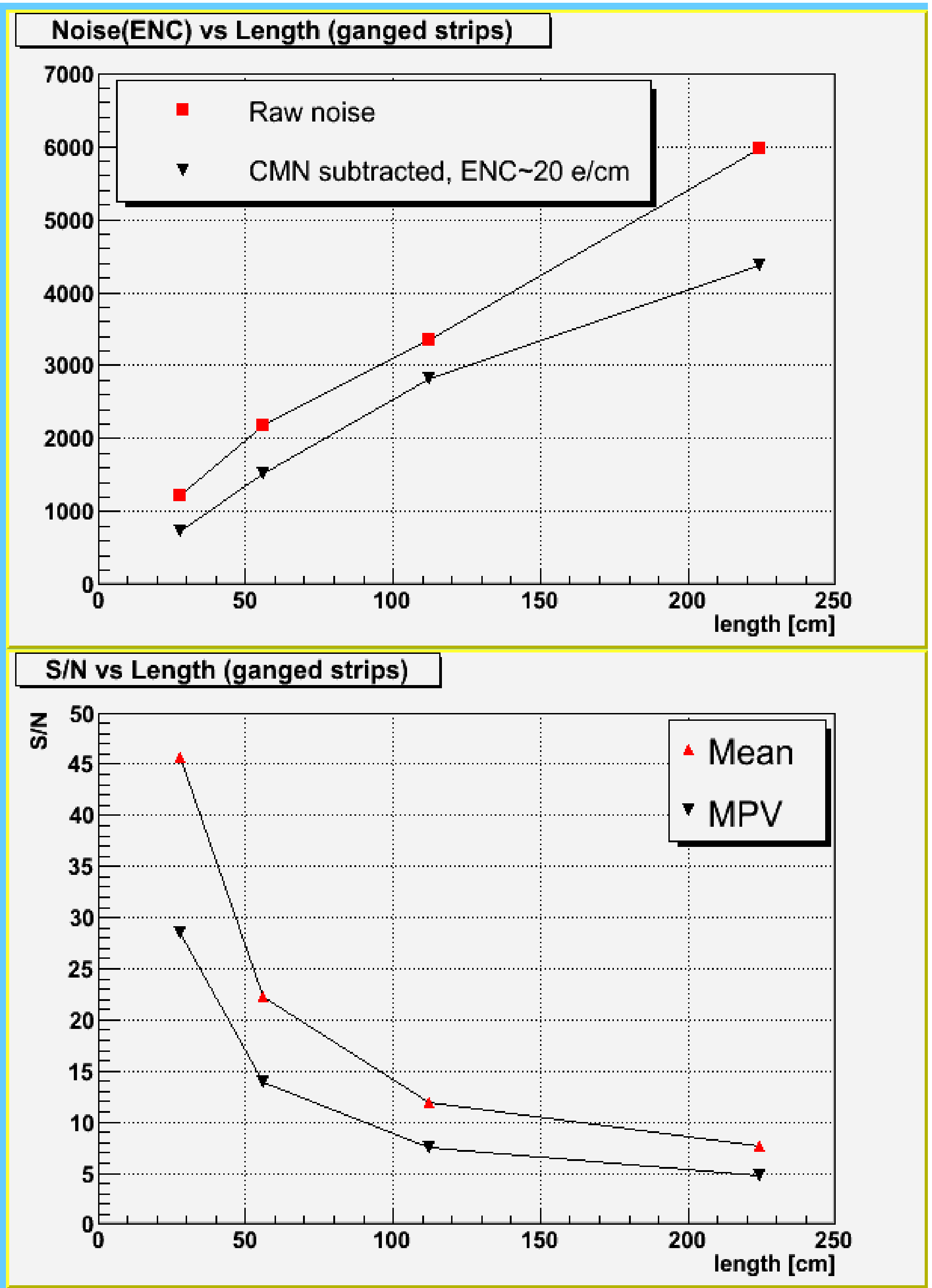
All these test facilities will be used and further improved to test new wafers (not only strips)

Sr ^{90} Source tests
(*Paris-Prague*)

- **Noise scales with strip length: ENC~20 e/cm**
- **S/N drops below 10 for 224 cm**
- **Noise optimisation of the setup needed**
- **Improved FE electronics (here VA_64hdr)**

(Z. Dolezal & F. Kapusta)

Forthcoming test beams for confirming these Lab test bench results

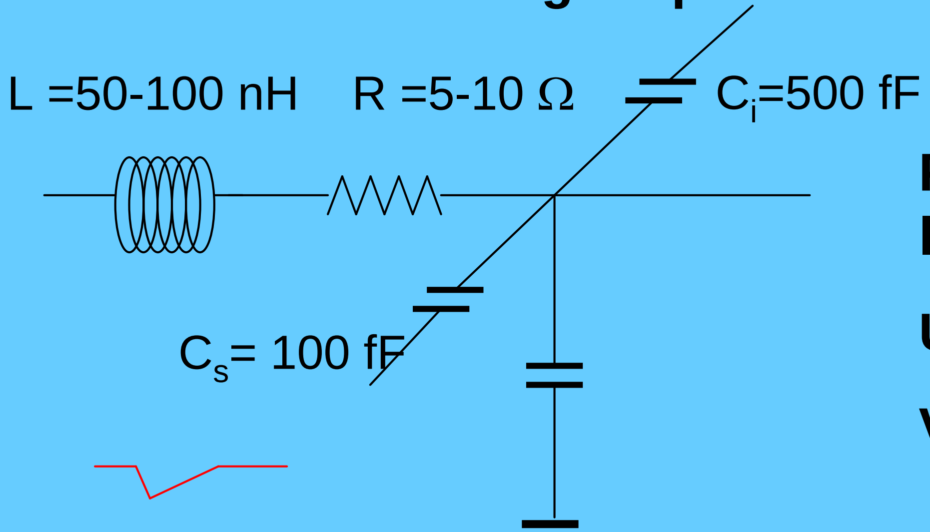


Position using Timing

Jacques David, Jean François Genat, Frederic Kapusta, Hervé Lebbolo,
François Rossel, LPNHE-Paris

Detector linear model (Spice) :

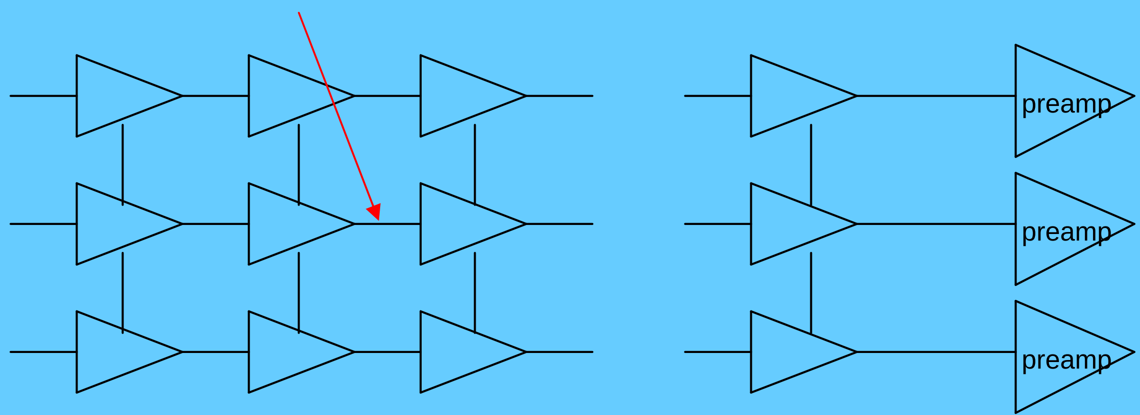
1cm long strip cell: Delay line element: R, L, Ci, Cs



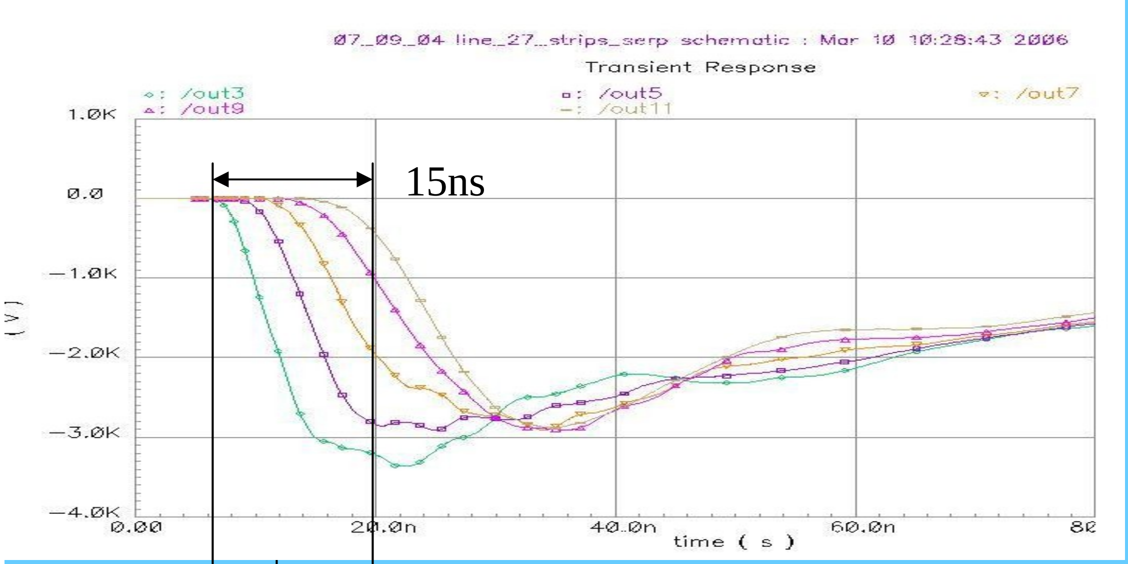
Pulse velocity in a simple LC line: V a 1/sqrt(LC)

Using L = 50 nH, C = 100 fF,

$V_{calculated}$ = 14ns/m (no interstrip)

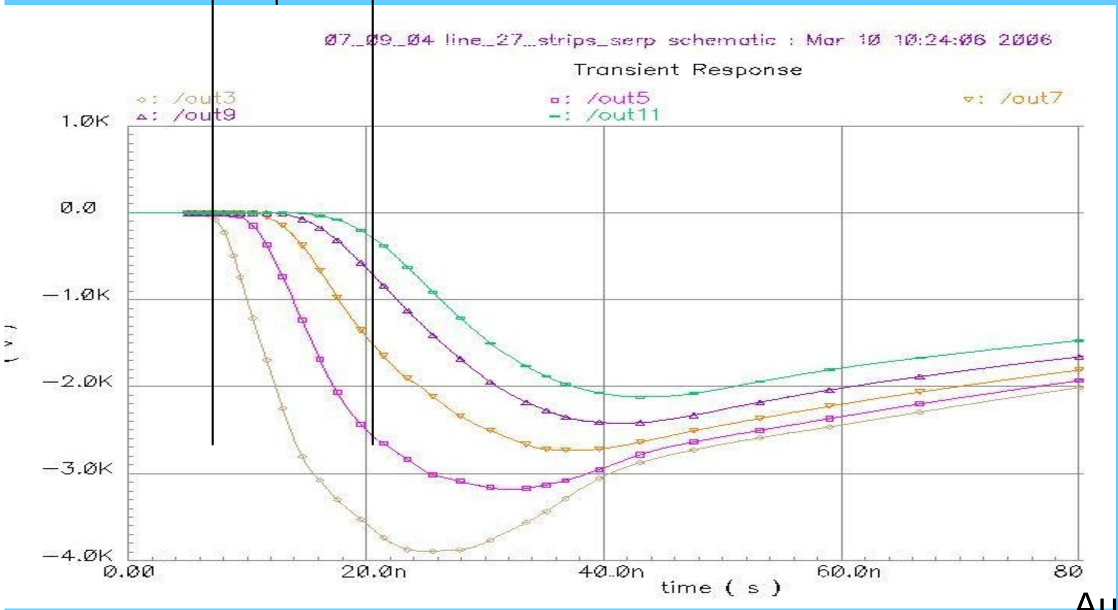


Simulated pulse propagation along a 80cm strip detector



L=50nH/cm
C=100fF/cm
R=5.6W/cm

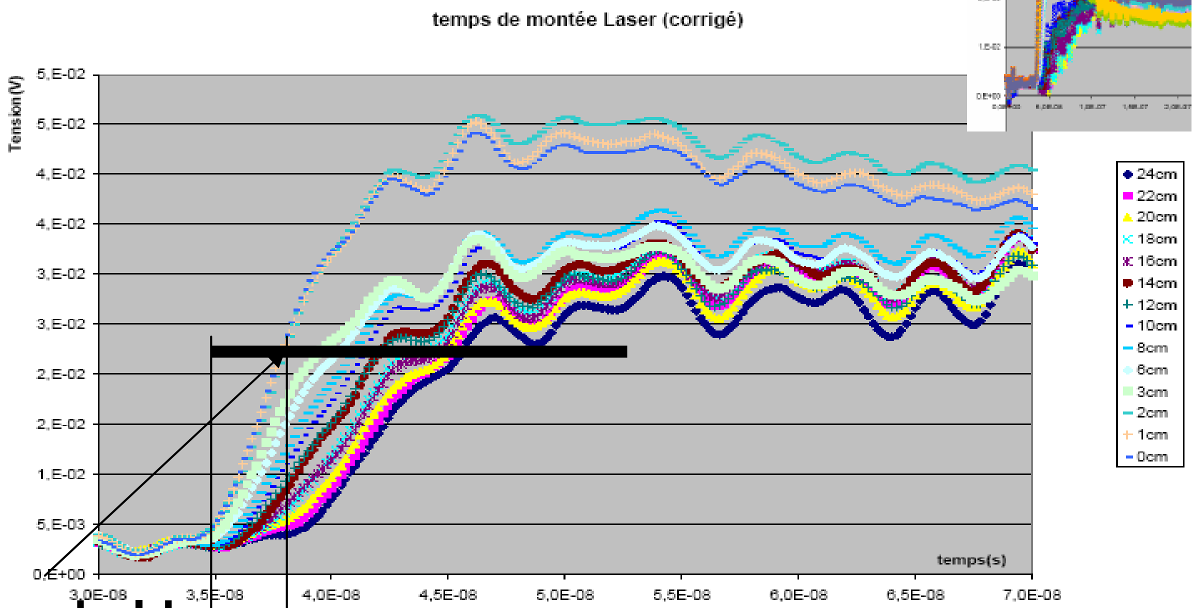
Conclusions:
- Line propagation at 18ns/m velocity
- Damping if strip resistive

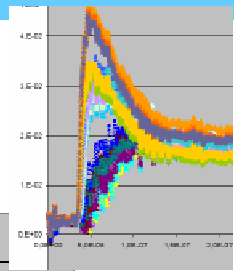


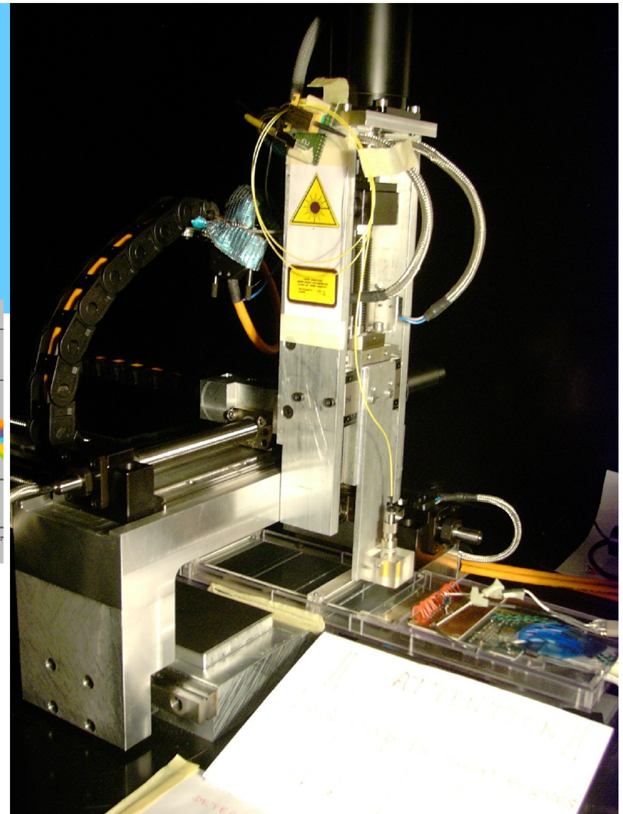
L=50nH/cm
C=100fF/cm
R=13W/cm

Measured Pulse Velocity on Lab test bench: reality

Measured velocity: 22ns/m







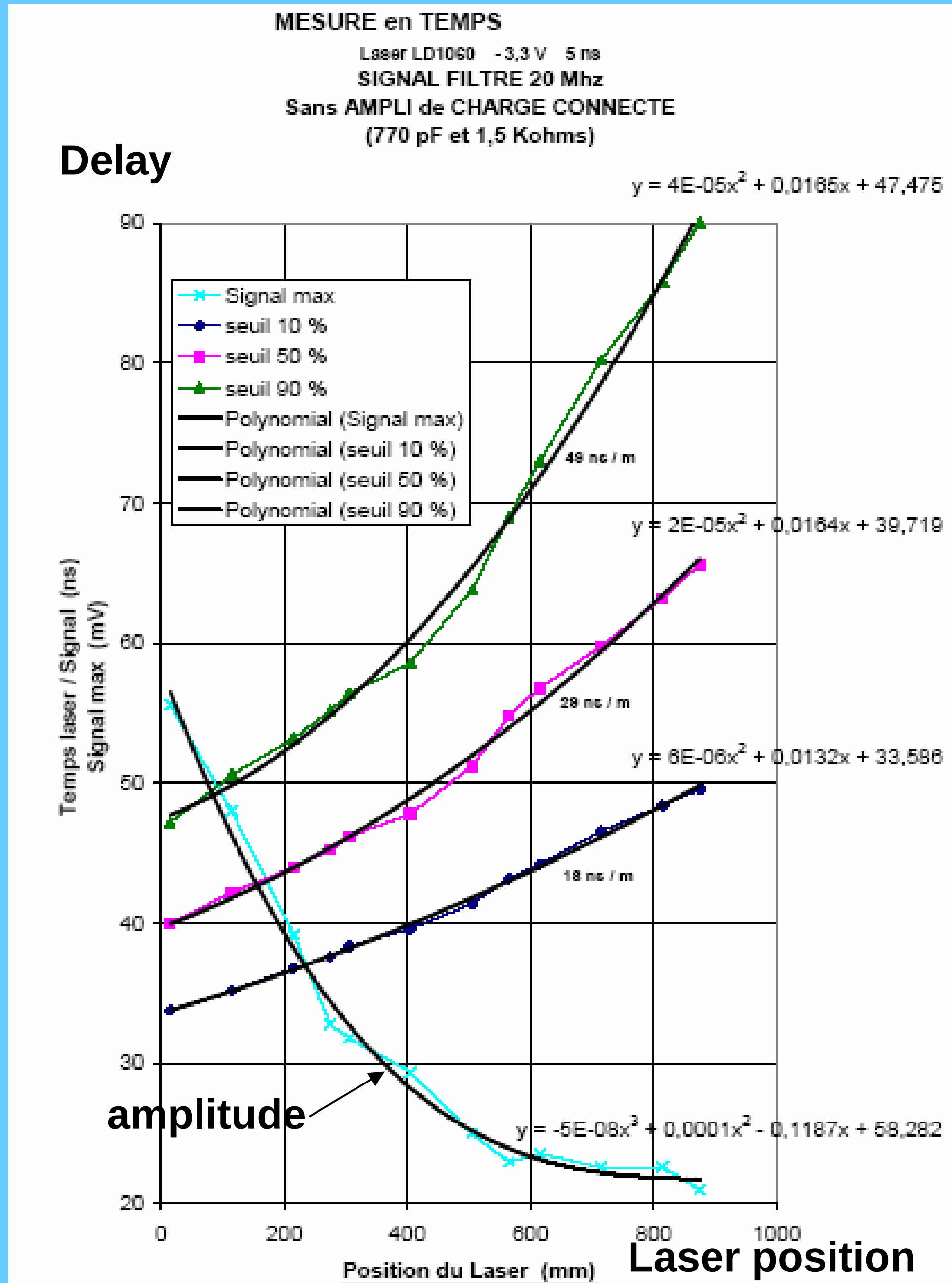
Threshold

Δt

Jacques David: SiLC Paris meeting 02/06

4.5 cm/1ns Measured moving a laser diode along 24 cm strip

Measured delay and amplitude



Constant Fraction Threshold measurement after filtering the pulse

Green: Threshold 90%

Pink Threshold 50%

Black Threshold 10%

Blue: Damping

Electronics Timing resolution

Multiple sampling simulated with the following assumptions:

- 180nm CMOS technology front-end chip
  Noise: as measured 375 + 10.5 e-/pF,

  Assume S/N = 25 at 30 pF detector

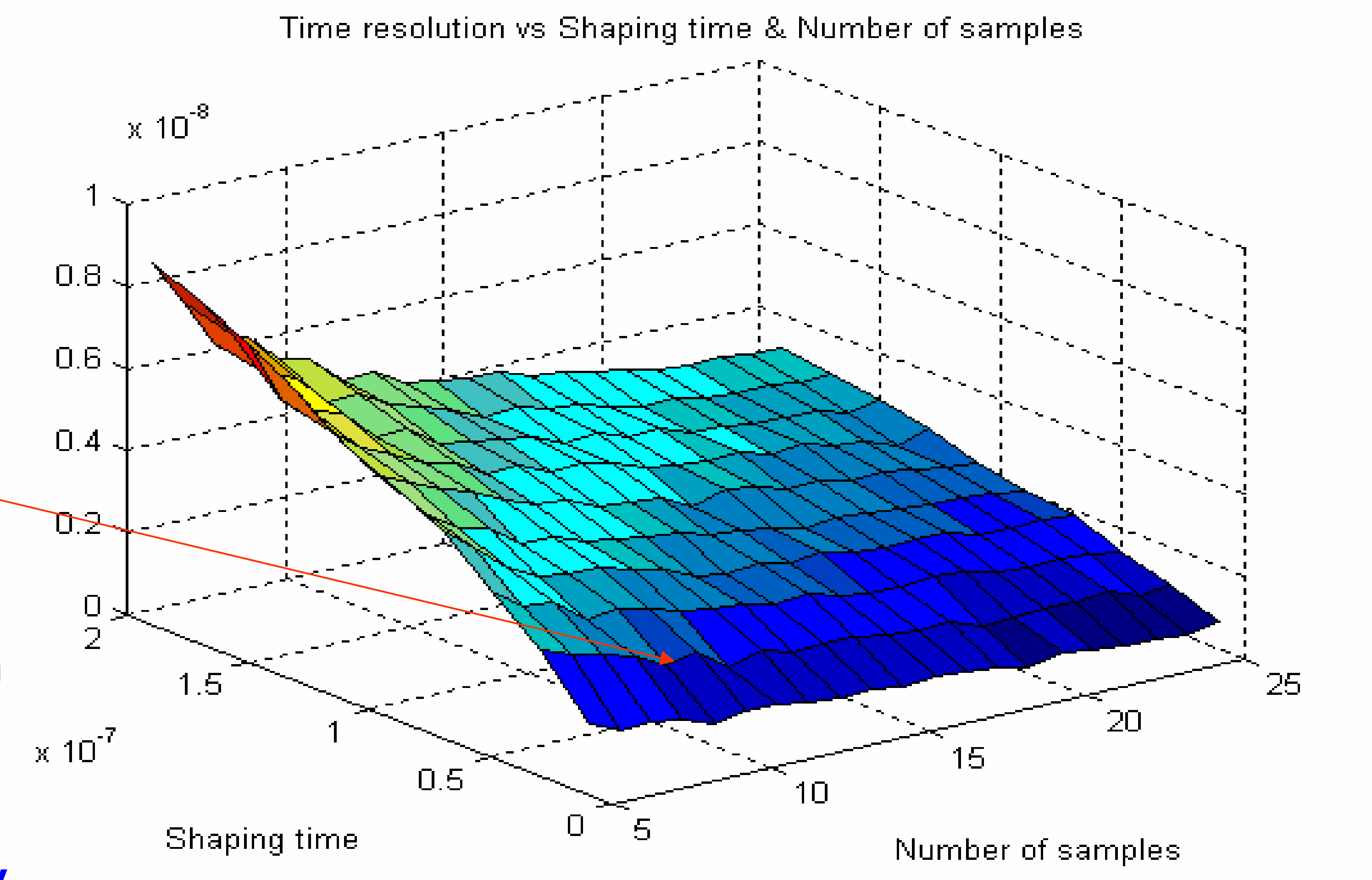
- n-points pulse sampling over 2 shaping times
  + least squares minimization time estimation

Simulated electronics time resolution

Simulated time resolution of the whole electronics chain using multiple sampling and least square fit algorithm (Bill Cleland)

- **S/N =25**
- **8 samples**
- **50 ns shaping**

⟶ **1.8 ns time resolution**



Improves with actual ILC Silicon detector events time distribution

SiGe technology

Next…

- Stimulate with 25,000 electrons, amplify with “ideal” electronics (ORTEC…)
- Reconstruct measurement using multiple sampling and LSQ algorithm from digital oscilloscope after shaping
- Implement chip in SiGe if successful…

R&D on Mechanics

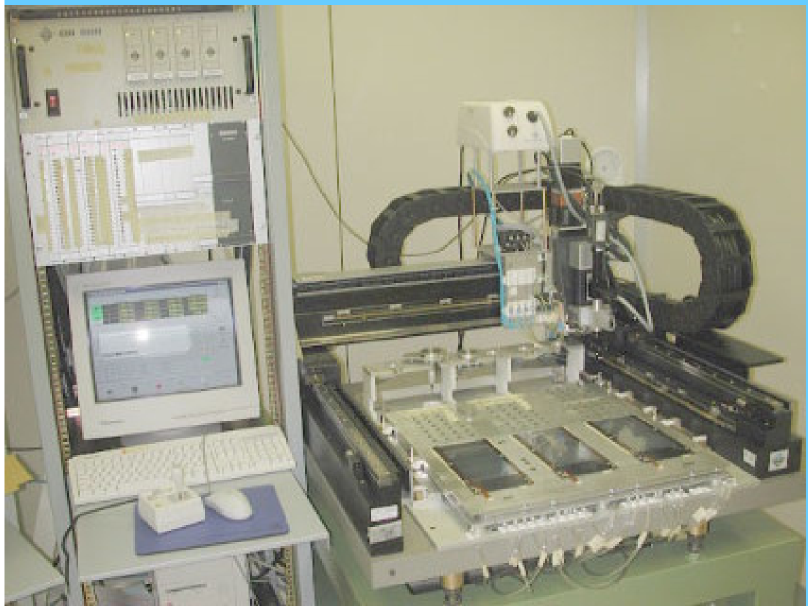
LPNHE-Paris is going to be joined now by several LHC teams of SiLC

- Developing the elementary module
- CAD design studies of the various components (light & large mechanical structure) and,
- Prototype design and construction
- Cooling thermo mechanical studies
- Related positioning, alignment and
- integration issues (with other subdetectors

  for combined test beams)

The elementary module: tile of the overall architecture

Based on present experience (LHC) must be light, precise, robust, easy to build & assemble:

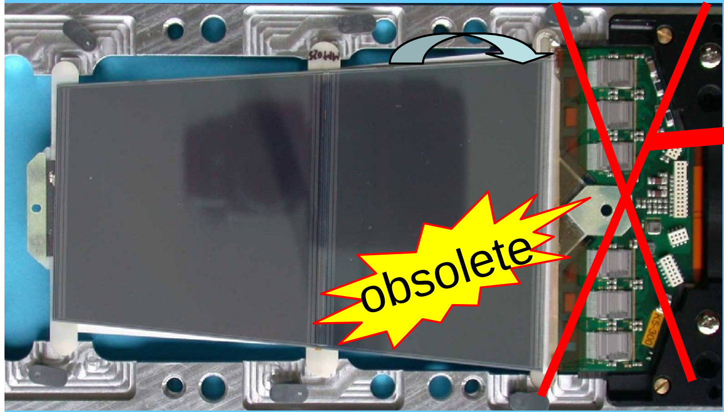


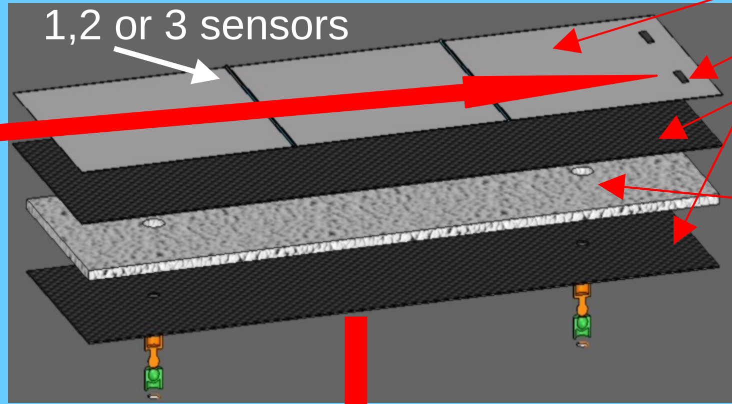
Robotic assembly (CMS)

- **New sensors (next generation)**
- **Support: new material &design**
- **VDSM FE electronics & wiring**
- **Precise positioning on the module & the support structure**
- **Easy to build (robotisation ?)**
- **Industry transfer: big number**
- **Favouring a ‘’universal tile’’ (instead of different shapes)**

R&D on the new elementary module concept

LPNHE-Paris, IMB-CSIC, and others in SiLC



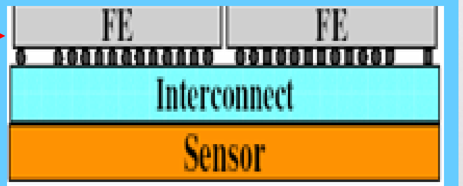


Si sensors: 0.2%X0
FE chips: ~0.1%X0+?
Foam Rohacell
0.05% X0 thick ~4mm
C fibre 0.15% X0
thickness ~ 0.4mm

Total ~ 0.55 %X0

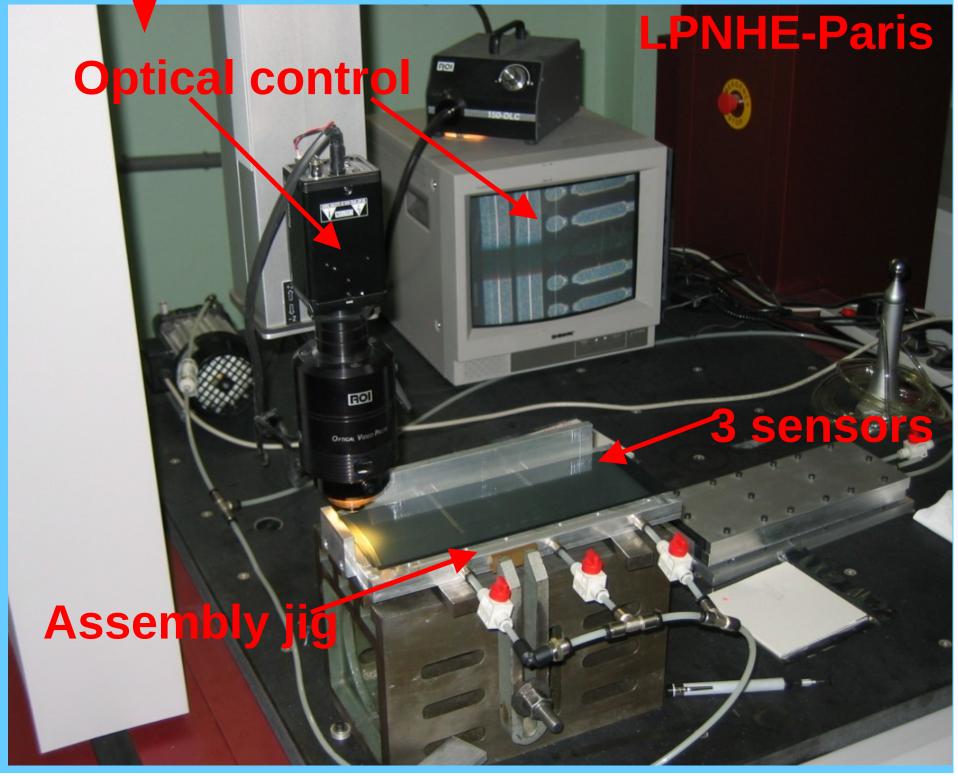
New wiring of FE chips onto the detector under investigation:

Conservative:
Large chip 2.5x0.625cm^2
≤ 0.13µm tech, 1024 ch
will sit on detector
using flip chip bump bonding



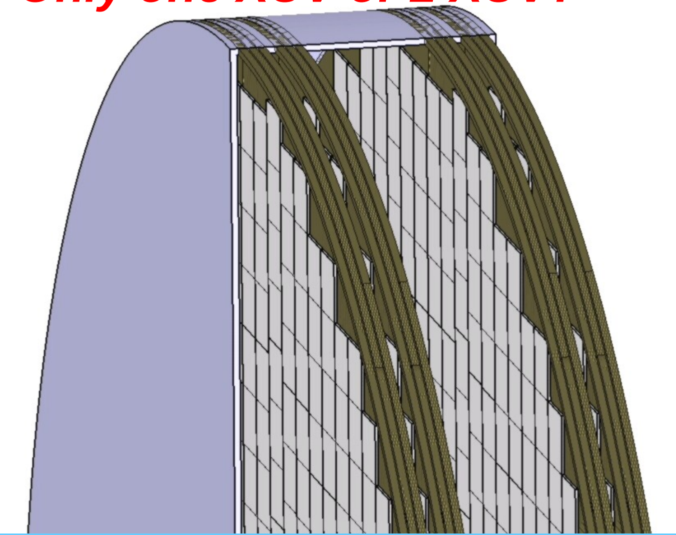
Or 3D integration technology when available

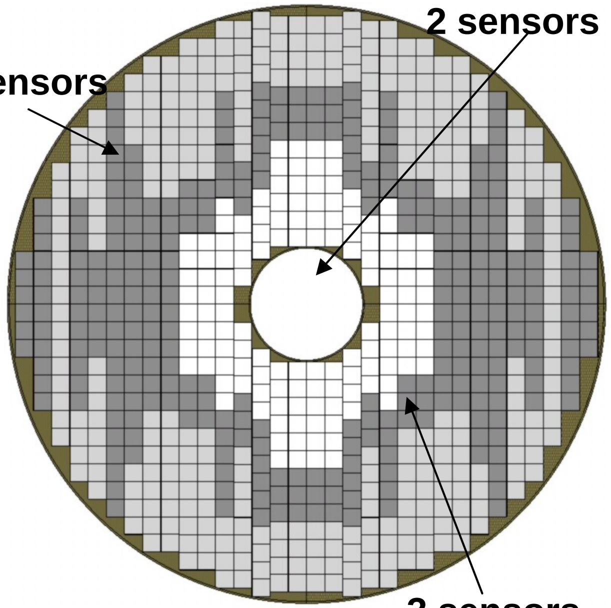
Serial links used wherever possible to avoid multiple wire connexion improving transparency & reliability



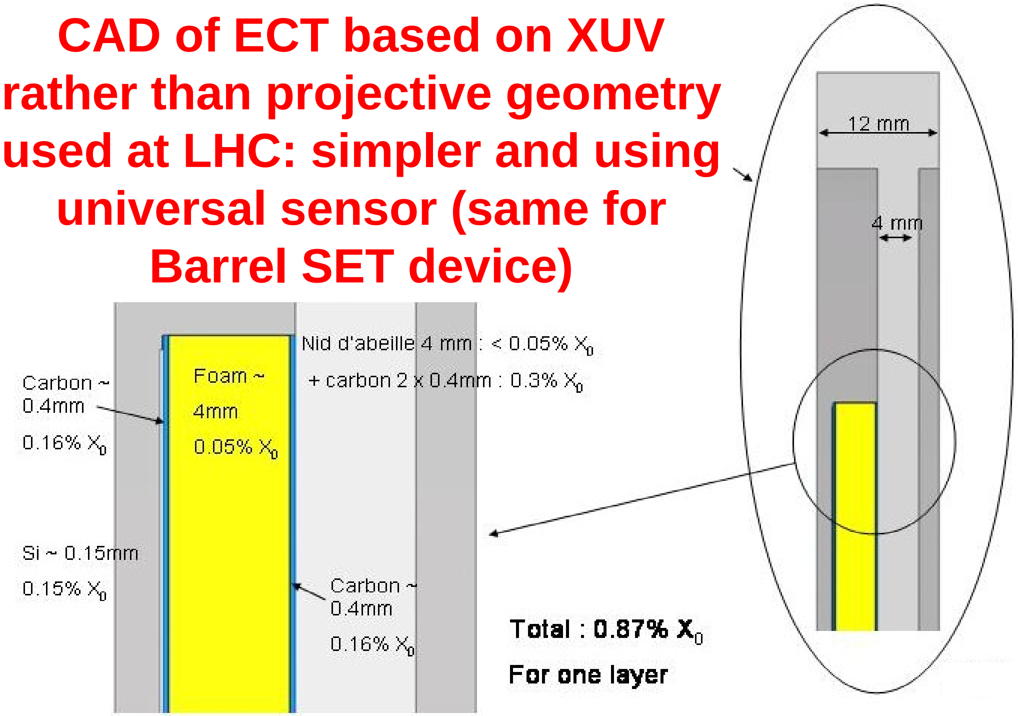
R&D on Mechanics: End Cap Tracker *LPNHE-Paris*

Only one XUV or 2 XUV?





CAD of ECT based on XUV rather than projective geometry used at LHC: simpler and using universal sensor (same for Barrel SET device)



Total area per XUV: ~15 m2

Nb modules x 2, 3 or 4 (10x10 cm^2)/plane:68, 88, 92

Total modules/plan: 248 (248 µchips)

Total µchips/plan: 248 (1 per module)

Total Nb of channels/plan: 253952

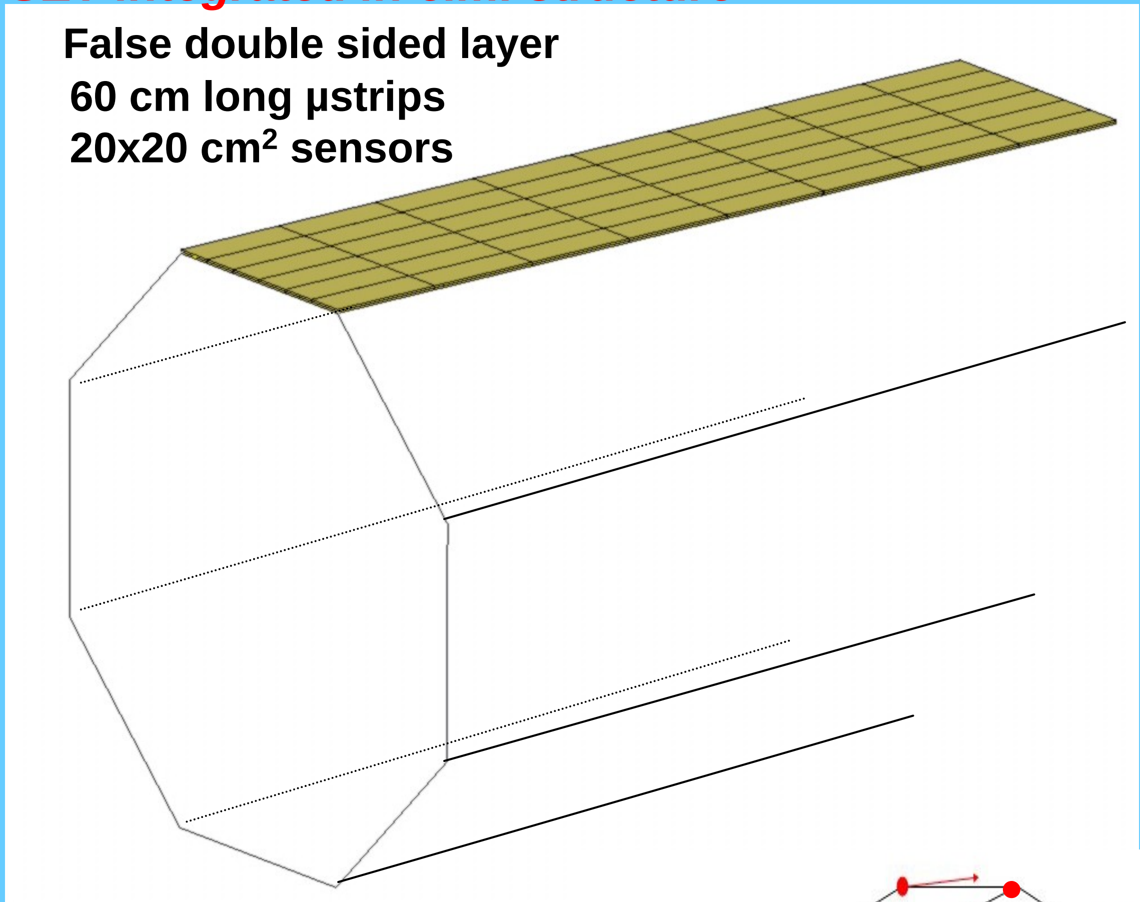
Total Nb of channels/XUV: 661856

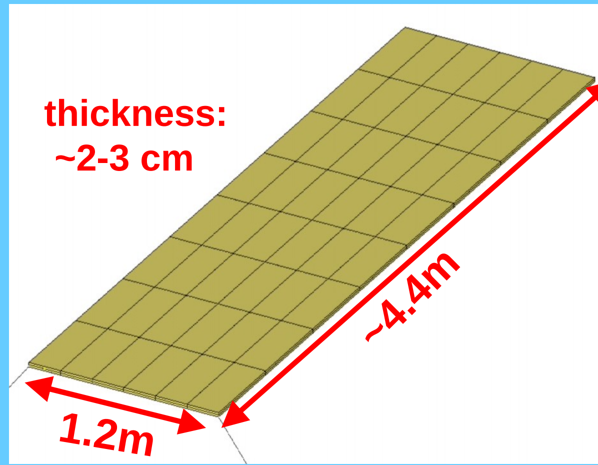
All these numbers X 2 because 2 sides!

Under design: octagonal ECT planes with 20x20 cm2 sensors (10''), 1 or 2 sensors/module & less channels

R&D on Mechanics: CAD of SET component *(LPNHE-Paris)*

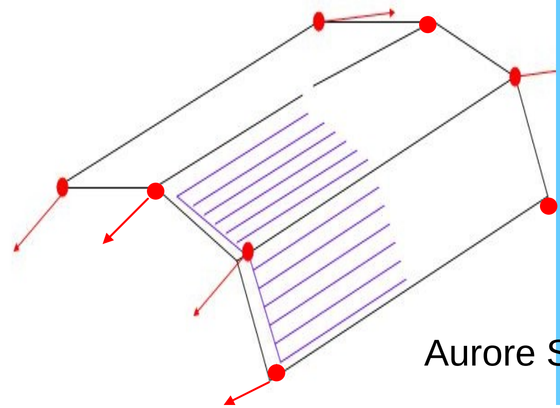
SET integrated in e.m. structure



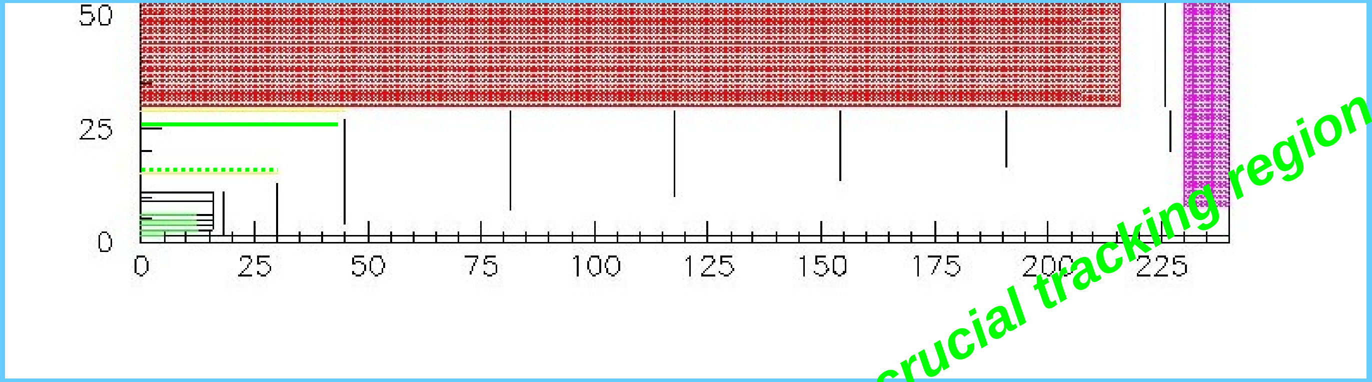


# ladders/octagone	96
# sensors/octagone	288
# channels/octagone	196608
# µchips/octagone	192
# µcoax/octagone	192
# fibres/octagone	2
# µchips/fibre	96
# voies/fibre	98304

Total surface: ~86 m^2
Nb channels: 1,572864
Nb of fibres: 8 per side



R&D on Mechanics: Inner Si components

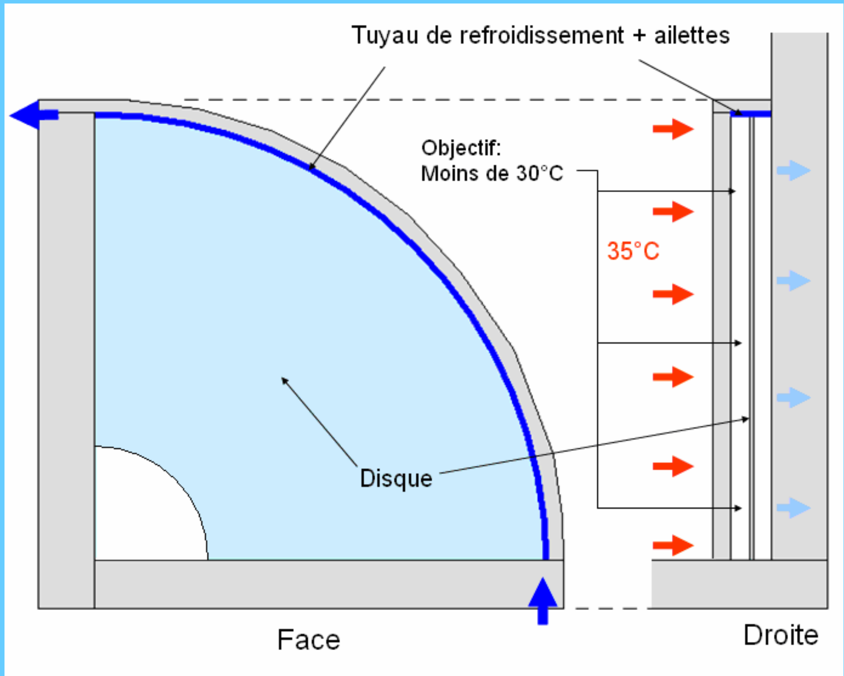


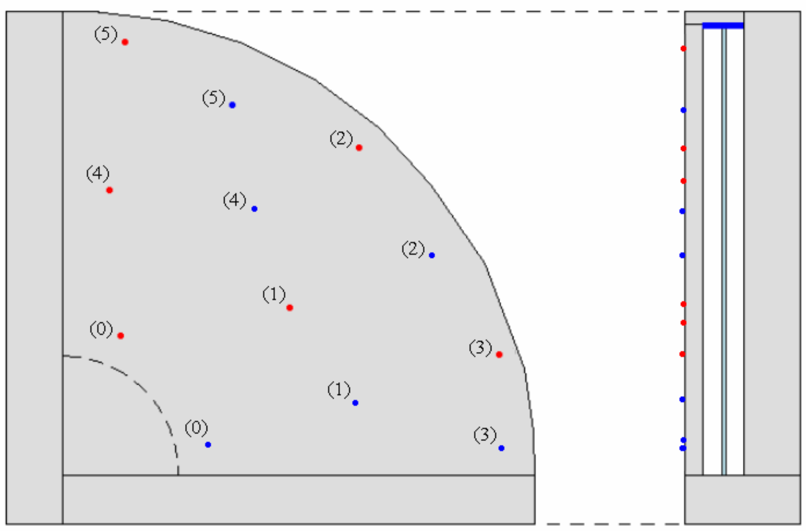
Lots of very important studies in this crucial tracking region

A number of questions:
What technology(ies) ??
For inner layers (outer one could stay in standard double sided technology
But interest to explore applying pixel technology(ies?) to the inner layer(s)?
Also for the first disks near the vertex detector
Some answers from simulations (see later)
Interest to have an extension in the very forward region with disks just in front of the very forward subdetector.

COOLING STUDIES: End Cap tracker

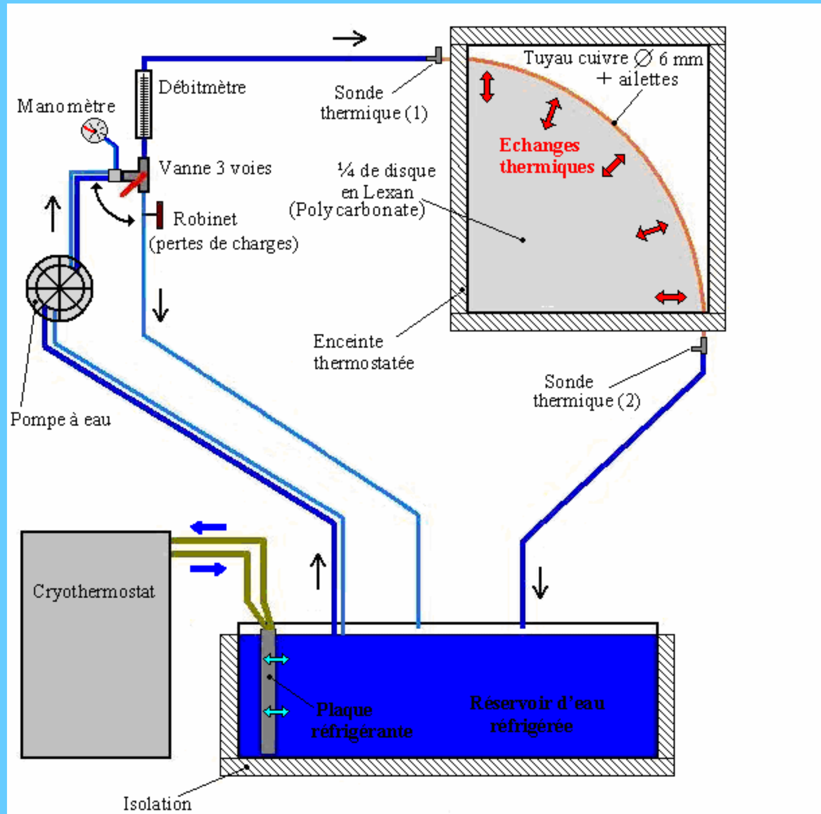
Guillaume Davée, Guillaume Daubard
& Mechanical staff LPNHE-Paris

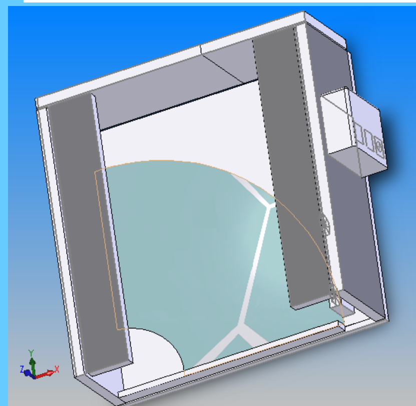


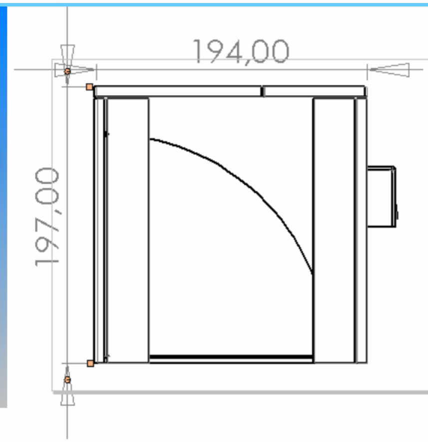


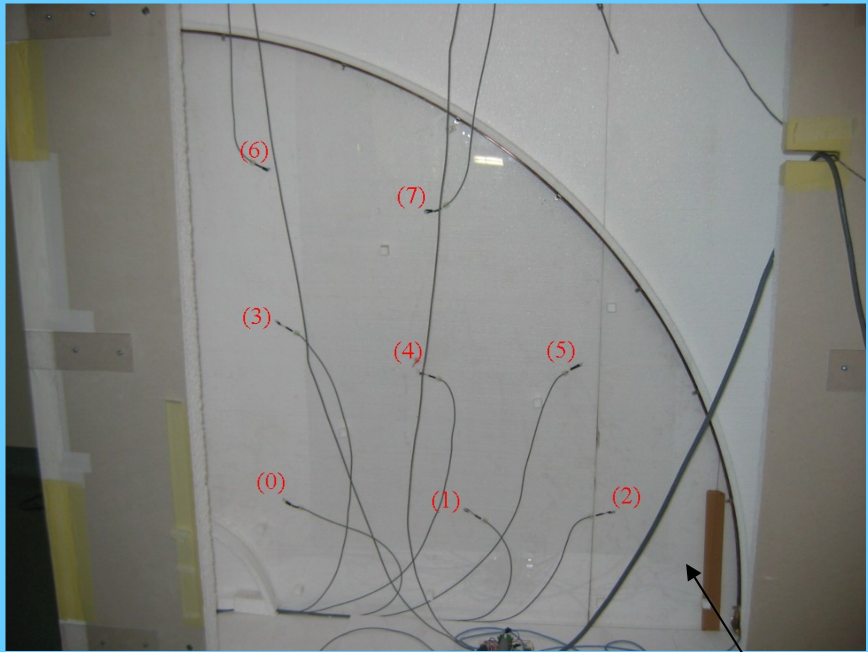
• : 1ère série de mesures

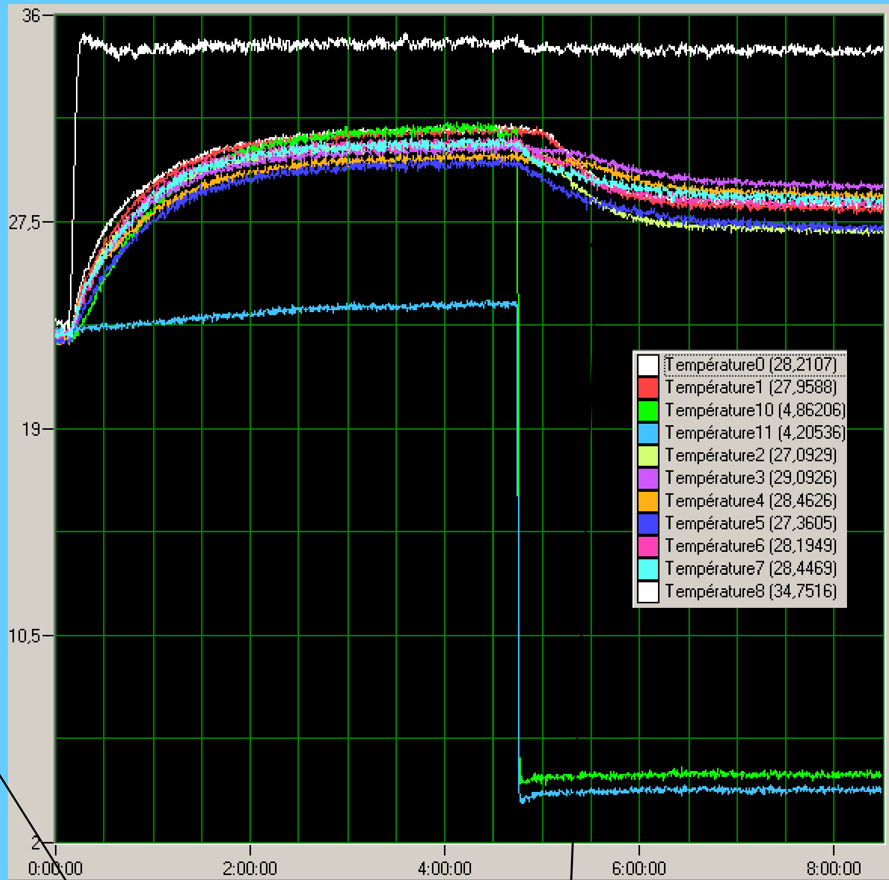
• : 2ème série

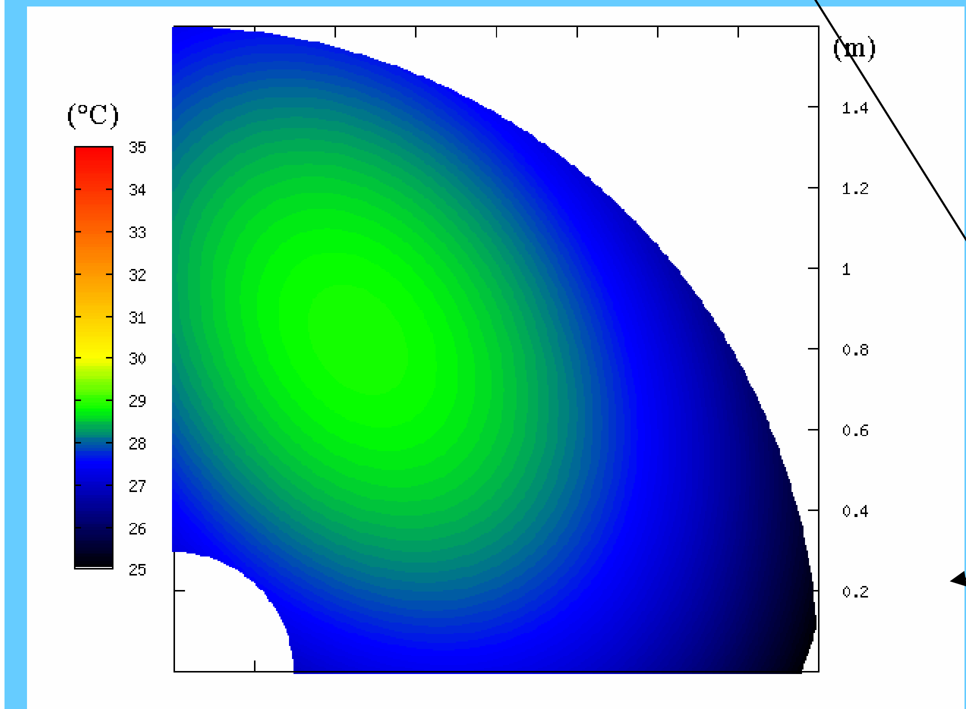










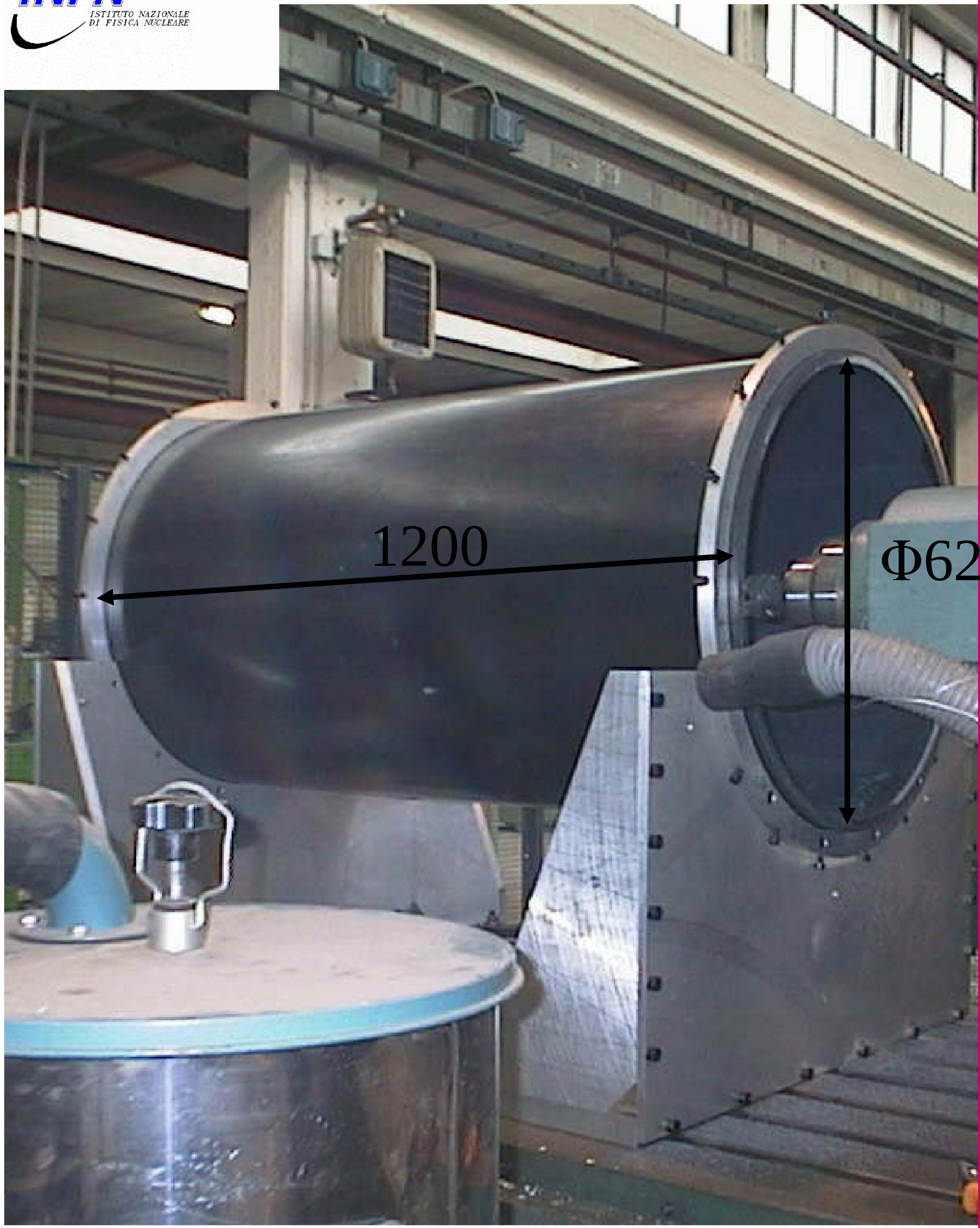


Measurements, results and modelling

Aurore Savoy-Navarro, SiLC, LCWS06, Bangalore

THE SSD CYLINDER

Courtesy of Giuseppe Giraudo
INFN-Torino (ALICE)

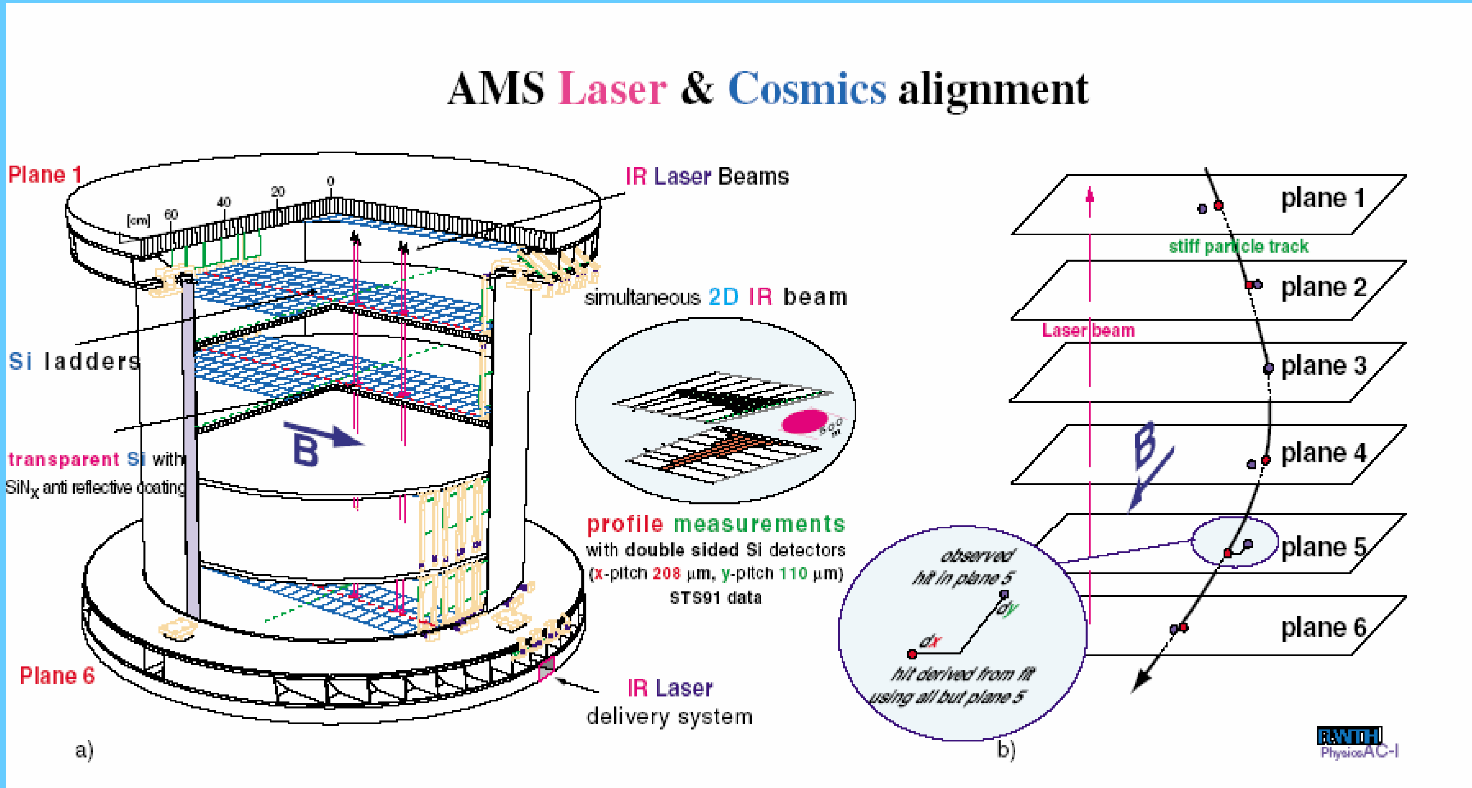


4+4 PLIES => 1,2 mm
ROHACELL => 5 mm
$0,5\%\ X_0$
WEIGHT = 10 kg

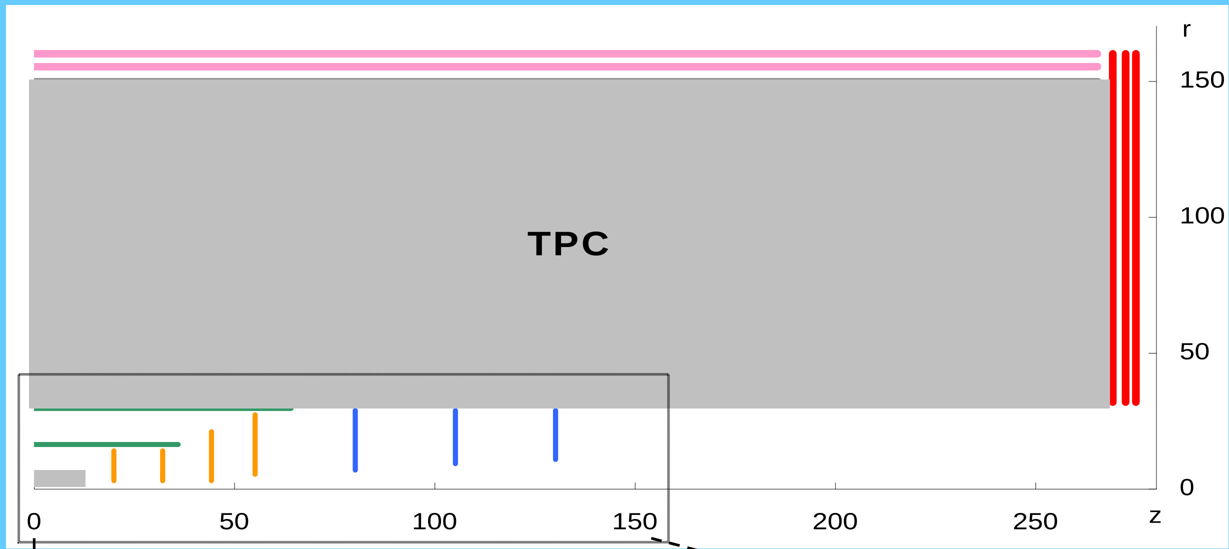
Alignment for Si sensors

IFCA-Santander (courtesy of Ivan Vila)

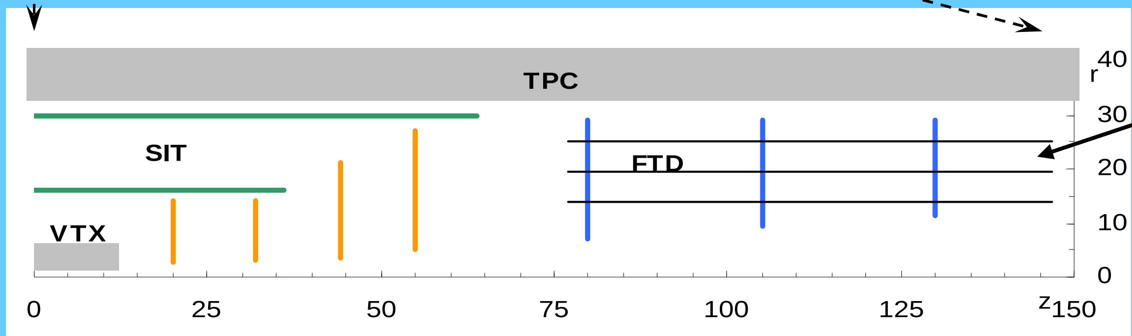
- Usage of collimated laser beams (IR spectrum) going through silicon detector modules. The laser beams would be detected directly in the Si-modules.
- Based on previous AMS-1 experience we can project that few microns (<2 um) resolutions would be achieved.



- ***Main advantages:***
  - Particle tracks and laser beam share the same sensors removing the need of any mechanical transfer.
  - Minimum interference with Silicon support structures
- ***Start up plan:*** feasibililty study (optical treatment of the Si wafer, test stand to determine achievable position resolution).



Proposal: Connecting other sub-detector units (barrel –forward) using steering optics Angular tilts using inclinometers.



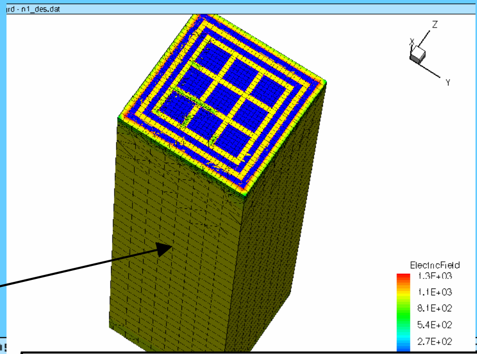
Laser lines

Alignment system for combined tracking tests Si-tracking+TPC will be applied for EUDET

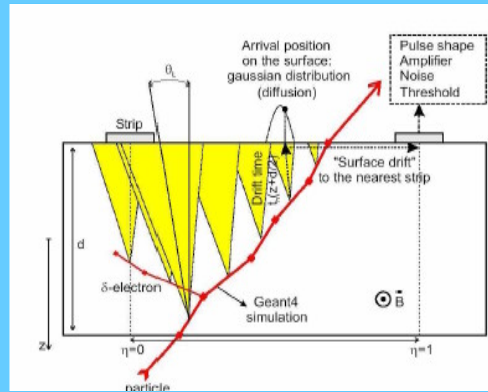
Si detector & electronic component simulation:

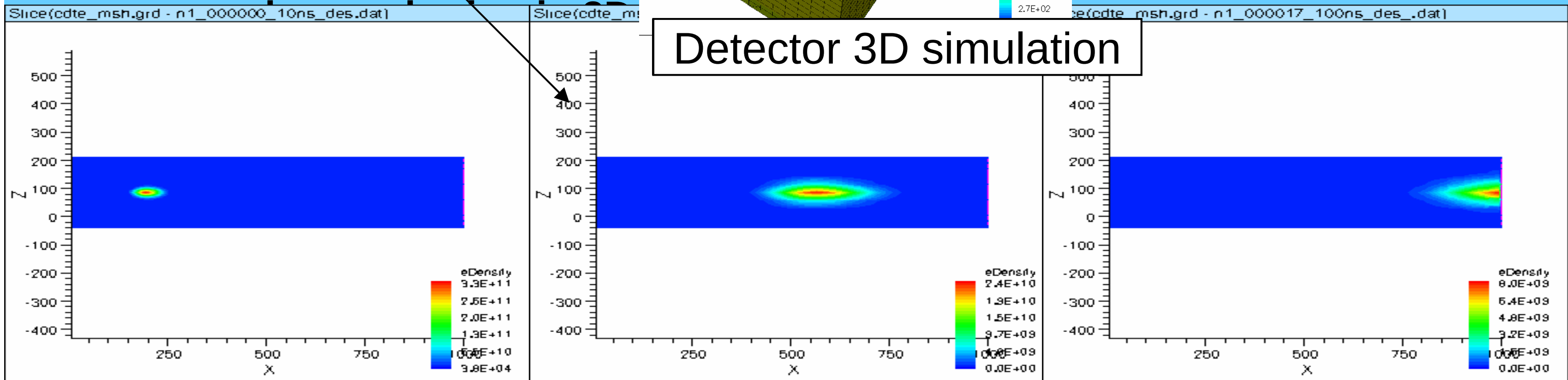
(ex: IMB-CNM, Helsinki, Karlsruhe, Prague, Paris)

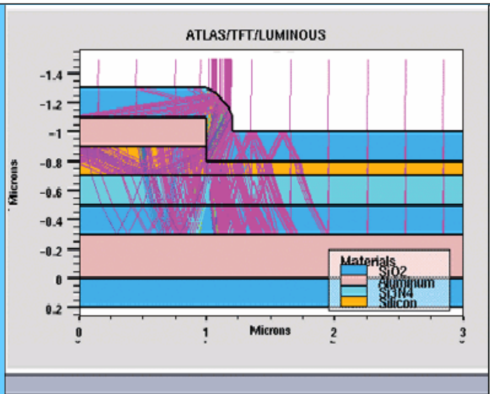
- ISE-TCAD, TMA, Silvaco
- Technology simulation
- Electrical simulation
  - Charge collection

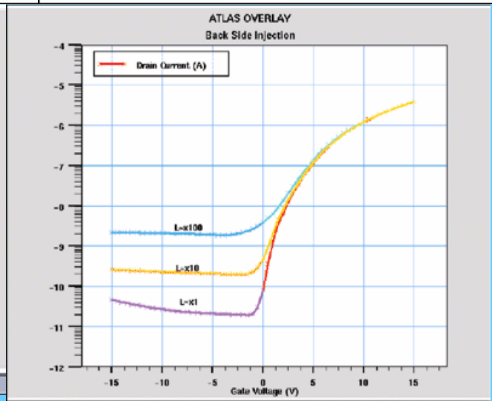


Detector 3D simulation





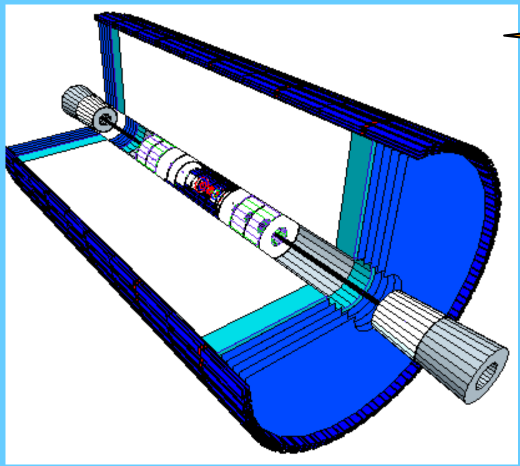




3D simulations of detector responses on adjacent strips
Crosstalk, substrate thinning
Pulse propagation along the strip
Sensitivity analysis (temperature, biasings, supplies…)
Matching of detector to preamp
Spice model of the detector

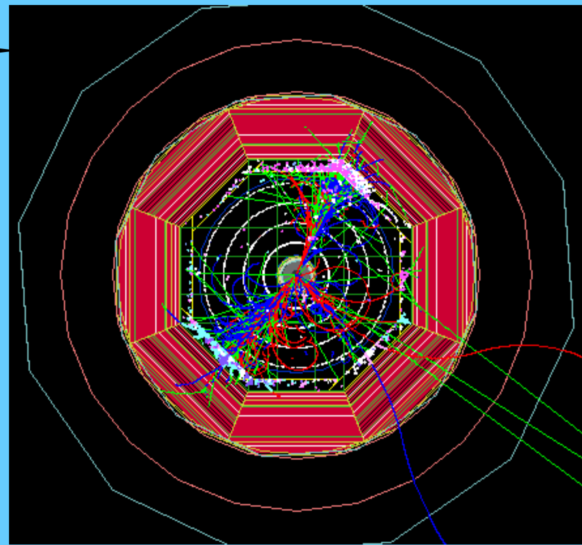
SIMULATIONS

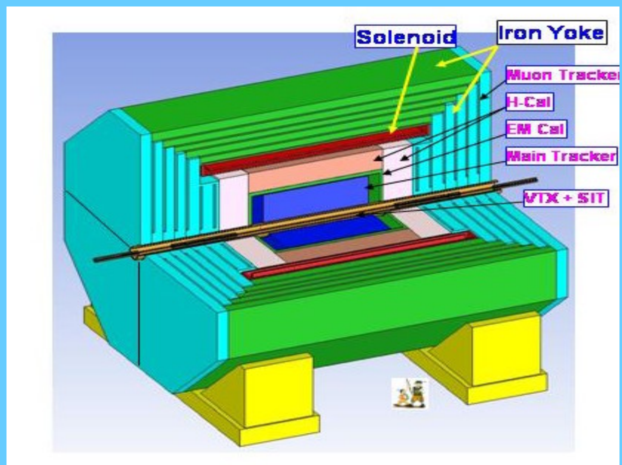
Obninsk St Uni., IHEP-Vienna, LPNHE-Paris, developing collaboration with LHC Si tracking experts



But still lacking:
pattern recognition & reconstruction prog.

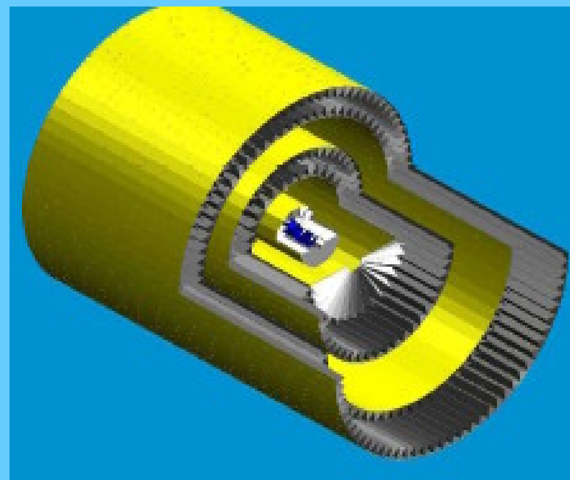
New direction:
Standalone Si tracking reconstruction inclu-ding the µvertex





With or without TPC:

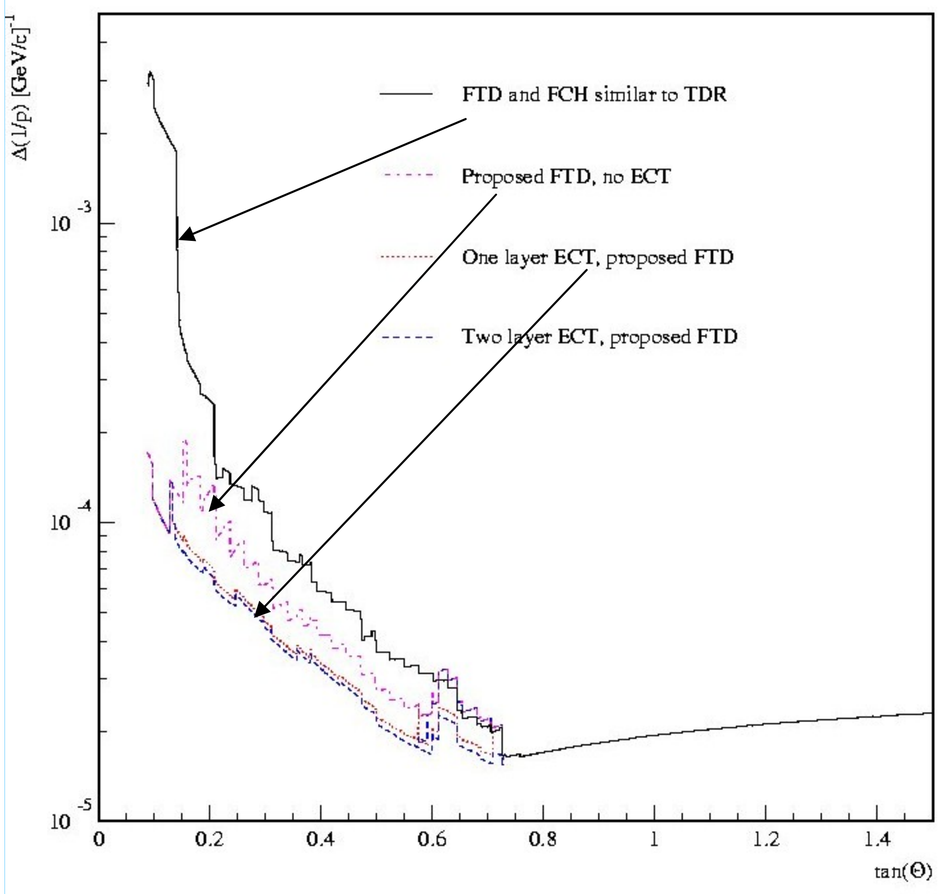
How it compares ?

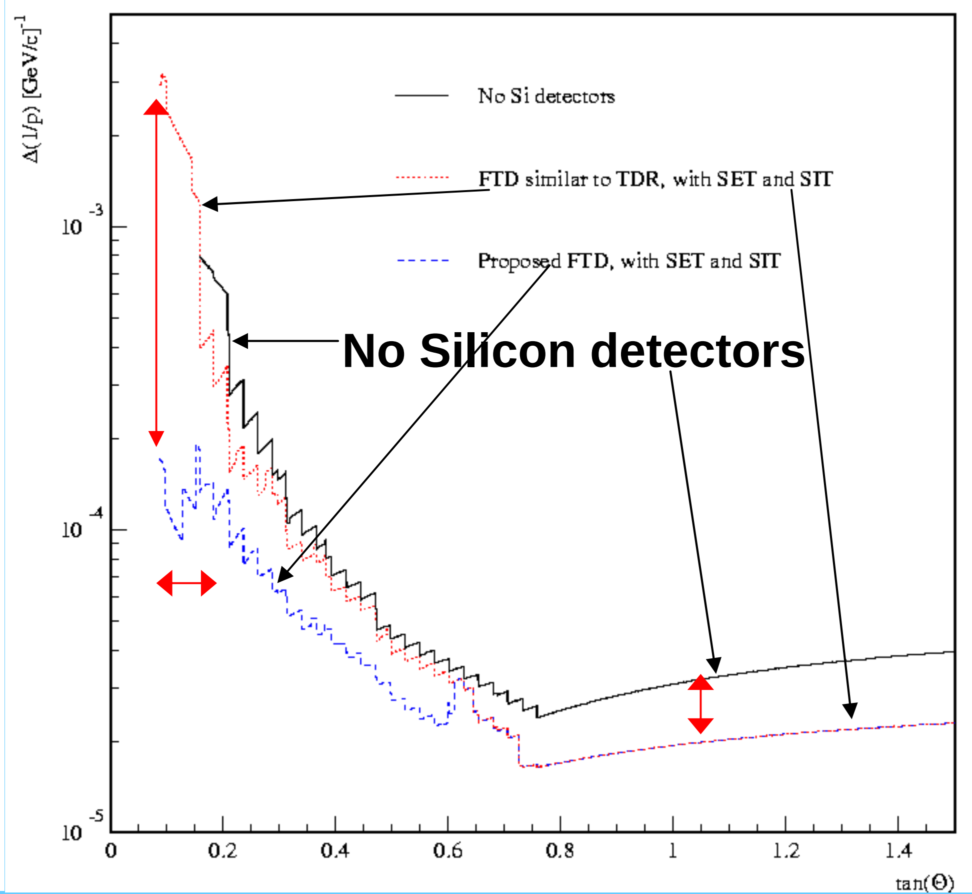


Preliminary simulation studies:end cap components

Studies with SGV by Mikael Berggren (LPNHE)

Forward region is crucial for Physics and indeed request an active R&D

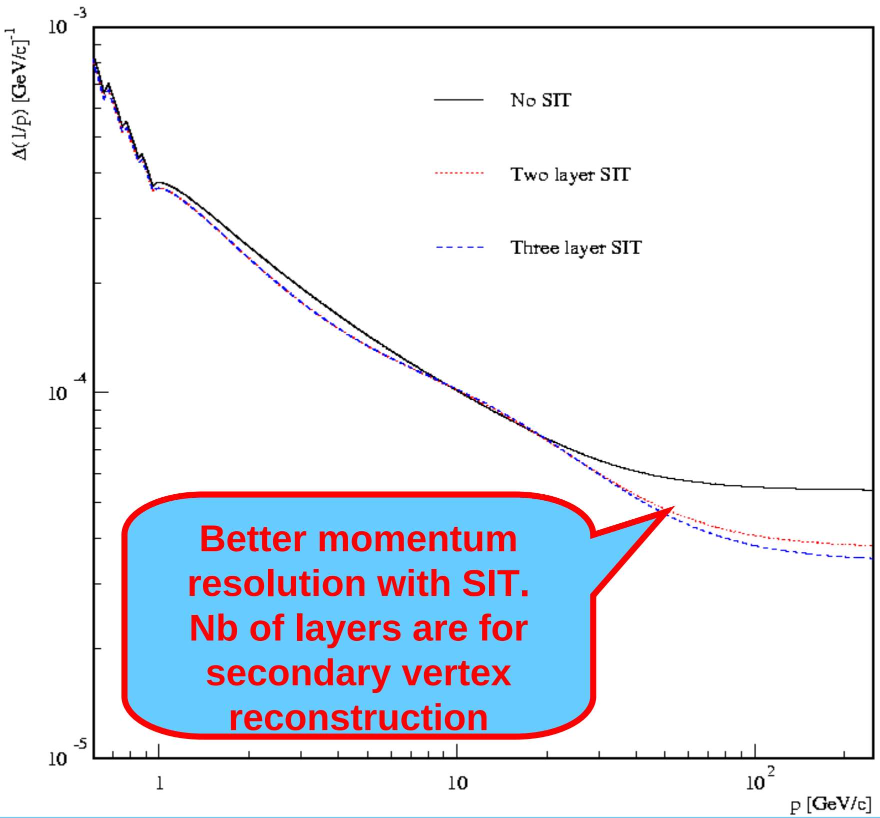


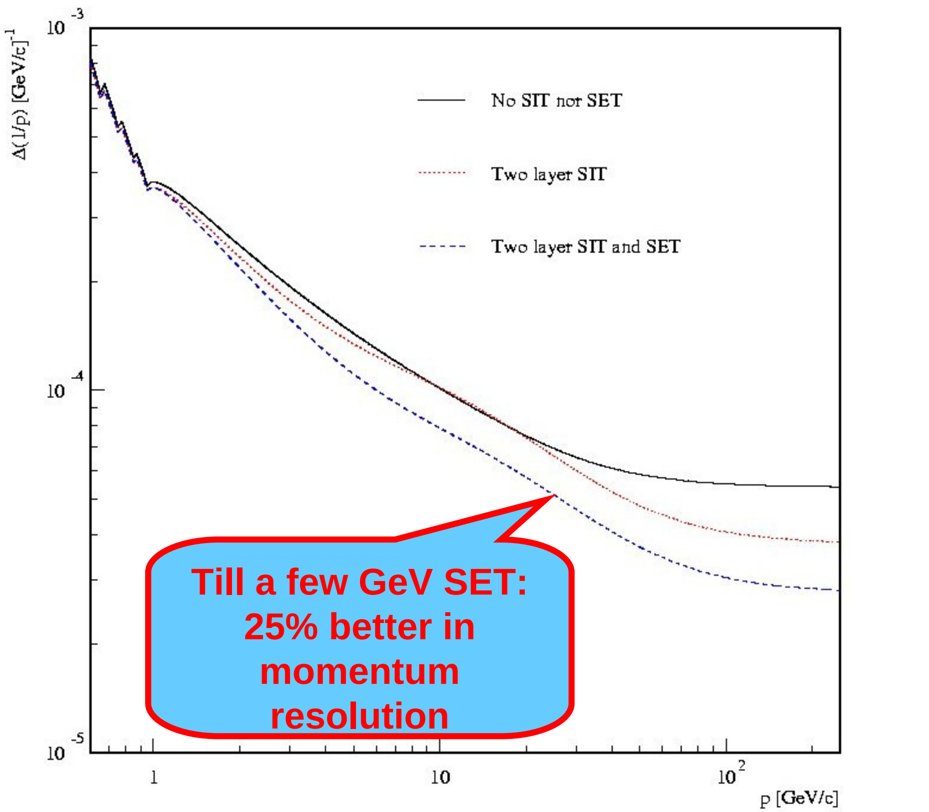


FTD + FCH (5 XUV straws, i.e.TESLA TDR)
FTD new with or without ECT(Si XUV)

Only TPC (no Silicon trackers)
FTD as TESLA TDR + SIT & SET
FTD new + SIT + SET

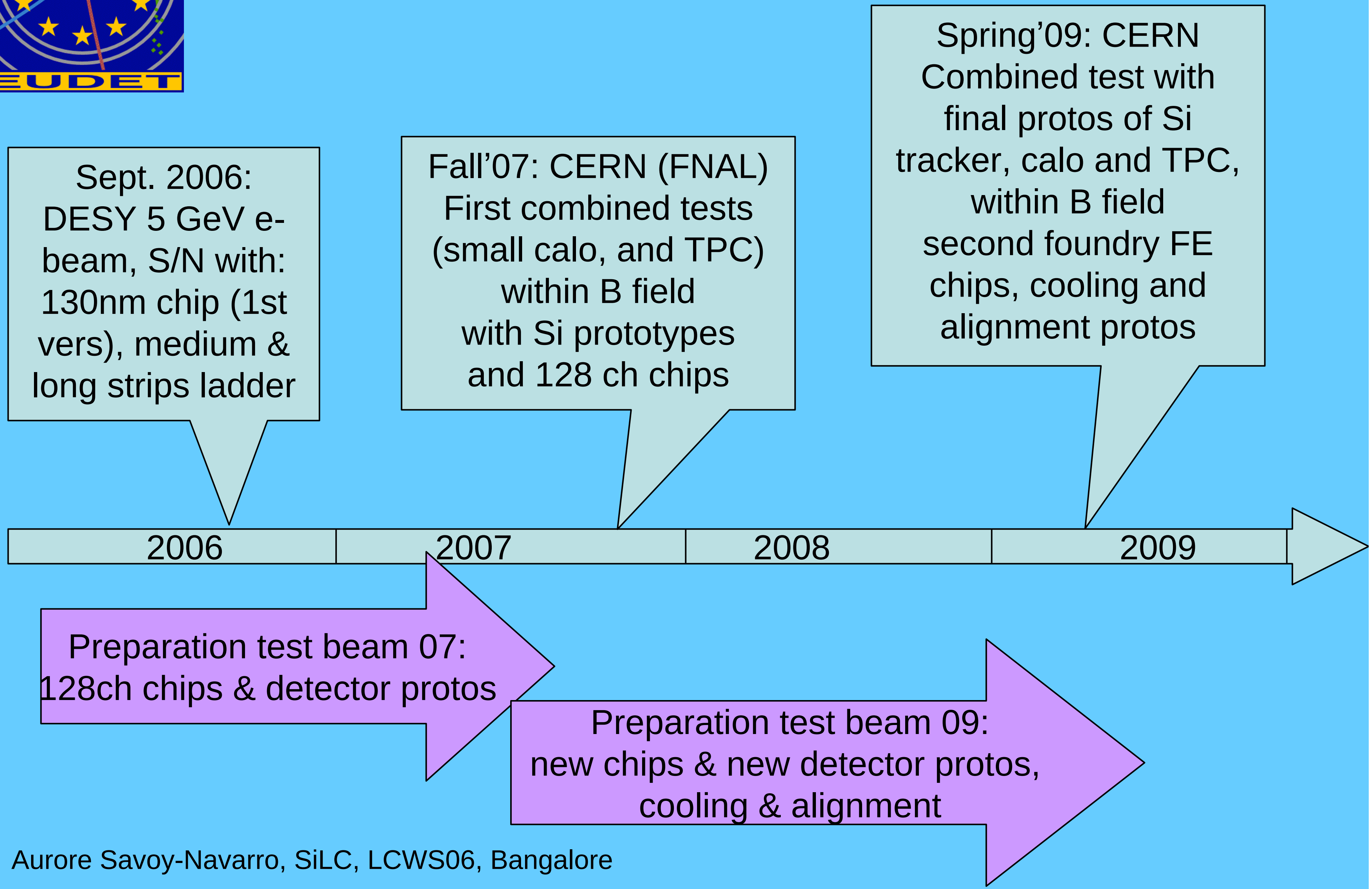
Preliminary simulation studies: barrel Silicon components





Dramatic improvement in momentum resolution by adding Silicon tracking to the TPC. Starting studies GEANT 4 based on improvements from the point of view of secondary vertex reconstruction, track linking after the end plate TPC & comparing all Si tracking design wrt to tracking including central TPC

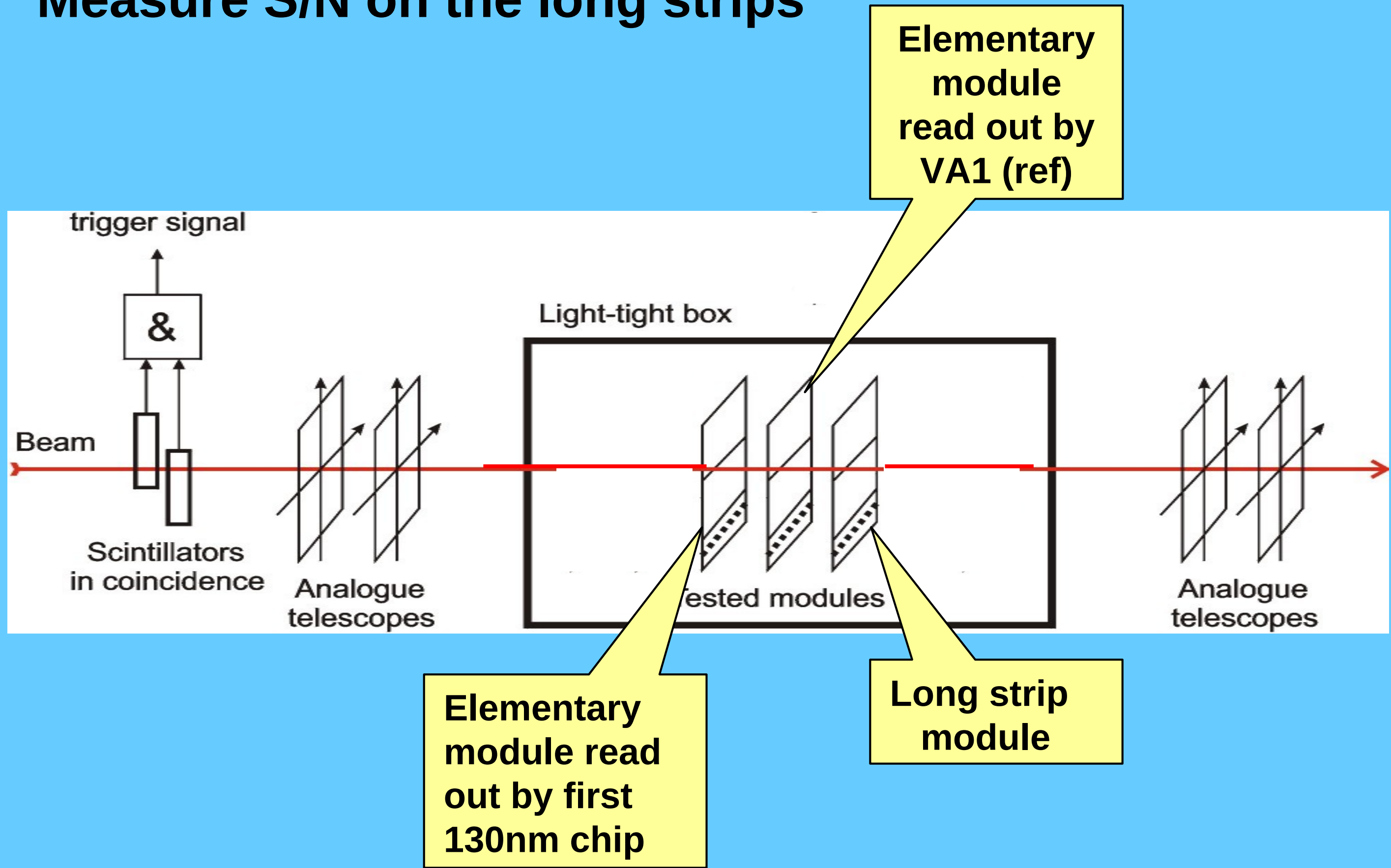
EUDET testbeam Roadmap



EUDET Test beams with Silicon tracking

First series of tests in September 2006 at DESY electron test beam, no magnetic field:

- **Test new FE chip prototype (first 130 nm prototype)**
- **Measure S/N on the long strips**

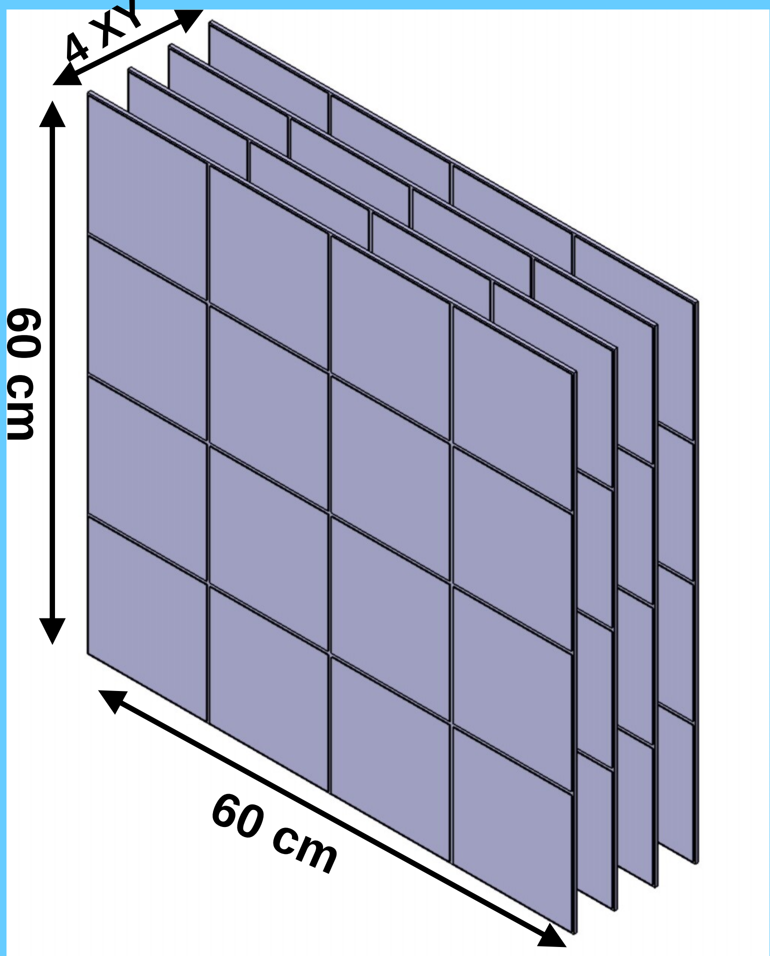


Coordinated by CU Prague team, with the participation of all SiLC teams

EUDET test beams with Silicon tracking(cont'd)

Series of tests in 2007 and 2009, combined test beams with other Subdetectors and high magnetic field:

- **Test new FE chip prototype (first 130 nm prototype)**
- **Various detector prototypes with new sensors and new FE chips**



Example:
4 '' telescope layers '' made of 15 x15 cm sensors (≥ 8''), false double sided, thinned, equipped with new chips.

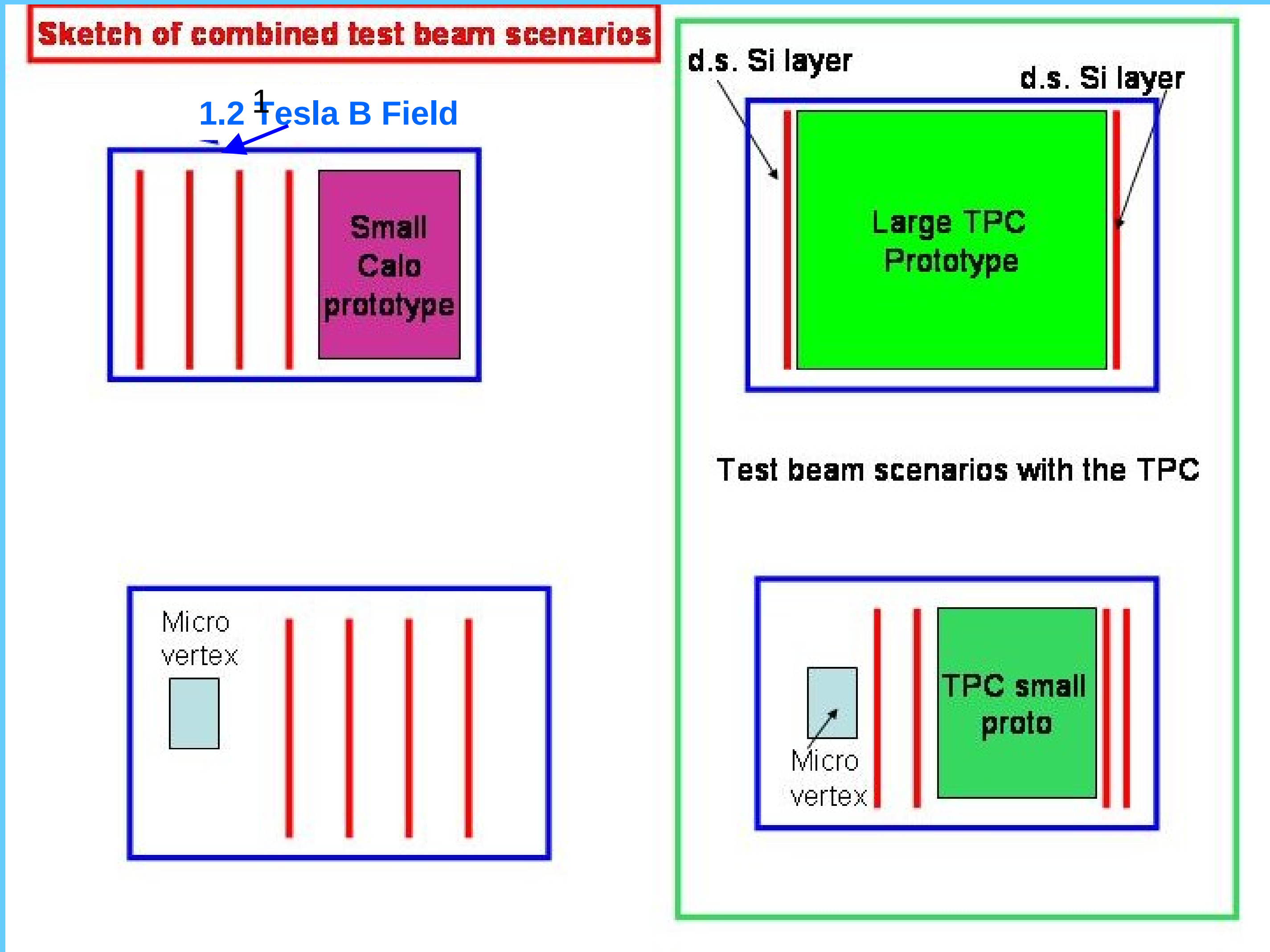
Total: 128 sensors
60000 channels
(~150µm r.o.pitch)
About 250 FE chips

EUDET test beam scenarios (cont’d)

- Test beams with larger telescopes, FWD and barrel prototypes, combined with other subdetectors:
- Calorimeter prototype
- Microvertex prototype
- TPC (field cage proto etc..)

Included in the B magnetic field,various scenarios are foreseen sketched in the next slide

EUDET test beams with Silicon tracking(cont'd)



Deliverables for EUDET from SiTRA

- **Front-end chips to equip the SiTRA prototypes (partially funded by EUDET: CUPrague, HIP, LPNHE)**
  - Order of 60 K channels to be equipped
  - Two foundries foreseen in VDSM
    128 ch/chip in 130nm CMOS techno
    ≥ 512ch/chip in 90nm (?) CMOS techno
- **Detector Prototypes (No EUDET funds)**
  (Large & light mechanical support for Si trackers)
  - Telescopes with microstrips and various pixel technolgies
  - Forward prototype
  - Barrel prototype
- **Alignment prototype (No EUDET funds)**
  IFCA-CSIC is in charge
- **Cooling prototype (partially funded by EUDET)**
  LPNHE-CNRS/P6 is in charge

Related items to deliver these workpages

➢ F.E. Chips

Electronics module linking the FE chips to the EUDET DAQ system

Standalone & Transportable DAQ system

(to set-up and test the SiTRA system in the test beam set-up before introducing it in the overall DAQ and also for Lab test bench purposes; The intention is to equip SiTRA & further on SiLC partners with this common tool for cross-checks at Lab test benches)

Wiring and cabling FE electronics onto the detector (new techs)

➢ Detector Prototypes

Sensors are crucial items: the detector prototypes will be made experiencing new sensors technologies, namely:

New microstrip sensors (larger size, thinning)

New pixel technologies (New hybrid pixels, DEPFET, MAPS, SOI …)

Exploiting new Fab lines plus sensor simulations and Test Quality set-ups

➢Detector Prototypes (cont’d)

Mechanical issues:

- Design and construction of basic element prototypes: (closely related to wiring the FE chip on the detector), thus mechanical & electronics are closedly related)
- Design & contruction of Telescopes, End Cap and Barrel trackers (adressing issues on new material, lightness and robustness etc…)

➢Alignment:

To be defined by IFCA, team in charge, with some focus on:

Precision (resolution & accuracy), technologies (?), integrated to the overall Si tracker design, minimizing material budget, position monitoring, different scenarios (with or without TPC), dependant of the Si trackers components, integration issues

➢Cooling prototype

To be developed by the team in charge (LPNHE), inspired by the valuable experience of SiLC LHC colleagues.

Will study a light cooling system (based on ongoing studies on prototypes at the Lab) Plus an e.m compatible frame (Faraday cage); Closely linked to the Mechanics.

Outer thermal Enclosure for SCT-ATLAS by IFIC

Concluding remarks

- A lot of progress since last year at SLAC: LCWS05, on all the fronts of the SiLC R&D (minus 1: simulations!)
- We are just at the beginning: a lot more is needed
- The SiLC collaboration is also developing well from sociological point of view: SiLC collab meetings (Vienna-Nov 05, Paris-Feb 06, Liverpool-May 06…)
- EUDET will be a fantastic asset to achieve the R&D objectives of SiLC and vis & versa.
- All the SiLC partners including the non E.U. ones, will be contributing to EUDET, and
- will have access to the EUDET facilities.
- **EUDET: unique opportunity for combined tests & collaborative contacts between subdetectors**.

S I L C
Silicon for the Linear Collider

http://lpnhe-lc.in2p3.fr/silc2