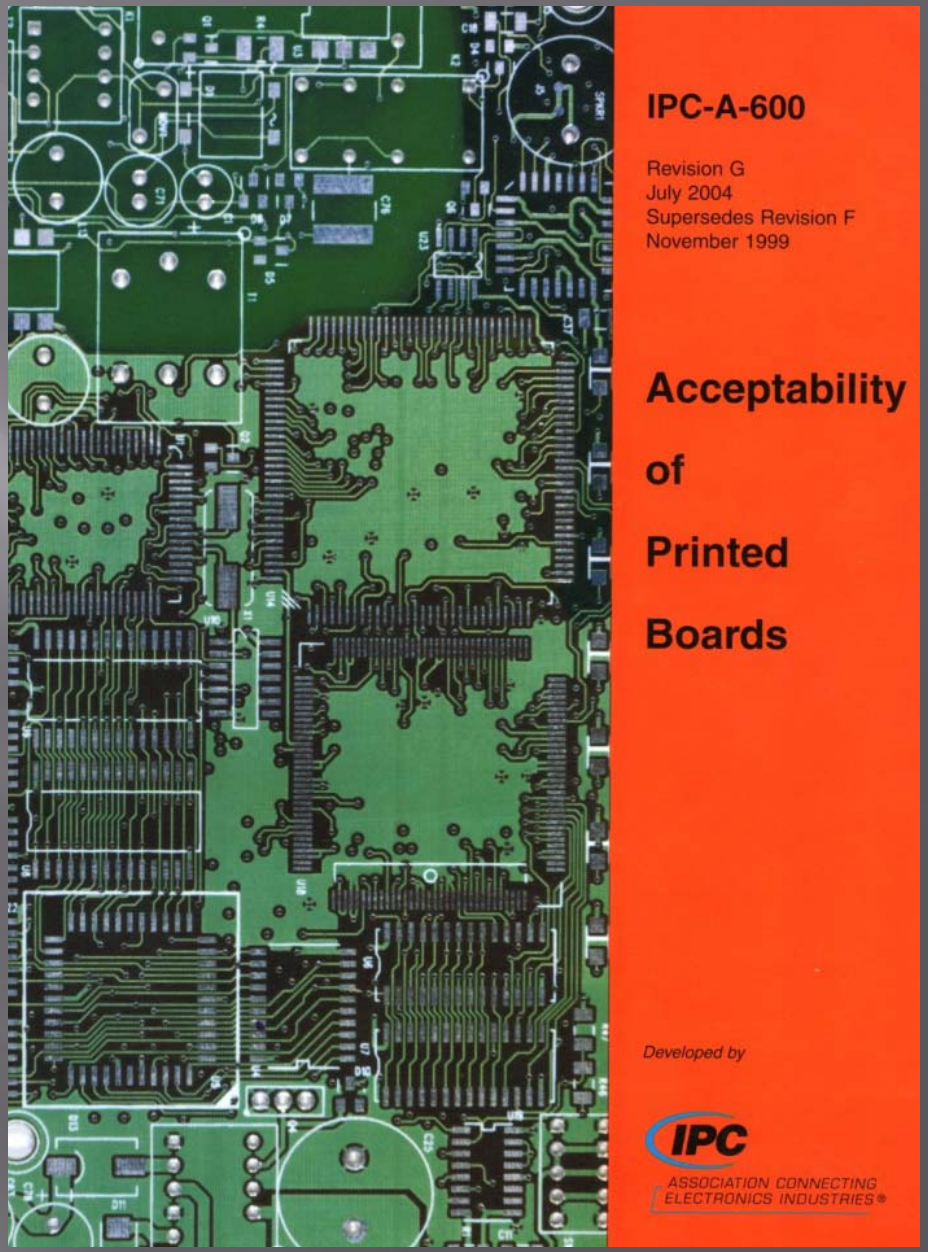
PCB PRODUCTION PTH RELIABILITY

PH ESE seminar 26/05/2009

- Electronic industry heavily depend on PCBs and surprisingly little literature exist on reliability assessments.
- Most of PCB books address production techniques and not the problems.
- However IPC-A-600 (acceptability of printed circuit boards) and IPC-TM-650 (test method manual) can help a lot.
- IPC do not solve the problems , IPC define levels in the problem
- But even with the IPC guidelines an inspector or buyer should have a reasonable broad background knowledge of PCB defects.

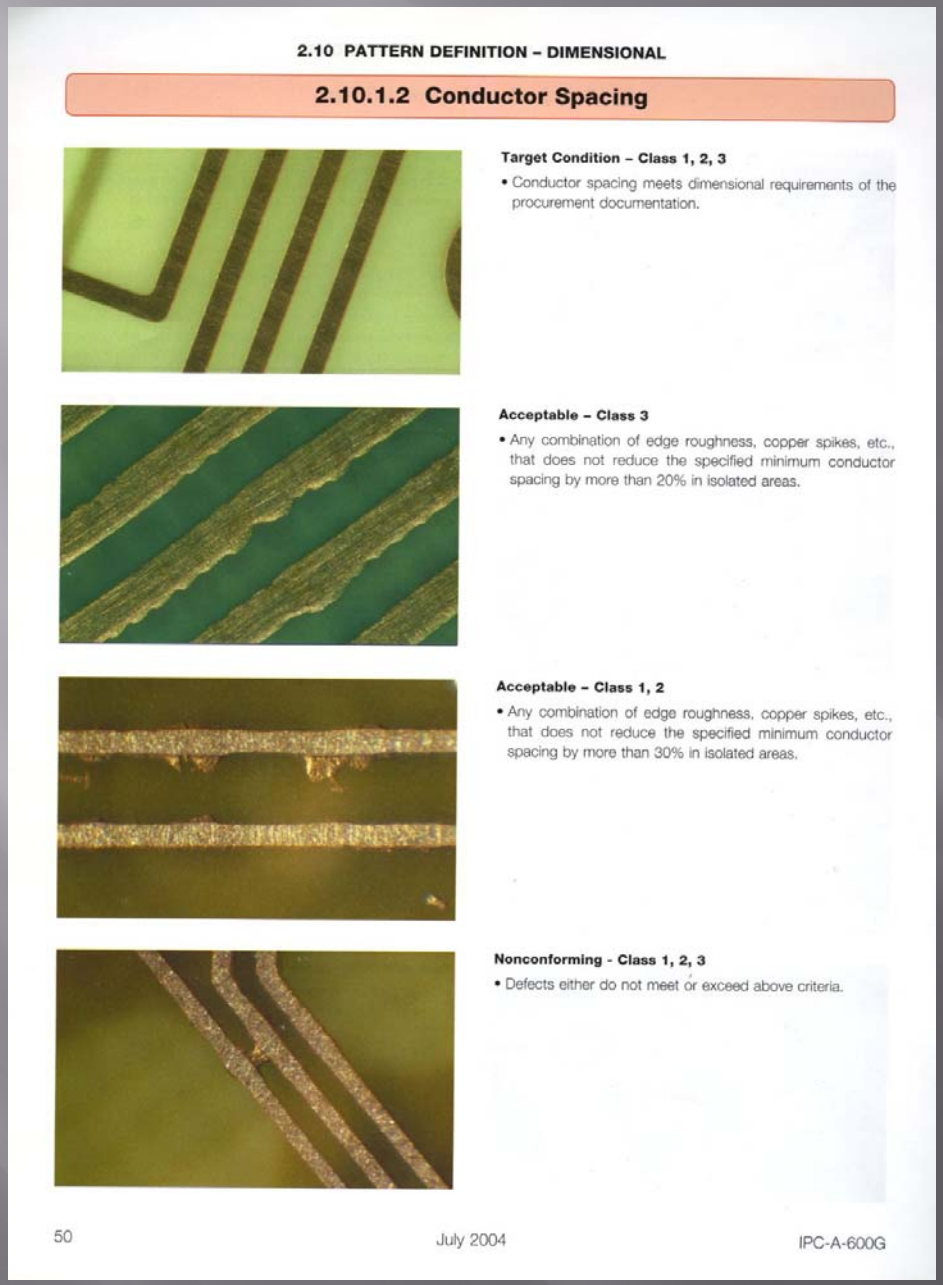
What is IPC-A-600?

Standard made in association between producers and users.



IPC-A- 600 Acceptability of printed circuit boards

- Mainly it defines visual inspection criterions
- It defines around 110 parameters to check on a bare PCB
- Some of these tests are destructive
- This document gives to the producer and the customer the same reference
- Let's look at a few examples from the IPC-A-600



2.10 PATTERN DEFINITION – DIMENSIONAL

2.10.1.2 Conductor Spacing

Target Condition – Class 1, 2, 3

- Conductor spacing meets dimensional requirements of the procurement documentation.

Acceptable – Class 3

- Any combination of edge roughness, copper spikes, etc., that does not reduce the specified minimum conductor spacing by more than 20% in isolated areas.

Acceptable – Class 1, 2

- Any combination of edge roughness, copper spikes, etc., that does not reduce the specified minimum conductor spacing by more than 30% in isolated areas.

Nonconforming - Class 1, 2, 3

- Defects either do not meet or exceed above criteria.

50 July 2004 IPC-A-600G

IPC define the parameter to check and define also 3 classes of quality

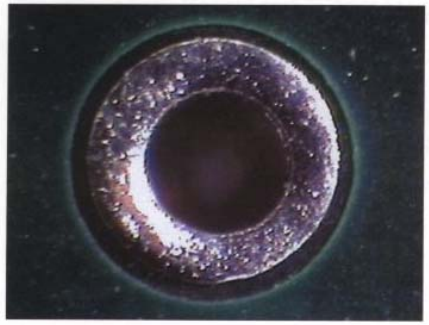
Class1: The worse but the PCB still work, general electronic products

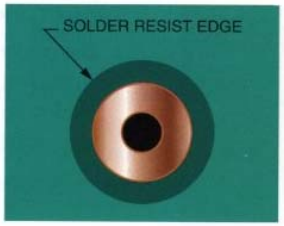
Class2: Industrial products for which uninterrupted service is desired but not critical

Class3: High reliability electronics products

2.9 SOLDER RESIST (Solder Mask)

2.9.2 Registration to Holes (All Finishes)



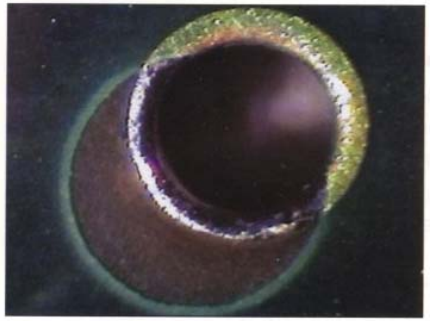


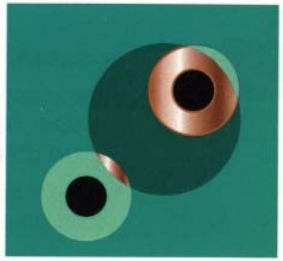
Target Condition – Class 1, 2, 3

- No solder resist misregistration. The solder resist is centered around the lands within the nominal registration spacings.

Acceptable – Class 1, 2, 3

- Misregistration of the resist to the land patterns but the resist does not violate minimum annular ring requirements.
- No solder resist in plated-through holes, except those not intended for soldering.
- Adjacent, electrically isolated lands or conductors are not exposed.

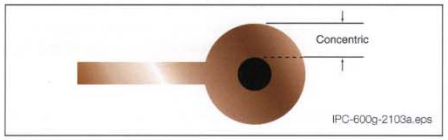




Nonconforming – Class 1, 2, 3

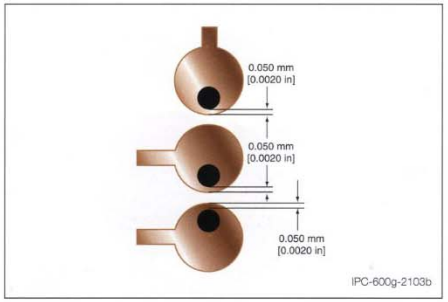
- Defects either do not meet or exceed above criteria.

2.10.3 External Annular Ring - Supported Holes



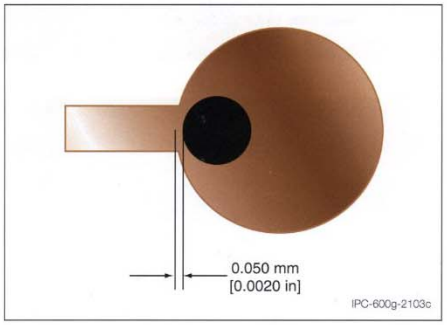
Target Condition – Class 1, 2, 3

- Holes are centered in the lands.



Acceptable – Class 3

- Holes are not centered in the lands, but the annular ring measures 0.050 mm [0.0020 in] or more.
- The minimum external annular ring may have 20% reduction of the minimum annular ring at the measurement area due to defects such as pits, dents, nicks, pinholes, or splay.

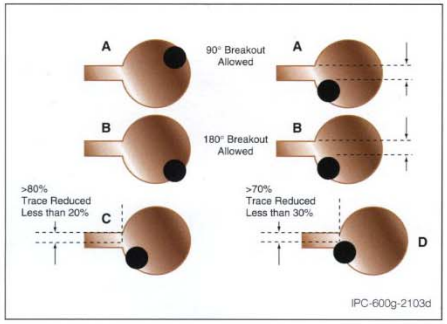


Acceptable – Class 2

- 90° breakout or less. (A)
- If breakout occurs at the conductor to land junction area, the conductor is not reduced by more than 20% of the minimum conductor width specified on the engineering drawing or the production master nominal. The conductor junction should never be less than 0.050 mm [0.0020 in] or the minimum line width, whichever is smaller. (C)
- Minimum lateral spacing between conductors is maintained.

Acceptable – Class 1

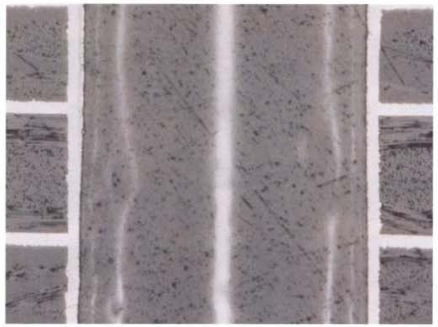
- 180° breakout or less. (B)
- If breakout occurs at the conductor to land junction area, the conductor is not reduced by more than 30% of the minimum conductor width specified on the production master nominal. (D)
- Form, fit and function are not affected.
- Minimum lateral spacing between conductors is maintained.



Nonconforming - Class 1, 2, 3

- Defects either do not meet or exceed above criteria.

3.3.3 Foil Crack - (Internal Foil) "C" Crack

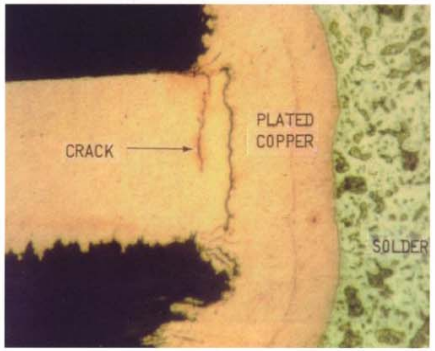


Target Condition – Class 1, 2, 3

- No cracks in foil.

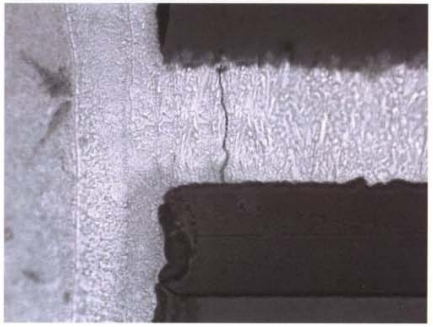
Acceptable – Class 2, 3

- No evidence of cracks in foil.



Acceptable – Class 1

- Allowed on one side of hole only and **shall not** extend through foil thickness.



Nonconforming - Class 1, 2, 3

- Defects either do not meet or exceed above criteria.

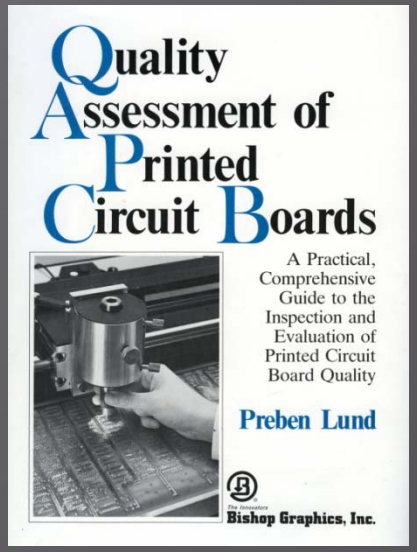
Inspection of PCBs

- A lot of inspections are done during PCB production
  - Visual inspection
  - Electrical inspection
  - Process parameters
    - Bath controls
    - Ovens
    - Processing times etc…
- Some of them are on a 100% basis and other ones done by sampling (AQL "acceptable quality level" MIL-STD-105) and rarely (but it exist!) there is no or no adapted test for some parameters.

Why?

Infos taken from

The reason is the cost



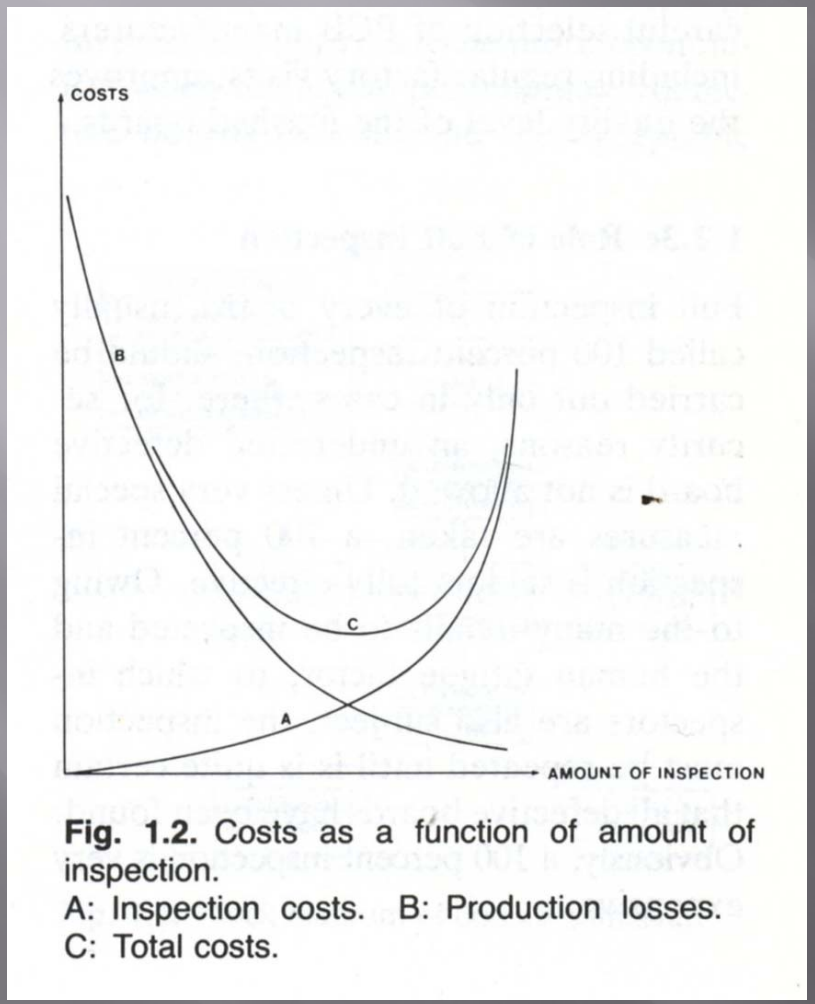


Fig. 1.2. Costs as a function of amount of inspection.
A: Inspection costs. B: Production losses.
C: Total costs.

Companies usually adapt their inspection methods to reach at least 95% good pieces, They also adapt their methods to the targeted Market (consumer, aeronautic, military)

Some companies skip completely or simplify a lot some tests because it will affect only a few % of their productions.

In any case 100% yield for any application is not possible today!

- Fortunately and thanks to modern equipments the cost of some tests is reduced and they are now on a 100% basis ex:
  - Electrical (Flying probe testers)
  - Track pattern (Automatic optical inspection machines)
  - Mask inspection (AOI also)
- But there is still tests to be made by sampling for :
  - Plated through holes quality
  - Finishing quality (Ni/Au, tin lead etc…)
    - Thicknesses
    - Wetting

Now let's have a look to some CERN big PCB problems in order to find which is the dominant cause of defects

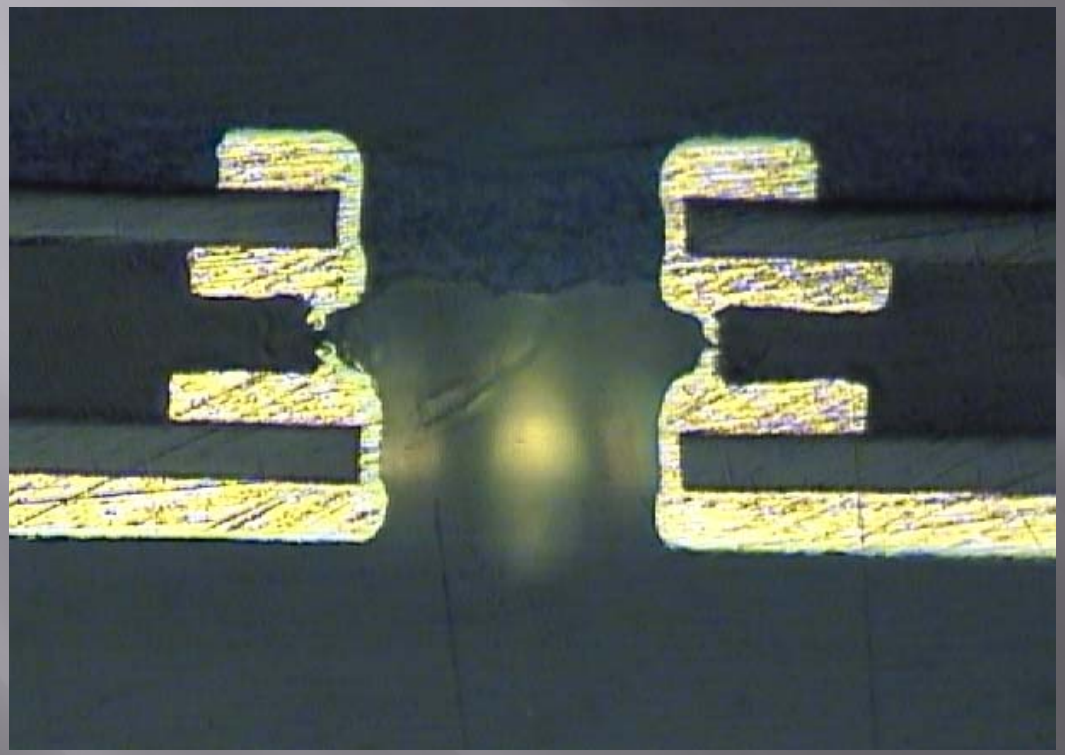
List of some big problems met at CERN (not exclusive)

name	problem	Alert	First signs
CMS flex rigid for inner tracker	Micro via cracks	After 3000 pieces assembled.	Low yield in pcb production and non explained bad boards at test after assembly
Tell1/ LHC-B multilayer	Hole cracks	Breakdowns after installation in the experiment .	A fraction of non explained Bad boards after assembly
Preshower/CMS flex rigid	Hole cracks	During PCB production .	Found before delivery of PCB
LHC multilayer	Hole cracks	After installation In experiment.	A fraction of non explain bad boards at electrical test after assembly
CMS/ calorimeter flex	Bad hole plating	After all the intallation.	A large fraction of boards repared during assembly
TRT Atlas Flex rigid	Hole cracks in blind holes	During PCB production.	Found before delivery of PCB

Total non quality cost for these 6 projects over than 10 MCHF (my estimation)
Taking in account the cost of : PCB, assembly, components, installation, meetings, travels, expertise, dismounting, new installation + delays and stress

Now let's look at the metallographic cuts after expertise.

Made in Switzerland



Defects:

Barrel Crack :3.3.5 IPC

Thickness too low :3.3.8 IPC

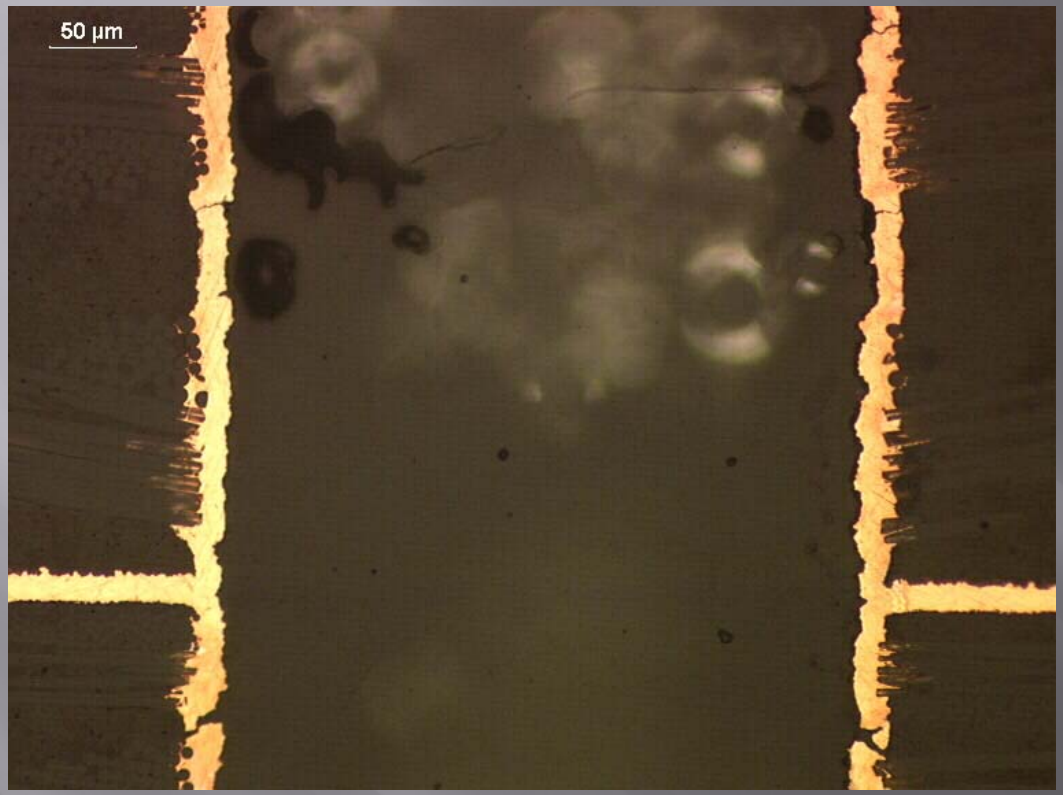
Etchback too big :4.1.9 IPC

Reasons

Wrong stack!

Wrong desmearing!

Made in Italy



Defects:

Barrel Crack :3.3.5 IPC

Thickness too low :3.3.8 IPC

Some wiking: 3.3.12 IPC

Reason:

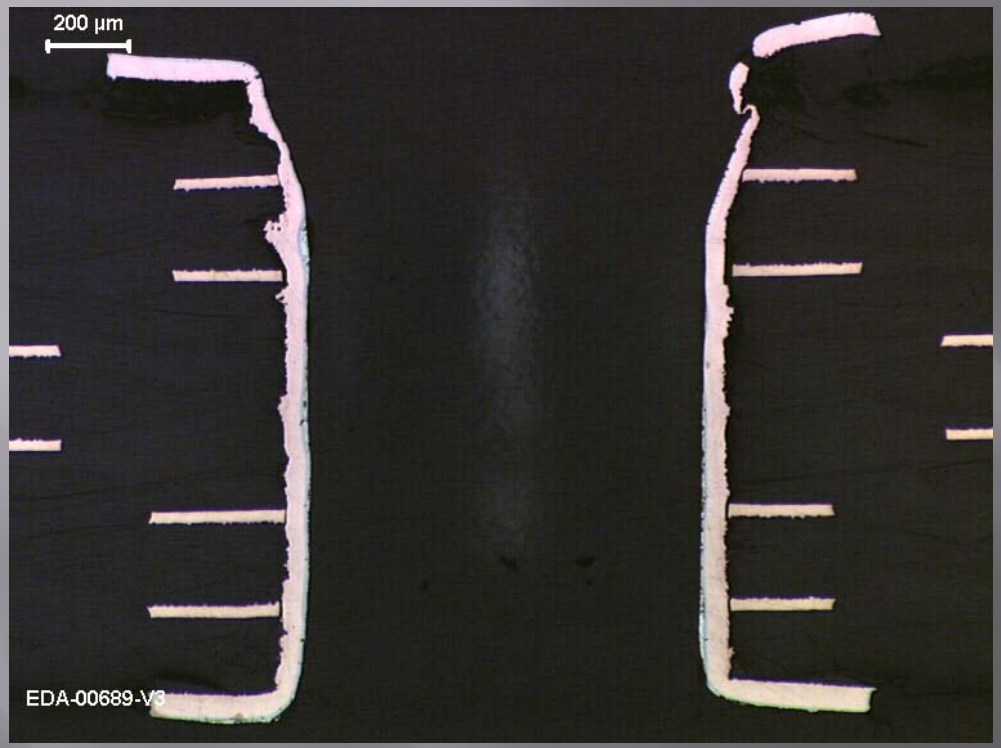
Copper ductility!

Z axis CTE of base material!

Copper plating time!

Drilling quality!

Finland



Defects:

Thickness too low : 3.3.8 IPC

Corner Crack: 3.3.6 IPC

Lifted lands : 3.3.2 IPC

Inner layer separation 3.3.13 IPC

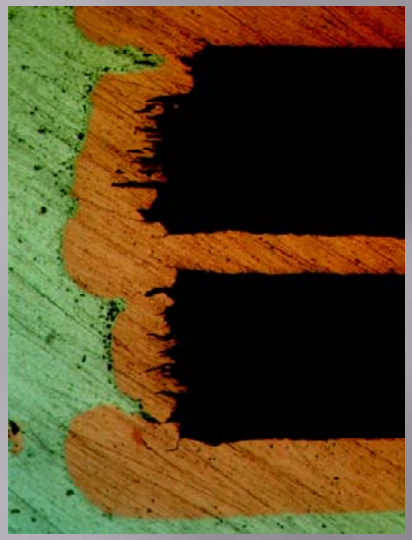
Reasons:

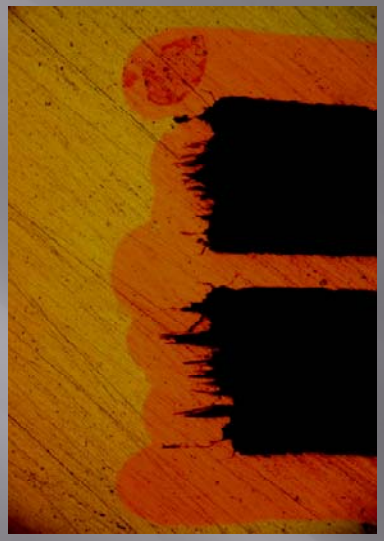
Bad desmearing

Bad Thermal cycles

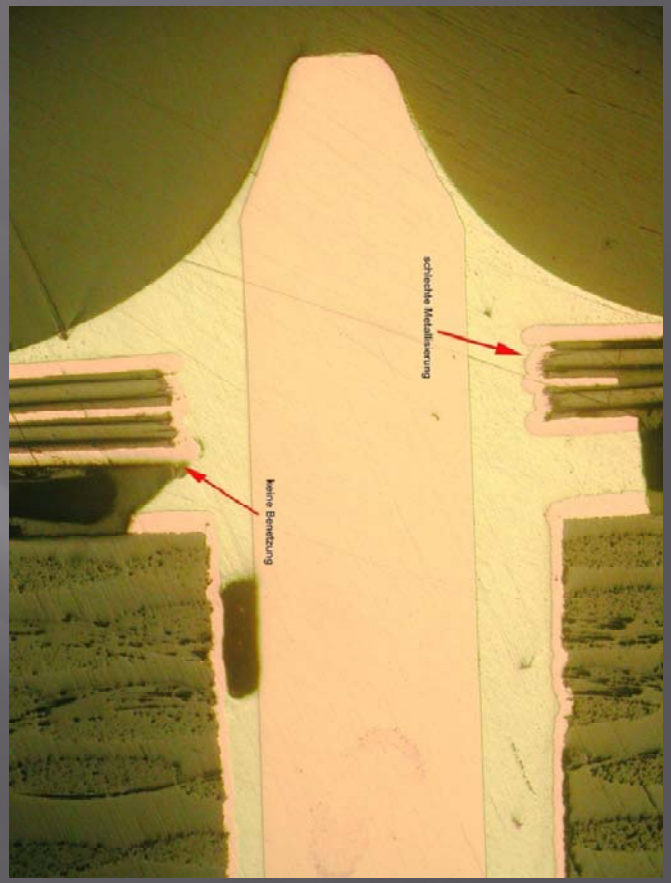
Bad drilling

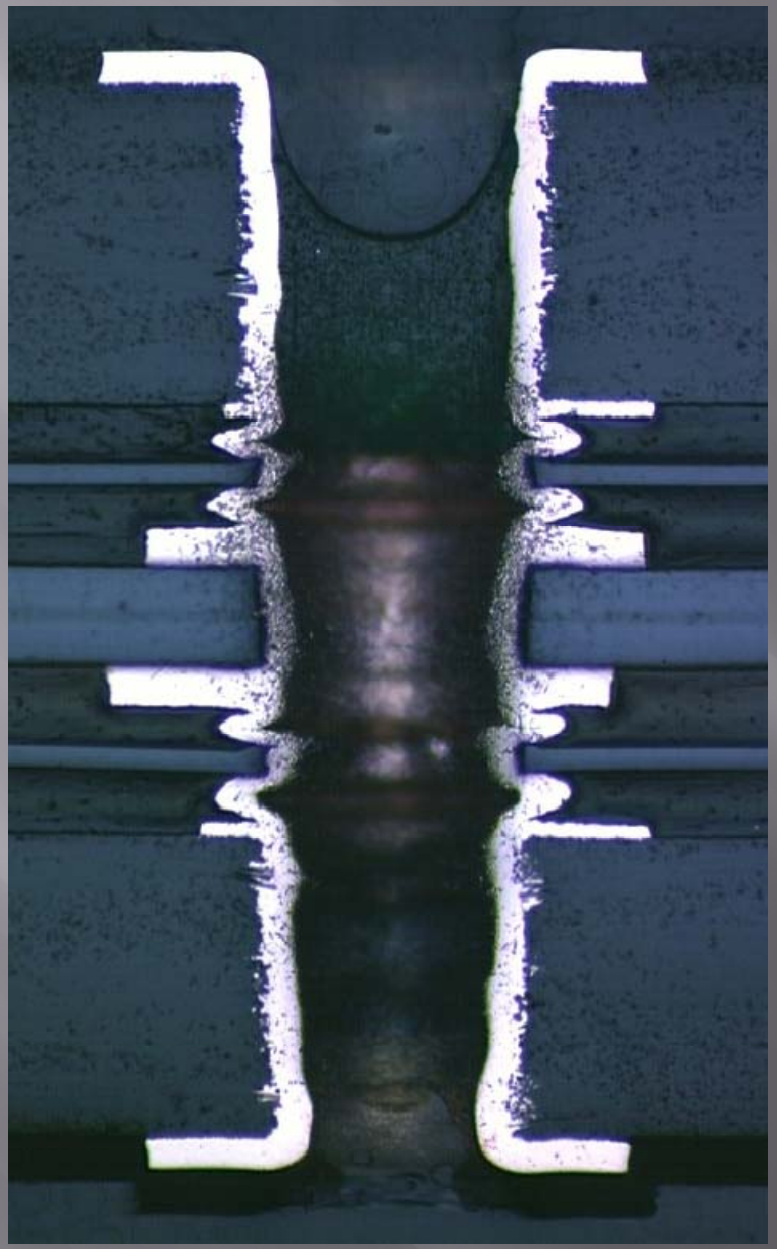
Italy





Amazing!

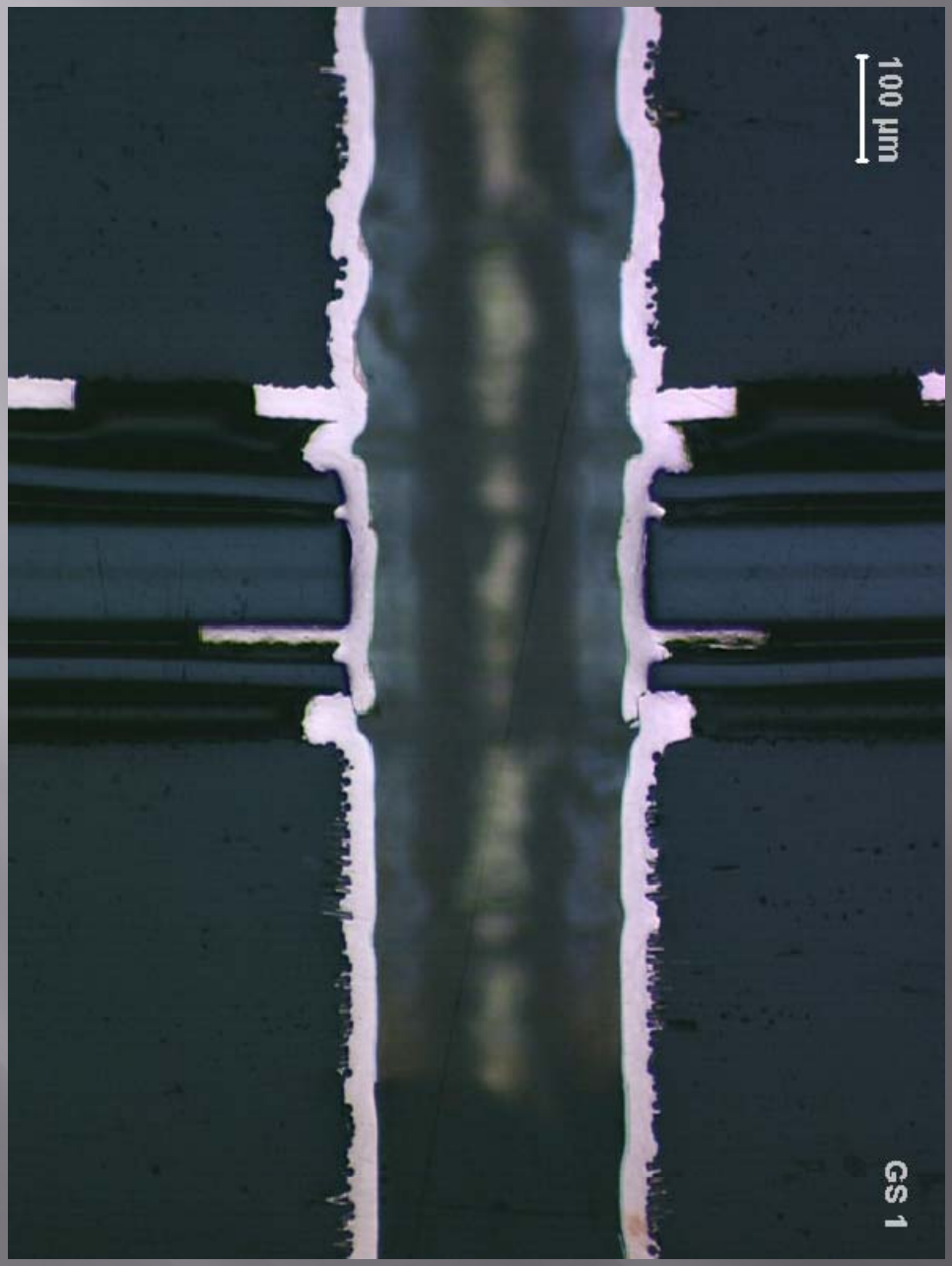




Switzerland

Etchback too big :4.1.9 IPC

Some thin inner layers?



Switzerland

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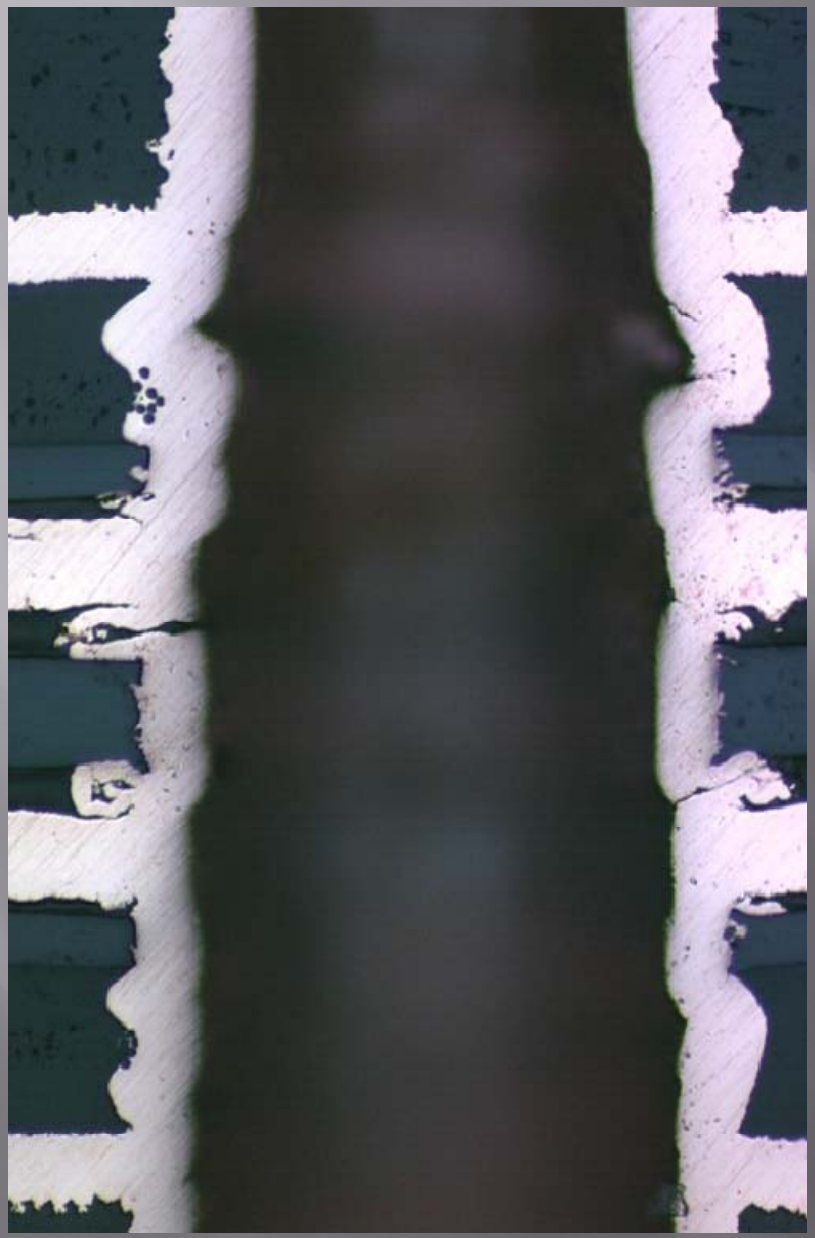
Barrel Crack: 3.3.5 IPC

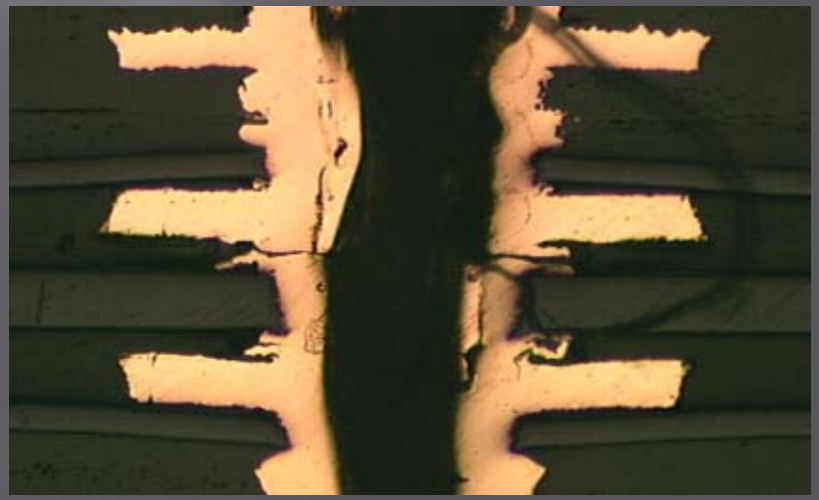
Bad stack!

Greece



Bad plating due to
non adapted desmearing

Chemical desmearing applied
to flex circuits?



???

- These cuts comes from “good pieces, electrically tested”
- All companies are following the acceptance test from IPC-A-600 .
- They are certified ISO 9000

So where is the problem?

Can we learn something from these examples ?

- 1: The main cause today of PCB breakdown after delivery at CERN is the Plated through Holes (PTH) failure.

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- 6: The problem completely appears in the application after few months or years and creates a disaster for 4 reasons:
  - Everything is installed
  - No more budgets, no time
  - Part of your experiment or machine is not working
  - And all the productions becomes suspect . When will they die?

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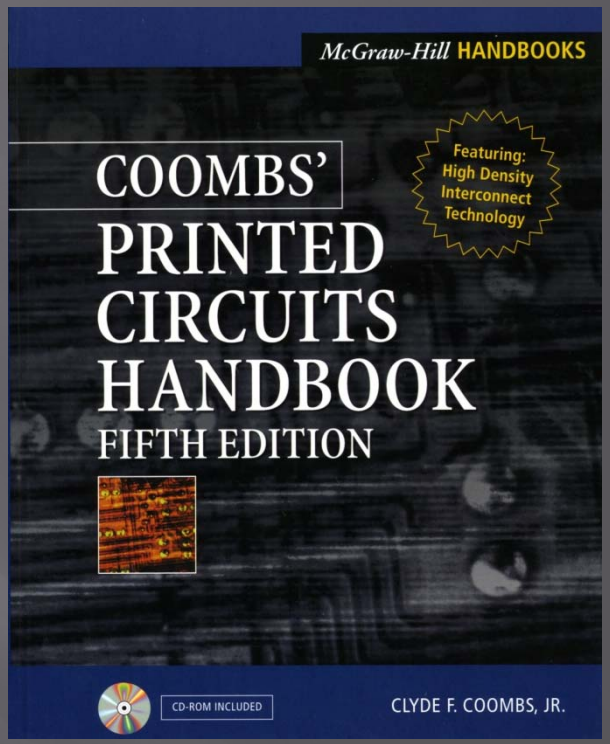
When will I die? (project manager)

Problem: PTH integrity

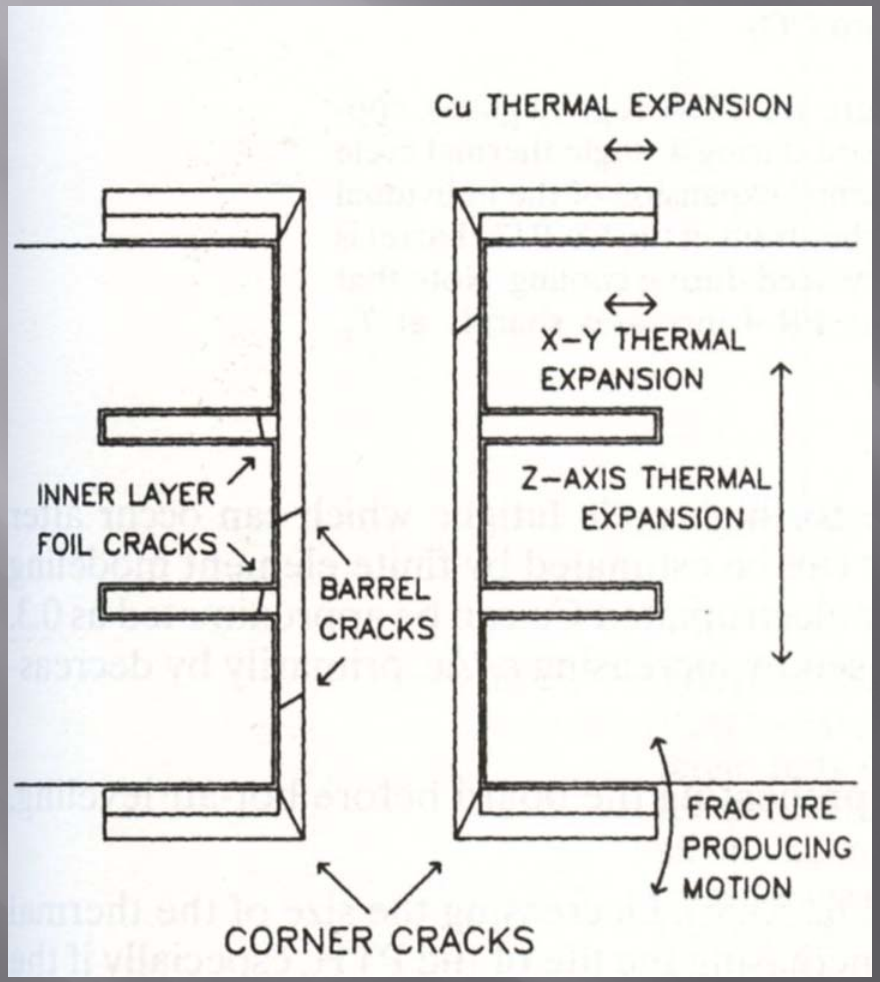
" PTHs are the most vulnerable features on PCBs to damage from thermal cycling and the most frequent Cause of printed circuit board failures in service"

Chapter: 53.2.1.1



- What is a good PTH?

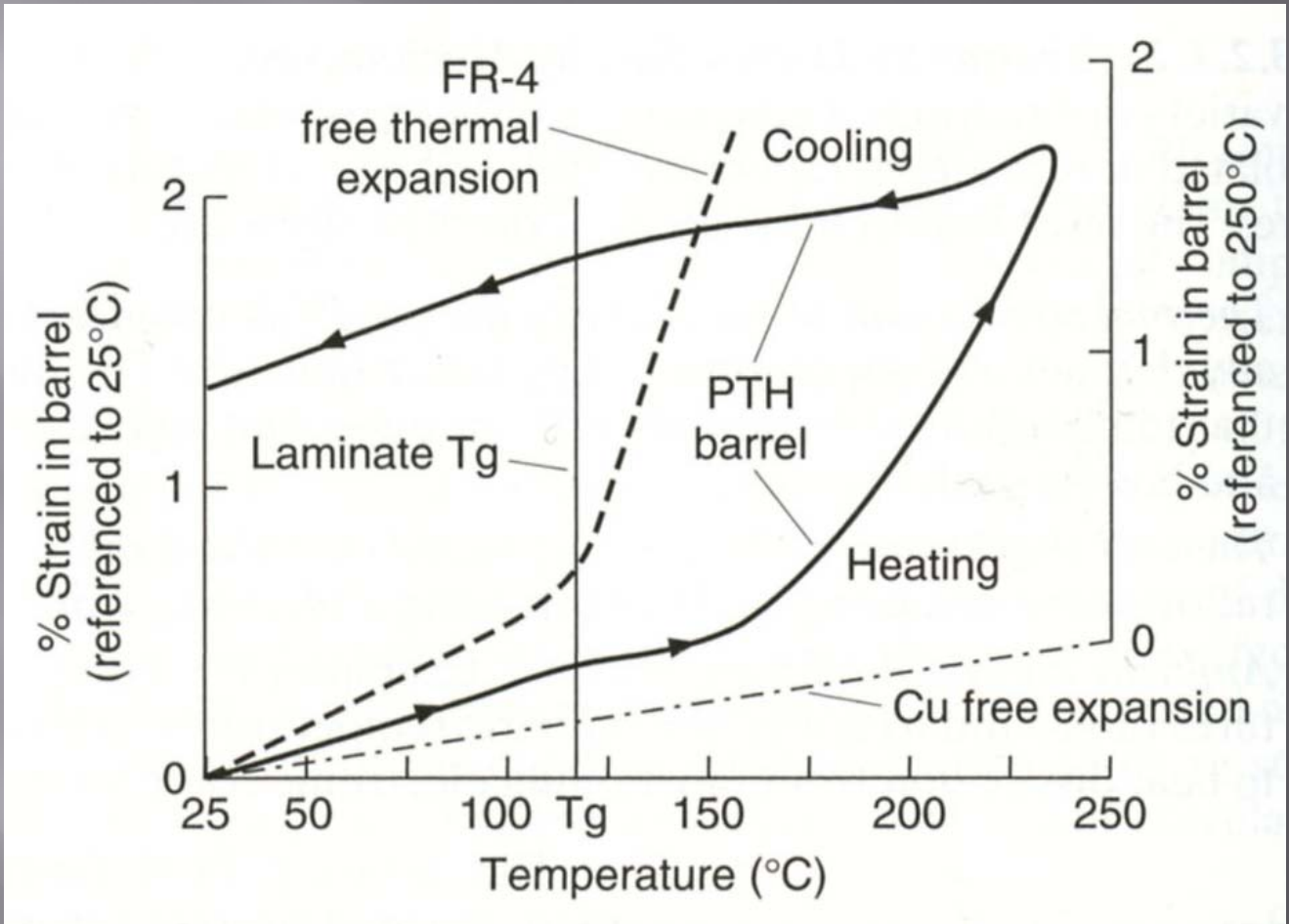
What is a PTH? Let's look at some qualification tests



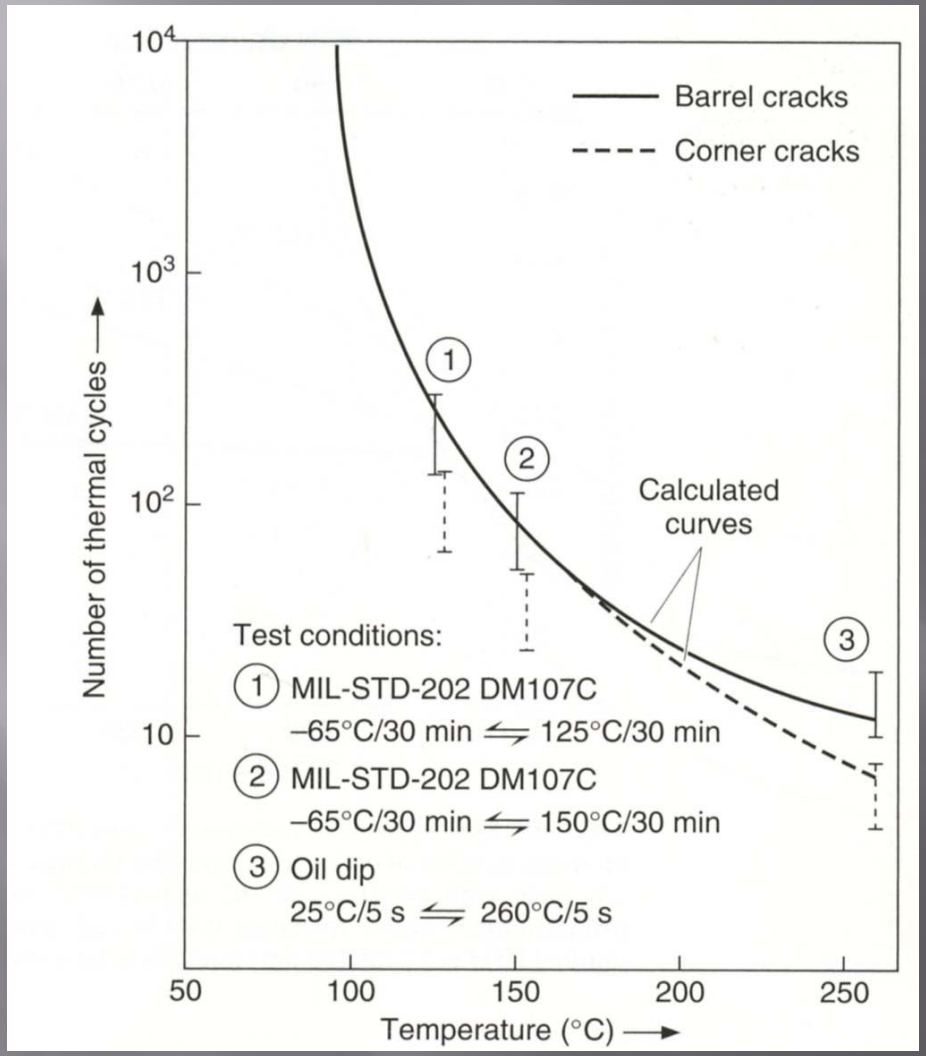
Even perfect PTH will break one day

The main reason is CTE mismatch between Epoxy, Glass and copper

Here you can see all the Different failure modes



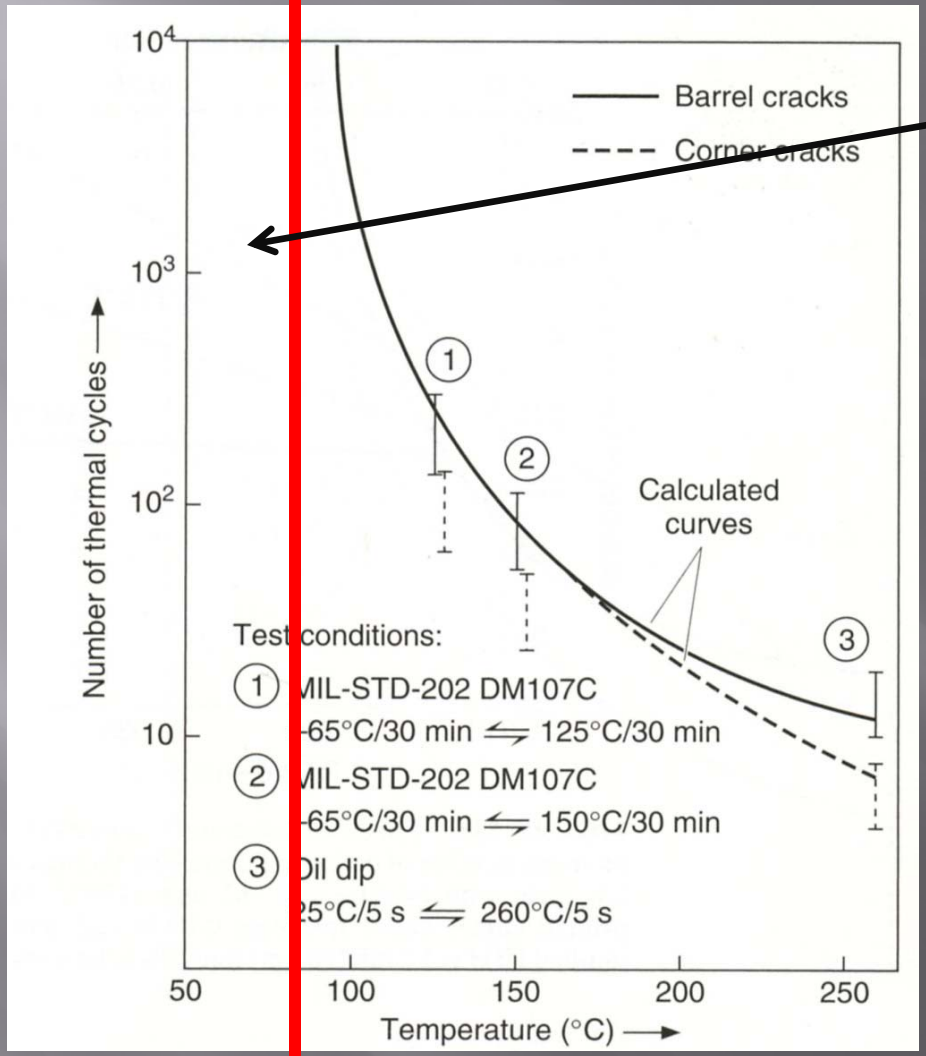
High TG materials and low Z axis CTE are preferred.



A good PTH can support 10 oil dips

A bad PTH can die after 2 dips

Assembly reflow cycles are close to Oil dip (3)



CERN applications

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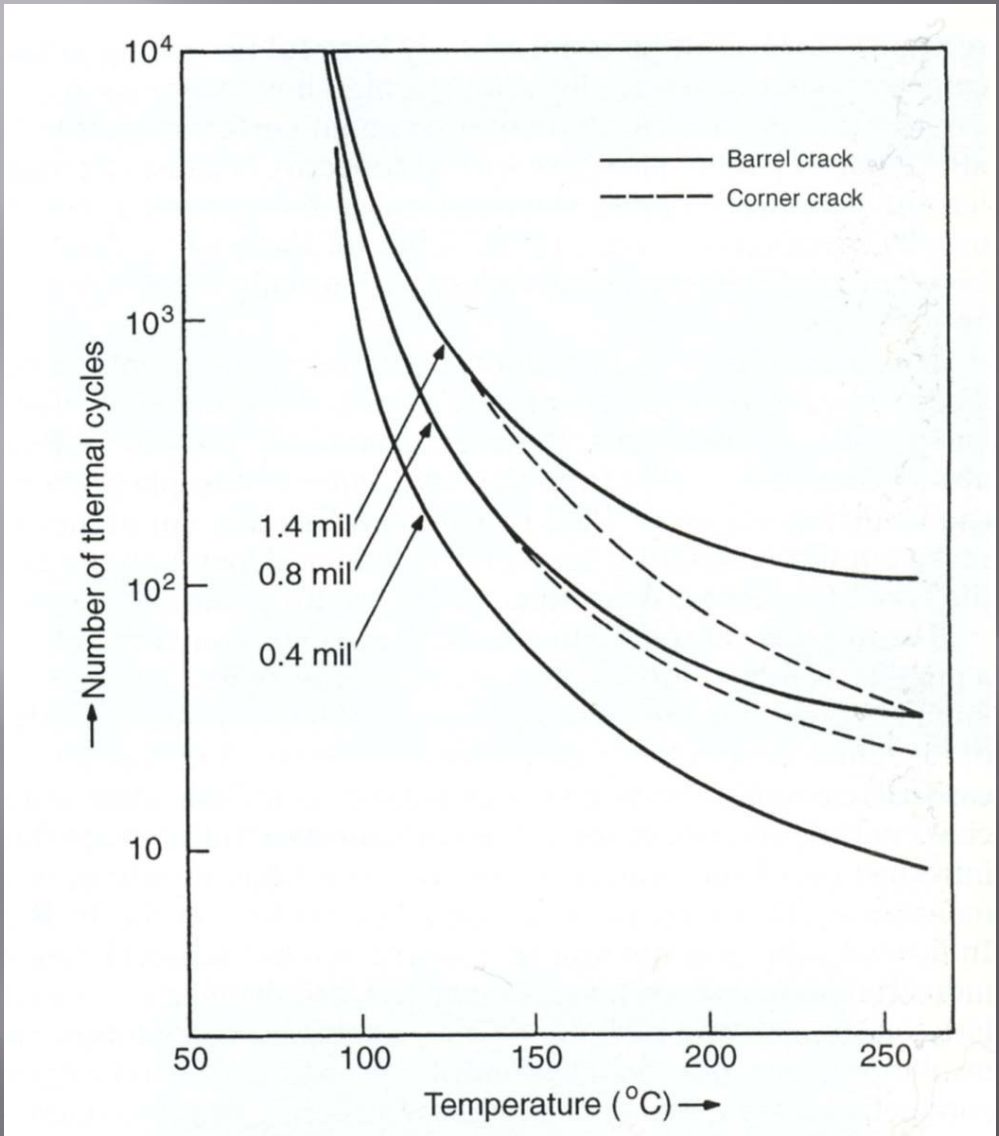
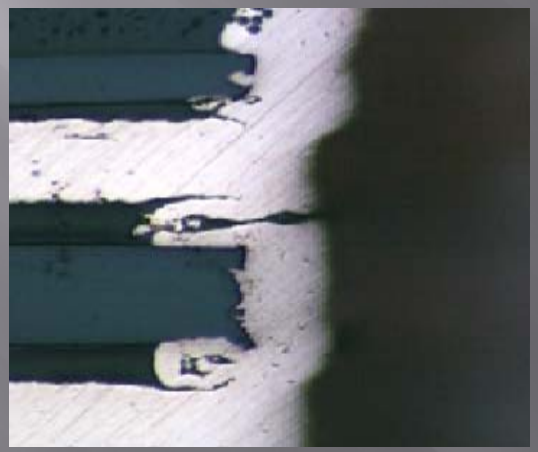
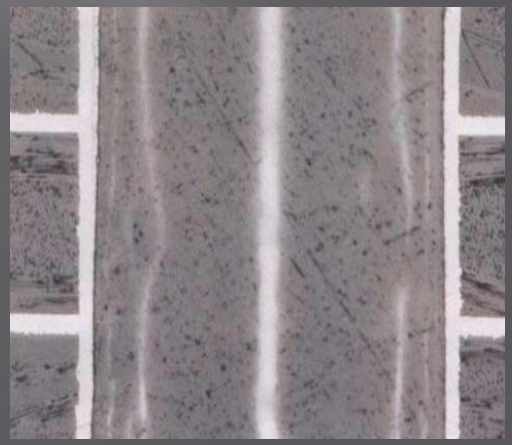


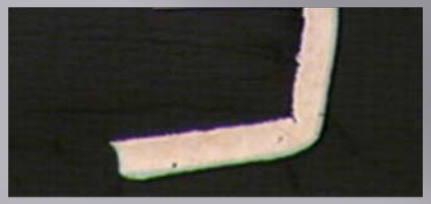
The reliability is also related to copper thickness in the PTH barrel

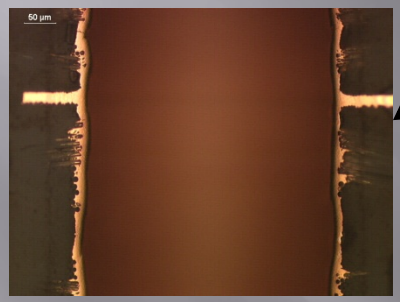
PTH conclusion

- The reliability of PTHs is usually above most of the industrial applications (no problem to fulfill CERN needs).
- These information are valid for all PTHs correctly produced.
- The problem is PTHs which are not properly made









Possible PTH defects:	Possible causes
-Annular ring	-Bad desmear
-Lifted lands	-Copper adhesion/heat
-Foil crack	-Heat
-Barrel crack	-Cu thickness/drill/heat
-Corner crack	-Copper polishing/heat
-Plating nodules	-Residues in hole
-Copper thickness	-Baths not tuned
-Plating voids	-Bad desmear
-Wicking	-Bad material/ drilling
-Wicking clearance	-Bad material
-Innerlayer separation	-Bad desmear
-Etch back	-Bad desmear
-All these defects are fully addressed in IPC-A-600 but they all need cross sections to be found.	-Most of them are not related to thermal cycles! -Bad desmear is one of the major causes!

- I’m not going to describe how to make a good PTH, it will take too long and it’s useless because none of you will try to train a company.
- But I’m going to describe how to find a non reliable batch from a production with simple actions.
- But unfortunately it needs “actions”

- What are the standard tests for PTH in industry? (Method 1)
  - Cross sections after plating
    - 1 cross section every hour in the best case
    - It means 1 cross section for 10e5 or 10e6 holes produced
    - This cross section only detects failures that affect 100% of the PTHs
    - It mainly verifies the copper thickness
  - Thermal stress + cross section
    - Daisy chain deep in oil (250°) for 10 cycles
    - This test is done on test coupons .
    - It should be done by the company regularly.
    - 1 test per month usually .
    - Not enough when you know that a problem can appear in one day.

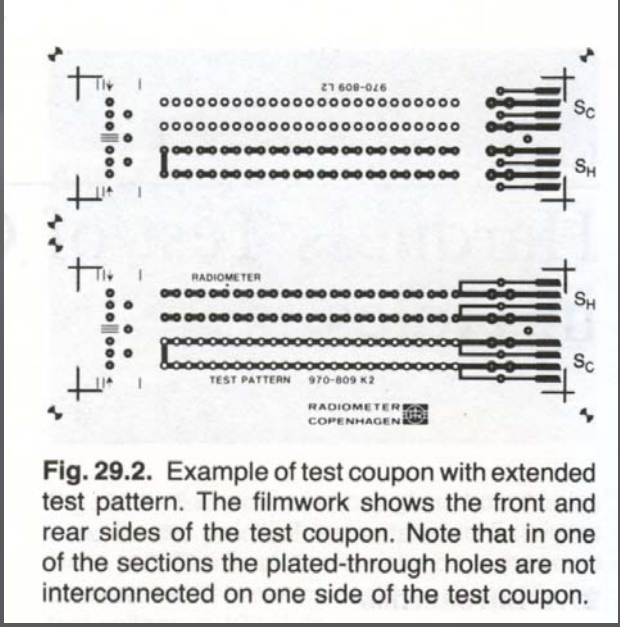


Fig. 29.2. Example of test coupon with extended test pattern. The filmwork shows the front and rear sides of the test coupon. Note that in one of the sections the plated-through holes are not interconnected on one side of the test coupon.

- Some customers need higher quality (Method 2)
  - Cross sections:
    - 1 per panel (not one every hour)
      - 1 PTH tested over 10e4
      - Again this method can only check the copper thickness
      - But you are sure that copper thickness on every panel is OK
  - Thermal stress +cross section
    - 1 daisy chain per panel (not every month)
    - Daisy chain deep in oil (250°) 10 cycles
    - Electrical test, resistive measurement
    - Cross section of broken PTHs
    - Heavy and costly method
    - Depends a lot on the daisy chain design

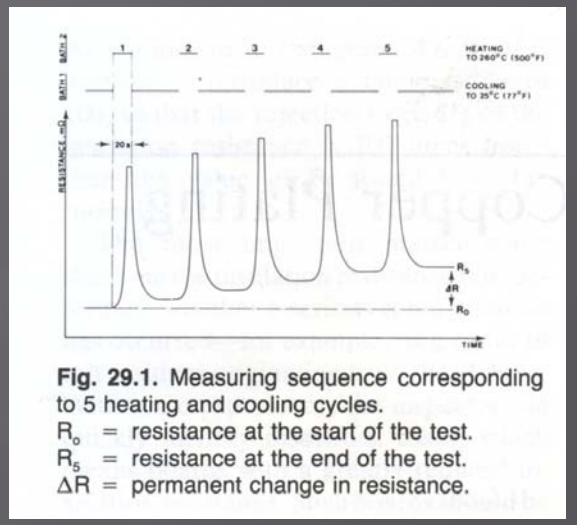
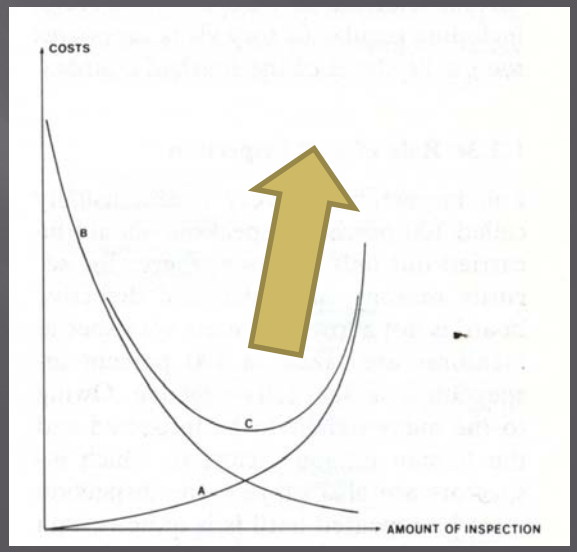


Fig. 29.1. Measuring sequence corresponding to 5 heating and cooling cycles.
R_o = resistance at the start of the test.
R_5 = resistance at the end of the test.
ΔR = permanent change in resistance.



- A third solution exist (Method 3)

- Small reminder
  - A few % of bad PTHs always start to break during production due to:
    - Curing steps (solder mask cure)
    - NI/Au plating (thermal shock)
  - Bad PTHs exibit always a higher resistive value
  - Each thermal process will break again some PTHs
    - Assembly (2 or 3 reflow)
    - Real life of the board

- The idea is the following:
  - Intoduce in each board a daisy chain
    - At least 10% of the board holes count (gives 99% chance to find a bad hole)
    - Enough holes to create a resistor of a few ohms (easier for the test)
    - Layout should integrate the more critical PTHs (the smaller ones)
    - It should also use the inner layers.
  - Test them 100% during std production e-test
    - If no cut and resistive value consistent with all production : OK
    - If one cut or resistive value different from other batches/panels
      - cross section on bad PTHs → stop the batch/panel
      - Thermal stress→ cross section→ stop the batch/panel
  - To be even more effective one thermal cycle can be added before e-test to all the production
    - 1 reflow cycle: 25° to 210° in 2 min

- The resistive value of a daisy chain can be calculated for the first panels.

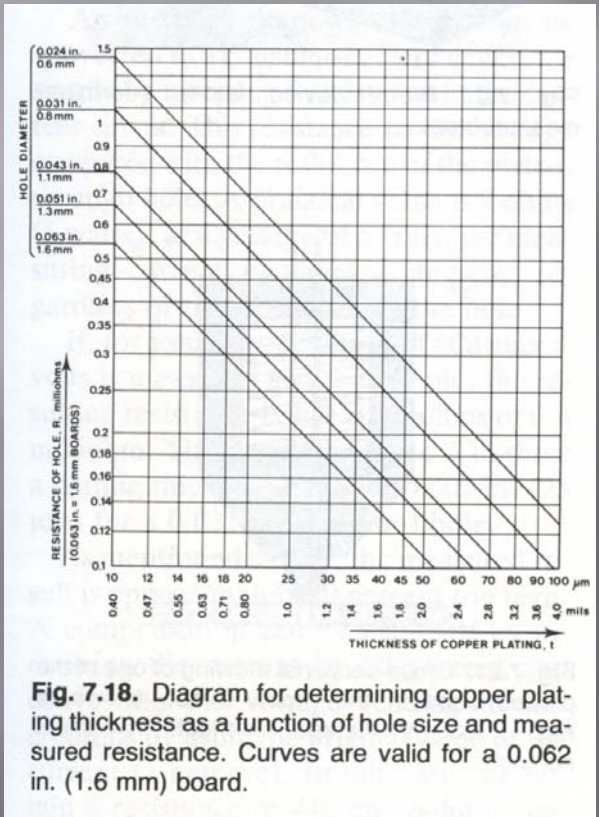
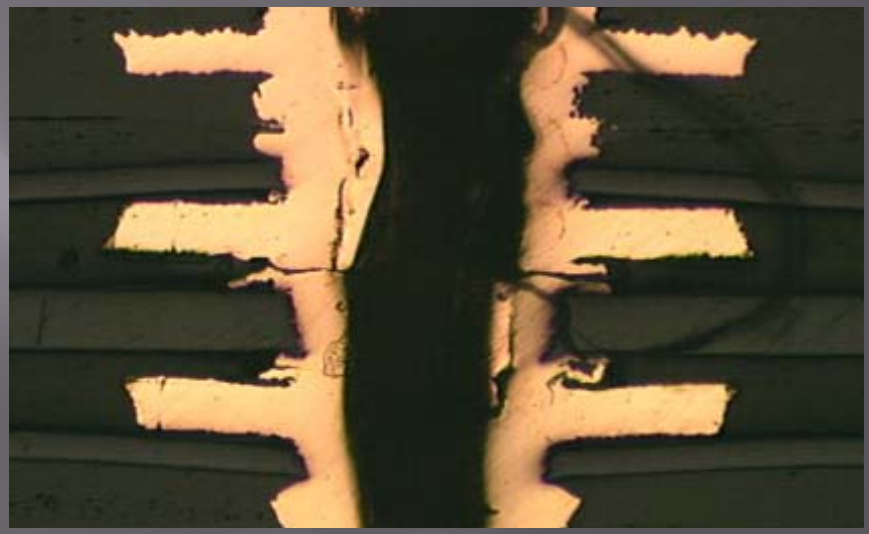
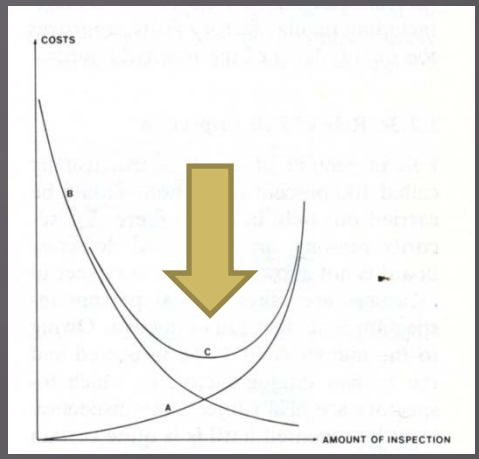


Fig. 7.18. Diagram for determining copper plating thickness as a function of hole size and measured resistance. Curves are valid for a 0.062 in. (1.6 mm) board.



This hole will have a bigger resistive value than a good one

- Advantages of this third method:
  - If production is OK → no extra tests
  - Low cost
  - Statistically gives the maximum security
  - Test is made during standard e-test
  - The e-test can not be avoided
  - Can be easely reported: list of resistive measurements



QA
Why and which

- QA (quality assessment):
  - It avoids problems, it should define exactly what kind of tests the PCBs should go through.
  - I think I've convinced you that some rules should be set with PCB manufacturers
- Which QA:
  - Every production needs QA , but the level of controls should be tuned to the application.

Different QAs? Some examples

- Case 1: prototypes made for functional test
  - The boards will be used during a few months and then destroyed
  - If any breakdown appears: no problem
  - To buy a PCB you need:
    - PCB specifications only, you can trust the company for the QA (ISO 9000 can be an indicator)
  - Exception to the rule : the cost of one board and components become not negligible (a limit value should be define)

Different QAs? Some examples

- Case 2: Circuits will be used all their life in « non critical » applications
  - What means not critical?
    - The board can be exchange easely in the application and the cost of the board and the exchange is low
  - A few % of defects are tolerated
  - Ex: Mother board of a computer (always a few % defects and everybody accept)
  - A QA should be set to define some rules:
    - Compagny audit
    - PCB Specification
    - Specify IPC levels
    - Method 1 for PTH should be implemented
    - Batch identification
    - Etc…

Different QAs? Some examples

- Case 3: Circuits will be used all their life in «critical » application
  - What means critical?
    - the board can not be exchanged easely and the cost of the board and the exchange is high.
  - One defect can stop the machine or a great part
  - Ex: LHC Temperature control boards or detectors front-end electronics
  - A QA should be set up to define the rules:
    - Company audit
    - PCB Specification
    - Specify IPC levels
    - Method 2 or 3 for PTH should be implemented
    - Batch identification
    - Etc…

Conclusion
Guide line to buy a PCB

- 1: Are you in QA case1, 2 or 3

Conclusion
Guide line to buy a PCB

- 1: Are you in QA case1, 2 or 3
- 2: Choose the technology that fits your application
  - Ask for qualification tests (Case 2,3)

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- 1: Are you in QA case1, 2 or 3
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- 3: Audit the company (Case 2,3)

Conclusion
Guide line to buy a PCB

- 1: Are you in QA case1, 2 or 3
- 2: Choose the technology that fits your application
  - Ask for qualification tests (Case 2,3)
- 3: Audit the company (Case 2,3)
- 4: Ask for an offer with:
  - Specification, materials (Case 1,2,3)
  - IPC-A-600 levels (Case 1,2,3) for 100% tests
  - IPC-A-600 + AQLs (define the sampling policy) (Case 2,3)
  - Define a policy concerning bad PCBs (Case 3)
  - Special tests for PTHs (Case 2,3)
  - Special solderability tests(Case 2,3)

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- 5: Ask for production

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  - Special tests for PTHs (Case 2,3)
  - Special solderability tests(Case 2,3)
- 5: Ask for production
- 6: Organize visits as an "inspector" and randomly check some boards before delivery
  - Following IPC-A-600 criterions and sampling policy (case 2,3)

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- 7: Product ready
- 8: Organize the same for assembly

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  - Special tests for PTHs (Case 2,3)
  - Special solderability tests(Case 2,3)
- 5: Ask for production
- 6: Organize visits as an "inspector" and randomly check some boards before delivery
  - Following IPC-A-600 criterions and sampling policy (case 2,3)
- 7: Product ready
- 8: Organize the same for assembly
- 9: Always expertise bad boards after assembly, all the problems can be found at this level.

Thank you